(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
4 August 2016 (04.08.2016)

WIPO | PCT

(10) International Publication Number
WO 2016/122948 A1

(51) International Patent Classification:
H01L 21/288 (2006.01)

(21) International Application Number:
PCT/US2016/014164

(22) International Filing Date:
20 January 2016 (20.01.2016)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
14/606,775 27 January 2015 (27.01.2015) US

(71) Applicant: **APPLIED MATERIALS, INC.** [US/US]; 3050 Bowers Avenue, Santa Clara, CA 95054 (US).

(72) Inventors: **WILSON, Gregory J.**; 427 6th Avenue East, Kalispell, MT 59901 (US). **MCHUGH, Paul R.**; 127 Sherry Lane, Kalispell, MT 59901 (US).

(74) Agents: **OHRINER, Kenneth H.** et al.; Perkins Coie LLP, P.O. Box 1247, Seattle, WA 98111-1247 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

(54) Title: ELECTROPLATING APPARATUS WITH NOTCH ADAPTED CONTACT RING SEAL AND THIEF ELECTRODE

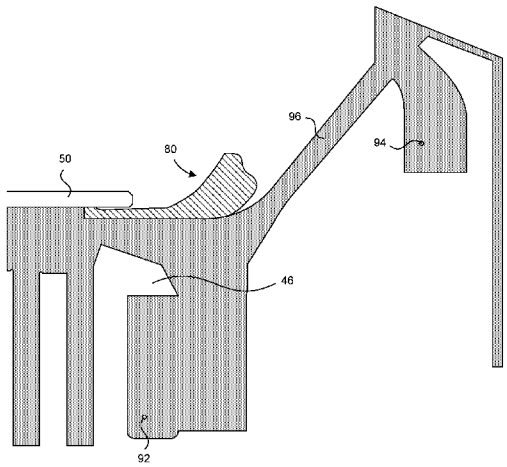

FIG. 9

(57) Abstract: An electro-processing apparatus has a contact ring including a seal which is able to compensate for electric field distortions created by a notch (or other irregularity) on the wafer or work piece. The shape of the contact ring at the notch is changed, to reduce current crowding at the notch. The change in shape changes the resistance of the current path between a thief electrode and the wafer edge to increase thief electrode current drawn from the region of the notch. As a result, the wafer is plated with a film having more uniform thickness.

WO 2016/122948 A1

ELECTROPLATING APPARATUS WITH NOTCH ADAPTED CONTACT RING SEAL AND THIEF ELECTRODE

BACKGROUND OF THE INVENTION

[0001] Manufacture of semiconductor integrated circuits and other micro-scale devices typically requires formation of multiple metal layers on a wafer or other substrate. By electroplating metals layers in combination with other steps, such as planarizing, etching and photolithography, patterned metal layers forming the micro-scale devices are created.

[0002] Electroplating is performed with the substrate, or one side of the substrate, in a bath of liquid electrolyte, and with electrical contacts touching a conductive layer on the substrate surface. Electrical current is passed through the electrolyte and the conductive layer. Metal ions in the electrolyte deposit or plate out onto the substrate, creating a metal film on the substrate. The metal ions also tend to plate out onto the electrical contacts as well. This affect, referred to as "plate-up", changes the electric field around the contacts, causing non-uniform plating. The metal plated onto the electrical contacts consequently must be removed, adding to the time requirements and complexity of the manufacturing process.

[0003] So called dry or closed contact rings have been developed to avoid plate-up of the contacts. In these designs, a seal seals the electrolyte away from the electrical contacts. The seal contacts the substrate surface radially inwardly of the electrical contacts, so that the contacts remain isolated from the electrolyte. Industry specifications for plating with a sealed contact ring increasingly require that the

annular band at the edge of the wafer covered by the seal must be as small as possible, currently towards about 1mm. To plate wafers having a notch in the edge of the wafer (to indicate a specific crystal orientation of the wafer material), the seal correspondingly must have an inward protrusion at the notch to maintain a continuous seal against the wafer. During electroplating, electric current is crowded at the notch due to the irregular geometry. This causes the plated film to be thicker around the notch than at the rest of the wafer. The yield of the wafer may therefore be reduced since the thicker plated film around the notch may negatively affect subsequent processing steps.

[0004] Accordingly, engineering challenges remain in electroplating wafers and similar work pieces having edge irregularities, such as a notch.

SUMMARY OF THE INVENTION

[0005] Current crowding resulting in thicker plating in the region of the notch is reduced or eliminated by increasing the influence of a current thief electrode at the region of the notch. A recess may be provided in the contact ring, or in the seal of the contact ring, or both. The recess provides a larger flow path through the electrolyte from the region of the notch on the wafer to the current thief electrode, causing the current electrode thief to draw more current from the region of the notch, relative to the rest of the wafer.

[0006] In a first design, an electro-processing apparatus has a thief current electrode operating with a contact ring having a seal, to compensate for electric field distortions created by a notch (or other irregularity) on the wafer or work piece. The shape of the seal is changed to provide a localized area around the notch having a

greater exposure to the thief electrode. The thief electrode consequently draws more current preferentially away from the region of the notch, improving plating uniformity. In a first aspect, a contact ring has a seal with a thin section at the notch. The shape of the seal at the notch is changed, relative to the rest of the seal, to reduce current crowding at the notch. The change in the shape of the seal at the notch reduces the resistance of current path between the thief electrode and the wafer edge to increase thief electrode current drawn from the region of the notch. As a result, the wafer is plated with a film having more uniform thickness.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] Fig. 1 is a schematic drawing of an electroplating apparatus.

[0008] Fig. 2 is a schematic drawing of the contact ring of the electroplating apparatus shown in Fig. 1.

[0009] Fig. 3 is an enlarged detail view of a section of the seal on the contact ring shown in Fig. 2.

[0010] Fig. 4 is a further enlarged detail view of tip of the seal of Fig. 3.

[0011] Fig. 5 is a perspective schematic view of the wafer shown in Fig. 4.

[0012] Fig. 6 is a perspective schematic view of the seal as shown in Fig. 2.

[0013] Fig. 7 is a schematic view of all sections of the seal in a processing position, except at the notch shown in Fig. 5.

[0014] Fig. 8 is a schematic section view of the seal of Figs. 6 and 7, at the notch.

[0015] Fig. 9 is a schematic section view of an alternative embodiment.

[0016] Fig. 10 is a perspective view of a contact ring.

[0017] Fig. 11 is an enlarged detail section view of the electrical connection between the contact fingers on the ring contact to the chuck assembly and the rotor.

[0018] Fig. 12 is section view showing unclamping the chuck assembly of Fig. 11 from a rotor.

DETAILED DESCRIPTION

[0019] To achieve a high yield of devices from each wafer, the edge zone which is contacted by the seal must be as small as possible. In the past, an edge zone of 2 or 3 mm (i.e., the annular ring at the wafer edge not useable for manufacturing devices) was often acceptable. With current industry requirements, the edge zone is now approaching or already at 1 mm. Referring momentarily to Fig. 5, some wafers 50 have a notch 52 (enlarged for illustration). On a 300 mm diameter wafer 50, the notch 52 extends in 1.5 mm. Therefore, the seal used for processing these types of wafers has an inward projection at the notch to avoid plating fluid leaking through the notch. The resulting seal covers more of the wafer around the notch. This changes the electric field in the region around the notch, causing the plated film around the notch to be thicker than the plated film on the rest of the wafer, due to current crowding at the notch.

[0020] One method to improve uniformity near the notch is to remove ring contact fingers at the notch. This is effective when the plated film is thin (<0.5 microns). For films greater than 0.5 microns thick, the notch region still plates preferentially when the fingers near the notch are removed. Because the wafer is rotating during plating, special shielding or geometry modifications to components of plating apparatus that do not rotate with the wafer are not practical.

[0021] The engineering challenges presented by the notch (or other edge irregularity) may be met with a seal having a flatted section at the notch. The shape of the seal at the notch is changed, relative to the rest of the seal, to reduce current crowding at the notch. The change in the seal shape changes the resistance or restriction of a thief electrode current between a thief electrode and the wafer edge. Thief electrode current is preferentially focused at the current crowding area near the notch and the film thickness uniformity is improved.

[0022] As an alternative or supplemental design feature for improving uniformity at the notch, a separate contact channel for the contact fingers in the flat region may be used. This channel can be driven to a slightly higher potential so that the plated film at the notch is more uniform with the rest of the wafer. In addition, a small external thief electrode may be imbedded in the external body of the seal near the flat. This external thief electrode may be controlled to the same potential as the rest of the ring and not require a separate power supply channel. The thieving region reduces the current crowding at the flat. The external thief electrode may be deplated during each ring maintenance step.

[0023] The techniques described above may be used for copper damascene plating with a sealed contact ring having a flat at the notch. They may also be used for wafer level packaging plating (WLP) if the electroplating apparatus has an edge thief electrode. In these applications, the seal shape at portions of the wafer circumference may be changed to allow more or less thieving in these regions. For example, while WLP wafers may not need a seal with a flat side because they have no notch, they may

have regions of less open area (i.e. more photoresist coverage) around the edge of the wafer that results in current crowding and reduced plating uniformity.

[0024] Many WLP wafers have a scribe region near the notch characterized by less open area. In processing these types of wafers, a seal with a smaller cross section at the notch allows the thief electrode to act preferentially at the scribe region, improving current flux uniformity. Where partial die are not patterned on the wafer (i.e. no dummy bumps), there may be varying regions of continuous photoresist around the wafer which can also be matched with an appropriate varying ring cross section to cause the thief electrode to act more or less strongly.

[0025] Turning now in detail to the drawing, as shown in FIG. 1, an electroplating apparatus 20 has a rotor 24 in a head 22. The rotor 24 includes a backing plate 26 and a contact ring 30 having a seal 80. Contact ring actuators 34 move the contact ring 30 vertically (in the direction T in FIG. 1), to engage the contact ring 30 and the seal 80 onto the down facing surface of a wafer or substrate 50. A bellows 32 may be used to seal internal components of the head.

[0026] The contact ring typically has metal fingers 35 that contact a conductive layer on the wafer 50. The head 22 is positioned to place the substrate 50 into a bath of liquid electrolyte held in a vessel 38 in a base 36. One or more electrodes are in contact with the liquid electrolyte. FIG. 1 shows a design having a center electrode 40 surrounded by a single outer electrode 42, although multiple concentric outer electrodes may be used. An electric field shaping unit 44 made of a di-electric material may be positioned in the vessel between the electrodes and the wafer.

[0027] A membrane 60 may optionally be included, with anolyte in a lower chamber below the membrane and with catholyte in an upper chamber above the membrane 60. Electric current passes from the electrodes through the electrolyte to a conductive surface on the wafer. A motor 28 in the head may be used to rotate the wafer during electroplating.

[0028] Turning to Figs. 2-4, the seal 80 typically has an elastomer tip 84 which contacts and forms a seal against the wafer, with the tip 84 supported on, or part of, a rim 86 having a beam-like or cantilever structure. The contact fingers 35, which are typically flexible metal elements, touch the wafer to the outside of the seal, so that they are not exposed to the electrolyte. Conventional seals 80 generally have a uniform cross section around the entire circumference.

[0029] Referring now to Fig. 6, to compensate for current crowding at the notch 52, the present apparatus 20 may have a seal 80 having a thin section 90. In use, the wafer 50 is loaded into the apparatus 20 with the notch 52 aligned with the flat section 90. As the seal 80 rotates with the wafer 50 during processing, the flat section 90 remains aligned with the notch 52. For a 300 mm diameter wafer having an industry standard notch, the flat section may have a width AA of 25-33 mm, or 27-31 mm.

[0030] In Figs. 7-9, the gray areas represent liquid electrolyte 46 in the vessel 38. The white areas 44 represent the solid material of the field shaping unit 44. Fig. 7 shows a cross section of seal 80 around the entire circumference, except at the flat section 90. An electric current flow path through the electrolyte 46 with characteristic dimension P1 is formed between the bottom or down-facing surface 82 of the seal 80 and the top surface 48 of the field shaping unit 44.

[0031] Fig. 8 shows a cross section of the seal 80 at the flat section 90. At the flat section 90, the seal 80 does not project down as far as it does over the rest of the circumference of the seal 80. As a result, the electric current flow path through the electrolyte 46 at the flat section 90 has a characteristic dimension P2, which is 20-400% or 50-200% greater than P1. As the resistance of the P2 path is less than the P1, the thief electrode 92 exerts a stronger influence on the electric field at the notch 52, helping to compensate for the current crowding at the notch 52.

[0032] Fig. 9 shows an alternative design having an outer current flow path 96 leading to a second or outer electrode 94. Both electrodes 92 and 94 may be connected to thief channels drawing thieving current, or the electrode 94 may act as a current thief while electrode 92 acts an anode (with the contact fingers acting as a cathode). With electrode 92 acting as an additional anode and electrode 94 acting as a current thief, current flow through section 96 is increased, allowing for better compensation for wafer offset and notch correction. The cross section area and length of the section or space 96 (which is a volume of electrolyte) influences the amount of current drawn from the wafer edge to the thief electrode 94. The cross section area of the space 96 may be increased around the notch by providing a local recess in the contact ring (which rotates with the wafer so that the recess remains aligned with the notch during plating).

[0033] Turning now to Figs. 10, 11 and 12, in certain newer wafer processing systems, the wafer is placed into a chuck 100 which includes a ring contact 30 with the seal 80. The chuck (with the wafer enclosed) travels through a processing system having an array of various apparatus or chambers to perform different processing steps.

In this type of system, seals modified as discussed above may be matched to specific types of wafers. For example, the seal on one set of chucks for wafers may have reduced thickness regions near the scribe, and other chucks may have seals specially modified for use with wafers having dummy bumps. With this approach, no changes to the electroplating apparatus itself are needed to handle various wafers and their unique plating uniformity issues around the wafer circumference.

[0034] As used here, wafer means a substrate, for example a silicon wafer, on which microelectronic, micro-mechanical and/or micro-optical devices are formed. The techniques described above may similarly be used to reduce plating deviations caused by scribe regions.

CLAIMS:

1. Electroplating apparatus, comprising:

a vessel for holding electrolyte;

at least one anode and at least one current thief electrode in the vessel; and

a head having a rotor including a contact ring for holding a wafer having a notch, the contact ring having a seal, and with the contact ring having a recess adapted to align with the notch on a wafer, with the recess allowing greater current to flow from the region of the notch on the wafer to the current thief electrode in comparison to the rest of the wafer, to improve plating thickness uniformity.

2. The apparatus of claim 1 comprising a first inner current thief electrode and a second outer current thief electrode.

3. The apparatus of claim 2 with the second current thief electrode vertically above the first current thief electrode.

4. The apparatus of claim 1 with the recess subtending an arc of 1 to 15 degrees.

5. The apparatus of claim 1 with the contact ring having first and second groups of contact fingers on a circle, with the first group of contact finger adjacent to the notch and with a first electrical connection to the first group of contact fingers and a second electrical connection to the second group of contact fingers, and with the first electrical connection at a higher voltage than the second electrical connection.

6. The apparatus of claim 1 further comprising an auxiliary current thief electrode imbedded in the seal at the notch.

7. The apparatus of claim 1 with the seal having a flat at the notch.

8. The apparatus of claim 1 further comprising a recess in the vessel, with the notch of the wafer aligned with the recess.

9. The apparatus of claim 1 with the seal supported on a dielectric material ring of the contact ring, and with the dielectric material ring having a recess aligned with the notch of the wafer.

10. An electroplating method, comprising:

holding a wafer having an edge feature in a contact ring of an electroplating apparatus;

contacting the wafer with a seal having a uniform cross section, except at the edge feature where the seal has a reduced height segment;

placing at least one side of the wafer into contact with a plating a solution and passing a first electric current of a first polarity through plating solution, through a conductive film on the at least one side of the wafer, and through electrical contacts on the contact ring;

passing electric current of a second polarity through a thief electrode in contact with the plating solution, with the thief electrode drawing a fraction of the first current through the reduced height segment, to compensate for current crowding at the edge feature.

11. The method of claim 10 wherein the edge feature is a notch in the edge of the wafer.

12. A method for processing a wafer, comprising:

identifying at least one irregularity on the wafer;

placing the wafer into a chuck having a contact ring including a seal, with the contact ring and/or the seal having a modification adapted to reduce electric current crowding at the irregularity;

moving the chuck into an electroplating apparatus; and

electroplating the wafer while compensating for the irregularity by reducing current crowding at the irregularity via a thief electrode.

13. The method of claim 12 wherein the irregularity is a notch in the edge of the wafer.

14. The method of claim 12 wherein the irregularity is a scribe region on the wafer.

15. The method of claim 12 wherein the wafer has first and second irregularities, and the seal has first and second reduced height segments aligned with the first and second irregularities.

16. The method of claim 12 wherein the modification is a recess in the contact ring.

17. The method of claim 12 wherein the modification is a change in the shape of the contact ring at the irregularity which increases the exposure of the irregularity to the thief electrode.

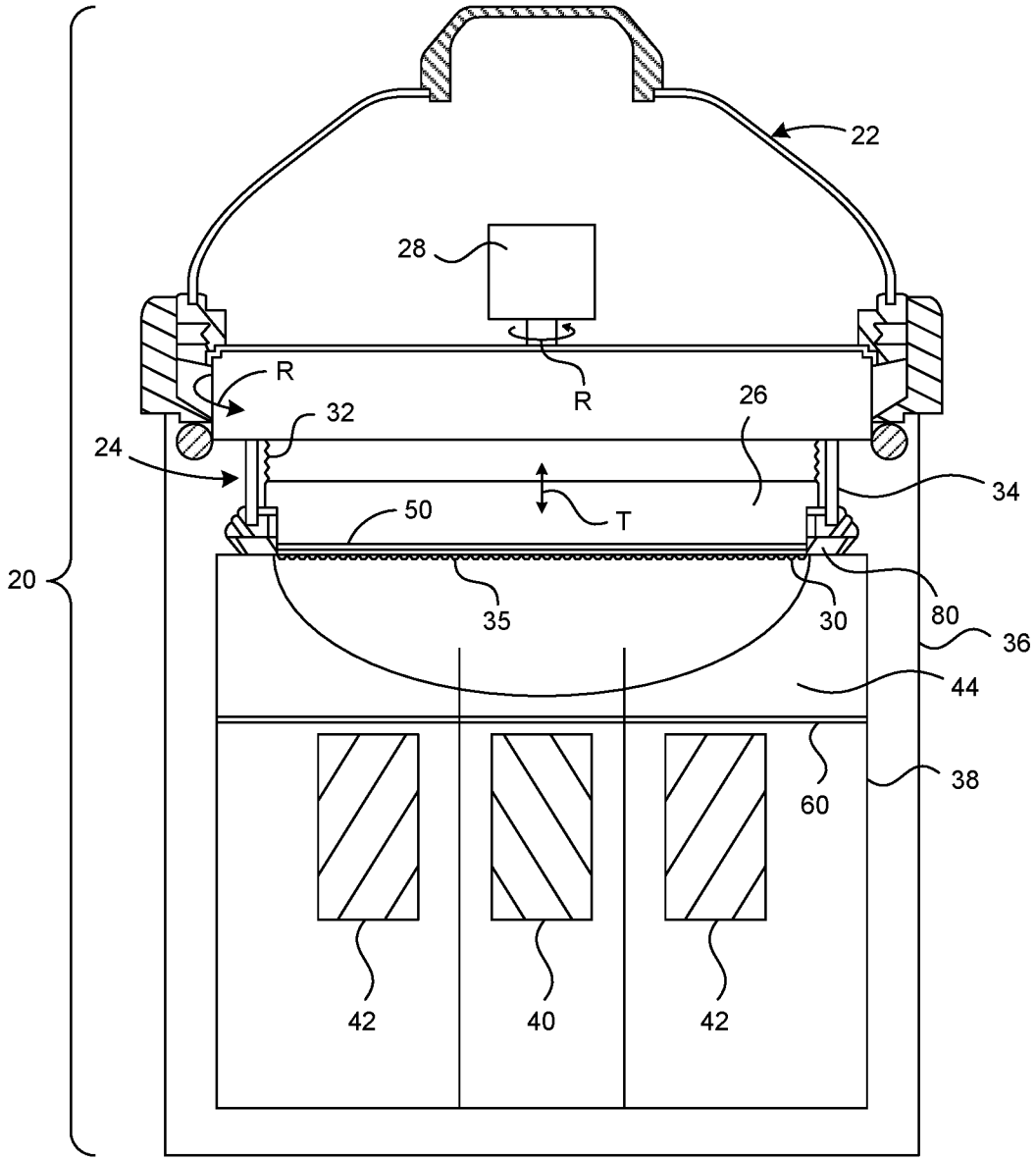

FIG. 1
(Prior Art)

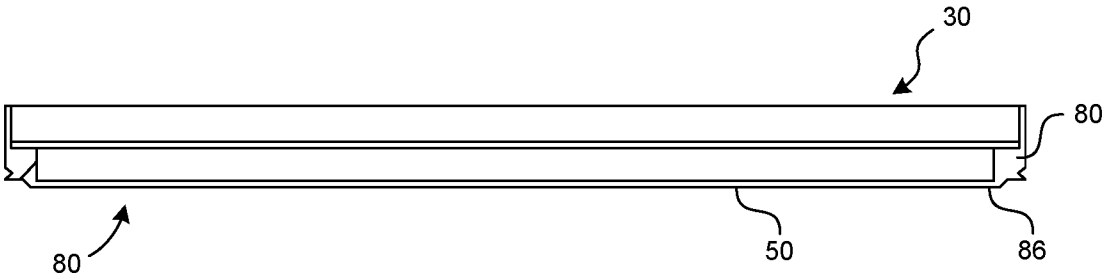

FIG. 2
(Prior Art)

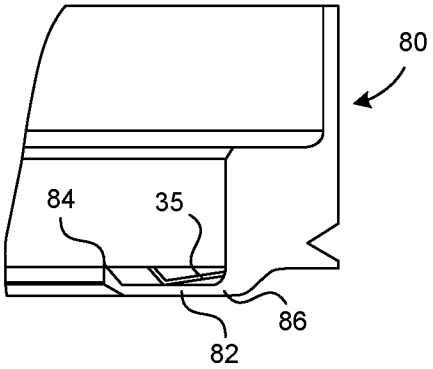

FIG. 3
(Prior Art)

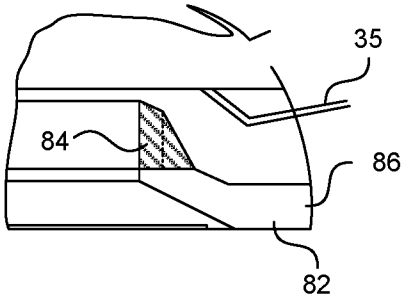

FIG. 4
(Prior Art)

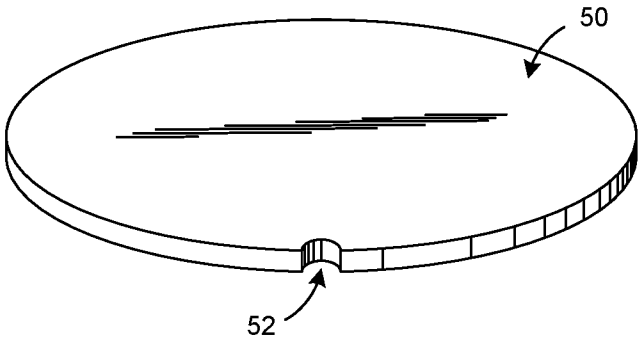

FIG. 5
(Prior Art)

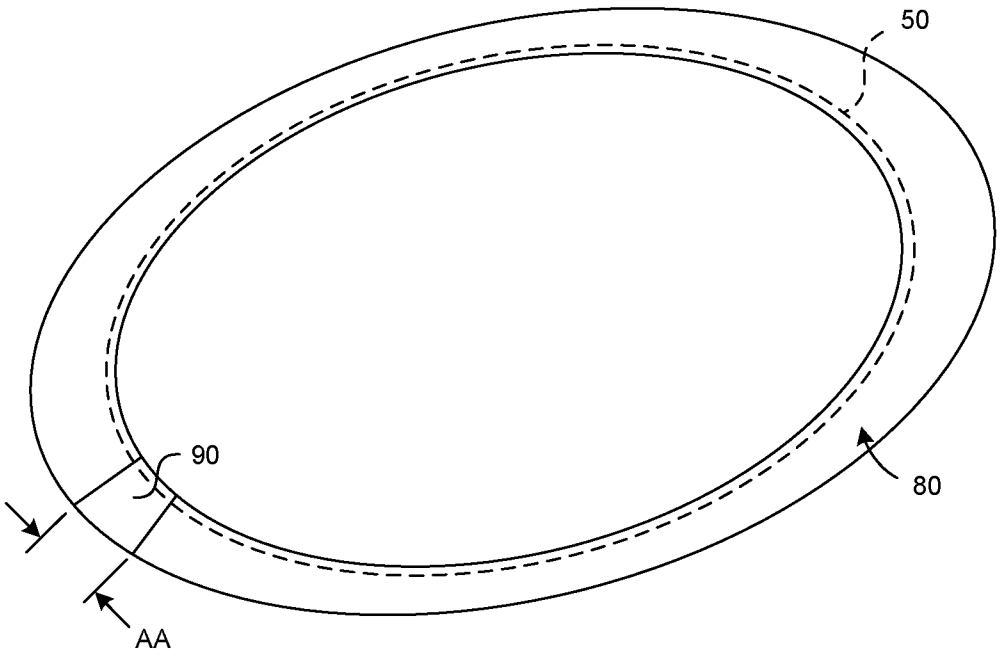

FIG. 6

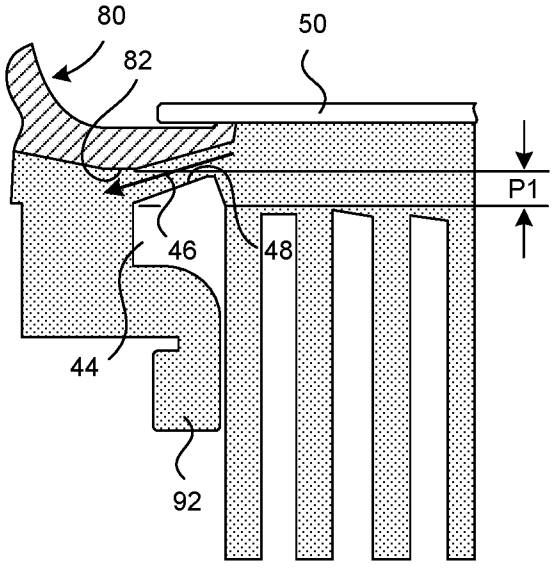

FIG. 7

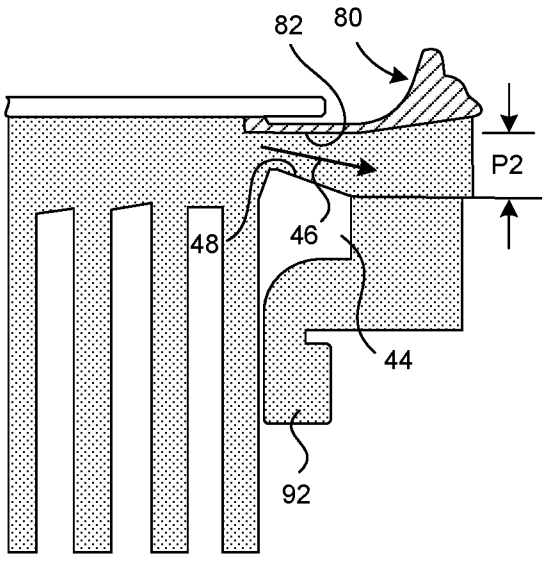

FIG. 8

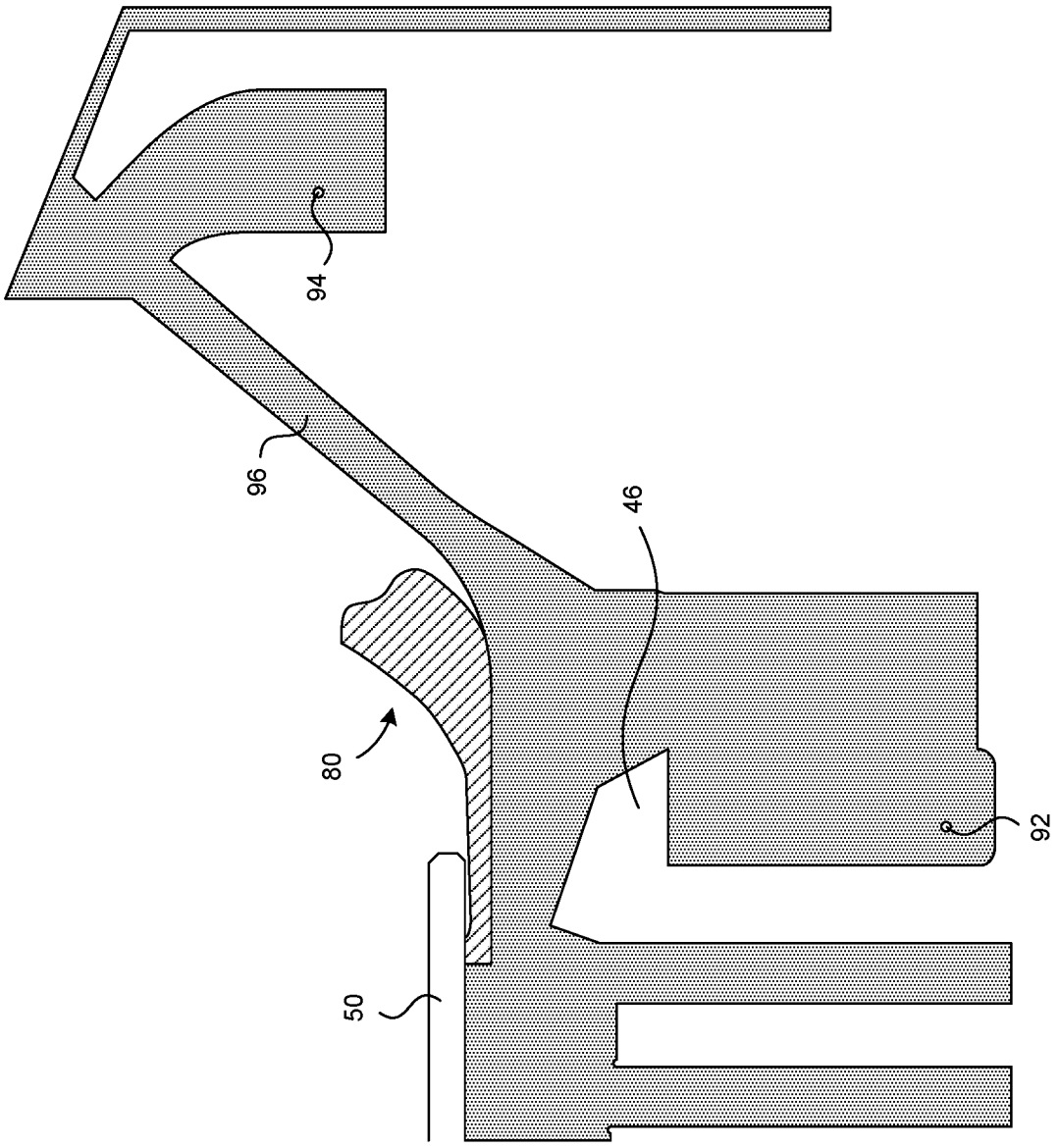

FIG. 9

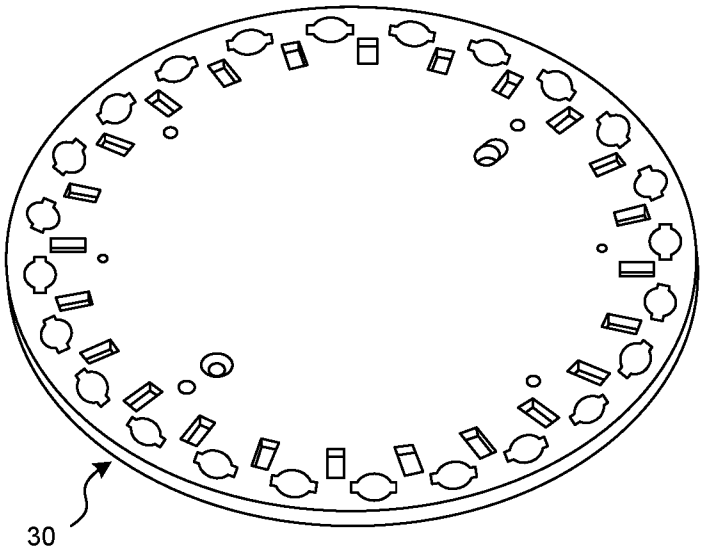

FIG. 10

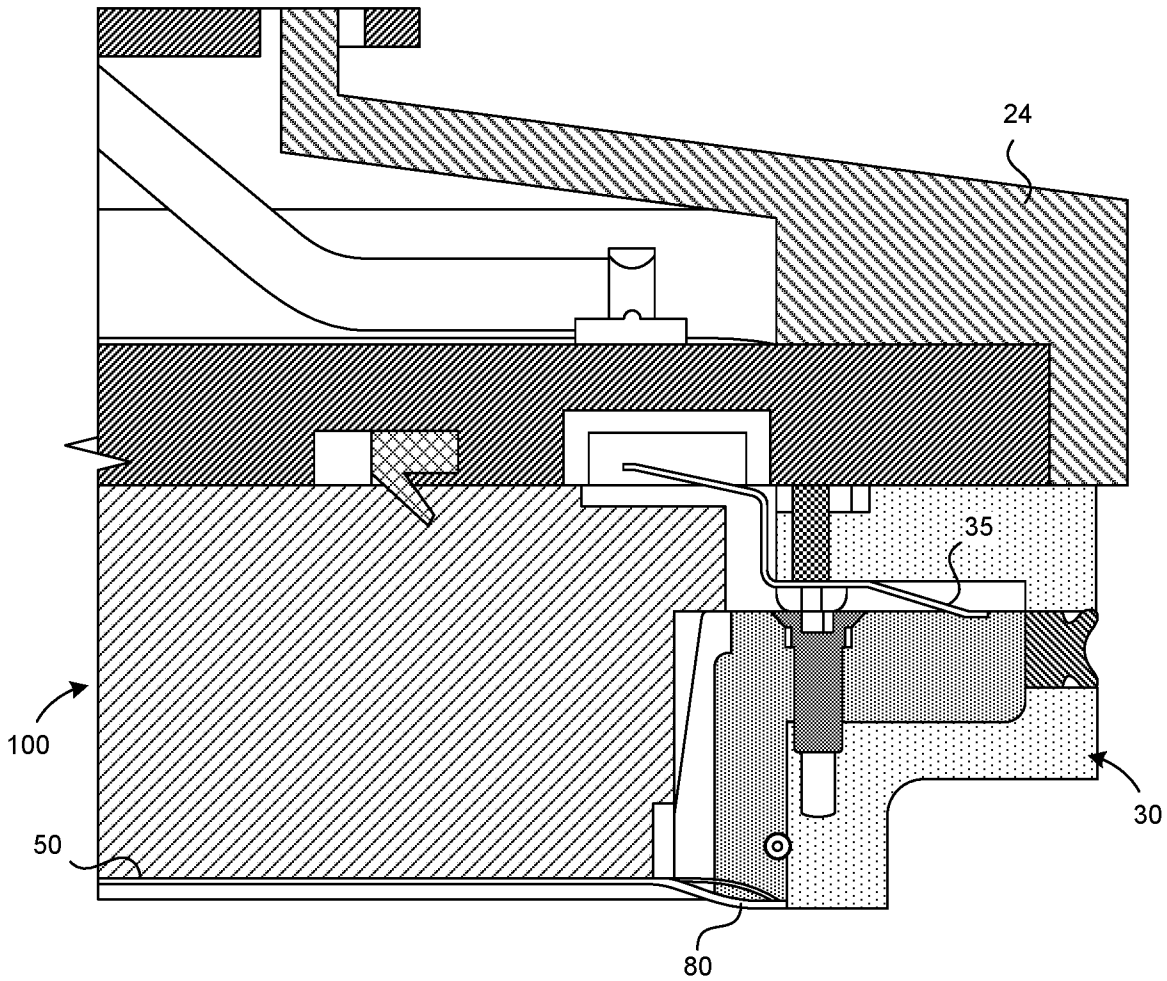

FIG. 11

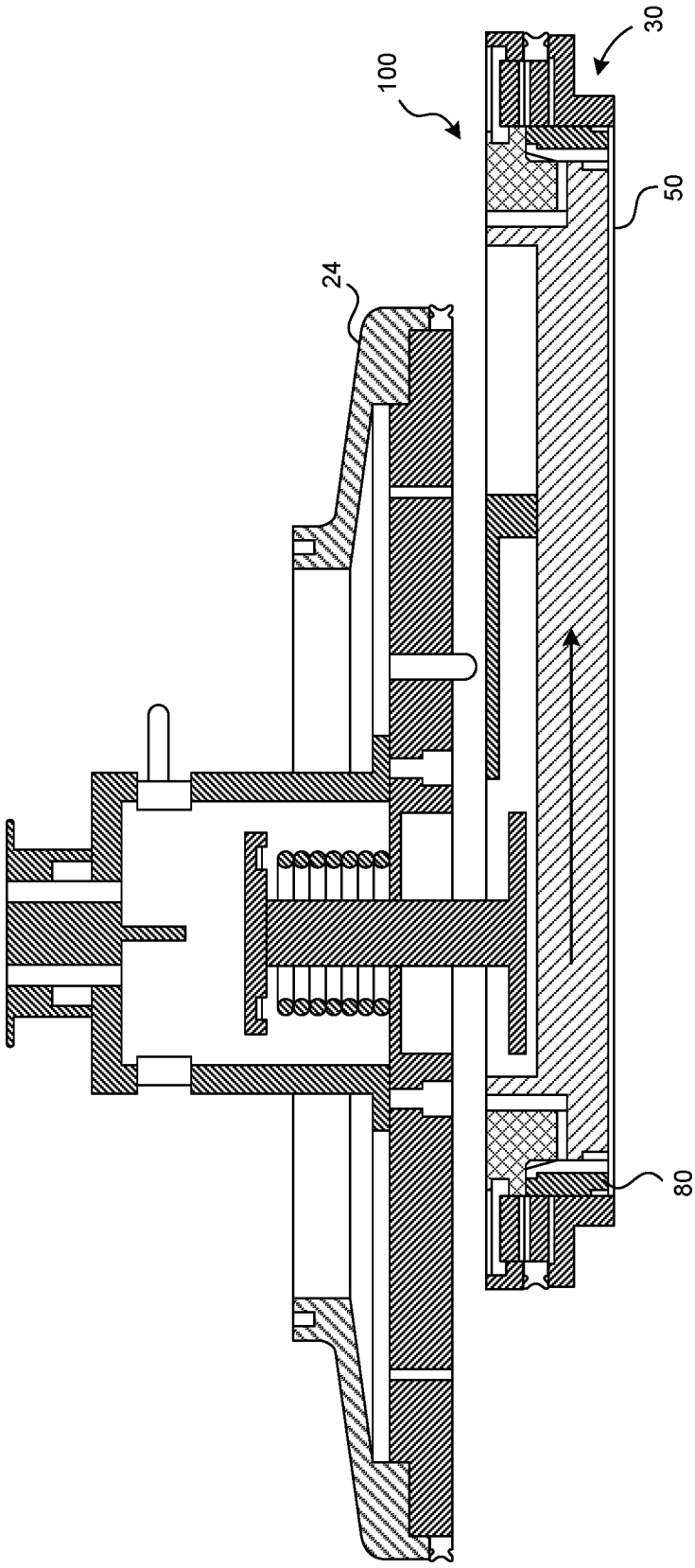

FIG. 12

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/014164

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/288(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/288; C25C 7/00; C25D 7/12; C25D 17/12; C25D 17/00; H01L 21/02; C25D 17/06; C25D 21/00; C25F 7/00; C25D 5/06

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: electroplating, thief electrode, notch, contact ring, current

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2014-0144781 A1 (LAM RESEARCH CORPORATION) 29 May 2014 See paragraphs [0052]-[0057], claim 1 and figure 1A.	1-17
A	US 2003-0085119 A1 (GREG DAVIS et al.) 08 May 2003 See paragraphs [0020]-[0022], claim 1 and figure 1.	1-17
A	US 6228231 B1 (CYPRIAN EMEKA UZOH) 08 May 2001 See column 4, line 33 - column 11, line 45, claims 1-14 and figures 4-11.	1-17
A	JP 2007-009241 A (EBARA CORP.) 18 January 2007 See paragraph [0059], claims 1, 11 and figure 12.	1-17
A	JP 2008-297586 A (ELECTROPLATING ENG OF JAPAN CO.) 11 December 2008 See paragraphs [0022], [0023], claim 1 and figure 1.	1-17

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30 May 2016 (30.05.2016)	**30 May 2016 (30.05.2016)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
KANG, Min Jeong
Telephone No. +82-42-481-8131

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2016/014164

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2014-0144781 A1	29/05/2014	JP 2014-111831 A	19/06/2014
		KR 10-2014-0067948 A	05/06/2014
		TW 201439380 A	16/10/2014
US 2003-0085119 A1	08/05/2003	US 6579430 B2	17/06/2003
US 6228231 B1	08/05/2001	None	
JP 2007-009241 A	18/01/2007	JP 2006-312780 A	16/11/2006
		JP 2007-070720 A	22/03/2007
		JP 4624873 B2	02/02/2011
		US 2007-0238265 A1	11/10/2007
		US 2010-0163408 A1	01/07/2010
JP 2008-297586 A	11/12/2008	None	