Title: IMPROVEMENTS IN TRANSCIEVERS

Abstract: A transceiver capable of operating over a frequency range of substantially 10 GHz to substantially 18 GHz, and comprising one or more multifunction monolithic microwave integrated circuits (MMICs) is provided. The transceiver preferably comprises a single multifunction MMIC, which comprises a switched attenuator, a low noise amplifier (LNA), a transmit/receive switch, a mixer and a local oscillator (LO) buffer amplifier. The transceiver preferably operates in two modes, a receive mode and a transmit mode. In the receive mode the noise figure of the transceiver is substantially 4 dB or less. In the receive mode the conversion gain of the transceiver is substantially 10 dB or more. In the transmit mode the insertion loss of the transceiver is substantially -12 dB. The size of the transceiver is substantially 30 mm\(^2\) or less. The transceiver port return losses are preferably greater than substantially 10 dB over at least a 10 GHz to 17 GHz frequency range.
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IMPROVEMENTS IN TRANSCIEVERS

This invention relates to improvements in transceivers, and to transceivers comprising multi-function integrated circuits, particularly multifunction monolithic microwave integrated circuits operable in the frequency range of 10 to 18 GHz.

There is an increasing interest in transmitting and receiving frequencies in the range 10 to 18 GHz, i.e. J-band frequencies, particularly for communication and radar applications. For example, in phased array radar systems use of such frequencies advantageously allows the size of the array elements to be reduced. Known array elements have typically used a combination of single function integrated circuits. These can be disadvantageous as they limit the element size reduction that can be achieved, and can be prone to problems in coupling between each circuit.

According to a first aspect of the present invention there is provided a transceiver capable of operating over a frequency range of substantially 10 GHz to substantially 18 GHz, and comprising one or more multifunction monolithic microwave integrated circuits (MMICs).

At these frequencies use of one or more multifunction MMICs allows realisation of microwave circuits such as transceivers in a very small area which are also cost effective.

The transceiver preferably comprises a single multifunction MMIC. This MMIC preferably comprises a switched attenuator, a low noise amplifier (LNA), a transmit/receive switch, a mixer and a local oscillator (LO) buffer amplifier. The integration of these circuit functions and the level of performance achieved is believed to be a significant step forward in the
development of MMIC technology. A transceiver is provided which has a high level of functionality realised through the integration of a number of elements as above.

The transceiver preferably operates in two modes, a receive mode and a transmit mode. Overall, the performance of the transceiver can be separated into these two modes. In the receive mode the noise figure of the transceiver is preferably substantially 4 dB or less. In the receive mode the conversion gain of the transceiver is preferably substantially 10 dB or more. In the transmit mode the insertion loss of the transceiver is preferably substantially -12 dB.

The size of the transceiver is preferably substantially 30 mm² or less. The size of the transceiver may be 6.48 mm x 4.47 mm.

The transceiver may be biased using a drain voltage of 3 V, with a current of 400 mA. The transceiver port return losses are preferably greater than substantially 10 dB over at least a 10 GHz to 17 GHz frequency range.

The transceiver is preferably fabricated using the GMMT 0.25 μm gate length, H40 pseudomorphic high electron mobility transistor (pHEMT) process. The elements present in the transceiver may be designed using HP Eesof, for electrical simulation, Sonnet, for electromagnetic simulation, and may be laid out using Barnard microsystems Wavemaker. Preferably care is taken during lay out of the elements to minimise electromagnetic coupling between elements. Each circuit is preferably simulated extensively to assess performance against temperature and process variations, preferably prior to integration into the transceiver.

The switched attenuator may receive a signal received by the transceiver.
The switched attenuator may operate in an 'on' state, where it receives the signal. When in the on state, the attenuator preferably has as low as possible an insertion loss, for example the switched attenuator preferably has an insertion loss of substantially 1.0 dB or less in this state. The switched attenuator may operate in an 'off' state, where the transceiver transmits a signal. When in the off state, the attenuator preferably has a high attenuation value, to prevent feedback of the transmitted signal into the transceiver, and to protect subsequent parts of the transceiver to which the attenuator is connected. The switched attenuator preferably has an isolation of greater than substantially 20 dB in the off state. The switched attenuator is preferably provided with one or more controls to switch the attenuator between the on and off states. The or each of these may be accessed from a position external to the transceiver.

The switched attenuator preferably consists of three transistors. Each transistor may be a pseudomorphic high electron mobility transistor (pHEMT), and may have 0.25 \( \mu \text{m} \) gate length. The transistors may be arranged in a Pi configuration. Two of the transistors may be shunt transistors. The remaining transistor may be positioned in series with the shunt transistors. Each transistor may have an inductor associated with it, to resonate out the transistor parasitic capacitance. Each transistor may have an inductor in parallel with it. The inductors may be spiral inductors. Each shunt transistor may have a resistor associated with it, to ensure good impedance matching when the attenuator is in the off state. Each shunt transistor may have a resistor in series with it. The resistors may be 50 ohm resistors. The switched attenuator is preferably laid out such that coupling between components is minimised. The switched attenuator is preferably connected to the low noise amplifier (LNA), and signals received by the attenuator passed to the LNA.
The low noise amplifier (LNA) may comprise an input line by which it receives signals received by the transceiver. The input line may be connected to the switched attenuator. The input line may be provided with one or more DC blocking elements such as capacitors. The LNA preferably comprises three amplification stages. Each stage may comprises one or more transistors, preferably one transistor. The or each transistor may be a pHEMT which may have a 0.25 µm gate length. The or each transistor of the first two amplification stages preferably use one or more source degeneration elements, to simultaneously provide low noise and a good input port match. The or each transistor of the second and third amplification stages preferably make use of parallel LR feedback, for gain shaping, i.e. a flat gain response, and stability. The or each transistor of the amplification stages preferably have one or more source to ground connections, such as via connections. The connections between the or each transistor of each amplification stage are preferably designed to provide impedance matching between stages. The LNA is preferably biased using a single drain voltage of, for example, 3 V and a single gate voltage of, for example, −0.46 V. The bias current of the LNA is preferably approximately 160 mA. The LNA is preferably impedance matched to operate in a substantially 50 ohm environment. The noise figure of the LNA is preferably substantially 3 dB or less. The gain of the LNA is preferably substantially 22 dB or more.

The transmit/receive switch is preferably provided with a transmit path through which signals to be transmitted by the transceiver are passed. The transmit/receive switch is preferably provided with a receive path through which signals received by the transceiver are passed. The transmit path is preferably connected to an output port on the transceiver and to the mixer, and a signal to be transmitted by the transceiver is received from the mixer and passed to the output port. The receive path
is preferably connected to the LNA and to the mixer, and a signal received by the transceiver is received from the LNA and passed to the mixer. There is preferably high isolation between the receive and transmit paths. Each path may contain two transistors, preferably pHEMTs, in series and a shunt transistor, also preferably a pHEMT. The transistors are preferably operated such that they act as resistors. Preferably, when it is desired to transmit a signal the transmit/receive switch is switched such that the transistors of the transmit path are caused to have a relatively low resistance in comparison to the resistance of the shunt transistor in this path. A signal may then pass through the transistors to an output port on the transceiver, and is prevented from passing through the shunt transistor. At the same time, the transistors of the receive path are caused to have a relatively high resistance in comparison to the resistance of the transistors in the transmit path, to prevent a signal from passing through the receive path. Preferably, when it is desired to receive a signal the transmit/receive switch is switched such that the transistors of the receive path are caused to have a relatively low resistance in comparison to the resistance of the shunt transistor in this path. A signal may then pass through the transistors to the next element of the transceiver, e.g. the mixer, and is prevented from passing through the shunt transistor. At the same time, the transistors of the transmit path are caused to have a relatively high resistance in comparison to the resistance of the transistors in the receive path, to prevent a signal from passing through the transmit path. The transmit/receive switch is preferably provided with one or more controls to control the switching thereof. The or each of these may be accessed from a position external to the transceiver. The parasitic capacitances of the or each transistor and/or shunt device are preferably resonated out using inductors. The inductors may be spiral inductors. The transmit/receive switch preferably has an insertion loss of substantially 2 dB or less. The transmit/receive
switch preferably has an isolation of substantially 30 dB or better.

The mixer preferably receives signals to be transmitted by the transceiver, preferably intermediate frequency (IF) signals, and mixes each of these with a reference signal and outputs mixer signals, preferably to the transmit/receive switch. The isolation between the mixer and the transmit path of the transmit/receive switch is preferably substantially 26 dB or more. The mixer preferably receives signals received by the transceiver, preferably from the transmit/receive switch, preferably from the LNA via the transmit/receive switch, and mixes each of these with a reference signal and outputs mixer signals, preferably IF signals, preferably to a coupler external to the transceiver. The isolation between the mixer and the LNA is preferably substantially 26 dB or more. The mixer may be an image rejection mixer. This may consist of two double-balanced mixers. Each of these may comprise four transistors, which may be pHEMTs, which may have 0.25 μm gate lengths. The transistors are preferably configured to operate as diodes, preferably by connecting the source and drain of each transistor together. Each double-balanced mixer is preferably connected to a Lange coupler. Each double-balanced mixer preferably receives a part of a signal to be transmitted by the transceiver, and mixes this with a part of a reference signal and outputs a double-balanced mixer transmit signal. The double-balanced mixer transmit signals may be combined using the Lange coupler. Each double-balanced mixer preferably receives a part of a signal received by the transceiver, and mixes this with a part of a reference signal and outputs a double-balanced mixer receive signal. The parts of the signal received by the transceiver and input to each double-balanced mixer may be produced by the Lange coupler. A 90 degree, 3 dB split in a received signal may be produced by the Lange coupler. Each double-balanced mixer may be provided with one or more Marchand baluns. These may comprise edge
coupled, meandered transmission lines. Each double-balanced mixer transmit signal may be output via a Marchand balun. The parts of the signal received by the transceiver and input to each double-balanced mixer may be input via a Marchand balun. The Marchand baluns preferably produce balanced parts of the received signal, i.e. the parts of the signal are 180° out of phase with each other. The two double-balanced mixers preferably provide in-phase and quadrature channels. Each double-balanced mixer is preferably connected to a Wilkinson divider, which may be an in-phase lumped Wilkinson divider. A reference signal is preferably fed to the Wilkinson divider, which splits this and feeds a part of the reference signal to each double-balanced mixer. Each part of the reference signal may be fed to each double-balanced mixer via a Marchand balun. These preferably produce balanced parts of the reference signal. These Marchand baluns may comprise edge-coupled, meandered transmission lines. The mixer input and output ports are preferably impedance matched to substantially 50 ohms. The mixer preferably has a conversion loss of 8 dB or less. The level of image rejection achieved is preferably better than 20 dB, and preferably better than 25 dB.

The local oscillator (LO) buffer amplifier may provide the reference signals for the mixer. The LO buffer amplifier preferably receives input signals and amplifies these and outputs them as reference signals. The LO buffer amplifier preferably consists of two amplification stages. Each stage may contain a transistor, which may be a pHEMT, which may have 0.25 μm gate length. Each transistor may be provided with parallel LR feedback. The LO buffer amplifier preferably has a gain of substantially 12 dB or more. The LO buffer amplifier may be biased using a single drain supply voltage of, for example, 3 V and a single gate voltage of, for example, −0.3 V. The LO buffer amplifier is preferably impedance
matched to substantially 50 ohms.

According to a second aspect of the present invention there is provided a transceiver comprising a multifunction MMIC comprising a switched attenuator, a low noise amplifier (LNA), a transmit/receive switch, a mixer and a local oscillator (LO) buffer amplifier.

According to a third aspect of the present invention there is provided a phased array radar system comprising one or more transceivers according to the first aspect of the invention.

According to a fourth aspect of the present invention there is provided a phased array radar system comprising one or more transceivers according to the second aspect of the invention.

An embodiment of the present invention will now be described with reference to the accompanying drawings, in which

**Figure 1** is a schematic diagram of a transceiver according to the invention, and

**Figure 2** shows the layout of the transceiver of Figure 1.

Referring to Figure 1, the transceiver comprises a single multifunction MMIC, comprising a switched attenuator 1, a low noise amplifier (LNA) 2, a transmit/receive switch 3, a mixer 4 and a local oscillator (LO) buffer amplifier 5. When in receive mode, the transceiver receives a signal via port 6. The signal passes to the attenuator 1, from there to the LNA 2, on to the transmit/receive switch 3 and from there to the mixer 4. Here it is mixed with a reference signal from the LO buffer amplifier 5,
and is output through ports 8,9 as two intermediate frequency (IF) signals. When in transmit mode, the transceiver receives a signal to be transmitted via ports 8,9, which are mixed in the mixer and passed to the transmit/receive switch 3, and from there output via port 7. Each of the elements of the transceiver will now be described in detail, with reference to Figure 2.

The switched attenuator 1 operates in two states, an ‘on’ state, where it receives a signal received by the transceiver, and an ‘off’ state, where the transceiver transmits a signal. The switched attenuator is provided with controls 11, which are accessed from a position external to the transceiver, to switch the attenuator between the on and the off state. When in the on state, the attenuator has as low as possible an insertion loss, for example the switched attenuator has an insertion loss of substantially 1.0 dB or less in this state. When in the off state, the attenuator has a high attenuation value, to prevent feedback of the transmitted signal into the transceiver, and to protect subsequent parts of the transceiver to which the attenuator is connected. The switched attenuator has an isolation of greater than 20 dB in the off state. The switched attenuator 1 comprises three transistors 12, 13, 14. Each transistor is a pHEMT, and has 0.25 μm gate length. The transistors are arranged in a Pi configuration. Transistors 12, 13 are shunt transistors, and transistor 14 is positioned in series with transistors 12, 13. Each transistor has a spiral inductor 15 in parallel with it, to resonate out the transistor parasitic capacitance. Transistors 12, 13 also have a 50 ohm resistor 16 in series with them, to ensure good impedance matching when the attenuator is in the off state. The switched attenuator 1 is also provided with high value resistors 17, to give a radio frequency (RF) open circuit at the gate of the transistors. The switched attenuator is connected to the low noise amplifier 2, and receives a signal received by the
transceiver via port 6 and passes this to the LNA.

The low noise amplifier (LNA) 2 comprises an input line 20 by which it receives a signal received by the transceiver from the switched attenuator 1. The input line 20 is provided with a DC blocking capacitor 21. The LNA comprises three amplification stages, each stage comprising one pHEMT 22, 23, 24 respectively, having a 0.25 μm gate length. The transistors 22, 23 of the first two amplification stages use source degeneration elements 24, to simultaneously provide low noise and a good input port match. The transistors 23, 24 of the second and third amplification stages make use of parallel LR feedback 25, for gain shaping, i.e. a flat gain response, and stability. The transistors 23, 24 of the amplification stages have source to ground via connections 26. The connections between the transistors of each amplification stage are provided with impedance matching elements 27. Impedance matching elements 28, 29 are also provided in the input and output lines respectively. The LNA is provided with stabilisation circuits 29’. The LNA is biased using a single drain voltage of 3 V and a single gate voltage of −0.46 V. The bias current of the LNA is approximately 160 mA. The LNA is impedance matched to operate in a substantially 50 ohm environment. The noise figure of the LNA is substantially 3 dB or less, and the gain of the LNA is substantially of 22 dB or more. The signal received by the LNA 2 from the switched attenuator 1 is amplified and passed to the transmit receive switch 3.

The transmit/receive switch 3 is provided with a transmit path 30 through which signals to be transmitted by the transceiver are passed, and a receive path 31 through which signals received by the transceiver are passed. The transmit path 30 is connected to port 7 on the transceiver and to the mixer 4, and a signal to be transmitted by the transceiver is
received from the mixer 4 and passed to port 7. The receive path 31 is connected to the LNA 2 and to the mixer 4, and a signal received by the transceiver is received from the LNA 2 and passed to the mixer 4. There is high isolation between the receive and transmit paths. The transmit path 30 comprises two pHEMTs 32, 33 in series and a shunt pHEMT 34. A 50 ohm resistor 39 is positioned in series with the shunt pHEMT 34. The receive path 31 comprises two pHEMTs 35, 36 in series and a shunt pHEMT 37. A 50 ohm resistor 40 is positioned in series with the shunt pHEMT 37. The transistors are operated such that they act as resistors.

When it is desired to transmit a signal the transistors 32, 33 of the transmit path 30 are caused to have a relatively low resistance in comparison to the resistance of the shunt pHEMT 34 in this path. A signal may then pass through the transistors 32, 33 to the port 7 on the transceiver, and is prevented from passing through the shunt pHEMT 34. At the same time, the transistors 35, 36 of the receive path 31 are caused to have a relatively high resistance in comparison to the resistance of the transistors 32, 33 in the transmit path 30, to prevent a signal from passing through the receive path 31. Any background or other signal received by the transceiver during transmission is prevented from passing through transistors 35, 36 into the mixer, but instead passes through the 50 ohm resistor 40 into the shunt transistor 37 and thence to ground. When it is desired to receive a signal the transistors 35, 36 of the receive path 31 are caused to have a relatively low resistance in comparison to the resistance of the shunt pHEMT 37 in this path. A signal may then pass through the transistors 35, 36 to the mixer 4, and is prevented from passing through the shunt pHEMT 37. At the same time, the transistors 32, 33 of the transmit path 30 are caused to have a relatively high resistance in comparison to the resistance of the transistors 35, 36 in the receive path 31, to prevent a signal from passing through the transmit path 30. Any signal received via port 7 is prevented from passing through transistors
32, 33, but instead passes through the 50 ohm resistor 39 into the shunt transistor 34 and thence to ground. The transmit/receive switch 3 is provided with controls 11 to control the switching thereof. These are accessed from a position external to the transceiver. The parasitic capacitances of the transistors and shunt transistors are resonated out using spiral inductors 38. The transmit/receive switch 3 has an insertion loss of substantially 2 dB or less, and an isolation of substantially 30 dB or better.

The mixer 4 receives signals to be transmitted by the transceiver, preferably intermediate frequency (IF) signals, and mixes each of these with a reference signal and outputs mixer signals, to the transmit/receive switch 3. The mixer also receives signals received by the transceiver, from the transmit/receive switch 3, and mixes each of these with a reference signal and outputs mixer signals, preferably IF signals via ports 8, 9, preferably to a coupler external to the transceiver. The mixer is an image rejection mixer, and consists of two double-balanced mixers 40, 41. Each of these comprises four transistors 42, 43 respectively, which are pHEMTs of 0.25 μm gate length. The transistors 42, 43 are configured to operate as diodes, by connecting the source and drain of each transistor together. Each double-balanced mixer 40, 41 is connected to a Lange coupler 44. Each double-balanced mixer receives a part of a signal to be transmitted by the transceiver, and mixes this with a part of a reference signal and outputs a double-balanced mixer transmit signal. The double-balanced mixer transmit signals are combined using the Lange coupler 44 and passed to the transmit/receive switch 3. The double-balanced mixers 40, 41 also each receive a part of a signal received by the transceiver, and mixes this with a part of a reference signal and outputs a double-balanced mixer receive signal via ports 8, 9 respectively. The parts of the signal received by the transceiver and input to each double-balanced mixer are
produced by the Lange coupler 44. A 90 degree, 3 dB split in a received signal may be produced by the Lange coupler. The double-balanced mixers 40, 41 are each provided with a Marchand balun 45, 46 respectively. These comprise edge coupled, meandered transmission lines. Each double-balanced mixer transmit signal is output via a Marchand Balun. The parts of the signal received by the transceiver and input to each double-balanced mixer are input via a Marchand balun. The Marchand baluns produce balanced parts of the received signal, i.e. the parts of the signal are 180° out of phase with each other. The two double-balanced mixers provide in-phase and quadrature channels. Each double-balanced mixer is connected to an in-phase lumped Wilkinson divider 47. A reference signal is preferably fed to the Wilkinson divider 47, which splits this and feeds a part of the reference signal to each double-balanced mixer 40, 41, via Marchand baluns 48, 49 respectively. The parts of the reference signal are balanced. The mixer input and output ports are impedance matched to substantially 50 ohms. The mixer 4 has a conversion loss of 8 dB or less. The level of image rejection achieved is better than 20 dB, and preferably better than 25 dB.

The local oscillator (LO) buffer amplifier 5 provides the reference signals for the mixer 4. The LO buffer amplifier 5 receives input signals via port 10 and amplifies these and outputs them as reference signals. The LO buffer amplifier 5 consists of two amplification stages. Each stage contains a 0.25 μm gate length pHEMT 50, 51 respectively, and each transistor is provided with parallel LR feedback 52. Impedance matching elements 53 are provided between the amplification stages, and impedance matching elements 54, 55 are provided in the input and output respectively of the LO buffer amplifier. DC blocking capacitors 56, 57 are also provided in the input and output respectively. The LO buffer amplifier 5 has a gain of substantially 12 dB or more. The LO buffer
amplifier is biased using a single drain supply voltage of 3 V and a single gate voltage of – 0.3 V. The LO buffer amplifier is impedance matched to substantially 50 ohms.

The transceiver is capable of operating over a frequency range of substantially 10 GHz to substantially 18 GHz. In the receive mode the noise figure of the transceiver is substantially 4 dB or less, and the conversion gain is substantially 10 dB or more. In the transmit mode the insertion loss of the transceiver is substantially -12 dB. The size of the transceiver is 6.48 mm x 4.47 mm. The transceiver is biased using a drain voltage of 3 V, with a current of 400 mA. The transceiver port return losses are greater than substantially 10 dB over at least a 10 GHz to 17 GHz frequency range. The transceiver was fabricated using the GMMT 0.25 µm gate length, H40 pHEMT process. The elements of the transceiver were designed using HP Eesof, for electrical simulation, Sonnet, for electromagnetic simulation, and were laid out using Barnard microsystems Wavemaker. Care was taken during lay out of the elements to minimise electromagnetic coupling between elements. Each circuit was simulated extensively to assess performance against temperature and process variations, prior to integration into the transceiver.
CLAIMS

1. A transceiver comprising a multifunction MMIC comprising a switched attenuator (1), a low noise amplifier (LNA) (2), a transmit/receive switch (3), a mixer (4) and a local oscillator (LO) buffer amplifier (5).

2. A transceiver according to claim 1 characterised in that in the receive mode the noise figure of the transceiver is substantially 4 dB or less and the conversion gain of the transceiver is substantially 10 dB or more, and in the transmit mode the insertion loss of the transceiver is substantially -12 dB.

3. A transceiver according to claim 1 or claim 2 characterised in that the size of the transceiver is substantially 30 mm$^2$ or less.

4. A transceiver according to any preceding claim characterised in that the switched attenuator (1) receives a signal received by the transceiver in an ‘on’ state and has an insertion loss of substantially 1.0 dB or less in the on state.

5. A transceiver according to claim 4 characterised in that the switched attenuator (1) operates in an ‘off’ state, where it transmits a signal and has a high attenuation value, to prevent feedback of the transmitted signal into the transceiver, and to protect subsequent parts of the transceiver to which it is connected, and in which state the switched attenuator (1) has an isolation of greater than substantially 20 dB.

6. A transceiver according to any preceding claim characterised in
that the switched attenuator (1) consists of three transistors (12,13, 14), each are arranged in a Pi configuration, and in which two of the transistors (12, 13) are shunt transistors and the remaining transistor (14) is positioned in series with the shunt transistors (12, 13).

7. A transceiver according to any preceding claim characterised in that the switched attenuator (1) is connected to the low noise amplifier (LNA) (2), and signals received by the attenuator are passed to the LNA.

8. A transceiver according to any preceding claim characterised in that the LNA (2) comprises three amplification stages, each stage comprises a pHEMT transistor (22, 23, 24) having a 0.25 μm gate length.

9. A transceiver according to any preceding claim characterised in that the noise figure of the LNA (2) is substantially 3 dB or less, and the gain of the LNA (2) is substantially 22 dB or more.

10. A transceiver according to any preceding claim characterised in that the transmit/receive switch (3) is provided with a transmit path (30) through which signals to be transmitted by the transceiver are passed and a receive path (31) through which signals received by the transceiver are passed, and the transmit path (30) is connected to an output port (7) on the transceiver and to the mixer (4), and a signal to be transmitted by the transceiver is received from the mixer (4) and passed to the output port (7), and the receive path (31) is connected to the LNA (2) and to the mixer (4), and a signal received by the transceiver is received from the LNA (2) and passed to the mixer (4).

11. A transceiver according to claim 10 characterised in that each path (30, 31) contains two transistors (32, 33, 35, 36) in series and a shunt
transistor (34, 37), the transistors being operated such that they act as resistors, and in which when it is desired to transmit a signal the transmit/receive switch (3) is switched such that the transistors (32, 33) of the transmit path (30) are caused to have a relatively low resistance in comparison to the resistance of the shunt transistor (34) in this path and a signal may then pass through the transistors (32, 33) to an output port (7) on the transceiver and is prevented from passing through the shunt transistor (34), and, at the same time, the transistors (35, 36) of the receive path (31) are caused to have a relatively high resistance in comparison to the resistance of the transistors (32, 33) in the transmit path (30) to prevent a signal from passing through the receive path (31).

12. A transceiver according to claim 10 characterised in that each path (30, 31) contains two transistors (32, 33, 35, 36) in series and a shunt transistor (34 37), the transistors being operated such that they act as resistors, and in which when it is desired to receive a signal the transmit/receive switch (3) is switched such that the transistors (35, 36) of the receive path (31) are caused to have a relatively low resistance in comparison to the resistance of the shunt transistor (37) in this path and a signal may then pass through the transistors (35, 36) to the next element of the transceiver and is prevented from passing through the shunt transistor (37), and, at the same time, the transistors (32, 33) of the transmit path (30) are caused to have a relatively high resistance in comparison to the resistance of the transistors (35, 36) in the receive path (31) to prevent a signal from passing through the transmit path (30).

13. A transceiver according to any preceding claim characterised in that the transmit/receive switch (3) has an insertion loss of substantially 2 dB or less, and an isolation of substantially 30 dB or better.
14. A transceiver according to any preceding claim characterised in that the mixer (4) receives signals to be transmitted by the transceiver and mixes each of these with a reference signal and outputs mixer signals to the transmit/receive switch (3), and receives signals received by the transceiver from the transmit/receive switch (3) and mixes each of these with a reference signal and outputs mixer signals.

15. A transceiver according to any preceding claim characterised in that the mixer (4) is an image rejection mixer, and consists of two double-balanced mixers (40, 41) each of which comprises four transistors (42, 43) configured to operate as diodes.

16. A transceiver according to claim 15 characterised in that each double-balanced mixer (40, 41) is provided with one or more Marchand baluns (45, 46).

17. A transceiver according to claim 16 characterised in that each Marchand baluns (45, 46) comprises an edge coupled, meandered transmission lines.

18. A transceiver according to any of claims 15 to 17 characterised in that each double-balanced mixer (40, 41) is connected to a Wilkinson divider (47), a reference signal is fed to the Wilkinson divider (47), which splits this and feeds a part of the reference signal to each double-balanced mixer via a Marchand balun (48, 49).

19. A transceiver according to any preceding claim characterised in that the mixer (4) has a conversion loss of 8 dB or less, and the level of image rejection achieved is better than 25 dB.
20. A transceiver according to any preceding claim characterised in that the local oscillator (LO) buffer amplifier (5) provides reference signals for the mixer (4), and has a gain of substantially 12 dB or more.

21. A transceiver characterised in that it operates over a frequency range of substantially 10 GHz to substantially 18 GHz, and comprising one or more multifunction monolithic microwave integrated circuits (MMICs).