(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
22 November 2018 (22.11.2018)

WIPO | PCT

(10) International Publication Number
WO 2018/213557 A1

(51) International Patent Classification:
G01D 5/24 (2006.01) *G01R 27/26* (2006.01)

(21) International Application Number:
PCT/US2018/033157

(22) International Filing Date:
17 May 2018 (17.05.2018)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
15/598,582 18 May 2017 (18.05.2017) US

(71) Applicant *(for all designated States except US)*: **CIRRUS LOGIC INTERNATIONAL SEMICONDUCTOR LTD.** [GB/GB]; Westfield House, 26 Westfield Road, Edinburgh EH11 2QB (GB).

(72) Inventors; and

(71) Applicants *(for US only)*: **MELANSON, John, L.** [US/US]; 901 W. 9th Street, #201, Austin, TX 78703 (US). **BHATTACHARYA, Anindya** [US/US]; 8400 Evelina Trail, Austin, TX 78737 (US). **THOMSEN, Axel** [DE/US]; 2715 w. 49th Street, Austin, TX 78731 (US). **SMITH, Eric** [US/US]; 2808 Montebello Road, Austin, TX 78746 (US). **PARUPALLI, Vamsikrishna** [IN/US]; 12304 Cardinal Flower Drive, Austin, TX 78739 (US). **MAY, Mark** [US/US]; 3111 Mistyglen Circle, Austin, TX 78746 (US). **GABORIAU, Johann, G.** [FR/US]; 360 Nueces Street, 50, Austin, TX 78701 (US). **LI, Junsong** [US/US]; 10720 Senna Hills Drive, Austin, TX 78733 (US).

(74) Agent: **SMITH, Darren** et al.; Norton Rose Fulbright US LLP, 1301 McKinney, Suite 5100, Houstn, TX 77010-3095 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(54) Title: CAPACITANCE SENSOR

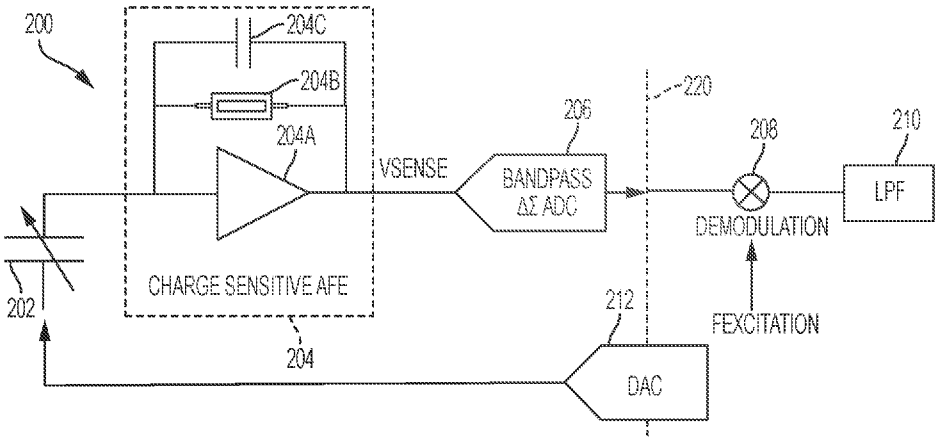

FIG. 2

(57) Abstract: Sensing electronics may be used to measure capacitance of components, such as speakers in mobile devices. A sensing circuit (200) may include a charge-sense front end (204) with sine wave excitation, an analog-to-digital conversion block (206), and a digital demodulator (208). The component (202) being measured by the sensing electronics may be excited by a high-frequency sine wave excitation (212). The digitization of the output from the component may be performed using a bandpass filter synchronized with the excitation signal by centering the bandpass filter near (e.g., within 5% of) the frequency of the excitation signal.

WO 2018/213557 A1

[Continued on next page]

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

CAPACITANCE SENSOR

FIELD OF THE DISCLOSURE

[0001] The instant disclosure relates to electronic sensors. More specifically, portions of this disclosure relate to capacitance-based sensors.

BACKGROUND

[0002] Sensing circuits for measuring a capacitance of a component may be used to determine, for example, a capacitance of a speaker or a physical sensor. One example of a capacitance sensor is shown in FIGURE 1. FIGURE 1 is a block diagram illustrating a capacitance sensing circuit using a transimpedance amplifier (TIA) according to the prior art. A circuit 100 may include a TIA stage 104 coupled to a component 102. An output of the TIA stage 104 is provided to demodulator 106. The demodulated signal is provided to an audio delta-sigma analog-to-digital converter (ADC) 108. The ADC 108 defines a boundary 120 between analog circuitry and digital circuitry. Other digital circuitry may be coupled at node 110 to receive a capacitance value representative of the component 102.

[0003] One disadvantage of the TIA-based circuit 100 is that low-frequency 1/f flicker noise affects performance of the circuit 100. Furthermore, performance is limited by noise current introduced by a resistor of the TIA stage 104, a maximum value for the resistor of the TIA stage 104 is determined by swing limitations of subsequent stages, the analog demodulation at stage 106 and signal recovery adds additional power and distortion to the circuit 100, and flicker noise from the audio ADC 108 affects low frequency performance.

[0004] Shortcomings mentioned here are only representative and are included simply to highlight that a need exists for improved electrical components, particularly for sensing circuits employed in consumer-level devices, such as mobile phones. Embodiments

described herein address certain shortcomings but not necessarily each and every one described here or known in the art. Furthermore, embodiments described herein may present other benefits than, and be used in other applications than, those of the shortcomings described above.

SUMMARY

[0005] Sensing electronics that operate to measure and digitize a capacitance value with improved operation may perform demodulation and may generate the excitation signal with a demodulator and a signal generator in the digital domain. This is unlike TIA-based conventional capacitance sensors described above, which perform demodulation and other tasks in the analog domain. An embodiment of such sensing electronics may include a charge-sense front end with sine wave excitation, a voltage-to-digital conversion block, and a digital demodulator. The component being measured by the sensing electronics may be excited by a high-frequency sine wave excitation. The digitization of the output from the component may be performed using a bandpass filter synchronized with the excitation signal by centering the bandpass filter near (e.g., within 5% of) the frequency of the excitation signal. Using a high-frequency signal, such as between approximately 20 kiloHertz and 1000 kiloHertz, reduces 1/f flicker noise in the signal measured from the component. The high-frequency signal may be outside of the usual audio frequency bands recognized by humans, which are between 20 Hertz and 20 kiloHertz.

[0006] This sensing electronics and sensing methods using the high-frequency excitation signal described herein offers several advantages. The charge input stage has an improved signal-to-noise ratio (SNR) and is more immune to interference. The low frequency performance is improved based on reduced flicker noise contribution. Furthermore, performing signal processing in the digital domain reduces noise in the final signal, power consumed in processing the signal, area for the circuits that process the signal, and improved linearity. That is, digital circuits offer several advantages for determining the capacitance based on an output from the component upon application of an excitation signal. The digital processing may be performed in dedicated circuitry or a generic processor, such as a digital signal processor (DSP).

[0007] Electronic devices incorporating the sensing circuit, such as for sensing capacitance, described above may benefit from improved capacitance measurements of components of integrated circuits in the electronic devices. For example, a mobile phone may include a speaker or other transducer having an unknown capacitance or changing capacitance. The capacitance of the speaker component may be measured by the sensing circuit and used to control output from the speaker to improve sound quality. The sensing capability provided by a circuit or code executed by a processor may be included in an audio controller. The audio controller may also include an analog-to-digital converter (ADC). The ADC may be used to convert an analog signal, such as an audio signal, to a digital representation of the analog signal. Such an ADC, or a similar digital-to-analog converter (DAC), may be used in electronic devices with audio outputs, such as music players, CD players, DVD players, Blu-ray players, headphones, portable speakers, headsets, mobile phones, tablet computers, personal computers, set-top boxes, digital video recorder (DVR) boxes, home theatre receivers, infotainment systems, automobile audio systems, and the like.

[0008] According to one embodiment of the invention, an electronic circuit for measuring and digitizing a capacitance value of a component may include a charge-sense analog front end (AFE) with sine wave excitation to create a voltage signal proportional to input capacitance. The created voltage signal may be provided to a voltage-to-digital conversion block, such as a voltage-mode ADC, for converting the voltage signal to a digital code. The digital code may be provided to a digital demodulator and filtering block for processing the digital code and providing a digital representation of the input capacitance. In this example circuit, the processing of the created voltage is performed in the digital domain after conversion to a digital code by the voltage-to-digital conversion block. In some embodiments, a current signal may be created from the charge-sense analog front end (AFE), instead of a voltage signal. The created current signal may be used to generate a digital code using a current-mode ADC, and that digital code processed similar to the voltage-mode embodiment. In some embodiments, a current signal may be created from the component and provided to a current-mode ADC, and that digital code processed similar to the voltage-mode embodiment.

[0009] The foregoing has outlined rather broadly certain features and technical advantages of embodiments of the present invention in order that the detailed description that follows may be better understood. Additional features and advantages will be described hereinafter that form the subject of the claims of the invention. It should be appreciated by those having ordinary skill in the art that the conception and specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same or similar purposes. It should also be realized by those having ordinary skill in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims. Additional features will be better understood from the following description when considered in connection with the accompanying figures. It is to be expressly understood, however, that each of the figures is provided for the purpose of illustration and description only and is not intended to limit the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] For a more complete understanding of the disclosed system and methods, reference is now made to the following descriptions taken in conjunction with the accompanying drawings.

[0011] FIGURE 1 is a block diagram illustrating a capacitance sensing circuit using a transimpedance amplifier (TIA) according to the prior art.

[0012] FIGURE 2 is a block diagram illustrating a sensing circuit with digital signal processing according to some embodiments of the disclosure.

[0013] FIGURE 3 is a flow chart illustrating a method for sensing a capacitance of a component according to some embodiments of the disclosure.

[0014] FIGURE 4 is a block diagram illustrating a sensing circuit with current-mode operation in the analog domain according to some embodiments of the disclosure.

[0015] FIGURES 5A-5C are graphs illustrating outputs within a sensing circuit, such as that of FIGURE 2, when measuring a capacitance of a component according to some embodiments of the disclosure.

[0016] FIGURE 6 is a graph illustrating a bandpass analog-to-digital converter (ADC) response around an excitation frequency according to some embodiments of the disclosure.

[0017] FIGURE 7 is a graph illustrating a demodulator in-phase output according to some embodiments of the disclosure.

DETAILED DESCRIPTION

[0018] FIGURE 2 is a block diagram illustrating a sensing circuit with digital signal processing according to some embodiments of the disclosure. A circuit 200 may include a component 202 having an unknown capacitance. The capacitance may be a fixed unknown that is unknown due to variances in manufacturing of the component 202. The capacitance may also be a changing unknown that is changing during operation of the circuit 200. The capacitance value of the component 202 may be measured with a sensing circuit including components 204, 206, 208, 210, and/or 212. The output of the sensing circuit is a digital representation of the capacitance value for the component 202. The capacitance value may be monitored continuously, such that changes in the capacitance may be detected. In some circuits, the capacitance value may be monitored in real-time or near real-time to detect changes in the capacitance and allow other circuitry to respond to the changes.

[0019] The sensing circuit may include a charge-sensitive analog front end (AFE) 204. The AFE 204 may include an amplifier 204A with a feedback loop having a parallel coupled resistor 204B and a capacitor 204C. The AFE 204 may create a voltage sense VSENSE signal that is proportional to a capacitance of the component 202 when excited by an excitation signal from an excitation source. The excitation signal may be a sine wave excitation signal with a high frequency, such as between approximately 20 kiloHertz and 1000 kiloHertz or another frequency outside of the audio band. The created voltage

sense VSENSE signal is output from the AFE 204 to additional circuitry in the analog domain for conversion to a digital code. In some embodiments, the circuit 200 may include alterative circuits to the charge-sensitive AFE 204. In other embodiments, the circuit 200 may not include the AFE 204 or an alternative circuit. For example, an output of the component 202 may be coupled directly to analog-to-digital conversion (ADC) circuitry.

[0020] An analog value corresponding to the capacitance value of the component 202 may be converted to a digital code for processing in the digital domain. For example, the created voltage sense VSENSE signal from the AFE 204 may be input to an analog-to-digital converter (ADC) 206, such as a bandpass delta-sigma ADC. The ADC 206 may have a bandpass region centered around the excitation frequency. The bandpass region may be a region centered around the excitation frequency extending on either side of the excitation frequency in proportion to the signal bandwidth. The ADC 206 may be a delta-sigma modulator configured for the encoding of narrowband bandpass signals to achieve high signal-to-noise ratios and high resolution at low sampling rates in comparison to lowpass-based ADCs. Example bandpass delta-sigma modulators are described in "Multibit Bandpass Delta-Sigma Modulators Using N-Path Structures" by R. Schreier et al. published by the IEEE and "A Fourth-Order Bandpass Sigma-Delta Modulator" by Stephen A. Jantzi et al. published by the IEEE in the IEEE Journal of Solid-State Circuits, both of which are hereby incorporated by reference in their entirety. An output of the ADC 206 is digital codes that are representative of the capacitance of the component 202. The ADC 206 may define a boundary 220 between an analog domain and a digital domain. Processing performed on an output of the ADC 206 is performed in the digital domain; processing performed prior to conversion in the ADC 206 is performed in the analog domain.

[0021] The digital codes representative of the capacitance may be processed to determine the capacitance value of the component 202. For example, the digital codes may be demodulated in demodulator 208 using the excitation frequency to generate a digital representation of the capacitance. The digital representation may be further processed by the low-pass filter (LPF) 210. The LPF 210 may remove out-of-signal band components, including modulation noise. The processing in the digital domain may be performed using

digital circuitry and/or a programmable processing circuit such as a digital signal processor (DSP). The demodulator 208 may be matched with the bandpass ADC 206 to allow operation at high frequencies, such as frequencies over 20 kHz.

[0022] The excitation signal for performing sensing of the component 202 may be generated by an excitation source based on control from digital circuitry. The digital circuitry may control switching on and off of the excitation signal. The digital circuitry may also or alternatively control the excitation frequency or other aspects of the excitation signal. For example, the digital circuitry may control a digital-to-analog converter (DAC) 212 to function as an excitation source by outputting a sine wave excitation signal with a high frequency. The output of the DAC 212 may be coupled to one terminal of the component 202, and the other terminal of the component 202 coupled to sensing circuitry. In some embodiments, the excitation signal may be applied to a first common mode terminal of the component 202 and the sensing circuitry coupled to a second common mode terminal.

[0023] A method for measuring a capacitance of a component is described with reference to FIGURE 3. The method of FIGURE 3 may be performed using the circuitry illustrated in FIGURE 2 or other circuitry for performing the described operations. FIGURE 3 is a flow chart illustrating a method for sensing a capacitance of a component according to some embodiments of the disclosure. A method 300 may begin at block 302 with applying an excitation signal to a component that causes the generation of an input signal proportional to a capacitance of the component. The generated input signal is used as an input signal to sensing circuitry for conversion and processing of the input signal to determine the capacitance of the component. At block 304, the input signal is digitized with a bandpass analog-to-digital converter (ADC) to generate a digital signal. The output of the ADC is a boundary for digital domain processing of the signal. Processing between the component and the digitization at block 304 may be performed in the analog domain, while processing after the digitization at block 304 may be performed in the digital domain. At block 306, the digital signal is demodulated to generate a digital representation of the capacitance of the component. The demodulation at block 306 may be based on the excitation signal applied at block 302, such as based on the frequency of the excitation signal.

[0024] Although some circuitry in the analog domain described above processes voltage sense signals, the capacitance sensing may also be performed using current sense signals, such as shown in FIGURE 4. FIGURE 4 is a block diagram illustrating a sensing circuit with current-mode operation in the analog domain according to some embodiments of the disclosure. The AFE 204, or other circuitry coupled to the component 202, may be configured to create a current sense signal ISENSE that is proportional to a capacitance of the component 202. When a current signal ISENSE is fed to a current-mode DAC 406, the AFE 204 may be omitted, and instead the current through the component 202 used as input to the ADC 406. The current signal ISENSE may be provided at input node 402 to a current-mode ADC 406, such as a current-mode bandpass delta-sigma ADC. The bandpass ADC 406 receives the analog current signal ISENSE, which is proportional to capacitance of the component 202, and creates a digital code output to the modulator 208. The modulator 208 may process the received digital codes from current-mode ADC 406 in the same manner as when the digital codes are generated with a voltage-mode ADC.

[0025] One example operation performed by a sensing circuit according to the embodiment described herein is described with reference to FIGURES 5A-5C. FIGURES 5A-5C are graphs illustrating outputs within a sensing circuit, such as that of FIGURE 2, when measuring a capacitance of a component according to some embodiments of the disclosure. The graph of FIGURE 5A includes a graph of an output of the component as a function of time. The signal 502 illustrates a capacitance signal output from the component, which may have a pattern similar to a sine wave excitation signal. The graph of FIGURE 5B illustrates an output signal 504 of the AFE 204 when the signal 502 is received. The graph of FIGURE 5C shows an output signal 506 from a demodulator. The output of graph 506 matches the created input signal shown in graph 502 produced from the component in response to an excitation signal.

[0026] The frequency response of components in the sensing circuit is shown in FIGURE 6 and FIGURE 7. FIGURE 6 is a graph illustrating a bandpass analog-to-digital converter (ADC) response around an excitation frequency according to some embodiments of the disclosure. A graph 602 illustrates a response of a bandpass ADC with a pass region

centered at range 604 around an excitation frequency of 187.5 kHz. FIGURE 7 is a graph illustrating a demodulator in-phase output according to some embodiments of the disclosure. A graph 702 illustrates a response of the demodulator with a peak output around an input signal frequency of 1 kHz in region 704 with thermal noise throughout the output.

[0027] The proposed methods and circuits described herein may solve one or more of the following problems with conventional capacitive sensing: achieving high SNR within constraints of low power and small area for mobile devices; achieving better linearity and total harmonic distortion (THD) performance when compared to existing solutions; achieving better immunity to various interference sources in mobile devices; and/or achieving better low frequency accuracy when compared to existing solutions.

[0028] The schematic flow chart diagram of FIGURE 3 is generally set forth as a logical flow chart diagram. Likewise, other operations for the circuitry are described without flow charts herein as sequences of ordered steps. The depicted order, labeled steps, and described operations are indicative of aspects of methods of the invention. Other steps and methods may be conceived that are equivalent in function, logic, or effect to one or more steps, or portions thereof, of the illustrated method. Additionally, the format and symbols employed are provided to explain the logical steps of the method and are understood not to limit the scope of the method. Although various arrow types and line types may be employed in the flow chart diagram, they are understood not to limit the scope of the corresponding method. Indeed, some arrows or other connectors may be used to indicate only the logical flow of the method. For instance, an arrow may indicate a waiting or monitoring period of unspecified duration between enumerated steps of the depicted method. Additionally, the order in which a particular method occurs may or may not strictly adhere to the order of the corresponding steps shown.

[0029] The operations described above may be performed by a controller configured with any circuit for performing the described operations. Such a circuit may be an integrated circuit (IC) constructed on a semiconductor substrate and include logic circuitry, such as transistors configured as logic gates, and memory circuitry, such as transistors and capacitors configured as dynamic random access memory (DRAM), electronically

programmable read-only memory (EPROM), or other memory devices. The logic circuitry may be configured through hard-wire connections or through programming by instructions contained in firmware. Further, the logic circuitry may be configured as a general purpose processor capable of executing instructions contained in software. The firmware and/or software may include instructions that cause the processing of signals described herein to be performed. In some embodiments, the integrated circuit (IC) that is the controller may include other functionality. For example, the controller IC may include an audio coder/decoder (CODEC) along with circuitry for performing the functions described herein. Such an IC is one example of an audio controller. Other audio functionality may be additionally or alternatively integrated with the IC circuitry described herein to form an audio controller.

[0030] If implemented in firmware and/or software, functions described above may be stored as one or more instructions or code on a computer-readable medium. Examples include non-transitory computer-readable media encoded with a data structure and computer-readable media encoded with a computer program. Computer-readable media includes physical computer storage media. A storage medium may be any available medium that can be accessed by a computer. By way of example, and not limitation, such computer-readable media can comprise random access memory (RAM), read-only memory (ROM), electrically-erasable programmable read-only memory (EEPROM), compact disc read-only memory (CD-ROM) or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that can be used to store desired program code in the form of instructions or data structures and that can be accessed by a computer. Disk and disc includes compact discs (CD), laser discs, optical discs, digital versatile discs (DVD), floppy disks and Blu-ray discs. Generally, disks reproduce data magnetically, and discs reproduce data optically. Combinations of the above should also be included within the scope of computer-readable media.

[0031] In addition to storage on computer readable medium, instructions and/or data may be provided as signals on transmission media included in a communication apparatus. For example, a communication apparatus may include a transceiver having signals

indicative of instructions and data. The instructions and data are configured to cause one or more processors to implement the functions outlined in the claims.

[0032] Although the present disclosure and certain representative advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the disclosure as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. For example, where general purpose processors are described as implementing certain processing steps, the general purpose processor may be a digital signal processors (DSPs), a graphics processing units (GPUs), a central processing units (CPUs), or other configurable logic circuitry. As another example, although processing of audio data is described in certain examples, other data may be processed through the filters and other circuitry described above. As one of ordinary skill in the art will readily appreciate from the present disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

CLAIMS

What is claimed is:

1. An apparatus, comprising:

a bandpass analog-to-digital converter (ADC) configured to receive an input signal proportional to a capacitance of a component and configured to output a digital signal;

a demodulator coupled to the bandpass ADC and configured to receive the digital signal from the bandpass ADC and configured to output a digital representation of the capacitance of the component; and

an excitation source configured to couple to the component to output an excitation signal to the component that causes generation of the input signal, wherein the excitation source is coupled to the demodulator to synchronize the demodulator with the excitation signal.

2. The apparatus of claim 1, wherein the bandpass ADC is configured to receive an input current signal as the input signal.

3. The apparatus of claim 1, wherein the bandpass ADC is configured to receive an input voltage signal as the input signal.

4. The apparatus of claim 3, further comprising a charge sense front end coupled to the bandpass ADC and configured to couple to the component to generate the input voltage signal based on the capacitance of the component.

5. The apparatus of claim 1, wherein the excitation source comprises a sine wave excitation source configured to couple to the component and apply a sine wave to the component for measurement of the capacitance of the component, wherein the demodulator is coupled to the sine wave excitation source and configured to synchronize with the sine wave.

6. The apparatus of claim 5, wherein the sine wave excitation source is configured to generate a sine wave with a frequency between approximately 20 kiloHertz and 1000 kiloHertz.

7. The apparatus of claim 1, further comprising a low-pass filter (LPF) coupled to the demodulator.

8. The apparatus of claim 1, further comprising a transducer, wherein the transducer is coupled to the bandpass ADC, and wherein the capacitance of the component is a capacitance of the transducer.

9. A method, comprising:

applying an excitation signal to a component that causes generation of an input signal proportional to a capacitance of the component;

digitizing the input signal with a bandpass analog-to-digital converter (ADC) to generate a digital signal; and

demodulating the digital signal with a demodulator to generate a digital representation of the capacitance of the component, wherein the demodulating is based, at least in part, on the excitation signal.

10. The method of claim 9, wherein the step of digitizing an input signal comprises digitizing an input current signal.

11. The method of claim 9, wherein the step of digitizing an input signal comprises digitizing an input voltage signal.

12. The method of claim 11, further comprising sensing, with a charge sense front end, the component to generate the input voltage signal.

13. The method of claim 9, further comprising applying a sine wave to the component for measurement of the capacitance of the component.

14. The method of claim 13, wherein the sine wave has a frequency between approximately 20 kiloHertz and 1000 kiloHertz.

15. The method of claim 9, further comprising low-pass filtering the digital representation generated by demodulating the digital signal.

16. The method of claim 9, further comprising determining a capacitance of a transducer based, at least in part, on the digital representation of the capacitance of the component.

17. An apparatus, comprising:

a controller configured to perform steps comprising:

applying an excitation signal to a component that causes generation of an input signal proportional to a capacitance of the component;

digitizing the input signal with a bandpass analog-to-digital converter (ADC) to generate a digital signal; and

demodulating the digital signal with a demodulator to generate a digital representation of the capacitance of the component, wherein the demodulating is based, at least in part, on the excitation signal.

18. The apparatus of claim 17, wherein the controller is configured to digitize the input signal by digitizing an input current signal.

19. The apparatus of claim 17, wherein the controller is configured to digitize the input signal by digitizing an input voltage signal, wherein the apparatus further comprises a charge sense front end coupled to the controller and configured to couple to the component to generate the input voltage signal based on the capacitance of the component.

20. The apparatus of claim 17, wherein the apparatus further comprises a transducer coupled to the controller, and wherein the controller is further configured to determine a capacitance of the transducer based, at least in part, on the digital representation of the capacitance of the component.

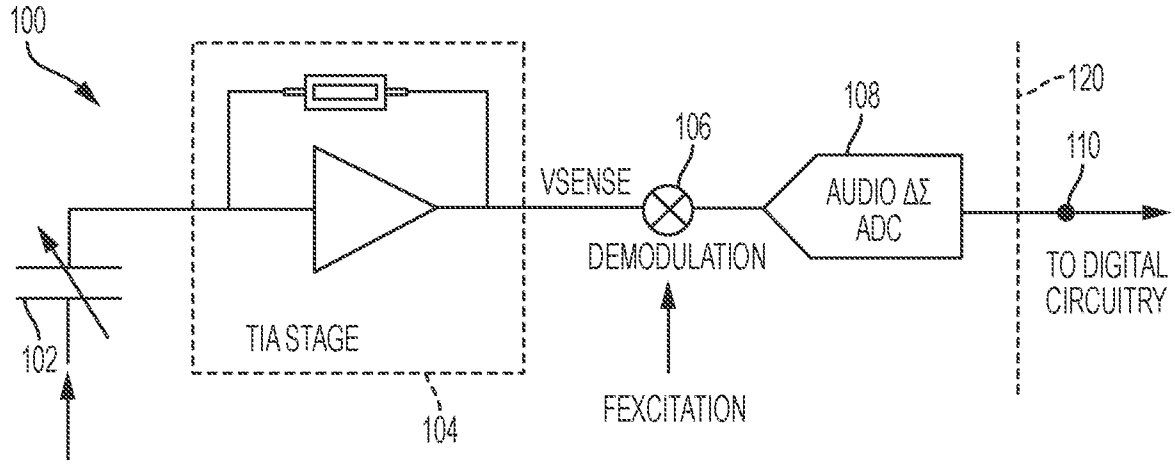

FIG. 1
PRIOR ART

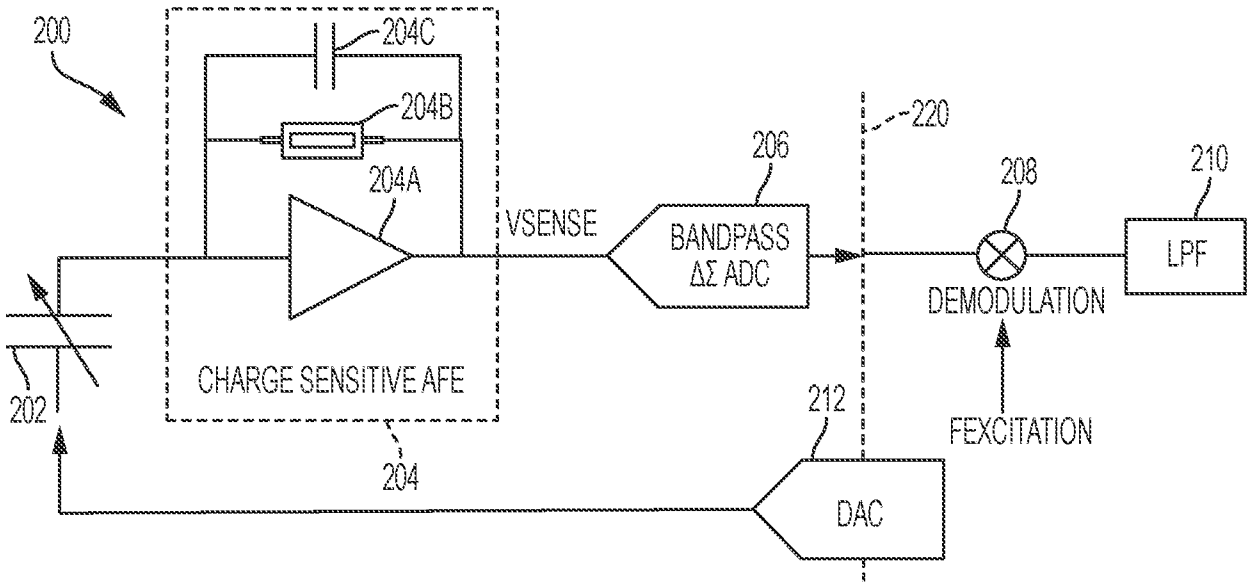

FIG. 2

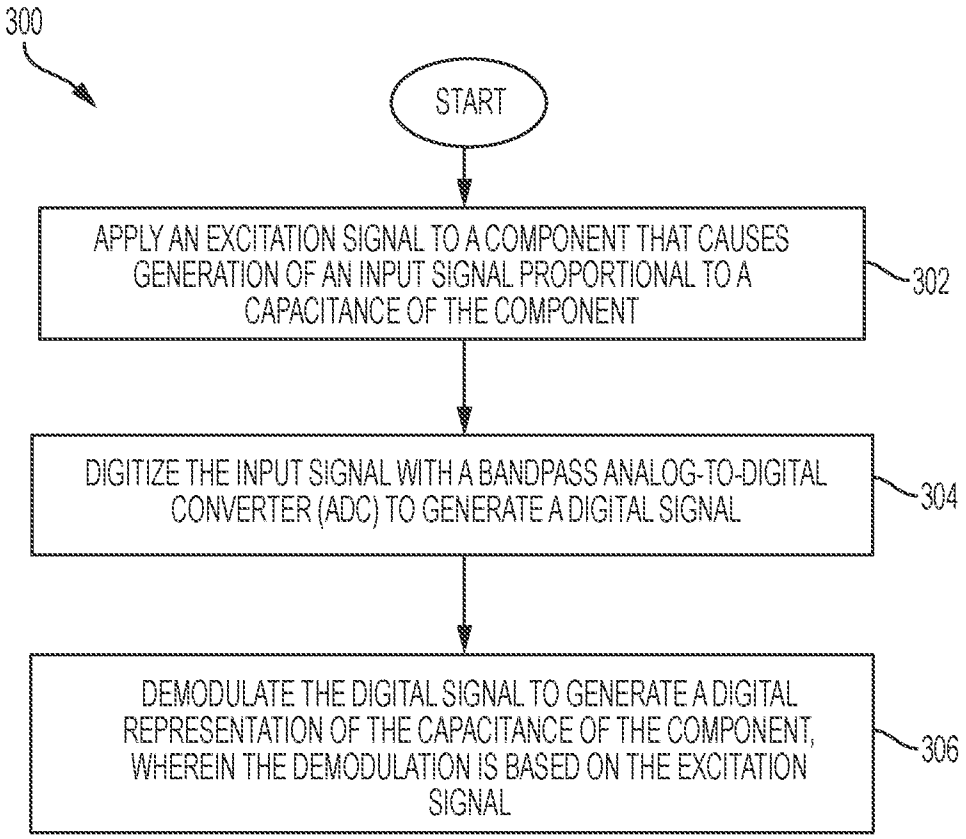
300
START
APPLY AN EXCITATION SIGNAL TO A COMPONENT THAT CAUSES GENERATION OF AN INPUT SIGNAL PROPORTIONAL TO A CAPACITANCE OF THE COMPONENT
302
DIGITIZE THE INPUT SIGNAL WITH A BANDPASS ANALOG-TO-DIGITAL CONVERTER (ADC) TO GENERATE A DIGITAL SIGNAL
304
DEMODULATE THE DIGITAL SIGNAL TO GENERATE A DIGITAL REPRESENTATION OF THE CAPACITANCE OF THE COMPONENT, WHEREIN THE DEMODULATION IS BASED ON THE EXCITATION SIGNAL
306

FIG. 3

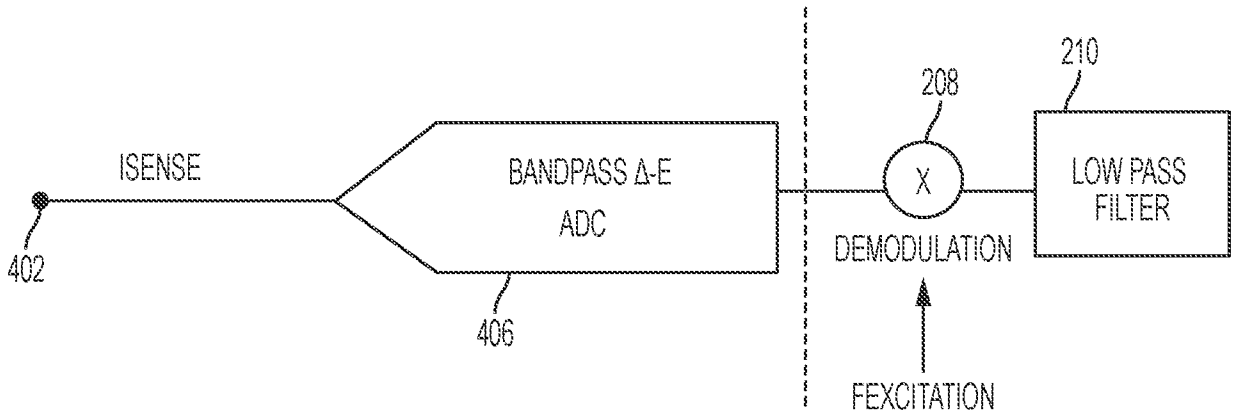
ISENSE
402
BANDPASS Δ-E
ADC
406
208
X
DEMODULATION
FEXCITATION
210
LOW PASS
FILTER

FIG. 4

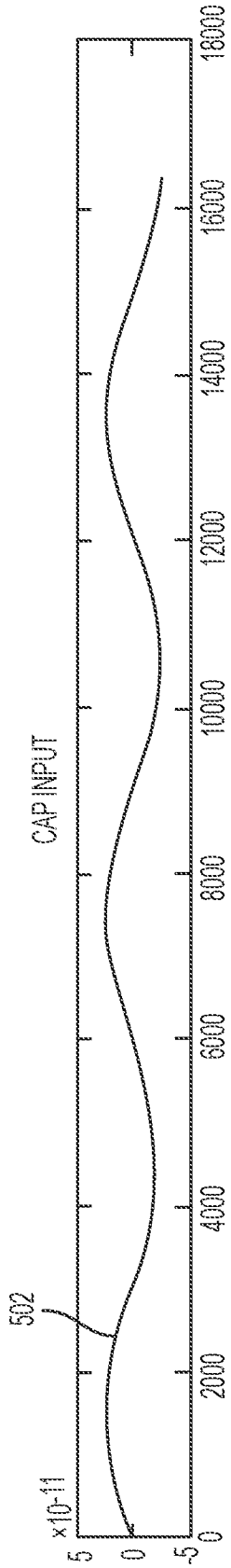

FIG. 5A

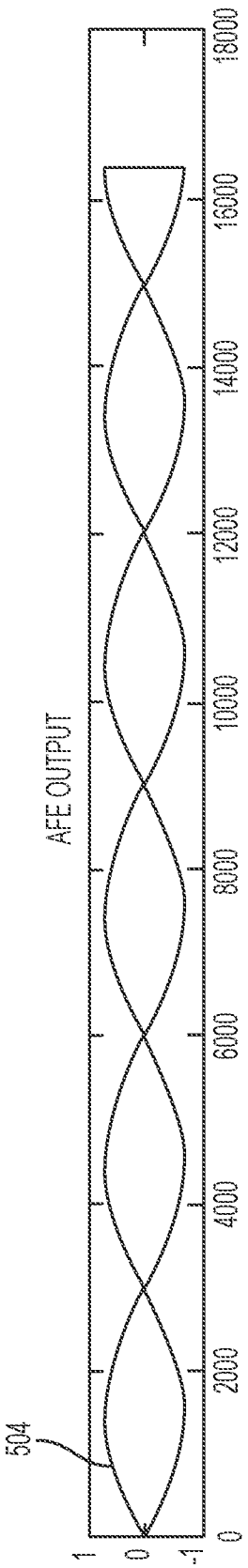

FIG. 5B

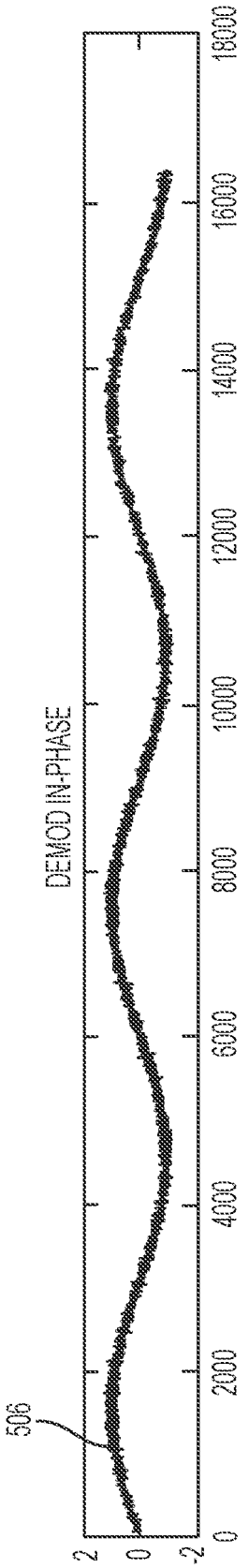

FIG. 5C

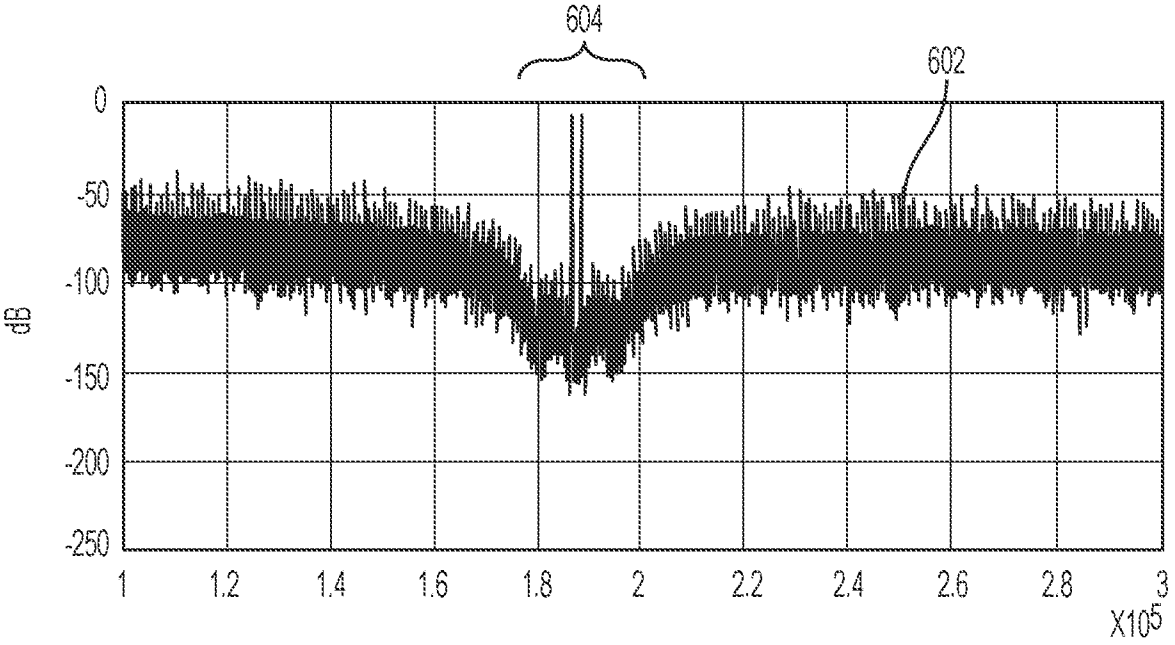
604
602
0
-50
-100
-150
-200
-250
dB
1
1.2
1.4
1.6
1.8
2
2.2
2.4
2.6
2.8
3
X10^5

FIG. 6

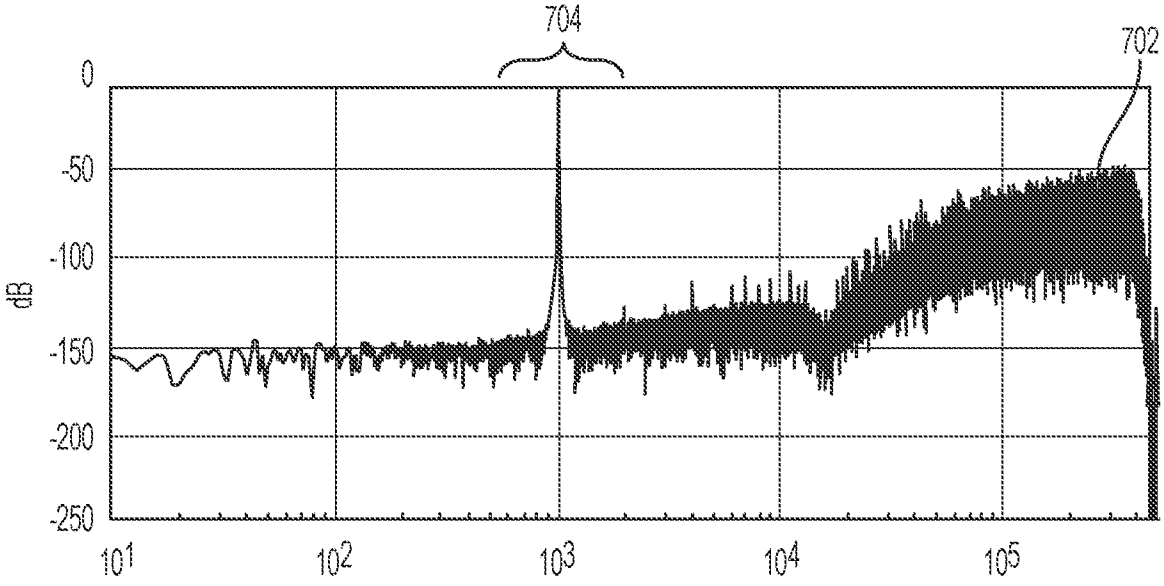
704
702
0
-50
-100
-150
-200
-250
dB
10^1
10^2
10^3
10^4
10^5

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2018/033157

A. CLASSIFICATION OF SUBJECT MATTER
INV. G01D5/24 G01R27/26
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G01D G01R G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, COMPENDEX, INSPEC, IBM-TDB, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2008/136666 A1 (HAMMERSCHMIDT DIRK [AT]) 12 June 2008 (2008-06-12) abstract paragraphs [0015], [0020], [0021], [0023], [0025], [0026], [0029], [0031], [0032], [0035]; figure 1 paragraphs [0042], [0048]; figure 2 -----	1-20
X	US 2004/174832 A1 (GEIGER WOLFRAM [DE] ET AL) 9 September 2004 (2004-09-09) abstract; figure 1 paragraphs [0018], [0019] paragraphs [0117] - [0122]; figure 4 ----- -/--	1-3, 5-11, 13-18,20

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 July 2018	27/07/2018

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Jakob, Clemens

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2018/033157

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2013/293244 A1 (LEEK ALAN HENRY [US]) 7 November 2013 (2013-11-07) abstract paragraphs [0015], [0016]; figure 2 paragraph [0027] -----	1,3,5,8, 9,11,13, 16,17, 19,20
A	US 2013/268227 A1 (OPRIS ION [US] ET AL) 10 October 2013 (2013-10-10) paragraph [0011] - paragraph [0014]; figure 3 -----	1,3,9, 11,17,19

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2018/033157

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2008136666 A1	12-06-2008	DE 102006058011 B3	17-07-2008
		US 2008136666 A1	12-06-2008
US 2004174832 A1	09-09-2004	AT 443872 T	15-10-2009
		DE 10059775 A1	13-06-2002
		EP 1337861 A1	27-08-2003
		JP 2004526942 A	02-09-2004
		US 2004174832 A1	09-09-2004
		WO 0244741 A1	06-06-2002
US 2013293244 A1	07-11-2013	CN 103383453 A	06-11-2013
		US 2013293244 A1	07-11-2013
		US 2016077639 A1	17-03-2016
US 2013268227 A1	10-10-2013	CN 103363983 A	23-10-2013
		CN 203719664 U	16-07-2014
		EP 2647952 A2	09-10-2013
		KR 20130113391 A	15-10-2013
		US 2013268227 A1	10-10-2013