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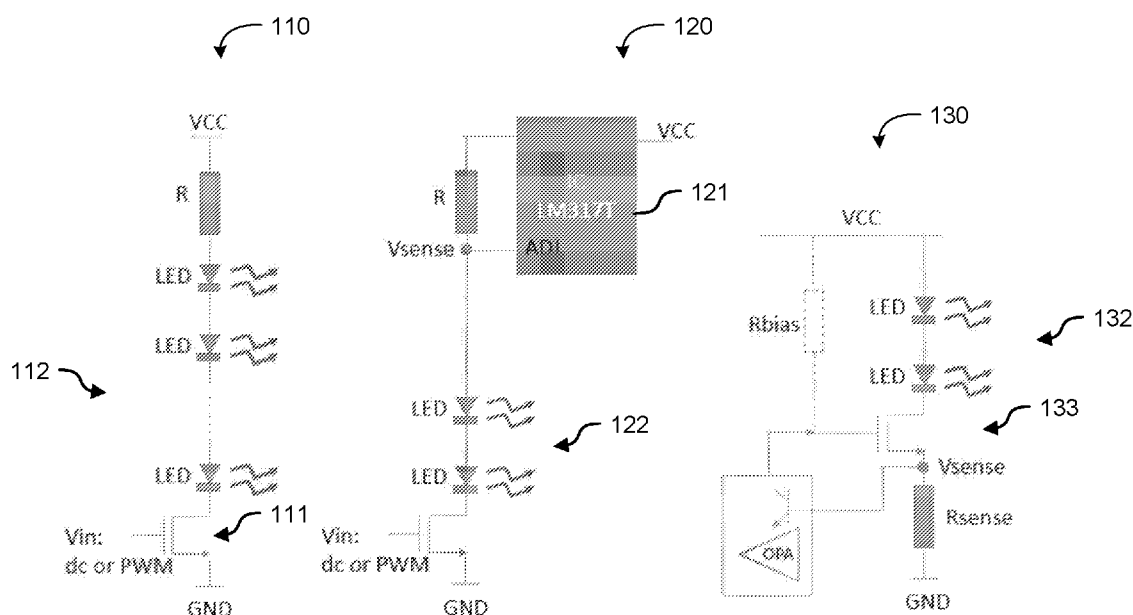


Fig. 1

(57) Abstract: Systems and methods for driving an LED may include: a preamplifier receiving a modulating signal and amplifying the modulating signal to generate an amplified modulating signal; a bias generator adding a DC bias component to the amplified modulating signal to generate a DC biased amplified modulating signal; an LED driver amplifying the DC biased amplified modulating signal to generate a drive signal at a desired signal level to drive in LED. The systems and methods may also include an error converter circuit receiving a sense signal from the LED driver, determining a DC bias component (DC bias level) and AC component (signal amplitude or RMS value) of the received sense signal, generating error values by comparing these extracted values with target values, and controlling the main amplifier bias at a desired bias point and VGA preamplifier for desired amplitude or RMS level of LED drive signal, respectively.

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LED DRIVER CIRCUIT

Technical Field

[0001] The disclosed technology relates generally to optical transmission, and more particularly, some embodiments relate to LED driver circuits for a variety of applications including optical ranging.

Description of the Related Art

[0002] Localization or ranging of target objects for volumetric positioning systems can be accomplished utilizing light (whether in the visible or invisible portions of the spectrum) as a communication medium. Some example systems may use light emitting diodes (LED) or laser diodes, such as infrared LEDs. Ranging applications generally require higher power and a higher operating frequency to transmit a properly modulated waveform and to detect the waveform at the receiver as compared to conventional LED drivers in other applications that may use various dimming controls. Modern LED driver circuits are aiming for high power drivers in the range of around several hundred milliamps (mA), but most of these operate at around 2MHz and are usually driven by a PWM (Pulse Width Modulation) modulated waveform. For example, conventional solutions rely on a pure DC current to power the LEDs and PWM techniques for dimming control.

[0003] Figure 1 illustrates examples of three conventional LED driver configurations. Driver circuit 110 is a typical LED array with a transistor 111 used as a constant current source and a resistor R between the power supply (VCC) and the diode array 112. Normally, a resistor is used to set the current and control the voltage across the diode, or diode array 112 in a linear fashion. An input voltage, V_{in} , is used to turn on the array, and this is driven by a DC voltage that can be adjusted and driven, for example, by a pulse modulated signal source for dimming control.

[0004] Driver circuit 120 is an example driver in which an integrated circuit (e.g., LM317T) 121 is used as a controller to control the current flowing through the LED or LED array 122. The resistor R is used as a sensor point to control the V_{sense} input to the integrated circuit 121, which controls the amount of voltage applied to the circuit. Similar to driver circuit 110, an input voltage V_{in} is used to drive the transistor device or a PWM signal source for dimming control.

[0005] Driver circuit 130 is an arrangement for sensing where the resistor is placed at the source of the transistor 133. The voltage at the source of transistor 133, V_{sense} , is monitored by a transistor or an operational amplifier to control the gate of transistor 133 directly. A bias resistor, R_{bias} , can be included to bias the circuit.

[0006] A common factor in these configurations is that the LED is driven by a constant current source, and that additional circuitry is included to control the intensity of the diode, such as a PWM dimming circuit for dimming control. There is no harmonic control over the signal itself for these conventional LED drivers, only

ripple or noise reduction to reduce noise from the power supply or the PWM waveform. Also, although LED power sensing is done via a sense resistor, control voltage is applied directly to the LED driver or is separated only by a simple buffer.

Brief Summary of Embodiments

[0007] According to an embodiment of the disclosed technology, An LED driver circuit, includes: a preamplifier including an input to receive a modulation signal and an output to drive a preamplified modulation signal; a bias generator circuit coupled to the preamplifier output to apply a DC bias level to the preamplified modulation signal; a main LED driver circuit including: a power transistor to amplify the preamplified modulation signal with the applied DC bias to generate an LED drive signal, the transistor including a gate coupled to the bias generator circuit, a drain coupled to a voltage source, and a source; a filter including an input coupled to the source of the transistor and an output, an LED including an anode coupled to the output of the filter and a cathode; and a resistor connected between the cathode of the LED and electrical ground; and an error converter circuit including an input coupled to receive a sense signal from the main LED driver circuit and an output to control a gain of the preamplifier to adjust output levels of the amplified modulation signal based on a difference between target signal levels and signal levels of the LED drive signal as determined using the sense signal; and a second output to control a DC bias level applied to the amplified modulation signal.

[0008] In various embodiments, the error converter circuit may include: a low-pass filter including an input coupled to receive the sense signal, and an output to output a DC bias component of the received sense signal; a differential amplifier including a first input coupled to receive the DC bias component of the received sense signal from the low-pass filter, a second input coupled to receive a target DC bias level for the LED drive signal, and an output to output a control voltage to control the DC bias level provided by the bias generator circuit.

[0009] The bias generator circuit may include a plurality of voltage-controlled resistors, and the control voltage output from the differential amplifier controls the resistance of at least one of the voltage-controlled resistors of the bias generator circuit.

[0010] The error converter circuit may include: a high-pass filter including an input coupled to receive the sense signal, and an output to output an AC component of the received sense signal; an AC to DC converter circuit to convert the AC component of the received sense signal to a DC amplitude or RMS level, including an input coupled to receive the AC component of the received sense signal from the high-pass filter and an output to output the DC amplitude or RMS level; and a differential amplifier including a first input coupled to receive the DC amplitude or RMS level and a second input coupled to receive a target level for the drive signal, and an output to output a control signal to control a gain of the preamplifier based on a difference between the received DC amplitude or RMS level and the received target level.

[0011] The error converter circuit may include: an analog-to-digital converter to convert the sense signal from an analog waveform to a digital value, including an input coupled to receive the sense signal from the main LED driver, and an output to output a digital representation of the sense signal; a digital processing circuit, including an input coupled to receive the digital representation of the sense signal, a first output to control a gain of the preamplifier, and a second output to control the amount of DC bias applied by the bias generator circuit.

[0012] In various embodiments, the digital processing circuit determines a DC bias component of the received sense signal, compares the DC bias component of the received sense signal to a target DC bias level for the LED drive signal and outputs via the second output a control signal to control the amount of DC bias applied by the bias generator.

[0013] The bias generator circuit may include a plurality of resistors and switches, and the output control signal from the digital processing circuit may include a codeword to switch at least one of the plurality of resistors into the bias generator circuit.

[0014] The In various embodiments, the digital processing circuit determines an AC amplitude or RMS value of the received sense signal, compares the AC amplitude or RMS value of the received sense signal to a target signal level for the LED drive signal and outputs via the first output a control signal to control the gain of the preamplifier.

[0015] The preamplifier may include an operational amplifier and a plurality of resistors in a feedback loop in parallel between an output and an input of the operational amplifier, and the control signal output from the digital processing circuit may include a codeword to switch at least one of the plurality of resistors into the feedback loop.

[0016] Comparing the AC amplitude or RMS value of the received sense signal to a target signal level for the LED drive signal may include comparing an RMS value of the AC amplitude or RMS value of the received sense signal to a target RMS reference level.

[0017] The In various embodiments, the control voltage to control the DC bias level provided by the bias generator circuit effectuates transistor bias control of the power transistor without being applied directly to the gate of the power transistor.

[0018] The digital processing circuit may further include an attenuator to attenuate the received sense signal before passing it to the analog-to-digital converter.

[0019] The first and second outputs of the error converter circuit may include control signals that avoid direct contact with the signal path of the modulating signal and the LED drive signal.

[0020] The error converter circuit may further include a power controller to turn off at least the transistor in the main LED driver or the preamplifier when the error converter circuit is disabled.

[0021] The bias generator circuit may include two sets of one or more voltage-controlled resistors and an inductor coupled between each set of resistors and the signal path of the modulating signal to reduce noise and signal interference to active devices in the LED driver circuit.

[0022] The bias generator circuit may be indirectly coupled to the preamplifier circuit to avoid introducing interference to the preamplified modulation signal due to direct contact.

[0023] In further embodiments, a method for driving an LED, may include: a preamplifier receiving a modulating signal and amplifying the modulating signal to generate an amplified modulating signal; a bias generator adding a DC bias component to the amplified modulating signal to generate a DC biased amplified modulating signal; an LED driver amplifying the DC biased amplified modulating signal to generate a drive signal at a desired signal power level to drive in LED.

[0024] The method may further include an error converter circuit receiving a sense signal from the LED driver, determining a DC bias component of the received sense signal and sending a control signal to control the amount of bias added by the bias generator based on a DC level of the DC bias component of the received sense signal.

[0025] The method may further include determining a difference between the DC bias component of the received sense signal and a desired amount of DC bias for the drive signal, and generating the control signal to control the amount of bias as a function of the determined difference.

[0026] The method may further include an error converter circuit receiving a sense signal from the LED driver, determining an AC component of the received sense signal and sending a control signal to control an amount of gain of the preamplifier based on the determined AC component of the received sense signal.

[0027] The method may further include determining a difference between characteristics of the AC component of the received sense signal and desired characteristics of the drive signal, and generating the control signal to control the amount of gain of the preamplifier as a function of the determined difference.

[0028] The method may further include converting the AC component of the receive sense signal to an amplitude or RMS level.

[0029] Other features and aspects of the disclosed technology will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, which illustrate, by way of example, the features in accordance with embodiments of the disclosed technology. The summary is not intended to limit the scope of any inventions described herein, which are defined solely by the claims attached hereto.

Brief Description of the Drawings

[0030] The technology disclosed herein, in accordance with one or more various embodiments, is described in detail with reference to the following figures. The drawings are provided for purposes of illustration only and merely depict typical or example embodiments of the disclosed technology. These drawings are provided

to facilitate the reader's understanding of the disclosed technology and shall not be considered limiting of the breadth, scope, or applicability thereof. It should be noted that for clarity and ease of illustration these drawings are not necessarily made to scale.

[0031] Figure 1 illustrates examples of three conventional LED driver configurations.

[0032] Figure 2 is a diagram illustrating an example of an LED driver circuit in accordance with one embodiment.

[0033] Figure 3 illustrates an example implementation of a VGA preamplifier circuit with digital control and a main LED driver in accordance with example embodiments.

[0034] Figure 4 illustrates an example of a high-frequency, high-power, low-harmonic-distortion LED driver in accordance with one embodiment.

[0035] Figure 5 illustrates an example of a digital implementation of an error converter circuit in accordance with one embodiment.

[0036] Figures 6 and 7 illustrate examples of bias generator circuits in accordance with various embodiments.

[0037] Figure 8 illustrates an example of a harmonic-free LED driver with a common-gate configuration.

[0038] Figure 9 illustrates an example process for providing an LED drive signal in accordance with one embodiment.

[0039] Figure 10 illustrates an example process for an error converter circuit implemented in the analog domain according to one embodiment.

[0040] Figure 11 illustrates an example computing module that may be used in implementing various features of embodiments of the disclosed technology.

[0041] The figures are not intended to be exhaustive or to limit the invention to the precise form disclosed. It should be understood that the invention can be practiced with modification and alteration, and that the disclosed technology be limited only by the claims and the equivalents thereof.

Detailed Description of the Embodiments

[0042] In various embodiments, an LED driver may provide a high power, low distortion output for a variety of applications including, for example, optical ranging and other applications. Figure 2 is a diagram illustrating an example of an LED driver circuit in accordance with one embodiment. The example illustrated in figure 2 includes a variable gain amplifier (VGA) preamplifier 232, an adder circuit 234, a main LED driver 236, an error converter circuit 238, and a bias generator circuit 242. The VGA preamplifier 232 may be configured to accept a sine wave input and can function as a preamplifier that drives the main LED driver 236. VGA preamplifier 232 can have an input connected to a digital-to-analog converter (DAC), voltage controlled oscillator (VCO) or other signal generator to generate the input signal 231. In various applications, the input signal 231 can be a sine wave or any analog signals ranging from a few MHz to tens of MHz. For example, the input signal 231 may be a

single tone (e.g., 10 MHz) sine wave for localization applications. It is understood that the frequency of such a signal, f_0 , might not be an absolutely perfect signal at the specified frequency, but may have some variation in accordance with factors such as, for example, tolerances of the components used, temperature variations, and other factors that may impact the precision at which a signal may be generated.

[0043] As discussed below, error converter circuit 238 generates a preamplifier automatic gain control (PAGC) signal to adjust the output signal, V_{sig} , from VGA preamplifier 232 to the desired range. The desired range may be chosen, for example, to provide sufficient signal amplitude to appropriately drive the MOSFET or other power transistor used in main LED driver 236. For example, some implementations, the desired range may be from 2Vpp-6Vpp. In other applications, the range may be a greater or lesser range. Depending on the application, for example, the range may be from 2Vpp-3Vpp, 2Vpp-4Vpp, 1Vpp-2Vpp, 2Vpp-8Vpp, and so on. Error converter circuit 238 may be controlled by an external controller such as, for example, via control signals 252.

[0044] Bias generator circuit 242 provides a bias voltage, V_g , which is mixed with the pre-amplified signal, V_{sig} , to provide the input signal, V_{in} , to main LED driver and amplifier circuit 236. In some embodiments, bias generator circuit 242 can be implemented as a bias network using a combination of pull-up and pull-down resistors to bias the transistor device appropriately. The bias voltage, V_g , can be used, for example, to ensure that the main drive transistor is set to a desired operating condition. The input voltage, V_{in} , to the main driver amplifier is the sum

of the AC signal, V_{sig} , and the DC bias voltage, V_g . Although illustrated as an adder 234 in the example of Figure 2, in various implementations the bias voltage can simply be applied to the signal using, for example, the bias network. In some embodiments, bias generator circuit 242 is driven by error converter circuit 238 to maintain the proper bias voltage, V_g , to drive the LED at a constant current without corrupting the input signal, V_{sig} .

[0045] Main LED driver 236 amplifies the input signal, V_{in} , to provide the voltage and current necessary to drive an LED light source. Main LED driver 236 may include, for example, a power MOSFET (metal oxide semiconductor field effect transistor) transistor device to provide the desired amplification. The input signal, V_{in} , to main LED driver amplifier circuit 236 is the sum of the input sine wave signal, V_{sig} , from VGA preamplifier 232 and the applied DC bias voltage, V_g , from bias generator circuit 242, which may be expressed as:

$$V_{in} = V_{sig}(\text{AC signal}) + V_g(\text{DC bias}).$$

[0046] Error converter circuit 238 receives a sense signal, V_{sense} , from the main LED driver 236, which indicates the voltage and current levels of the driver. Error converter circuit 238 uses this information to generate a transistor bias control signal 245 to control the amount of bias voltage, V_g , so that the LED can be properly driven. As noted above, in some embodiments, bias generator circuit 242 maintains the proper bias voltage, V_g , to drive the LED at a constant current without corrupting the input signal, V_{sig} .

[0047] Figure 3 illustrates an example implementation of a VGA preamplifier circuit with digital control and a main LED driver in accordance with example embodiments. The VGA preamplifier 340 can be implemented to drive the main LED driver (e.g., main LED driver 236). The example VGA preamplifier 340 includes an operational amplifier 342, and a bank of resistors, 1R, 2R ... 16R, that can be switched in and out digitally via a bank of switches 343 to control the gain of the amplifier 342. As noted above with reference to Figure 2, the digital control to switch in and out one or more of the resistors in the resistor bank may be provided by the error converter circuit (e.g., error converter circuit 238) in the form of analog or digital control signals based on the types of VGA control methods (e.g., a programmable automatic gain control signal). The Programmable Automatic Gain Control (PAGC) signal can include digital codes (e.g., codewords) to control the state of individual switches in the bank of switches 343 so that individual resistors can be switched ON or OFF. The PAGC signal may be generated as a result of comparing the AC signal magnitude (or RMS value) in the digital domain, examples of which are described in greater detail below.

[0048] In other embodiments, the VGA preamplifier may be implemented using other forms of analog or digital control techniques. As one example, voltage controlled resistor elements can be implemented with an analog control voltage to control the gain of the operational amplifier 342. Other gain control methods can also be used to provide gain compensation for any signal loss to the LED or due to harmonic filtering along the main driver output signal path.

[0049] A differential amplifier 342 may be implemented to handle a relatively large, high frequency signal. In some embodiments, for example, the input signal, V_{in} (e.g., input signal 231 in the example of Figure 2), may be a 10MHz sine wave with a 2Vpp-6Vpp swing. In other embodiments, other frequencies and voltage swings can be accommodated, depending on the application. Because the VGA preamplifier is not expected to drive the LED itself, but is instead driving a main LED driver, it may not be required to provide several hundreds of mA of current driving capability. Indeed, in such embodiments, it may need to provide a signal with sufficient power to drive power MOSFET devices in the main LED driver. Although not illustrated, bypass capacitors can be included to avoid oscillation and to filter noise from the power supply.

[0050] Main LED driver 350 in the example of Figure 3 includes a MOSFET power transistor 356, a harmonic trap and low-pass filter 357, a light-emitting diode 354, and a ballast resistor 358. Transistor 356 in this example is an NMOS transistor in a common drain configuration. The harmonic trap and low-pass filter 350 can be implemented using a second-order harmonic trap (notch filter) to reduce the second-order harmonic frequency component, combined with a low-pass filter to reduce higher-order harmonic frequency components.

[0051] In various applications, power transistor 356 is specified to have the ability to drive greater than 1 amp of current. The drive current specified can be a function of specifications for the given LED or LED array that the transistor is driving and the output power desired from the LED. VCCREG may be a regulated and filtered

voltage from a power supply. In one example, this clean power supply can be the main power supply that can provide power to the VGA preamplifier, the main LED driver, error converter circuit, and the bias generator circuit.

[0052] With MOS devices, it is expected that the signal path from the gate to the drain will show second-order harmonics due to device characteristics. This can be especially pronounced where a large signal is applied. In this case, the drain resistor may introduce undesirable levels of distortion to the signal. Accordingly, instead of a common-source configuration, a common-drain configuration is shown in this example to reduce harmonic tones from the gate-drain gain path. In some embodiments, the driver amplifier can be implemented as an NMOS device to provide a stable DC current LED drive signal at the anode of LED 354 to turn on LED 354.

[0053] Assume a 10 MHz input sine wave as mentioned above. Further assume an application where it is desired to provide a pure single-tone signal to the LED 354. Because harmonics will be generated and would otherwise flow through LED 354, filtering can be provided to remove second- and higher-order harmonics that may otherwise corrupt the transmitted signal from the LED and that could lead to significant errors at a photodiode receiver in ranging applications. Harmonic trap and low-pass filter 352 may be provided to reduce or remove these harmonics.

[0054] For example, if the transmitted signal frequency contains 10MHz (i.e., the desired frequency, f_0), 20MHz (i.e., second-order harmonics at $2*f_0$) and higher tones, the received signal at the photodiode receiver will suffer from

intermodulation distortion due to the harmonics component at 20MHz rather than higher-order tones. Consequently, a second-order harmonic trap (notch) filter may be used to effectively remove the second-order harmonic tone. If desired, a low-pass filter can be included to remove higher-order terms that may be introduced. Once the second-order harmonic is suppressed, the low-pass filter can be relaxed to filter out higher-order harmonic tones.

[0055] After filtering at trap and low-pass filter to LED 354, the LED drive signal develops a voltage across LED 354 and ballast resistor 358. This voltage across the ballast resistor 358 can be monitored to adjust the DC bias current. The order of the LED, resistor, and ground are arranged as shown in this example so that the sensed voltage, V_{sense} , is referenced to ground and therefore can provide direct measurements of the signal swing (RMS value) and the DC bias level. Accordingly, direct feedback can be provided to an error converter circuit to adjust the DC bias. In the illustrated example, V_{sense} is provided at a node coupled to the cathode of LED 354.

[0056] Figure 4 illustrates an example of a high-frequency, high-power, low-harmonic-distortion LED driver in accordance with one embodiment. This example includes a common-drain main LED driver configuration as illustrated in Figure 3, with an analog implementation of an error converter circuit 438. In the illustrated example, the analog error converter circuit 438 includes an AC-DC converter and low-pass filter 452, a high-pass filter 454, a low-pass filter 455, differential amplifiers 462, 464, a digital-to-analog converter 456. This example also includes an AC

coupling capacitor 433 to pass the AC signal from VGA preamplifier 432 to bias generator circuit 434.

[0057] The analog error converter circuit 438 receives the sense voltage signal, V_{sense} , 474 from main LED driver 436 (which is illustrated as being LED driver amplifier 350). The V_{sense} signal 474 is applied to high-pass filter (HPF) 454 to extract sine wave amplitude information from the V_{sense} signal, which is the sum of the DC bias and the sine wave signal. V_{sense} signal 474 is also applied to low-pass filter (LPF) 455 to extract bias level information from the signal.

[0058] The output from low-pass filter 455 is the DC bias level extracted from V_{sense} signal 474. This DC bias component is compared against a reference voltage (e.g., a target DC bias component) generated from DAC circuit 456 at differential amplifier 462. The output of differential amplifier 462 is an error signal representing the difference between the target DC bias component and the sensed DC bias component. This output signal may be applied to the voltage-controlled resistors 434, which are used as bias resistors to set the bias voltage (e.g. such as in bias generator circuit 242). This feedback voltage sets the transistor gate bias voltage indirectly to avoid direct contact of the bias voltage with the signal. This may reduce undesirable direct impacts on spectral purity of the signal. This may also help to avoid thermal runaway by monitoring the excessive current flowing through the output branch, which may cause device damage due to excessive heat.

[0059] The output from high-pass filter 454 is the AC component of the LED drive signal. Because there will be some signal attenuation along the main driver

output path, and the main driver cannot compensate for this signal attenuation, the preamplifier can be controlled to account for this to adjust the signal amplitude to deliver proper signal levels to the LED. This feedback path can provide an automatic control to ensure that the LED is transmitting at the desirable signal levels (RMS values). It is noted that in this and other embodiments, the output LED is illustrated as a single LED. In various implementations, the LED can be implemented as an array of two or more LEDs.

[0060] High-pass filter 454 filters out the DC bias component, providing the remaining AC component of the signal. The output signal is rectified by AC-DC converter circuit 452 to generate magnitude information for the signal. The AC to DC converter can be implemented as either a half-wave or full-wave rectifier, and can include a low-pass filter to clean up the resultant signal. For example, assume a scenario in which a full-wave rectifier is used and the desired target swing is a maximum magnitude of 3.5 V peak-peak across a 5 ohm resistor. The current across the resistor would be 700 mA peak-peak, and the RMS value of the current would be $350 \text{ mA} \times 0.707 = 247.45 \text{ mA rms}$. The average value can also be calculated as $350 \text{ mA} \times 0.637$. These values may be calculated for target values, and this can be set as a reference value that can be supplied by the DAC component 456. The DC value from AC to DC converter and LPF 452 can be compared with the reference value from DAC component 456 and the difference used to generate a signal 475 indicating the magnitude of the error.

[0061] The example of Figure 4 illustrates a differential amplifier 464 generating control signal 475 as a function of the difference between the actual signal level as sensed by Vsense signal 474 and the reference values from DAC component 456. The control signal 475 can be used to control the gain of variable gain amplifier 432 to control the output magnitude that provides the desired current RMS value at the LED. For example, if the filtered, converted Vsense signal 474 indicates that the actual current levels are below a target current level, this difference at the input of differential amplifier 464 results in an output control signal 475 that increases the gain of VGA preamplifier 432. On the other hand, if the filtered, converted Vsense signal 474 indicates that the actual current levels are above a target current level, this difference at the input of differential amplifier 464 results in an output control signal 475 that decreases the gain of VGA preamplifier 432.

[0062] In this and other examples described herein, the main LED driver is configured as a Vcc-Transistor-Filter-LED-Resistor-GND configuration. This configuration can provide direct peak-peak or RMS diode current calculation, observation, feedback and distortion control. This is in contrast to conventional Resistor-LED-GND or VCC-Resistor-LED-Transistor arrangements that are configured simply to control and define the I-V relationship of the output branch from VCC to GND.

[0063] Figure 5 illustrates an example of a digital implementation of an error converter circuit in accordance with one embodiment. This example digital error

converter circuit 538 includes a digital processing circuit 552, an analog-to-digital converter 554, an attenuator 556, a clock 557, encoders/decoders 558, and an I/O interface 559.

[0064] Because V_{sense} 574 is typically a large sine wave signal, signal attenuation may be required or desirable to meet the input requirements of the analog-to-digital converter, such as, for example, input dynamic range. The amount of attenuation can be preprogrammed, or a can be set via digital controls that can be received through I/O interface 559, encoders/decoders 558, or other input. The amount of attenuation can also be supplied to digital processing circuit 522 to reflect the original signal information to allow proper scaling while calculating any errors or offsets.

[0065] Analog-to-digital converter 554 converts the attenuated V_{sense} signal 574 from the analog domain to the digital domain. This allows the information from V_{sense} signal 574 to be processed by digital processing circuit 552. In some implementations, the resolution of analog-to-digital converter 554 can be relaxed because the target range of the bias voltage (or current) levels sensed from V_{sense} does not need to be tightly controlled with high precision. Accordingly, the resolution can be set based on system specifications or design choices.

[0066] The clock signal used to drive analog-to-digital converter 554 can be provided from clock generator circuit 557. Clock generator circuit 557 can be implemented using a phase locked loop (PLL) frequency synthesizer or other clock circuit. Output clocks can be provided at different clock frequencies depending on

the needs of the components of the system. A clock distribution network (not shown) can be used to distribute the desired clock signals to the various components. The distribution network may include buffers to match the delays introduced by various paths in the clock network based on distance, if necessary depending on the path loss and accuracy requirements. In the illustrated example, the clock frequency can be set via an external signal. In other implementations, the clock signal itself can be generated externally and provided to error converter circuit 538.

[0067] Digital processing circuit 552 receives the digitized form of the attenuated V_{sense} 574 signal and processes the signal to calculate signal characteristics such as, for example, peak, average or RMS and the DC offset (bias value) values. These data can be compared with reference values, which can be stored in registers or in memory. The reference values can be preset, or can be loaded such as, for example, via I/O interface 559. As a further example, the reference values can be stored in a ROM table or otherwise stored in memory. As a result of comparing the actual computed values from the digitized V_{sense} signal 574 with the reference values, digital processing circuit 552 generates proper digital control codes to control VGA preamplifier 532 and bias generator circuit 534. These are illustrated as gain control signal 575 and bias control signal 576. The main clock for digital processing circuit 552 can be provided by clock 557 or can be provided from an external clock. Digital processing circuit 552 can be implemented as a processor such as a general-purpose processor, a digital signal processor, or other

processing unit with associated memory to store processing instructions and provide register storage.

[0068] I/O interface 559 can include one or more interfaces to receive signals from or send signals to external components. This can be used, for example, to receive information to control or set values for error converter circuit 538. I/O interface 559 can include various interface components such as, for example, latches, shift registers, level shifters, receivers, and so on. It can be configured, for example, as a SIPO (Serial In – Parallel Out), or PIPO (Parallel In – Parallel Out) or other input/output scheme. Clock 557 or an external clock can provide any clocking necessary for I/O interface 559.

[0069] Encoder/decoder 558 can be included as a service block for miscellaneous logic that may be needed. For example, encoder decoder 550 may be included to encode and/or decode information from I/O interface 559. Encoder/decoder 558 may also include reference tables or other registers to keep serial or parallel data from I/O interface 559.

[0070] As noted above, a bias generator circuit can be implemented using two or more resistors to introduce the bias. Variable resistors can be used to control the bias at a desired point. In some embodiments, voltage controlled resistors can be used to allow feedback to control the resistance values. Figures 6 and 7 illustrate examples of bias generator circuits in accordance with various embodiments. Referring now to Figure 6, a simple bias network 610 is illustrated as a typical voltage controlled active device resistor, implemented in this example as MOS transistors

acting as voltage-controlled resistors (VCRs) to implement two bias resistors RB1, RB2. These resistors generate the bias voltage, V_g , in accordance with their relative values. This simple circuit may use fixed resistor values, which are not controllable via feedback.

[0071] In various embodiments, voltage-controlled resistors using active devices, or strings of resistors to control LED bias control are provided. One example using voltage-controlled resistors is illustrated at 620. In this example, the voltage-controlled resistor is implemented as a transistor 654 and an inductor 653 connected in series. The feedback signal provided by differential amplifier 632 (e.g., differential amplifier 462 illustrated in Figure 4) controls the resistance of transistor 654. Inductors 653 can be provided as AC block inductors, which prevent noise or interference coupling between the signal path and the DC bias path. The resultant gate voltage, V_g , can be pulled up or down based on the resistance values set by the control signals for the resistance between V_g and VCC and V_g and GND.

[0072] Figure 7 illustrates a digital approach to bias control. In this example, bias resistors RB1, RB2 may each be implemented using a string of two or more resistors 712 that can be switched in or out of the bias network via digital control. In the illustrated example, transistors are provided to switch each resistor, or a group of resistors, in or out of the bias network. In the illustrated example, AC block inductors are also provided to block AC signals while allowing a DC level to pass.

[0073] Figure 8 illustrates an example of a harmonic-free LED driver with a common-gate configuration. This example includes a VGA preamplifier 832, a bias

generator circuit 834, an error converter circuit 838, and a main LED driver 536. In various embodiments, VGA preamplifier 832, bias generator circuit 834, and error converter circuit 838 may be implemented in accordance with the various different embodiments described above. However, in the illustrated example, main LED driver 536 is shown with a common-gate configuration. This configuration may inherently provide harmonic-free output signals because the signal path does not go through the gate-drain path of the transistor T, and the signal is injected to the source node.

[0074] Generally, a common-gate configuration is normally used for current buffering, and the voltage gain is available over the drain-source resistor relationship. It may be hard to inject a large voltage signal to the source terminal due to the low impedance node when the source resistor 842 is a low value. This embodiment may be suitable for low-power, short-distance implementations, but may also be used for higher power applications where the components are chosen that can handle several amps of current. Because the high current may result in greater heat generation, heatsinks may be required for such applications.

[0075] As shown above, embodiments may be implemented in which an input sine wave (e.g., input to a VGA preamplifier) is effectively modulated and transmitted by an optical component, such as an LED, for optical communication or ranging purposes. Using a modulated signal instead of PWM dimming control as used in conventional LED dimming control methods, a large AC input signal should be applicable. When the sine wave input (or other analog input) is applied, for example, via an AC coupling capacitor as shown in the above examples, the sensing node for

the feedback loop will not be a static DC sense node any more. Especially in implementations where there is a large AC signal on top of the DC bias point. Accordingly, this sensing node cannot be directly applied via a feedback network as it might otherwise be applied in conventional solutions. Also applying a large, pre-amplified signal to MOSFET devices (or Bipolar Junction Transistors) will introduce second-order and higher-order harmonics, as discussed above. In LED-based ranging systems or other systems, the receiver photodiode may also generate harmonics. During this process, 2nd order harmonics may cause second-order Inter-Modulation Distortion and corrupt the received signal information. Accordingly, embodiments discussed above may be implemented to ensure that the signal provided to the LED is a single-tone with minimum or reduced harmonics.

[0076] Figure 9 illustrates an example process for providing an LED drive signal in accordance with one embodiment. With reference now to figure 9, at operation 911, a drive circuit receives the modulating signal for transmission using an LED. Modulating signal can be, for example, a sine wave or other signal as described above. The LED to be driven can include a single LED or an array of LEDs.

[0077] At operation 912, a preamplifier amplifies the modulating signal to generate a preamplifier modulating signal. The amount of pre-amplification supplied can be selected based on the desired output level of the LED to be driven. At operation 914, a bias circuit adds a DC bias component to the pre-amplified modulating signal. The DC biased pre-amplified modulating signal is amplified at operation 924 to create an LED drive signal.

[0078] At operation 928, the LED drive signal can be filtered to remove unwanted harmonics (e.g., second-order and higher-order harmonics) that might be present in the signal. The LED drive signal, after filtering, can be applied to an anode of the LED to drive the LED. This is illustrated at operation 944. Additionally, resistor can be connected between the cathode of the LED.

[0079] At operation 968, the drive signal can be used to provide feedback to an error converter circuit to adjust the amount of gain applied by the preamplifier or the amount of bias applied by the bias circuit, or both, depending on the characteristics of the drive signal. Accordingly, a sense signal can be provided as a feedback signal to the error converter circuit from a node coupled to the cathode of the LED. The error converter circuit can be implemented as an analog, digital, or mixed-signal circuit. Likewise, the LED driver circuit can be implemented as an analog circuit or various components as may be desired by the system designer.

[0080] Figure 10 illustrates an example process for an error converter circuit implemented in the analog domain according to one embodiment. As this diagram illustrates in the upper half of the figure, preamplifier gain can be controlled by the error converter circuit. At operation 1012, the received sense signal, V_{sense} , is high-pass filtered to obtain an AC component, and AC-DC conversion calculates the amplitude or RMS values. The received sense signal, V_{sense} , is also low-pass filtered as further described below.

[0081] At operation 1014, the AC amplitude or RMS values of the drive signal can be supplied to an input of a differential amplifier. Target AC amplitude or RMS

values of a target drive signal can be supplied to another input of the differential amplifier. The differential amplifier can generate a control signal (e.g., an error signal) based on the difference between the target magnitude or RMS value from the DAC and the magnitude or RMS value information extracted from the drive signal via Vsense.

[0082] At operation 1016, the control signals applied to the preamplifier to control the gain of the preamplifier based on the differences. This control signal may be used to control the amount of gain applied by the preamplifier to the modulating signal. For example, the control signal can be based on differences between the value of the LED drive signal and the target magnitude or RMS value set by the DAC. As a further example, where the drive signal is at a level that is too low as compared to the target signal, the control signal can increase the gain of the preamplifier. On the other hand, where the drive signal is at a higher level as compared to the target signal, and control signal can decrease the gain of the preamplifier.

[0083] Similarly, as illustrated in the lower half of the figure, the main amplifier's DC bias levels can be controlled by the error converter circuit as well. At operation 1022, the sense signal received from the drive circuit is low-pass filtered to obtain DC bias information of the drive signal.

[0084] At operation 1024, a differential amplifier is used to generate a bias signal based on a difference between the DC bias level information derived from the sense signal, Vsense, and a target DC level from the DAC reference output. A voltage

level at the output of the differential amplifier is proportional to the difference at the inputs. This output forms a control signal for the bias generator circuit.

[0085] At operation 1026, the control signal applied to the bias generator circuit to control the resistance of resistors (e.g., using voltage-controlled resistors) in the bias generator circuit. Where the detected level of the DC bias is too low, the control signal can adjust the resistance levels in the bias circuit to increase the level of DC bias applied to the amplified modulated signal. Likewise, where the detected level of the DC bias is too high, the control signal can adjust the resistance levels in the bias circuit to decrease the level of DC bias applied to the amplified modulated signal.

[0086] As described above, in addition to analog applications, the error converter circuit may be implemented using a digital application. In such applications, an attenuator may be included to attenuate the sense signal received from the LED driver. The attenuated signal can be digitized such that it can be processed in the digital domain. A DSP, general-purpose processor, or other digital circuit can be used to compare the sensed AC and DC signal characteristics of the drive signal with target AC and DC signal characteristics and generate the appropriate control signals to adjust the amount of gain applied by the preamplifier, the amount of bias supplied by the DC bias circuit, or both.

[0087] The terms “substantially” and “about” as may be used throughout this disclosure, including the claims, are used to describe and account for small fluctuations, such as due to variations in processing. For example, they can refer to

less than or equal to $\pm 5\%$, such as less than or equal to $\pm 2\%$, such as less than or equal to $\pm 1\%$, such as less than or equal to $\pm 0.5\%$, such as less than or equal to $\pm 0.2\%$, such as less than or equal to $\pm 0.1\%$, such as less than or equal to $\pm 0.05\%$.

[0088] The term “coupled” refers to direct or indirect joining, connecting, fastening, contacting or linking, and may refer to various forms of coupling such as physical, optical, electrical, fluidic, mechanical, chemical, magnetic, electromagnetic, optical, communicative or other coupling, or a combination of the foregoing. Where one form of coupling is specified, this does not imply that other forms of coupling are excluded. For example, one component physically coupled to another component may reference physical attachment of or contact between the two components (directly or indirectly), but does not exclude other forms of coupling between the components such as, for example, a communications link (e.g., an RF or optical link) also communicatively coupling the two components. Likewise, the various terms themselves are not intended to be mutually exclusive. For example, a fluidic coupling, magnetic coupling or a mechanical coupling, among others, may be a form of physical coupling.

[0089] As used herein, a circuit or other component might be implemented utilizing any form of hardware, software, or a combination thereof. For example, one or more processors, controllers, ASICs, PLAs, PALs, CPLDs, FPGAs, logical components, software routines or other mechanisms might be implemented to make up a circuit. In implementation, the various circuits described herein might be implemented as discrete circuits or the functions and features described can be

shared in part or in total among one or more circuits. In other words, as would be apparent to one of ordinary skill in the art after reading this description, the various features and functionality described herein may be implemented in any given application and can be implemented in one or more separate or shared circuits in various combinations and permutations. Even though various features or elements of functionality may be individually described or claimed as separate circuits, one of ordinary skill in the art will understand that these features and functionality can be shared among one or more common circuits, and such description shall not require or imply that separate circuits are required to implement such features or functionality.

[0090] Where circuits are implemented in whole or in part using software, in one embodiment, these software elements can be implemented to operate with a computing or processing system capable of carrying out the functionality described with respect thereto. One such example computing system is shown in Figure 11. Various embodiments are described in terms of this example-computing system 1100. After reading this description, it will become apparent to a person skilled in the relevant art how to implement the technology using other computing systems or architectures.

[0091] Referring now to Figure 11, computing system 1100 may represent, for example, computing or processing capabilities found within desktop, laptop and notebook computers; hand-held computing devices (smart phones, cell phones, palmtops, tablets, etc.); mainframes, supercomputers, workstations or servers; or

any other type of special-purpose or general-purpose computing devices as may be desirable or appropriate for a given application or environment. Computing system 1100 might also represent computing capabilities embedded within or otherwise available to a given device. For example, a computing system might be found in other electronic devices such as, for example, digital cameras, navigation systems, cellular telephones, portable computing devices, modems, routers, WAPs, terminals and other electronic devices that might include some form of processing capability.

[0092] Computing system 1100 might include, for example, one or more processors, controllers, control modules, or other processing devices, such as a processor 1104. Processor 1104 might be implemented using a general-purpose or special-purpose processing engine such as, for example, a microprocessor (whether single-, dual- or multi-core processor), signal processor, graphics processor (e.g., GPU) controller, or other control logic. In the illustrated example, processor 1104 is connected to a bus 1102, although any communication medium can be used to facilitate interaction with other components of computing system 1100 or to communicate externally.

[0093] Computing system 1100 might also include one or more memory modules, simply referred to herein as main memory 1108. For example, in some embodiments random access memory (RAM) or other dynamic memory, might be used for storing information and instructions to be executed by processor 1104. Main memory 1108 might also be used for storing temporary variables or other intermediate information during execution of instructions to be executed by

processor 1104. Computing system 1100 might likewise include a read only memory ("ROM") or other static storage device coupled to bus 1102 for storing static information and instructions for processor 1104.

[0094] The computing system 1100 might also include one or more various forms of information storage mechanism 1110, which might include, for example, a media drive 1112 and a storage unit interface 1120. The media drive 1112 might include a drive or other mechanism to support fixed or removable storage media 1114. For example, a hard disk drive, a floppy disk drive, a magnetic tape drive, an optical disk drive, a CD or DVD drive (R or RW), a flash drive, or other removable or fixed media drive might be provided. Accordingly, storage media 1114 might include, for example, a hard disk, a floppy disk, magnetic tape, cartridge, optical disk, a CD or DVD, or other fixed or removable medium that is read by, written to or accessed by media drive 1112. As these examples illustrate, the storage media 1114 can include a computer usable storage medium having stored therein computer software or data.

[0095] In alternative embodiments, information storage mechanism 1110 might include other similar instrumentalities for allowing computer programs or other instructions or data to be loaded into computing system 1100. Such instrumentalities might include, for example, a fixed or removable storage unit 1122 and an interface 1120. Examples of such storage units 1122 and interfaces 1120 can include a program cartridge and cartridge interface, a removable memory (for example, a flash memory or other removable memory module) and memory slot, a

flash drive and associated slot (for example, a USB drive), a PCMCIA slot and card, and other fixed or removable storage units 1122 and interfaces 1120 that allow software and data to be transferred from the storage unit 1122 to computing system 1100.

[0096] Computing system 1100 might also include a communications interface 1124. Communications interface 1124 might be used to allow software and data to be transferred between computing system 1100 and external devices. Examples of communications interface 1124 might include a modem or softmodem, a network interface (such as an Ethernet, network interface card, WiMedia, IEEE 802.XX, Bluetooth® or other interface), a communications port (such as for example, a USB port, IR port, RS232 port, or other port), or other communications interface. Software and data transferred via communications interface 1124 might typically be carried on signals, which can be electronic, electromagnetic (which includes optical) or other signals capable of being exchanged by a given communications interface 1124. These signals might be provided to communications interface 1124 via a channel 1128. This channel 1128 might carry signals and might be implemented using a wired or wireless communication medium. Some examples of a channel might include a phone line, a cellular link, an RF link, an optical link, a network interface, a local or wide area network, and other wired or wireless communications channels.

[0097] In this document, the terms "computer program medium" and "computer usable medium" are used to generally refer to media such as, for

example, memory 1108, storage unit 1120, media 1114, and channel 1128. These and other various forms of computer program media or computer usable media may be involved in carrying one or more sequences of one or more instructions to a processing device for execution. Such instructions embodied on the medium, are generally referred to as “computer program code” or a “computer program product” (which may be grouped in the form of computer programs or other groupings). When executed, such instructions might enable the computing system 1100 to perform features or functions of the disclosed technology as discussed herein.

[0098] While various embodiments of the disclosed technology have been described above, it should be understood that they have been presented by way of example only, and not of limitation. Likewise, the various diagrams may depict an example architectural or other configuration for the disclosed technology, which is done to aid in understanding the features and functionality that can be included in the disclosed technology. The disclosed technology is not restricted to the illustrated example architectures or configurations, but the desired features can be implemented using a variety of alternative architectures and configurations. Indeed, it will be apparent to one of skill in the art how alternative functional, logical or physical partitioning and configurations can be implemented to implement the desired features of the technology disclosed herein. Also, a multitude of different constituent module names other than those depicted herein can be applied to the various partitions. Additionally, with regard to flow diagrams, operational descriptions and method claims, the order in which the steps are presented herein

shall not mandate that various embodiments be implemented to perform the recited functionality in the same order unless the context dictates otherwise.

[0099] Although the disclosed technology is described above in terms of various exemplary embodiments and implementations, it should be understood that the various features, aspects and functionality described in one or more of the individual embodiments are not limited in their applicability to the particular embodiment with which they are described, but instead can be applied, alone or in various combinations, to one or more of the other embodiments of the disclosed technology, whether or not such embodiments are described and whether or not such features are presented as being a part of a described embodiment. Thus, the breadth and scope of the technology disclosed herein should not be limited by any of the above-described exemplary embodiments.

[00100] Terms and phrases used in this document, and variations thereof, unless otherwise expressly stated, should be construed as open ended as opposed to limiting. As examples of the foregoing: the term “including” should be read as meaning “including, without limitation” or the like; the term “example” is used to provide exemplary instances of the item in discussion, not an exhaustive or limiting list thereof; the terms “a” or “an” should be read as meaning “at least one,” “one or more” or the like; and adjectives such as “conventional,” “traditional,” “normal,” “standard,” “known” and terms of similar meaning should not be construed as limiting the item described to a given time period or to an item available as of a given time, but instead should be read to encompass conventional,

traditional, normal, or standard technologies that may be available or known now or at any time in the future. Likewise, where this document refers to technologies that would be apparent or known to one of ordinary skill in the art, such technologies encompass those apparent or known to the skilled artisan now or at any time in the future.

[00101] The presence of broadening words and phrases such as “one or more,” “at least,” “but not limited to” or other like phrases in some instances shall not be read to mean that the narrower case is intended or required in instances where such broadening phrases may be absent. The use of the term “module” does not imply that the components or functionality described or claimed as part of the module are all configured in a common package. Indeed, any or all of the various components of a module, whether control logic or other components, can be combined in a single package or separately maintained and can further be distributed in multiple groupings or packages or across multiple locations.

[00102] Additionally, the various embodiments set forth herein are described in terms of exemplary block diagrams, flow charts and other illustrations. As will become apparent to one of ordinary skill in the art after reading this document, the illustrated embodiments and their various alternatives can be implemented without confinement to the illustrated examples. For example, block diagrams and their accompanying description should not be construed as mandating a particular architecture or configuration.

Claims

What is claimed is:

1. An LED driver circuit, comprising:
 - a preamplifier comprising an input to receive a modulation signal and an output to drive a preamplified modulation signal;
 - a bias generator circuit coupled to the preamplifier output to apply a DC bias level to the preamplified modulation signal;
 - a main LED driver circuit comprising:
 - a power transistor to amplify the preamplified modulation signal with the applied DC bias to generate an LED drive signal, the transistor comprising a gate coupled to the bias generator circuit, a drain coupled to a voltage source, and a source;
 - a filter comprising an input coupled to the source of the transistor and an output,
 - an LED comprising an anode coupled to the output of the filter and a cathode; and
 - a resistor connected between the cathode of the LED and electrical ground; and
 - an error converter circuit comprising an input coupled to receive a sense signal from the main LED driver circuit and an output to control a gain of the preamplifier to adjust output levels of the amplified modulation signal based on a difference between target signal levels and signal levels of the LED drive signal as

determined using the sense signal; and a second output to control a DC bias level applied to the amplified modulation signal.

2. The LED driver circuit of claim 1, wherein the filter comprises a trap or notch filter to filter out second-order harmonics from the LED drive signal.

3. The LED driver circuit of claim 2, wherein the filter comprises a low-pass filter to filter out higher-order harmonics from the LED drive signal.

4. The LED driver circuit of claim 1, wherein the error converter circuit comprises:

a low-pass filter comprising an input coupled to receive the sense signal, and an output to output a DC bias component of the received sense signal;

a differential amplifier comprising a first input coupled to receive the DC bias component of the received sense signal from the low-pass filter, a second input coupled to receive a target DC bias level for the LED drive signal, and an output to output a control voltage to control the DC bias level provided by the bias generator circuit.

5. The LED driver circuit of claim 4, wherein the bias generator circuit comprises a plurality of voltage-controlled resistors, and the control voltage output from the differential amplifier controls the resistance of at least one of the voltage-controlled resistors of the bias generator circuit.

6. The LED driver circuit of claim 1, wherein the error converter circuit comprises:

a high-pass filter comprising an input coupled to receive the sense signal, and an output to output an AC component of the received sense signal;

an AC to DC converter circuit to convert the AC component of the received sense signal to a DC amplitude or RMS level, comprising an input coupled to receive the AC component of the received sense signal from the high-pass filter and an output to output the DC amplitude or RMS level; and

a differential amplifier comprising a first input coupled to receive the DC amplitude or RMS level and a second input coupled to receive a target level for the drive signal, and an output to output a control signal to control a gain of the preamplifier based on a difference between the received DC amplitude or RMS level and the received target level.

7. The LED driver circuit of claim 1, wherein the error converter circuit comprises:

an analog-to-digital converter to convert the sense signal from an analog waveform to a digital value, comprising an input coupled to receive the sense signal from the main LED driver, and an output to output a digital representation of the sense signal;

a digital processing circuit, comprising an input coupled to receive the digital representation of the sense signal, a first output to control a gain of the preamplifier,

and a second output to control the amount of DC bias applied by the bias generator circuit.

8. The LED driver circuit of claim 7, wherein the digital processing circuit determines a DC bias component of the received sense signal, compares the DC bias component of the received sense signal to a target DC bias level for the LED drive signal and outputs via the second output a control signal to control the amount of DC bias applied by the bias generator.

9. The LED driver circuit of claim 8, wherein the bias generator circuit comprises a plurality of resistors and switches, and the output control signal from the digital processing circuit comprises a codeword to switch at least one of the plurality of resistors into the bias generator circuit.

10. The LED driver circuit of claim 7, wherein the digital processing circuit determines an AC amplitude or RMS value of the received sense signal, compares the AC amplitude or RMS value of the received sense signal to a target signal level for the LED drive signal and outputs via the first output a control signal to control the gain of the preamplifier.

11. The LED driver circuit of claim 10, wherein the preamplifier comprises an operational amplifier and a plurality of resistors in a feedback loop in parallel between an output and an input of the operational amplifier, and the control signal

output from the digital processing circuit comprises a codeword to switch at least one of the plurality of resistors into the feedback loop.

12. The LED driver circuit of claim 10, wherein comparing the AC amplitude or RMS value of the received sense signal to a target signal level for the LED drive signal comprises comparing an RMS value of the AC amplitude or RMS value of the received sense signal to a target RMS reference level.

13. The LED driver circuit of claim 1, wherein the control voltage to control the DC bias level provided by the bias generator circuit effectuates transistor bias control of the power transistor without being applied directly to the gate of the power transistor.

14. The LED driver circuit of claim 7, wherein the digital processing circuit further comprises an attenuator to attenuate the received sense signal before passing it to the analog-to-digital converter.

15. The LED driver circuit of claim 1, wherein the first and second outputs of the error converter circuit comprise control signals that avoid direct contact with the signal path of the modulating signal and the LED drive signal.

16. The LED driver circuit of claim 1, wherein the error converter circuit further comprises a power controller to turn off at least the transistor in the main LED driver or the preamplifier when the error converter circuit is disabled.

17. The LED driver circuit of claim 1, wherein the bias generator circuit comprises two sets of one or more voltage-controlled resistors and an inductor coupled between each set of resistors and the signal path of the modulating signal to reduce noise and signal interference to active devices in the LED driver circuit.

18. The LED driver circuit of claim 1, wherein the LED comprises a single LED or an array of LEDs.

19. The LED driver circuit of claim 1, wherein the modulating signal comprises a sine wave at a determined frequency.

20. The LED driver circuit of claim 1, wherein the bias generator circuit is indirectly coupled to the preamplifier circuit to avoid introducing interference to the preamplified modulation signal due to direct contact.

21. A method for driving an LED, comprising:

a preamplifier receiving a modulating signal and amplifying the modulating signal to generate an amplified modulating signal;

a bias generator adding a DC bias component to the amplified modulating signal to generate a DC biased amplified modulating signal;

an LED driver amplifying the DC biased amplified modulating signal to generate a drive signal at a desired signal power level to drive in LED.

22. The method of claim 21, further comprising an error converter circuit receiving a sense signal from the LED driver, determining a DC bias component of the received sense signal and sending a control signal to control the amount of bias added by the bias generator based on a DC level of the DC bias component of the received sense signal.

23. The method of claim 22, further comprising determining a difference between the DC bias component of the received sense signal and a desired amount of DC bias for the drive signal, and generating the control signal to control the amount of bias as a function of the determined difference.

24. The method of claim 22, wherein determining a DC bias component of the received sense signal comprises low pass filtering the received sense signal.

25. The method of claim 21, further comprising an error converter circuit receiving a sense signal from the LED driver, determining an AC component of the received sense signal and sending a control signal to control an amount of gain of the preamplifier based on the determined AC component of the received sense signal.

26. The method of claim 25, further comprising determining a difference between characteristics of the AC component of the received sense signal and desired characteristics of the drive signal, and generating the control signal to control the amount of gain of the preamplifier as a function of the determined difference.

27. The method of claim 25, further comprising converting the AC component of the receive sense signal to an amplitude or RMS level.

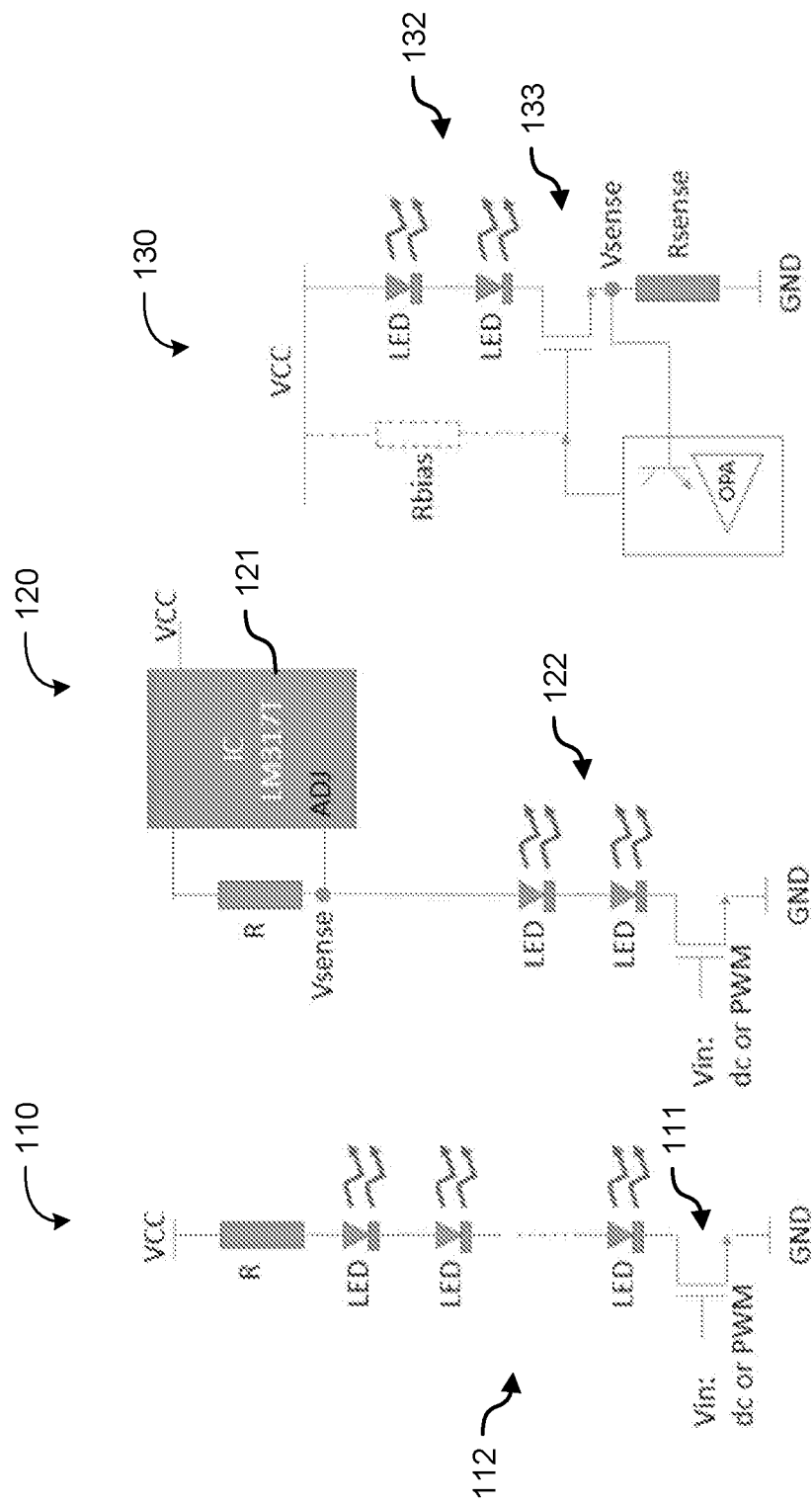


Fig. 1

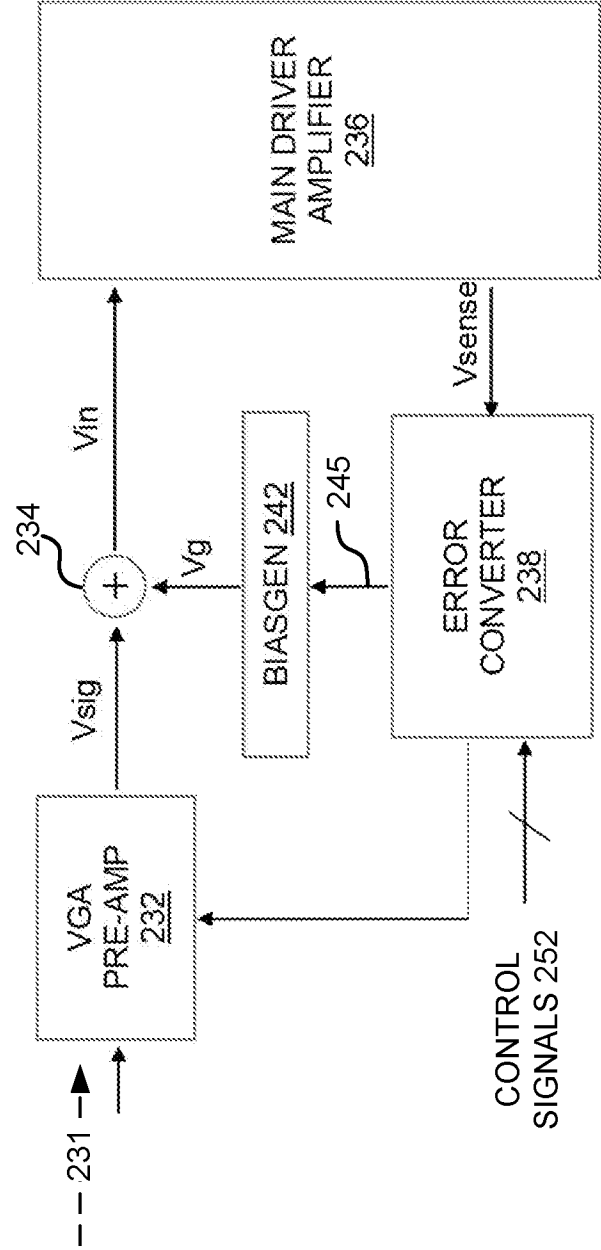


Fig. 2

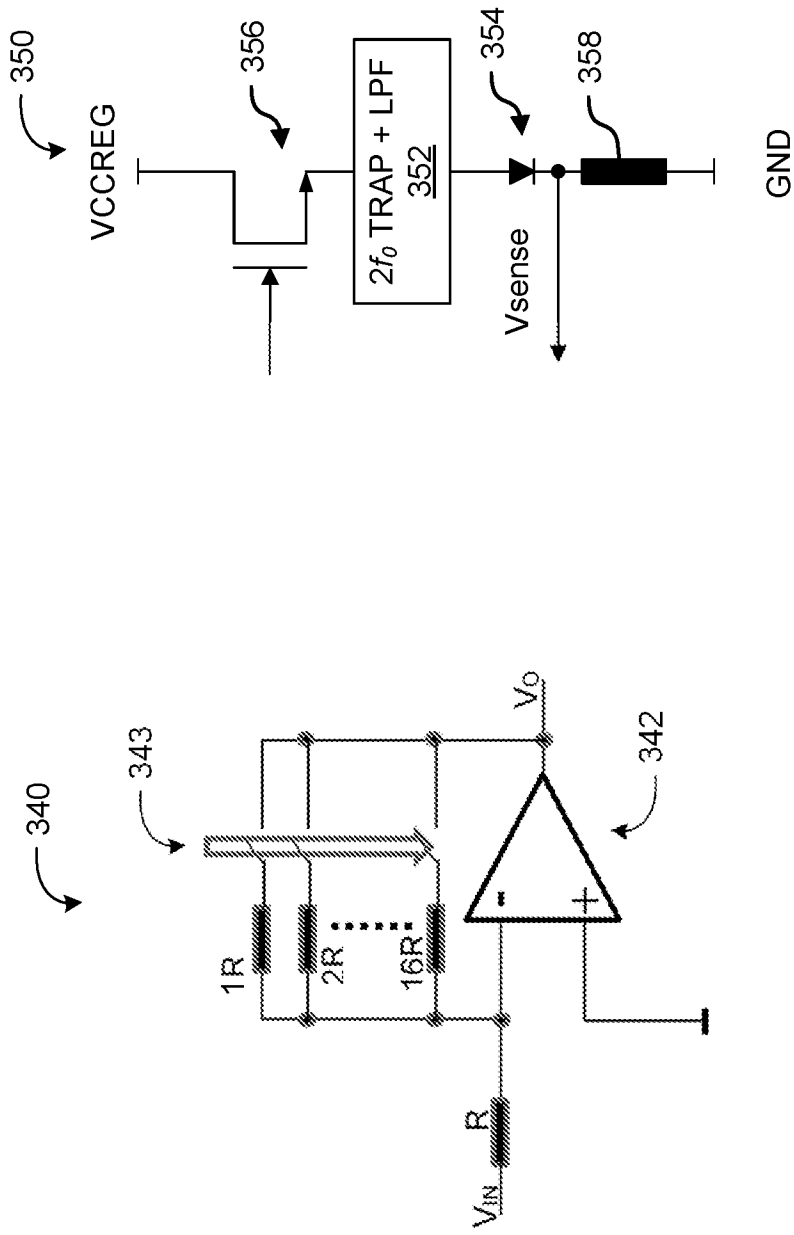


Fig. 3

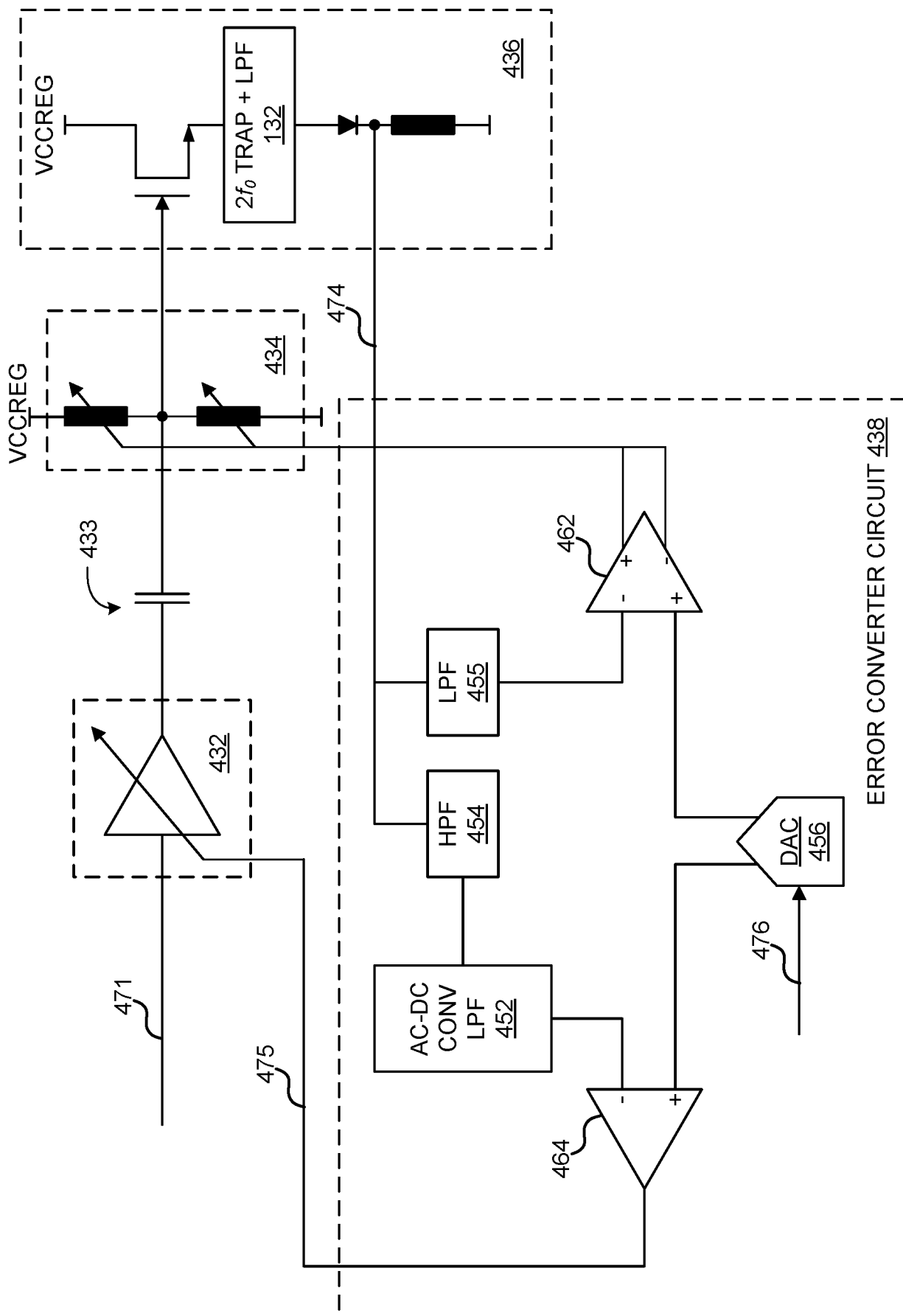


Fig. 4

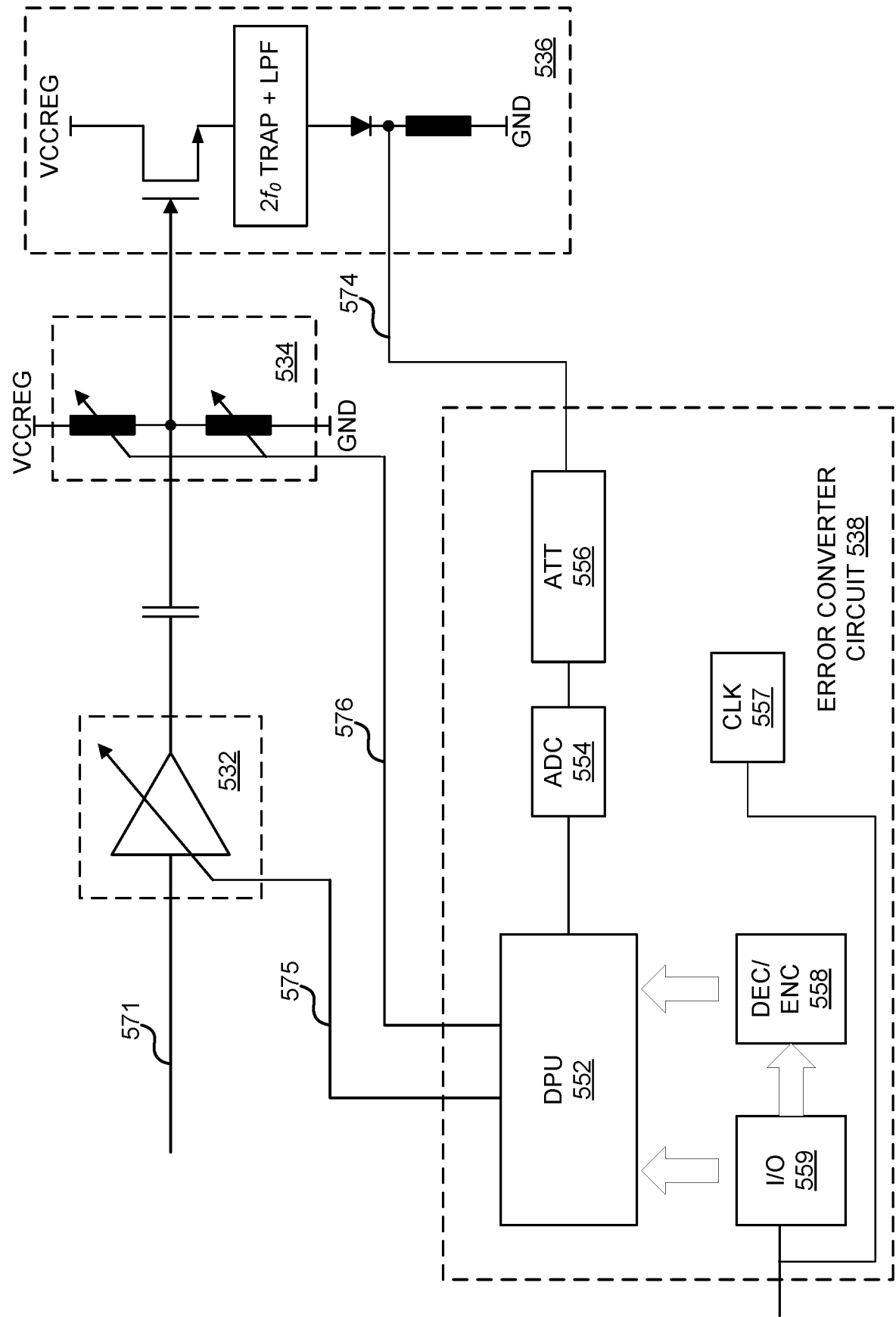


Fig. 5

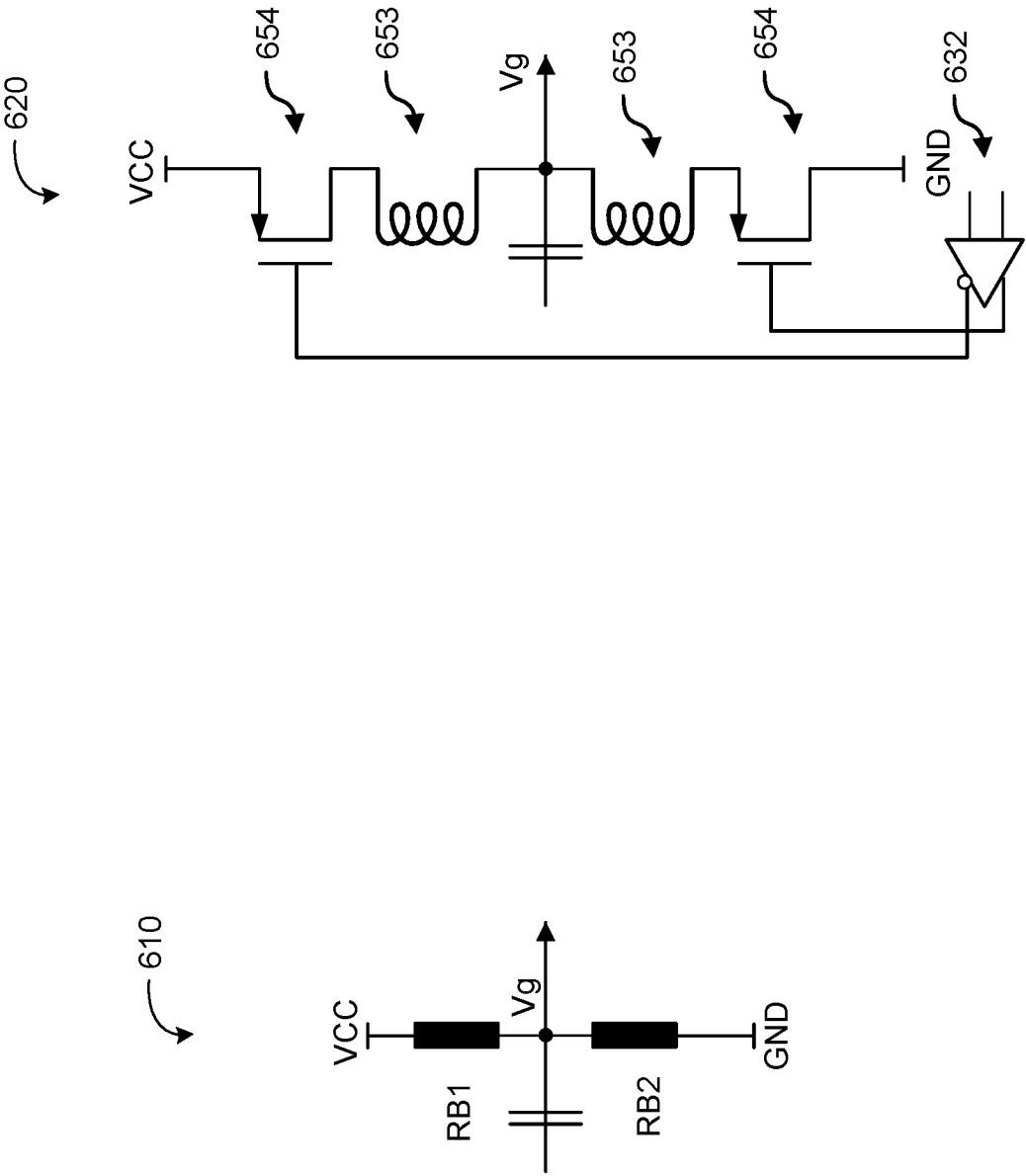


Fig. 6

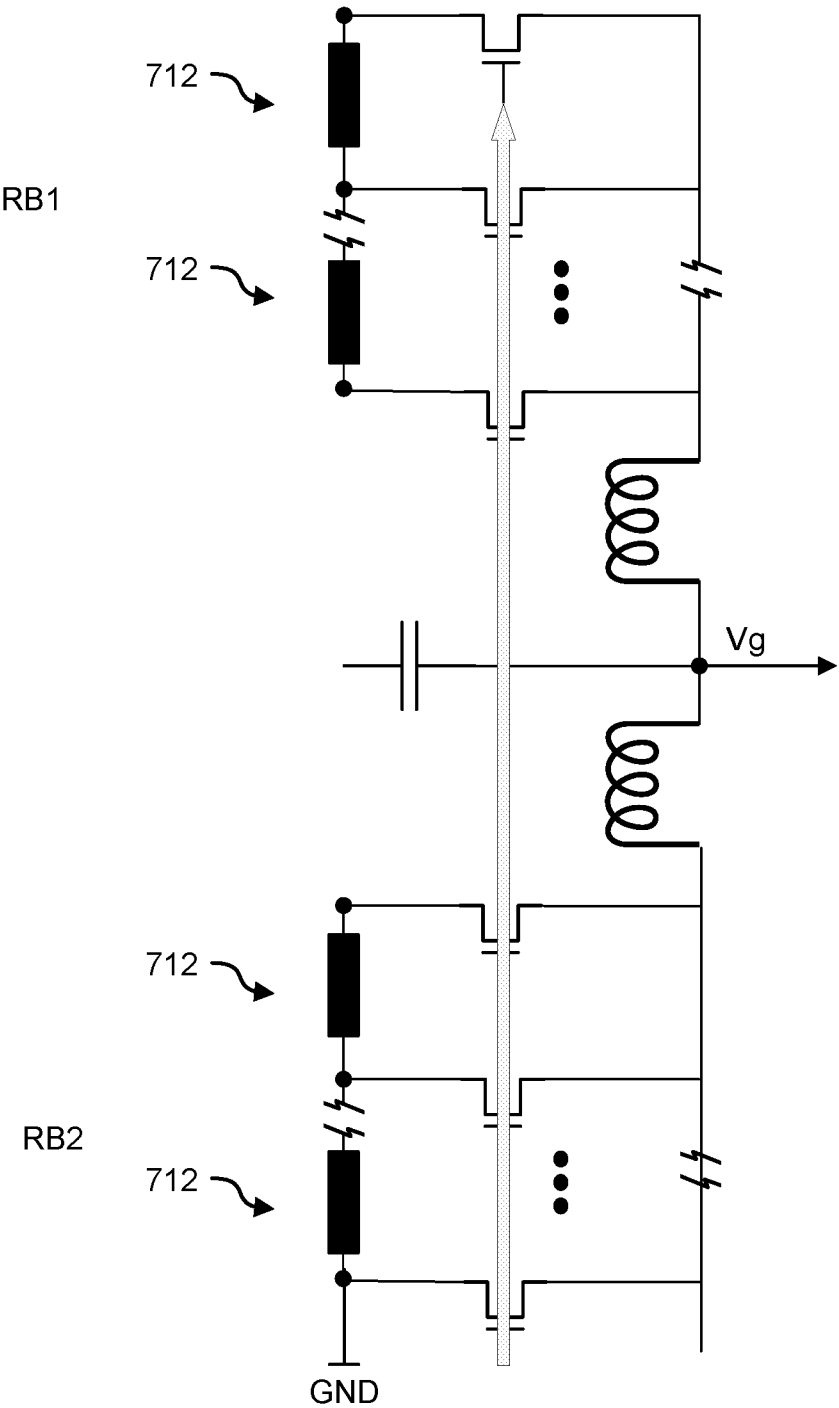


Fig. 7

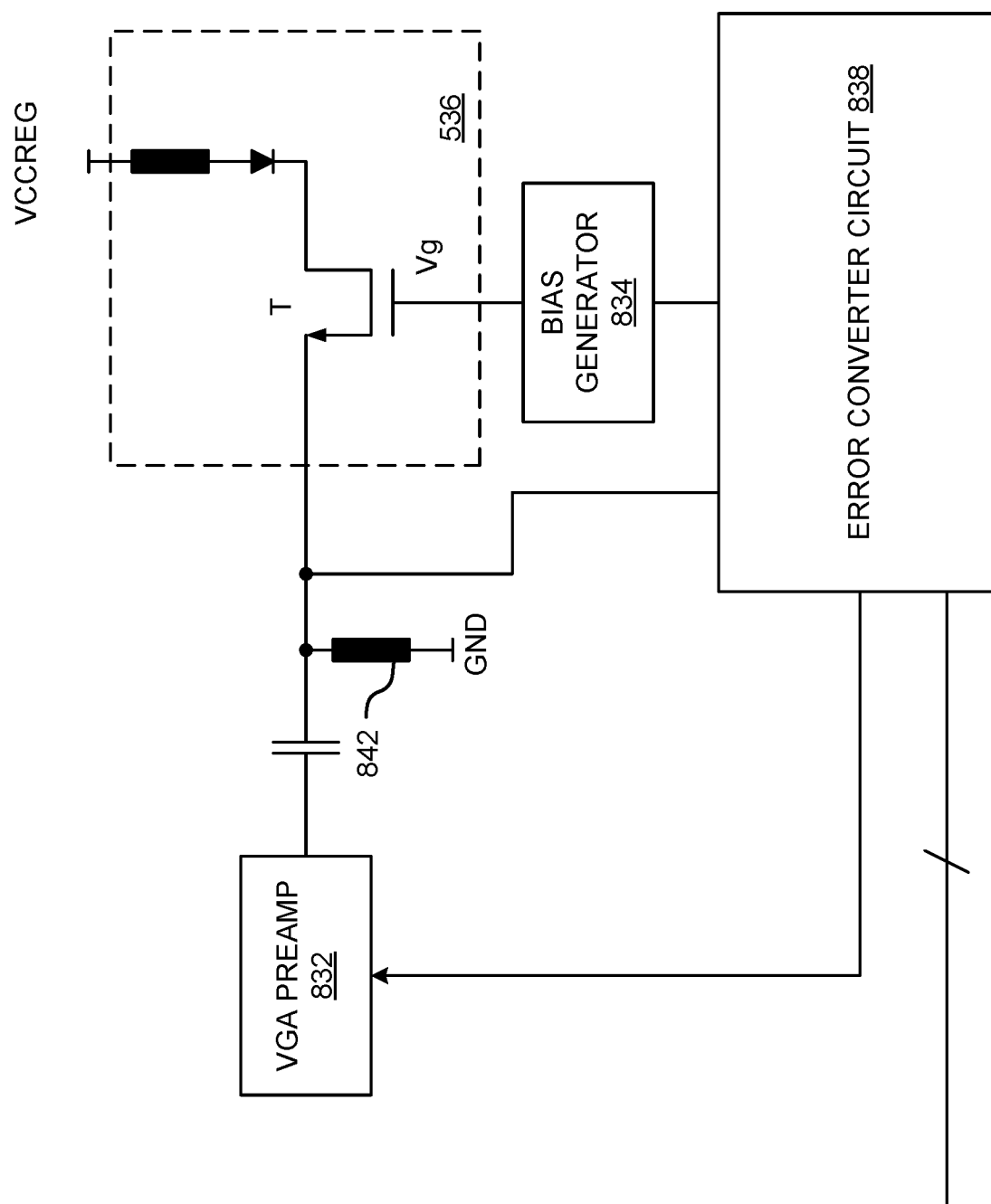


Fig. 8

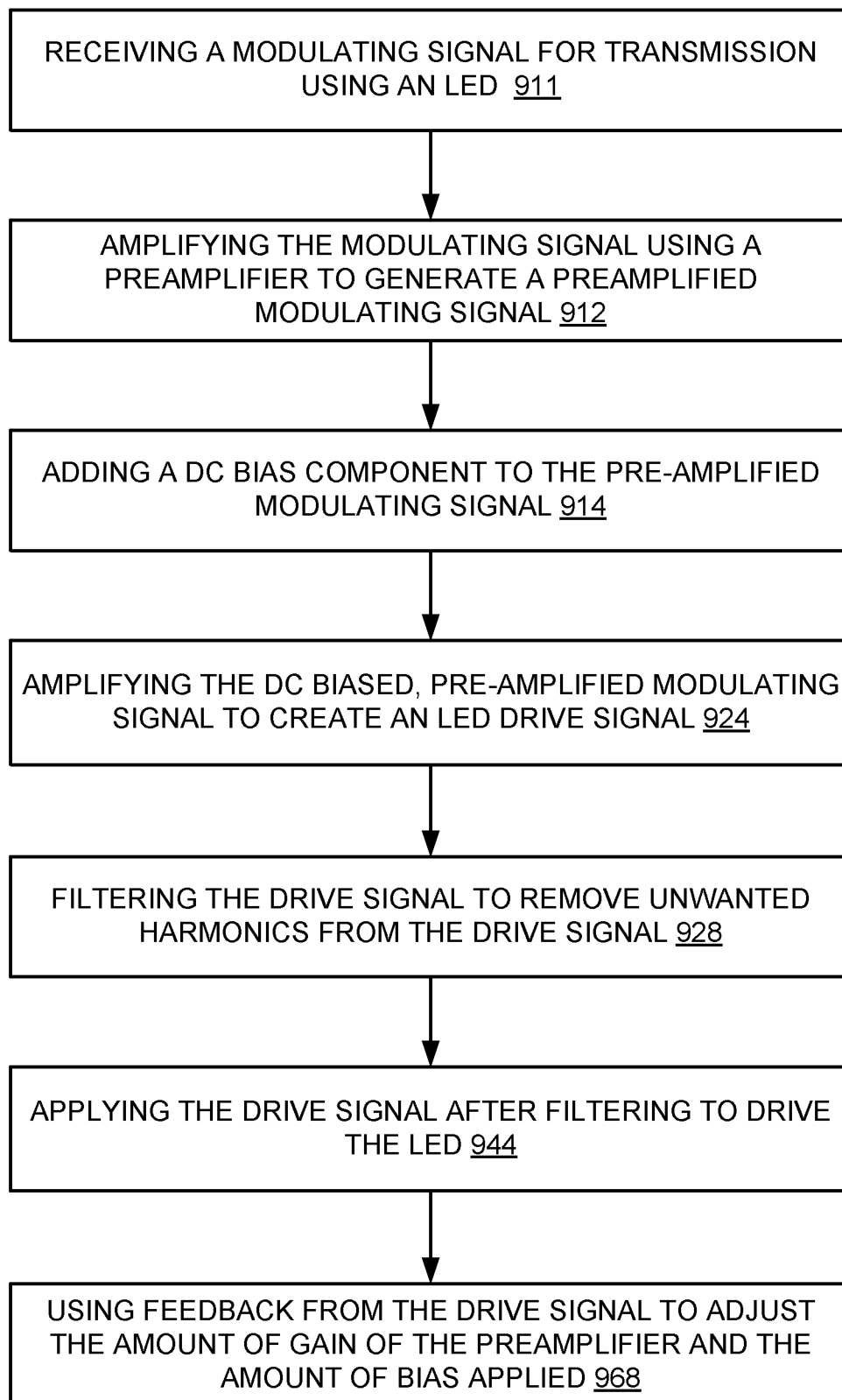


Fig. 9

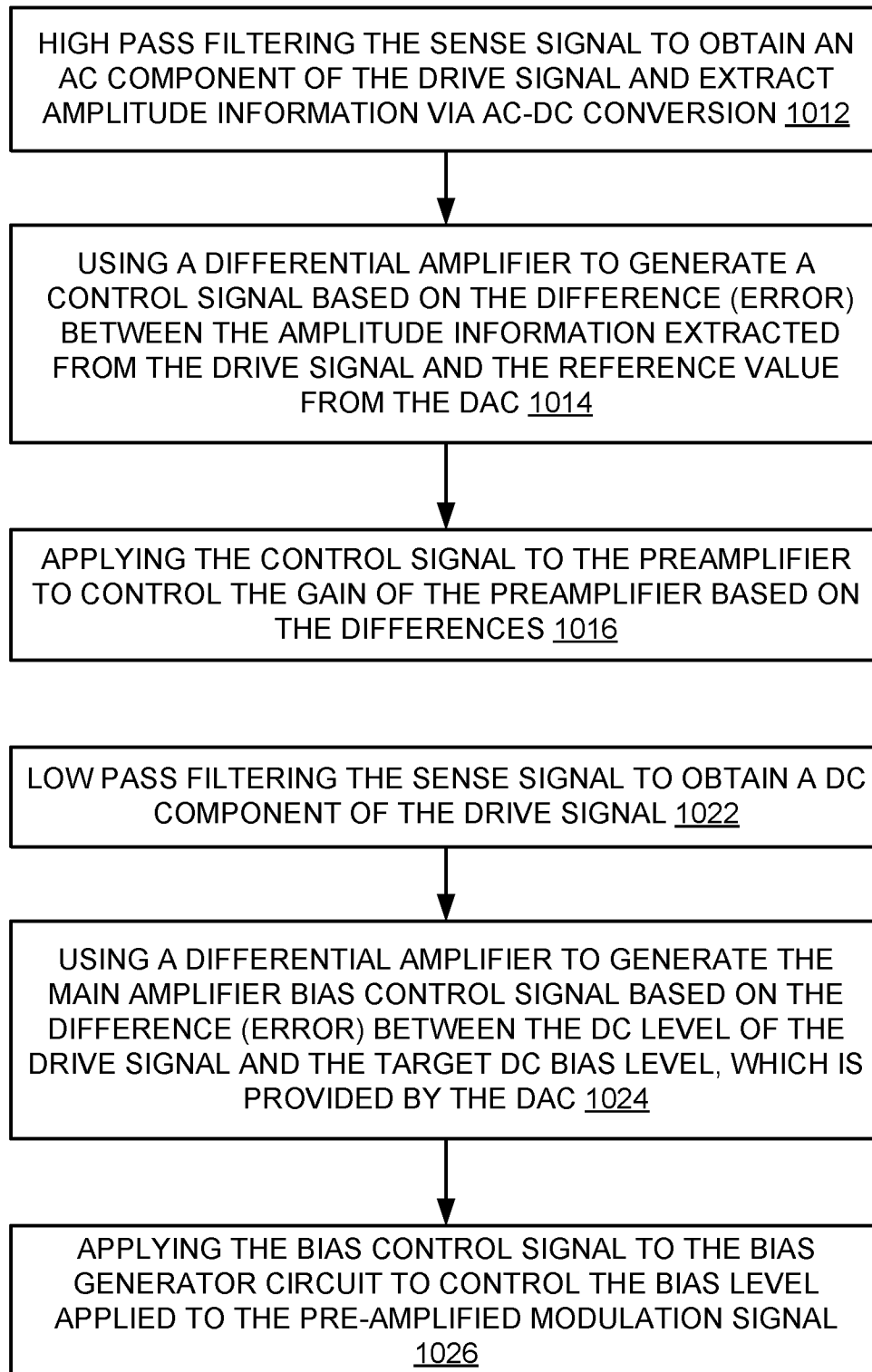


Fig. 10

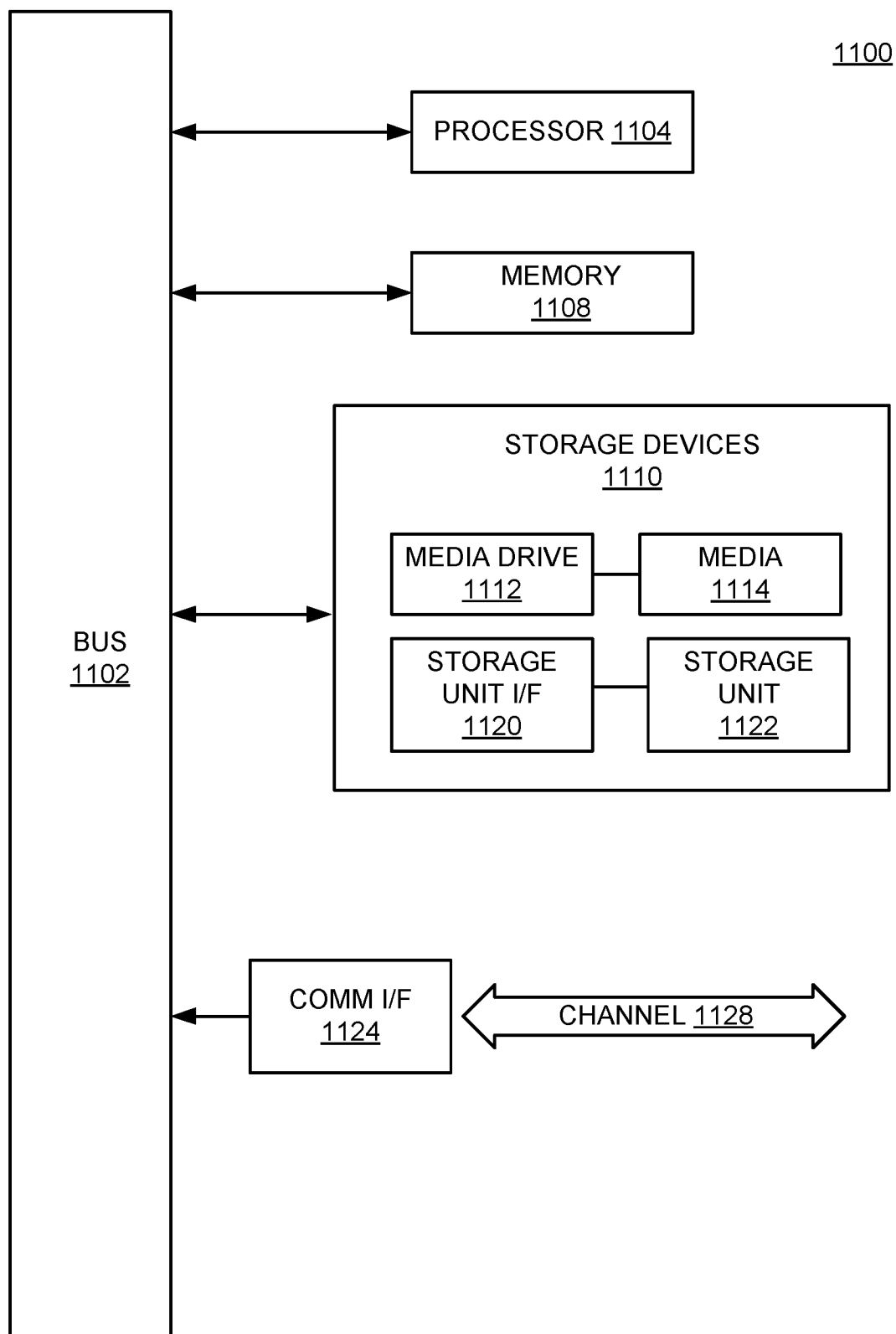


Fig. 11

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2018/001157

A. CLASSIFICATION OF SUBJECT MATTER

INV. G01S7/481 G01S7/484 H04B10/116 G01S7/491
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H04B H05B G01S H01L H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EP0-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP S55 93281 A (MATSUSHITA ELECTRIC IND CO LTD) 15 July 1980 (1980-07-15) the whole document -----	1-27
Y	JP S59 19382 A (FUJITSU LTD) 31 January 1984 (1984-01-31) the whole document -----	1-27
Y	US 2006/126683 A1 (KANG HO Y [KR] ET AL) 15 June 2006 (2006-06-15) paragraph [0052]; figure 1 -----	4,15,23, 25,26
Y	EP 0 595 018 A2 (BOSCH GMBH ROBERT [DE]) 4 May 1994 (1994-05-04) figure 1 -----	13,17, 20,22

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

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"&" document member of the same patent family

Date of the actual completion of the international search

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

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