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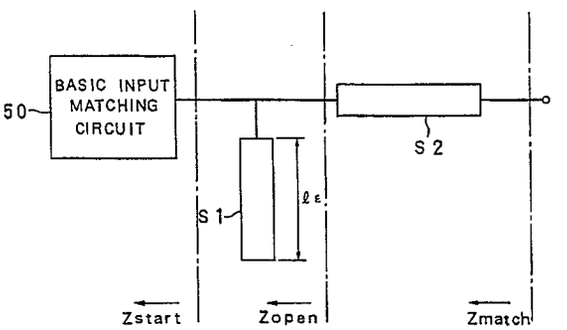
(54) Input matching circuit and method for adjusting the same.

(57) An input matching network in an input circuit of an amplifier comprises a basic input matching circuit (50) including a serial inductance, a strip line of an approximately quarter wavelength connected in series to the basic matching circuit, and a parallel capacitance including an open stub (S1) connected between the strip line and the basic input matching circuit (50). An electrical length (l_ϵ) of the open stub (S1) is selected such that a phase angle of a signal source reflection coefficient as viewed from the amplifier is larger than a mean value of manufacturing variations of a phase angle of an optimum signal source power reflection coefficient of the amplifier. By shortening the electrical length (l_ϵ) of the open stub (S1) by cutting it by a laser, a matching point can be adjusted to comply to substantially entire distribution of the manufacturing variations of the optimum signal source power reflection coefficient of the amplifier.

Fig. 7



EP 0 456 207 A2

Background of the Invention

(Field of the Invention)

The present invention relates to an input matching network (circuit) in an input circuit of a low noise amplifier used in a down-converter for use in a direct broadcast satellite (DBS) system.

(Related Background Art)

A noise figure (NF) of an amplifier which uses a field effect transistor (FET) varies with a source impedance as viewed from the FET into the signal source and it is minimum at a certain source impedance. This source impedance is called an optimum source impedance Z_{opt}. In a low noise amplifier, an input matching network in an input circuit of the FET is adjusted such that the source impedance as viewed from the FET is equal to the optimum source impedance Z_{opt}. Namely, the input matching network in the input circuit of the FET is adjusted such that a source reflection coefficient as viewed from the FET is equal to an optimum source reflection coefficient Γ_{opt}.

However, the optimum source reflection coefficient Γ_{opt} varies with a manufacturing variation of the FET. Thus, in the prior art input matching circuit of the low noise amplifier, design was made such that the reflection coefficient of the signal source as viewed from the FET is equal to a mean value of the manufacturing variations of the optimum source reflection coefficient Γ_{opt}.

However, where the input matching network is matched to the mean value of the manufacturing variations of the optimum source reflection coefficient Γ_{opt} of the FET, the NF of the amplifier includes a variation and a high manufacturing yield cannot be attained.

On the other hand, an attempt has been made to reduce the variation of characteristic of the amplifier due to the manufacturing variation of the FET by varying a shape and a size of a device of the input matching network every amplifier manufactured. For example, an article "A 2.5 Watts High Efficiency X-band Power MMIC", in IEEE 1989 microwave and millimeter wave monolithic circuits Symposium discloses the following technique. A MMIC (microwave monolithic integrated circuit) having a low noise amplifier built therein is packaged on a ceramic substrate, and an adjusting circuit is also formed on the ceramic substrate together with the MMIC. Wires are bonded to island-like pads on the opposite sides form a center strip line while a characteristic of the IC is measured in order to reduce the variation of the characteristic of the amplifier.

On the monolithic IC, the length and the width of the microstrip line which forms the input matching network may be cut by a YAG laser to adjust the characteristic of the amplifier.

However, the prior art technique to adjust the characteristic of the amplifier by forming the adjusting circuit on the ceramic substrate is riched in flexibility but provides a very low productivity. Further, in the Technique to cut the length or the width of the microstrip line on the monolithic IC by the laser, it is not possible to increase the length or the width. As a result, it is difficult to adjust the variation of the optimum source reflection coefficient Γ_{opt} of the FET to any matching point. It is technically possible to reduce the width but it is very difficult to attain and not practical.

Summary of the Invention

It is an object of the present invention to provide an input matching network and a method for adjusting the same, which solve the problems encountered in the prior art.

The input matching network of the present invention uses an open stub as a circuit component. As an electrical length of the open stub is reduced, a source reflection coefficient as viewed from an input end of an amplifier connected to the stub varies such that a phase angle increases along a constant resistance circle on a Smith Chart. Accordingly, if the electrical length of the open stub is set such that the phase angle of the source reflection coefficient as viewed from the amplifier is smaller than a mean value of manufacturing variations of the phase angle of the optimum source reflection coefficient of the amplifier, a matching point can be adjusted by reducing the electrical length of the open stub such that it is applicable over a substantially entire distribution of the manufacturing variation of the optimum source reflection coefficient of the amplifier.

The present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings which are given by way of illustration only, and thus are not to be considered as limiting the present invention.

Further scope of applicability of the present invention will become apparent from the detailed description given hereinafter. However, it should be understood that the detailed description and specific examples, while indicating preferred embodiments of the invention, are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from this detailed description.

Brief Description of the Drawings

Fig. 1 is a graph showing a relationship between $|\Gamma_{opt}|$ and or angle Γ_{opt} of a pulse doped structure FET,

Fig. 2 is a Smith Chart showing a relationship between $|\Gamma_{opt}|$ and angle $\Gamma_{opt}|$ shown in Fig. 1,

Fig. 3 is a Smith Chart for illustrating a path of movement of Γ_{opt} of the FET;

Fig. 4 shows an open stub;

Fig. 5 shows a block diagram of an input matching network which uses the open stub;

Fig. 6 is a Smith Chart for illustrating the change of an impedance Z_{match} shown in Fig. 5 with the length of the open stub;

Fig. 7 shows a block diagram of an input matching network which has a serial inductance for converting a parallel capacitance due to the open stub to a serial inductance;

Fig. 8 is a Smith Chart for illustrating an affect to an impedance Z_{open} which varies with the electrical length of the open stub S1 by the value of an impedance Z_{start};

Fig. 9 is a Smith Chart for illustrating an affect, to an impedance Z_{match} which varies with the electrical length of the open stub S1 by the value of the impedance Z_{start};

Fig. 10 shows a block diagram of an input matching network which includes a serial inductance for adjusting the impedance Z_{start};

Fig. 11 shows a circuit diagram of a low noise amplifier in one embodiment of the present invention; and

Figs. 12, 13, 14 and 15 are Smith Charts for illustrating the monument of Γ_{opt} when the electrical length of the open stub is reduced at various values of constants of the components of the input matching network shown in Fig. 1.

Detailed Description of the Preferred Embodiments

A low noise amplifier in accordance with one embodiment of the present invention is now explained. In the present embodiment, a pulse doped structure GaAs MESFET is used in an amplifier circuit of a low noise amplifier. In the pulse doped structure, a pulse doped GaAs layer having carriers confined therein is used as an activation layer of the MESFET.

In a pulse doped structure FET having a short gate length of approximately 0.3 μm, a manufacturing variation in a relationship between an absolute value $|\Gamma_{opt}|$ of an optimum source reflection coefficient Γ_{opt} at which the NF is minimum and a phase angle Γ_{opt} in the Γ_{opt} is shown in Fig. 1. The manufacturing variation is due to a manufacturing variation of the FET. In Fig. 1, black dots represent distribution and straight line represents an approximate line of the distribution. As seen from Fig. 1, there is a strong correlation between $|\Gamma_{opt}|$ and angle Γ_{opt}. Accordingly, when the distribution of Γ_{opt} is drawn on a Smith Chart, it does not distribute over a wide area but distributes in a narrow band, as shown in Fig. 2.

The input matching network of the low noise amplifier of the present embodiment is designed such that a matching point for impedance-converting an external impedance (50Ω) moves along the narrow band distribution. More specifically, an open stub is provided in the input matching network, and an electrical length of the open stub is selected such that the matching point by the input matching network is positioned at a point in the distribution of the manufacturing variation of Γ_{opt} which assures a minimum angle. In the present embodiment, the minimum angle point is shown by an arrow 40 in Fig. 3. The input matching network is constructed such that as the electrical length of the open stub is reduced, the matching point moves substantially along a constant resistance circle of Fig. 3. As a result, the matching point of the external impedance by the input matching network can move over the entire range of the manufacturing variation of Γ_{opt}. Accordingly, the conversion of the external impedance can be adjusted to the minimum NF point by cutting the open stub by a laser for tuning.

The characteristic of the amplifier can be adjusted by merely shortening the electrical length of the open stub, and the process is most practical and significantly improves a manufacturing yield of a wafer. A specific design method of such input matching network is now explained in sequence.

A circuit configuration to move the matching point substantially along the constant resistance circle of Fig. 3 may be attained by a combination of components but it is preferable to attain it with a minimum number of components, as is done in the present embodiment.

As the electrical length of the open stub is shortened, the matching point moves on a constant conductance circle on the Smith Chart. The open stub functions as a parallel capacitance as shown in Fig. 4, in which a left side corresponds a signal source and a right side corresponds to a load, and an open impedance Z_{open} when the circuit is opened at a position shown by a chain line is given by

$$Z_{open} = -j \cdot Z_o \cdot \cot(\beta l_\epsilon)$$

where Z_o is a characteristic impedance of the open stub, β is a phase constant ($=2\pi/\lambda$) of the open stub, and l_ϵ is the electrical length of the open stub.

It is seen from the above formula that the open stub functions as a parallel capacitance when the electrical length is smaller than $\lambda/4$ ($l_\epsilon < \lambda/4$). Accordingly, an impedance Z match as views from the load of the basic input matching network 50 to

the signal source varies with the electrical length l_ϵ of the open stub S1. The impedance Z match moves along an arrow shown on the Smith Chart of Fig. 6 by the change of length. A point A shows an impedance when the electrical length $l_\epsilon = 0$. The electrical length l_ϵ increase substantially along the direction of the arrow.

As shown in the distribution chart of $|\Gamma_{opt}|$ and angle Γ_{opt} of Fig. 1, the optimum source reflection coefficient Γ_{opt} has a small angle where the amplitude is large, and has a large angle where the amplitude is small. Accordingly, Γ_{opt} distribute substantially along the constant resistance circle on the Smith Charts shown in Figs.2 and 3, but distribute inwardly of the circle where the angle is large.

Thus, it is necessary to convert the impedance such that the impedance shown in Fig. 6 moves substantially along the constant resistance circle as shown in Fig. 6. To this end, the input matching network is configured as shown in Fig. 7. Namely, in addition to the open stub S1, a serial inductance S2 is connected to the basic input matching network 50. The movement on the constant resistance circle may be attained only by the serial inductance, but the series inductance S2 is formed by a strip line having an electrical length of approximately $\lambda/4$ in order to convert the parallel capacitance by the open stub S1 to a serial inductance.

On the other hand, a manner in which the impedance Z_{open} moves by the electrical length l_ϵ of the open stub S1 shown Fig. 7 differs with the impedance Z_{start}. The impedances Z_{open} and Z_{start} are impedances as viewed from the chain line position to the signal source. In the Smith Chart shown in Fig. 8, the movement of the impedance Z_{open} changes with the values B, C, D and E of the impedance Z_{start}. The electrical length l_ϵ of the open stub S1 increases along the direction of the arrow. As shown in Fig. 9 the movement of impedance Z_{match}, which are impedances as viewed from a load position to the signal source, also changes with the values F, G, H and I of the impedance Z_{start}. And in Fig. 9, the electrical length l_ϵ of the open stub S1 also increases along the direction of the allow.

In order to move the impedance Z_{start} substantially along bold arrows of Figs.8 and 9, it is necessary to construct an input matching network as shown in Fig. 10. That is, it is necessary to provide a serial inductance S3 in the signal source contacting with an interval circuit. The serial inductance S3 corresponds to a basic input matching network 50 of Fig. 7 and the impedance Z_{start} moves along the bold arrows shown in Figs.8 and 9 by the adjustment of the length of the serial inductance S3.

Although Γ_{opt} in the Smith Chart in distributed along the constant resistance circle, the path of the Γ_{opt} tends to be move somewhat inwardly of the circle where the angle Γ_{opt} may be realized by the serial insertion of a capacitance into the input matching network.

In the input matching network shown in Fig. 11, a capacitor C is inserted between the serial inductances S2 and S3. The serial capacitance may be formed by a MIM capacitor (overlay structure). Where a nitride film (Si_3N_4) having a firm thickness of 3000Å is used as an interlayer insulation film, the capacitance is approximately 0.2 fF/μm^2. Thus, when the capacitor C having 0.3 pF is to be formed by this structure, the area is approximately 1500 μm^2. The capacitor C may be formed by an interdigital capacitor having comb-shaped electrodes instead of the MIM capacitor.

The open stub S1 and the serial inductances S2 and S3 may be formed by microstrip lines. The series inductance S3 is connected to the signal source, and the serial inductance S2 is connected to the load, that is, the pulse doped structure GaAs MESFET.

In the low noise amplifier which used the input matching network shown in Fig. 11, the optimum source reflection coefficient Γ_{opt} moves as initially intended as shown in Fig. 3. Accordingly, Γ_{opt} moves over the entire range of the manufacturing variation by cutting the electrical length l_ϵ of the open stub set at the minimum angle position by the laser. The low noise amplifier having the optimum characteristic is attained by stopping the cutting of the open stub S1 at the minimum NF point. The cutting of the open stub S1 is effected after the wafer manufacturing process.

Figs.12-15 are Smith Charts for illustrating the movement of Γ_{opt} when the electrical length of the open stub S1 is cut at various values of constants of the components of the input matching network shown in Fig. 11.

In Fig. 12, the constants of the components are set as follows and the electrical length of the open stub is changed.

Open stab S1:
Electrical
length l1 = 0-600μm
Width W1 = 100μm
Serial inductance S2:
Electrical
length l2 = 2400μm
Width W2 = 40μm
Serial inductance S3:
Electrical
length l3 = 2600μm
Width W3 = 10μm
Capacitor C:
Capacitance C = 0.3pF

In Fig. 13, the constants of the components are set as follows and the electrical length of the open stub S1 is changed.

Open stub S1:
Electrical
length l1 = 500-800μm
Width W1 = 100μm
Serial inductance S2:
Electrical
length l2 = 2700μm
Width W1 = 110μm
Serial inductance S3:
Electrical
length l3 = 1200μm
Width W3 = 10μm
Capacitor C:
Capacitance C = 0.4pF

In Fig. 14, the constants of the components are set as follows and the electrical length S1 of the open stub S1 is changed.

Open stub S1:
Electrical
length l1 = 0-500μm
Width W2 = 800μm
Serial inductance S2
Electrical
length l2 = 2700μm
width W2 = 110μm
Serial inductance S3
Electrical
length l3 = 1200μm
width W3 = 10μm
Capacitor C:
Capacitance C = 0.3pF

In Fig. 15, the constants of the components are set as follows and the electrical length of the open stub S1 is changed.

Open stub S1:
Electrical
length l1 = 100-400μm
width W1 = 100μm
Serial inductance S2:
Electrical
length l2 = 2700μm
Width W2 = 80μm
Serial inductance S3:
Electrical
length l3 = 1800μm
width W3 = 10μm
Capacitor C:
Capacitance C = 0.3pF

As seen from Figs.12-15, the path of Γ_{opt} is moved somewhat inwardly of the constant resistance circle by the capacitor C, and Γ_{opt} moves along the distribution of the manufacturing variation shown in Fig. 3.

The statistical property of the amplitude and the angle of the optimum source power supply reflection coefficient Γ_{opt} of the pulse doped structure FET is utilized and the length of the open stub S1 in the input matching network is shortened by the laser cutter so that the NF is optimized to cope with the manufacturing variation of Γ_{opt} of the FET. As a result, the low noise amplifier with a high manufacturing yield is attained.

From the invention thus described, it will be obvious that the invention may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.

Claims

1. An input matching network in an input circuit of an amplifier, comprising:
   an open stub as a circuit component;
   wherein as an electrical length of said open stub is shortened, a source reflection coefficient as viewed from an input terminal of said amplifier moves to increase a phase angle substantially along a constant resistance circle on a Smith Chart.

2. An input matching network according to Claim 1 wherein the electrical length of said open stub is selected such that the phase angle of the source reflection coefficient as viewed from said amplifier is smaller than mean value of manufacturing variations of phase angle of an optimum signal source power reflections coefficient of said amplifier.

3. An input matching network is an input circuit of an amplifier, comprising;
   a basic input matching network including a serial inductance;
   a strip line of approximately one quarter wavelength serially connected to said basic input matching network; and
   a parallel capacitance including an open stub connected between said strip line and said basic input matching network,
   an electrical length of said open stub being selected such that a phase angle of a source reflection coefficient as viewed from said amplifier is smaller than a mean value of manufacturing variations of a phase angle of an optimum signal source reflection coefficient of said amplifier.

4. An input matching network according to Claim 3 wherein a serial capacitance is provided between said basic input matching network and said strip line of the quarter wavelength.

5. A method for adjusting an input matching network in an input circuit of an amplifier,

said input matching network having an open stub as a circuit component and being designed such that as an electrical length of said open stub is shortened, a source reflection coefficient as viewed from an input terminal of said amplifier moves to increase a phase angle substantially along a constant resistance circle on a Smith Chart,

said method comprising the step of:

shortening the electrical length of said open stub so that the phase angle of the source reflection coefficient as viewed from said amplifier is substantially equal to a phase angle of an optimum source reflection coefficient of said amplifier.

6. A method for adjusting an input matching network according to Claim 5 wherein the electrical length is shortened by cutting the open stub by a laser.

Fig. 1

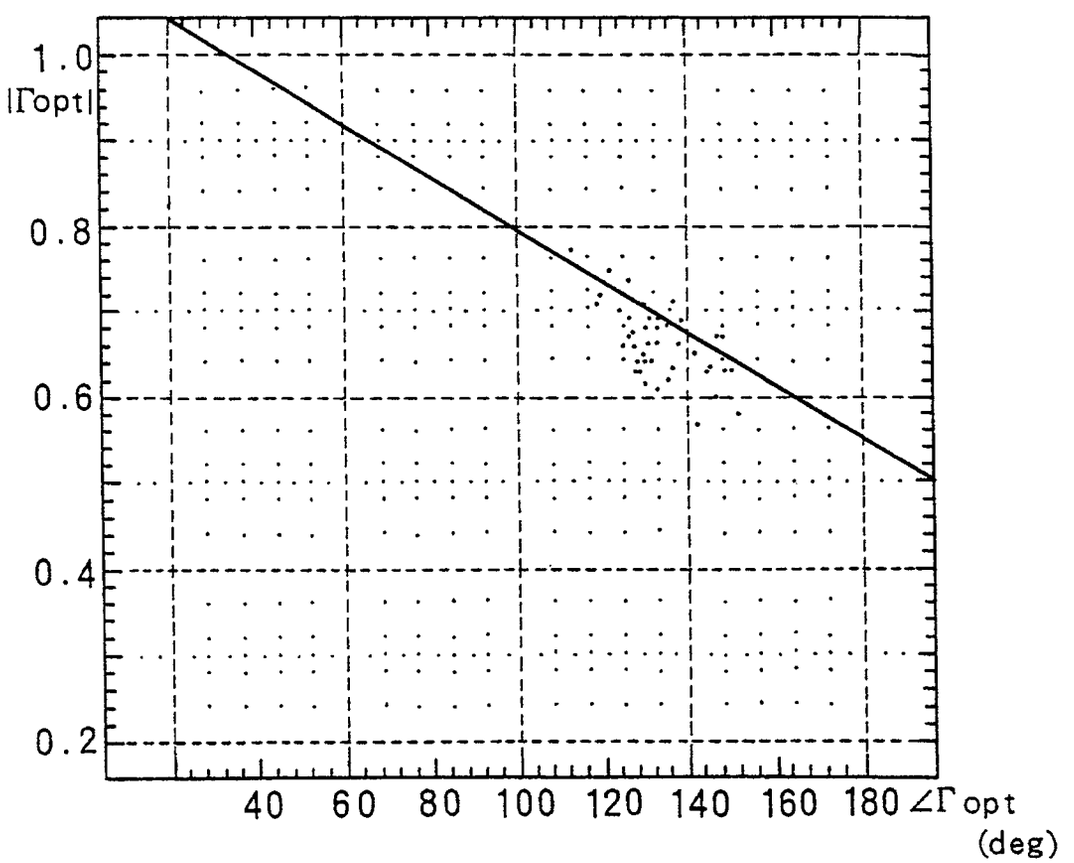


Fig. 2

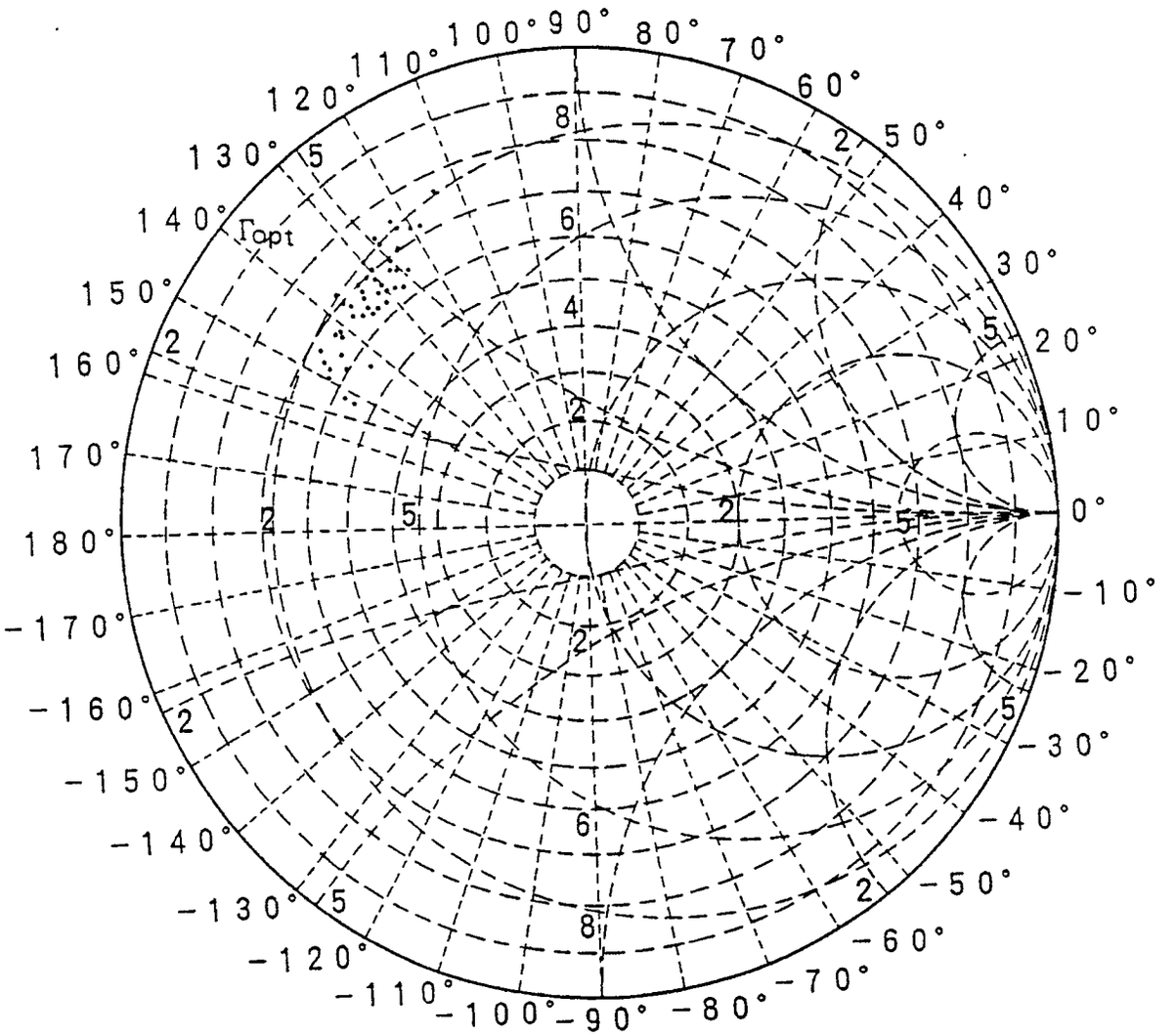
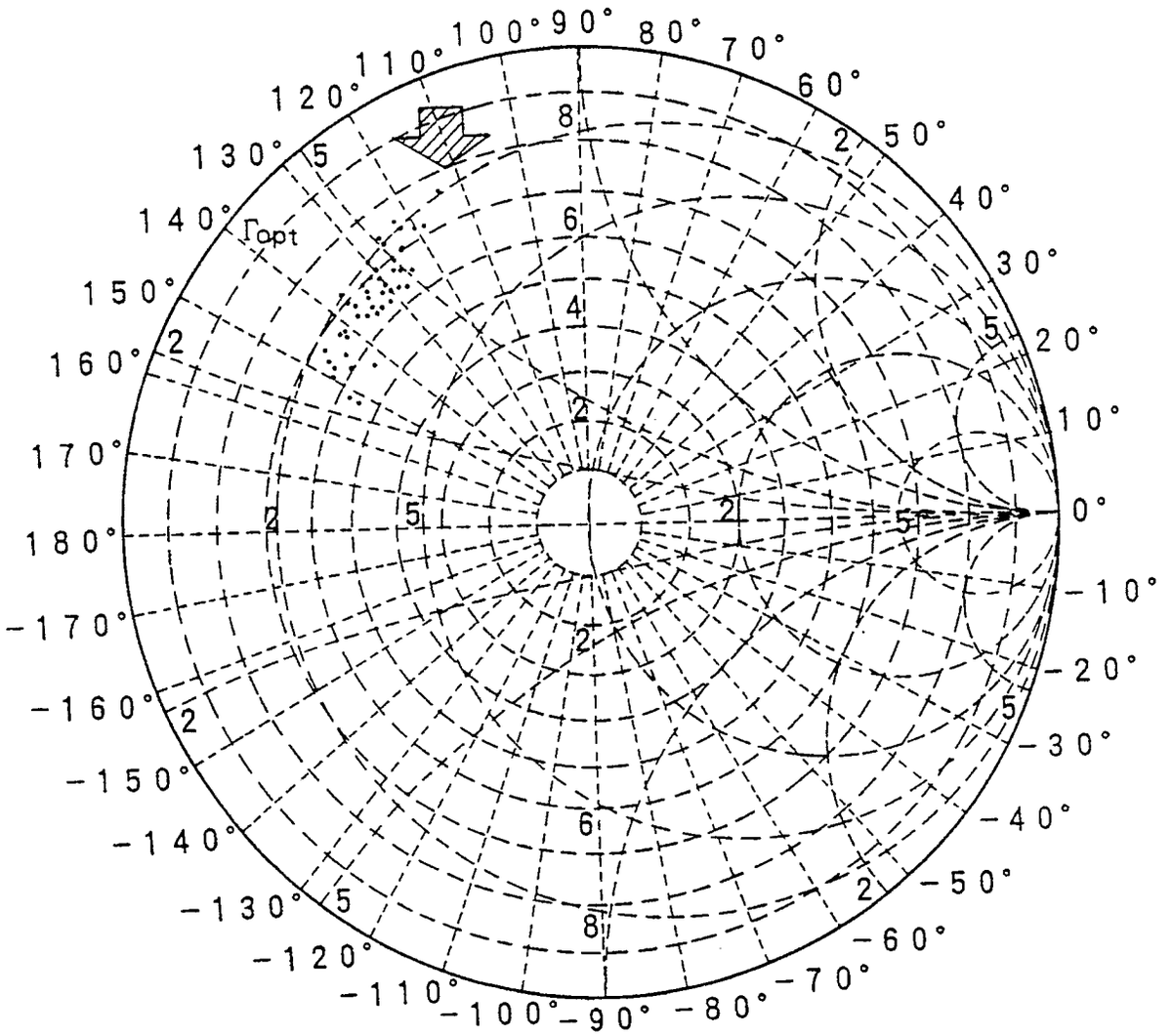

Γopt
100° 90° 80° 70° 60° 50° 40° 30° 20° 10° 0° -10° -20° -30° -40° -50° -60° -70° -80° -90° -100° -110° -120° -130° -140° -150° -160° -170° 180° 170° 160° 150° 140° 130° 120° 110°
8
6
4
2
5

Fig. 3


Гарт
90°
80°
70°
60°
50°
40°
30°
20°
10°
0°
-10°
-20°
-30°
-40°
-50°
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-90°
-100°
-110°
-120°
-130°
-140°
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140°
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100°

Fig. 4

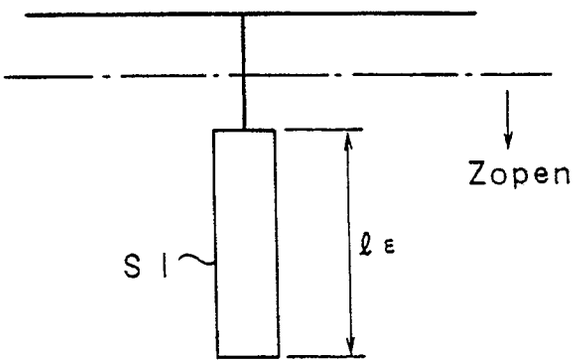

Fig. 5

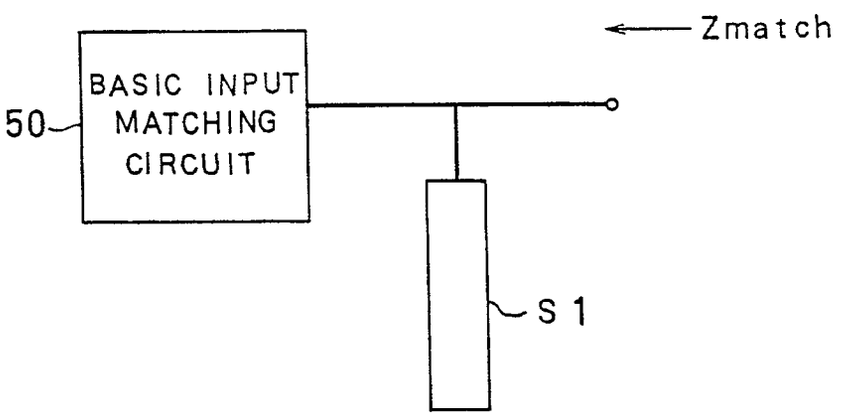

Fig. 6

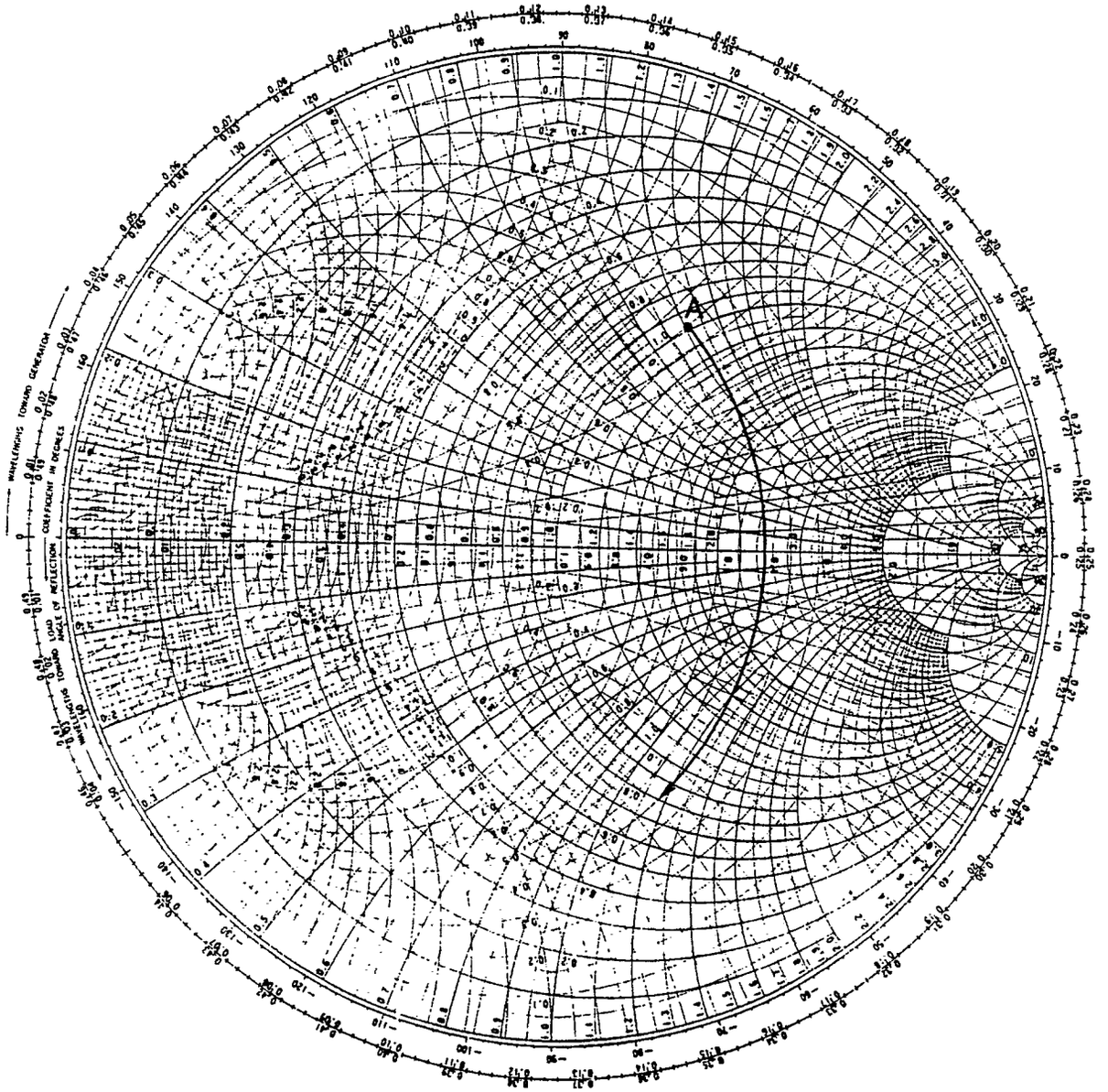

Fig. 7

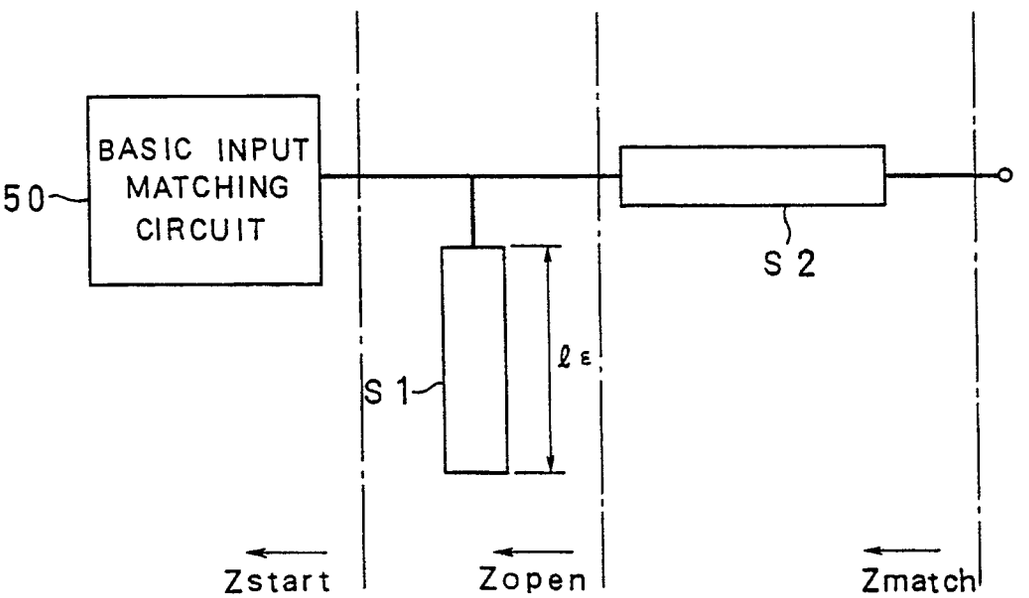
BASIC INPUT
MATCHING
CIRCUIT
50
S 1
S 2
ℓ ε
Zstart
Zopen
Zmatch

Fig. 8

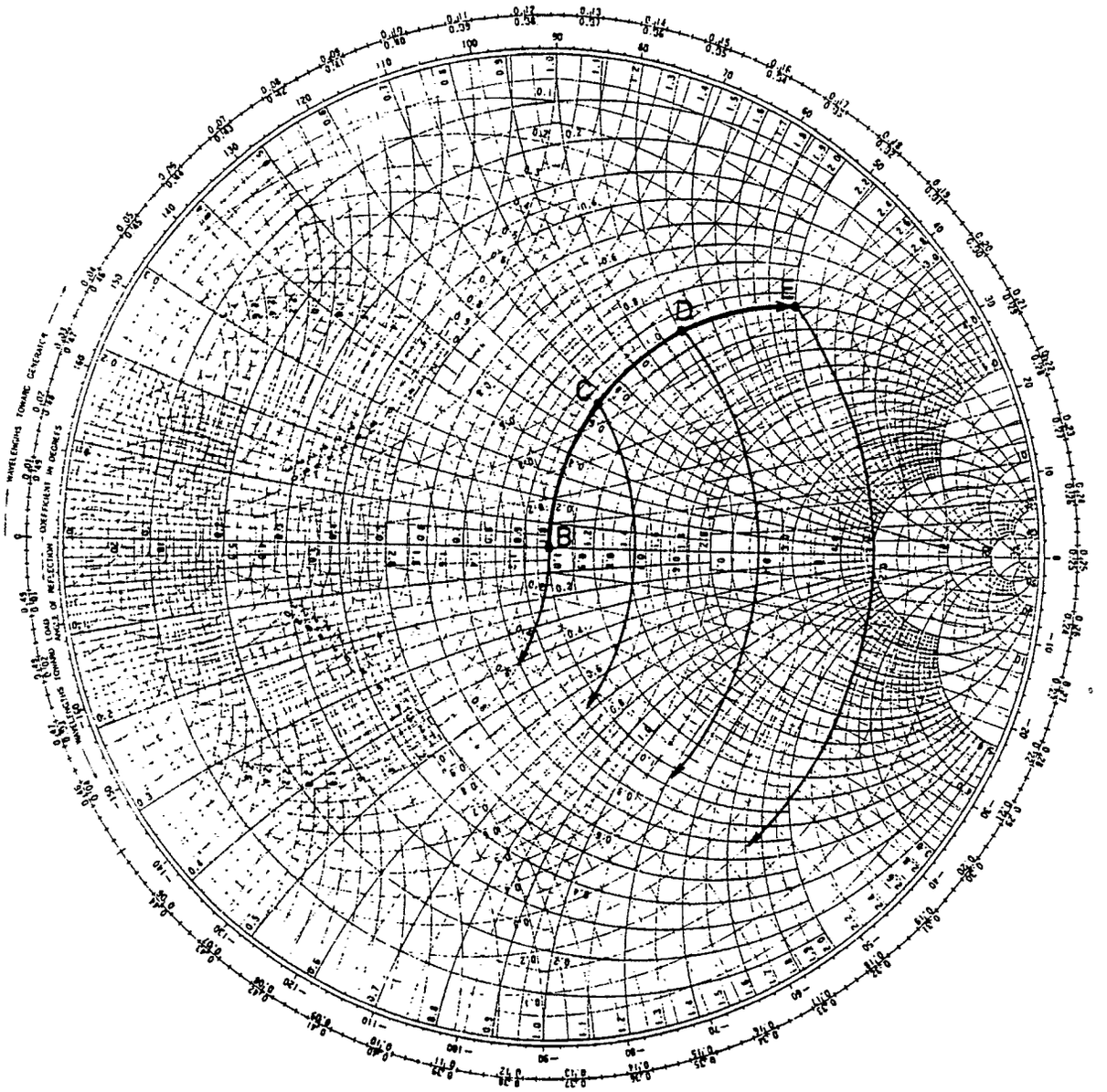

Fig. 9

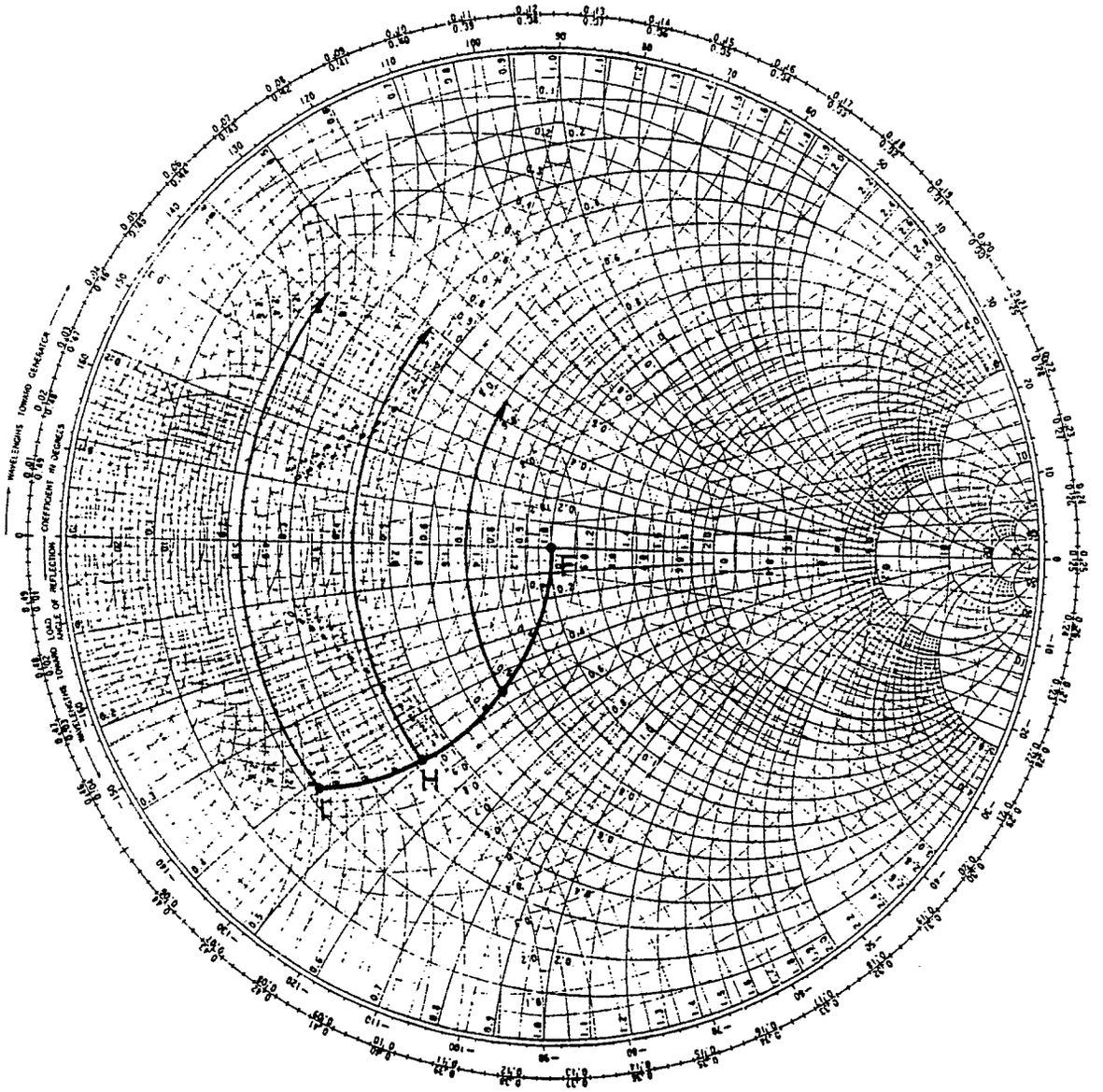

Fig. 10

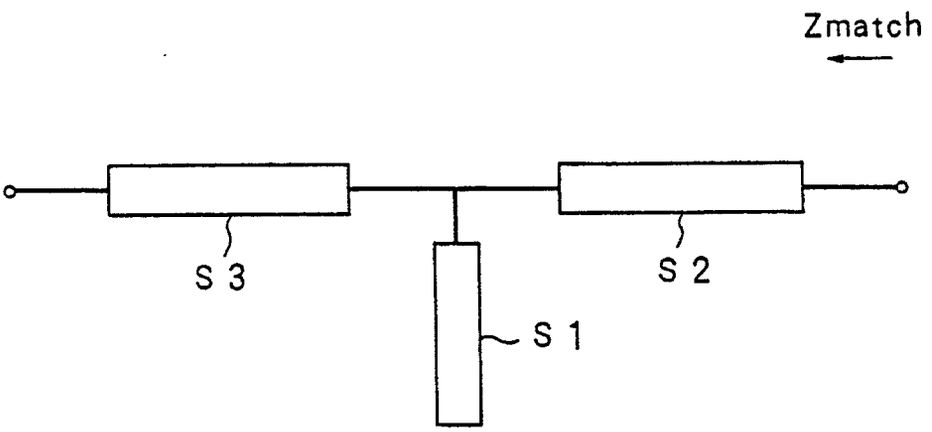

Fig. 11

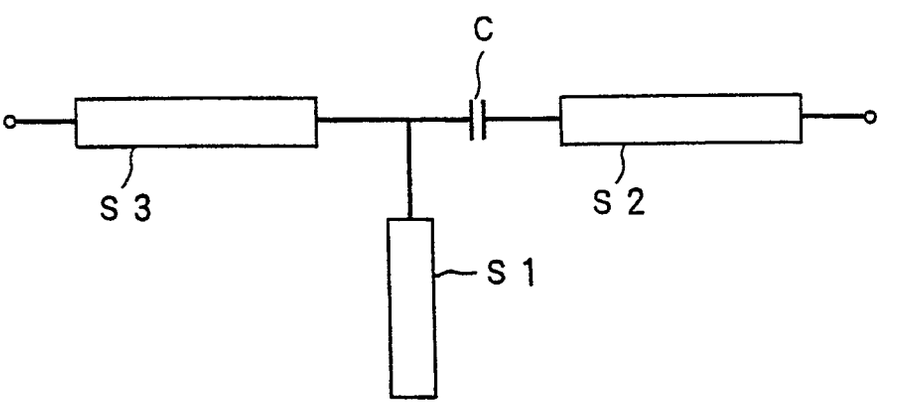

Fig. 12

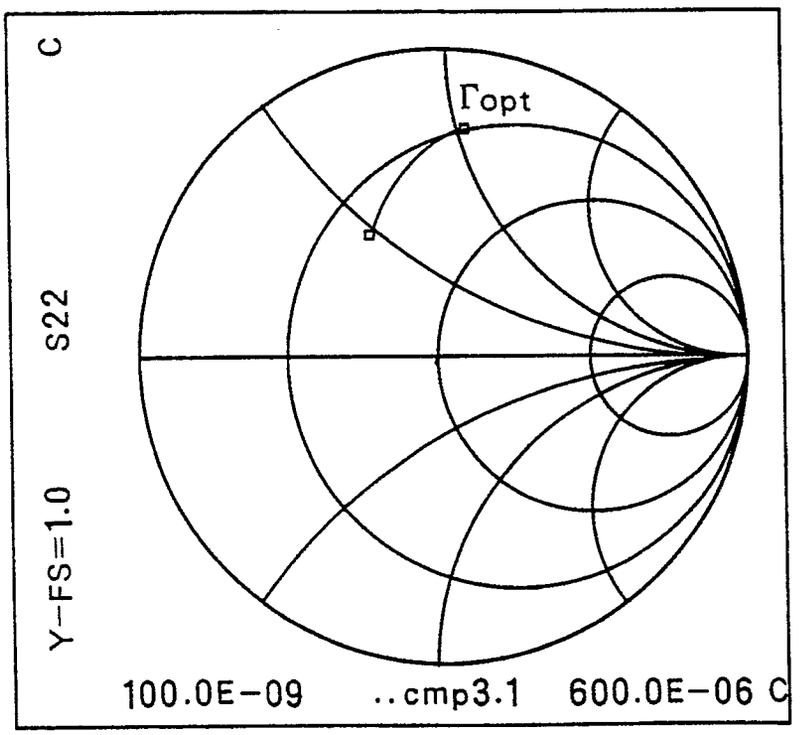

Fig. 13

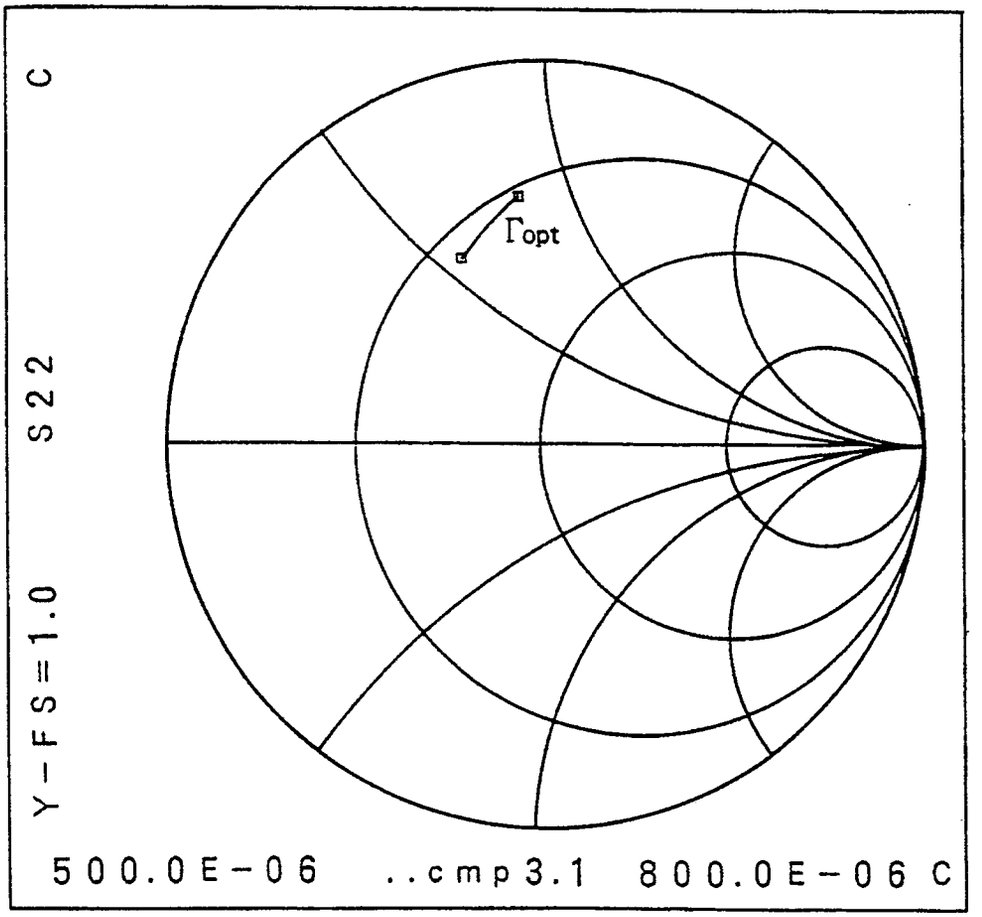

Fig. 14

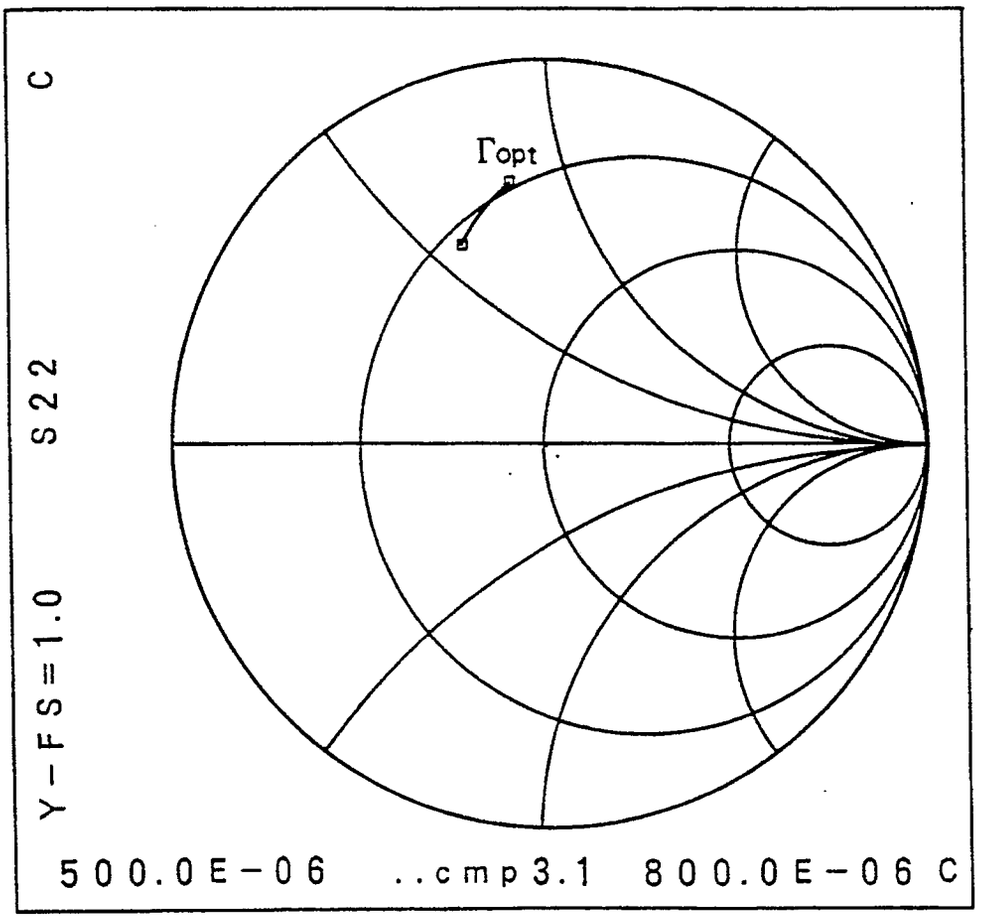

Fig. 15