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(54) **METHOD FOR APPLYING A TEXTURED INSULATION LAYER TO A METAL LAYER**

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(57) **ABSTRACT**

The present invention relates to a method for applying a structured insulating layer (**14**) onto a metal layer (**12**), in which insulation material (**14**) is applied onto the metal layer (**12**), overlayer material (**16**) is applied to the insulating layer (**14**) and insulating material (**14**) and overlayer material (**16**) are etched in a plasma etching process, the overlayer material (**16**) being structured following the application of insulating layer (**14**), and, following the structuring of overlayer material (**16**), a plasma etching process is carried out, a structured and planarized insulating layer (**14**) being created.

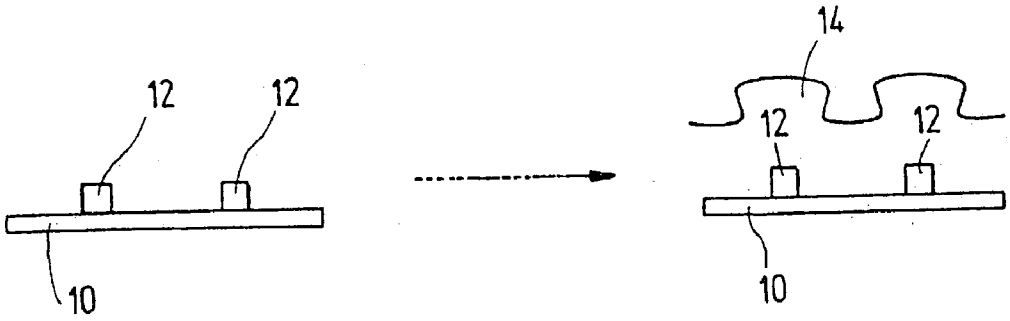

Fig.1

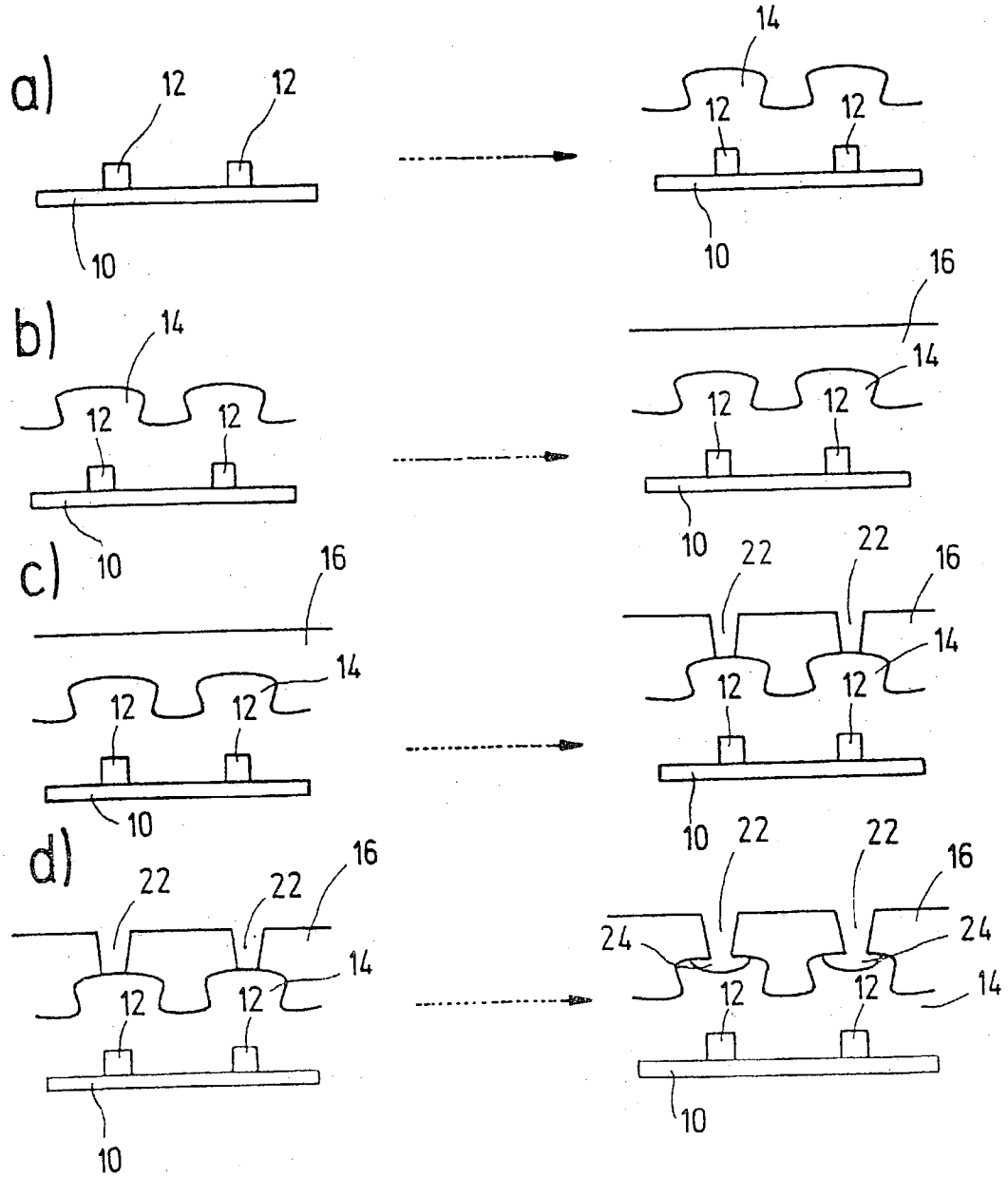
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Fig.1

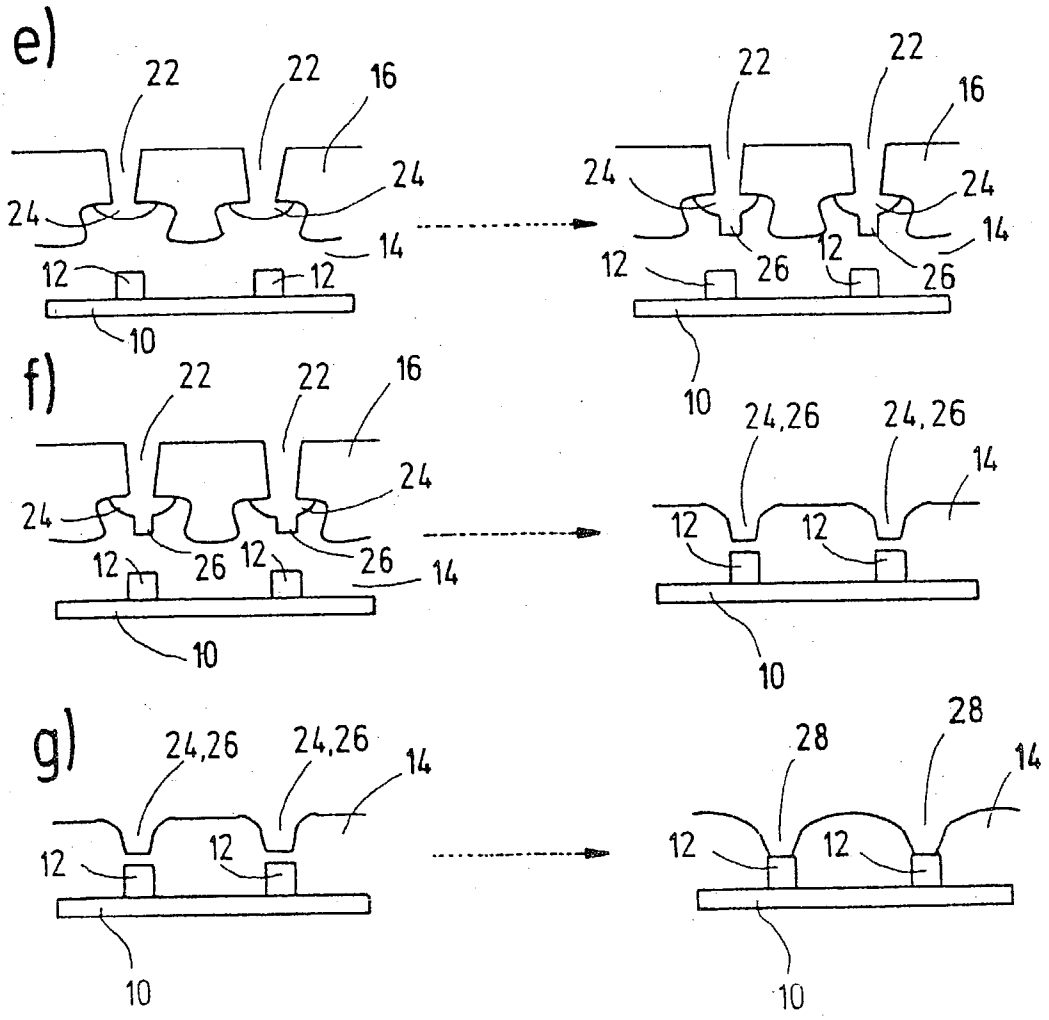
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Fig.2

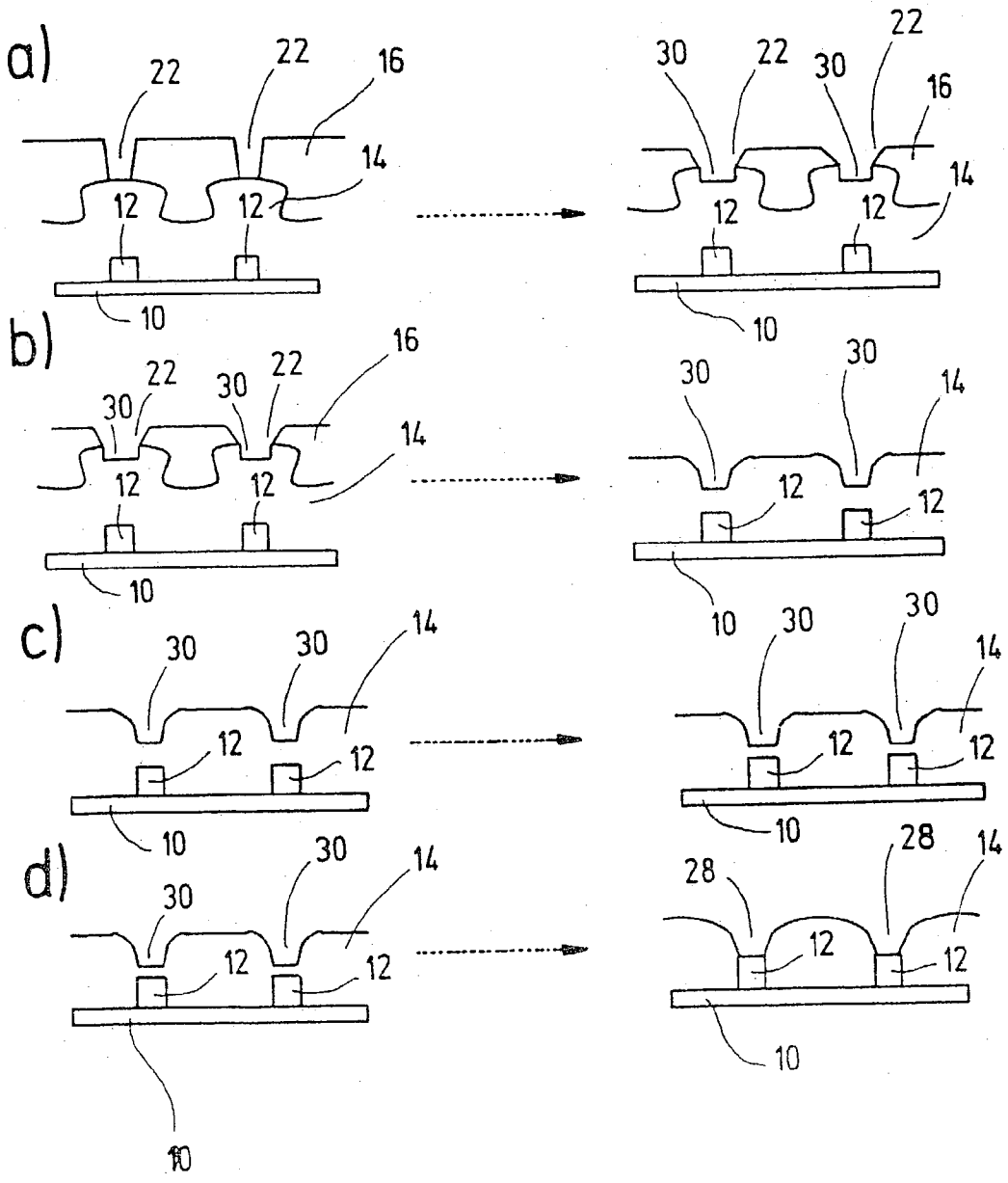
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Fig.3

(PRIOR ART)

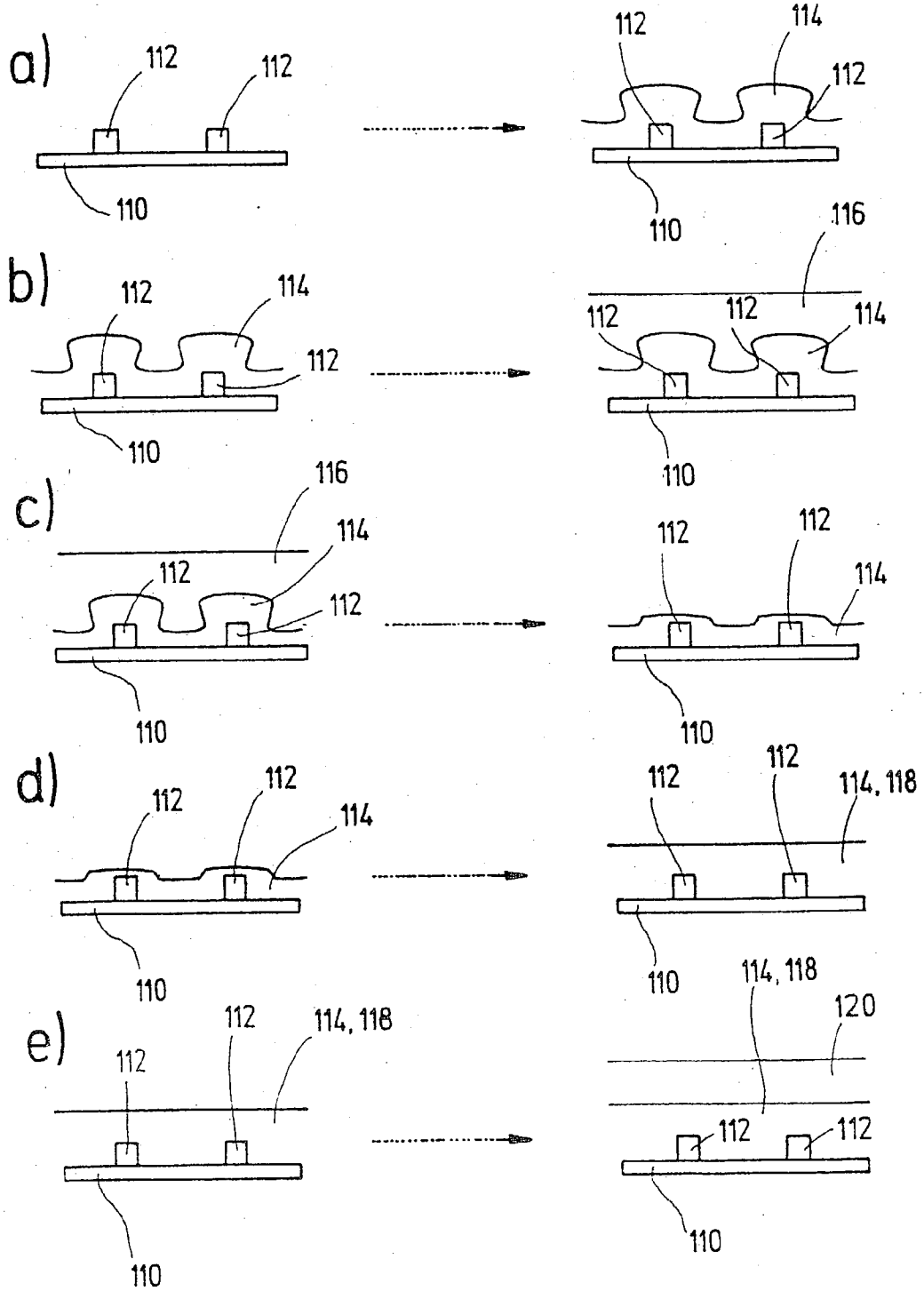
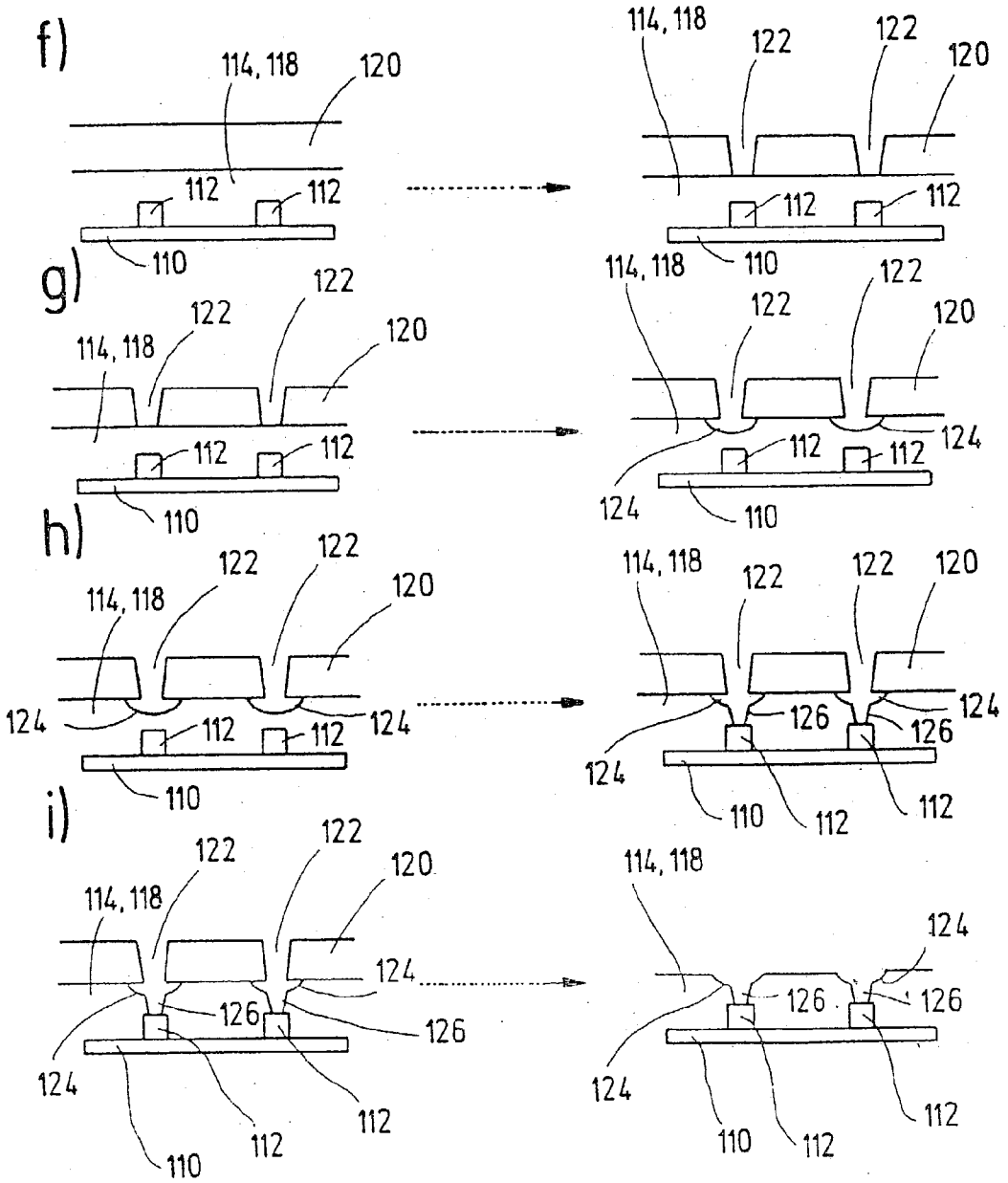


Fig.3
(PRIOR ART)



METHOD FOR APPLYING A TEXTURED INSULATION LAYER TO A METAL LAYER

BACKGROUND INFORMATION

[0001] The present invention relates to a method for applying a structured insulating layer onto a metal layer, in which insulation material is applied onto the metal layer, overlayer material is applied to the insulating layer and insulating material and overlayer material are etched in a plasma etching process.

[0002] During the manufacturing of integrated circuits, it is frequently necessary to apply an insulating layer onto a metal layer. This insulating layer is used for insulating the lower metal layer from an additional upper metal layer subsequently applied onto the insulating layer. For the specific contacting of the metal layers separated by the insulating layer, before the upper metal layer is applied, contact openings (Via) are inserted into the insulating layer. An oxide layer (TEOS) is frequently used as an insulating layer, and it is planarized before the application of the upper metal layer. A common way of introducing the contact openings into the planarized intermediate layer is an etching method.

[0003] **FIG. 3** shows the method steps of a standard method of the related art with the aid of cross sectional sketches.

[0004] **FIG. 3***a*, on the left side, shows a substrate **110**, on which two structured metal strips **112** are situated. After the structuring of this first metal layer **112**, an oxide layer (TEOS) **114** is deposited, as shown on the right side of **FIG. 3***a*.

[0005] **FIG. 3***b* shows a first lacquering of the device for the purpose of achieving planarization. The left side of **FIG. 3***b* corresponds to the right side of **FIG. 3***a*. On the right side of **FIG. 3***b* there is a good planarization lacquer **116** on oxide layer **114** in order to planarize the steps in oxide layer **114**.

[0006] **FIG. 3***c* shows a first plasma etching process. The left side of **FIG. 3***c* corresponds to the right side of **FIG. 3***b*. In a plasma etching method, lacquer **116** and oxide layer **114** are etched at approximately the same etching rate to a specified minimum thickness. Thus is obtained planarized oxide layer **114** shown on the right side of **FIG. 3***c*. The plasma etching process is set, for example by a suitable selection of the oxygen concentration, so that the etching rates with respect to lacquer layer **116** and oxide layer **114** are identical to the greatest extent possible. In this manner, in the ideal case, the surface of lacquer layer **116** is imaged on the surface of oxide layer **114**.

[0007] **FIG. 3***d* illustrates a second oxide deposit. The left side of **FIG. 3***d* corresponds to the right side of **FIG. 3***c*. After the second oxide deposit, one obtains an overall oxide layer **114**, **118**, having an at least approximately planarized surface.

[0008] **FIG. 3***e* shows a further step for applying a lacquer layer **120**. The left side of **FIG. 3***e* corresponds to the right side of **FIG. 3***d*. On account of the second lacquering taking place at this point, a lacquer layer **120** is obtained on oxide layer **114**, **118**.

[0009] **FIG. 3***f* shows how lacquer layer **120** is structured by photolithography. Openings **122** are created in lacquer layer **120** from the photolithography process. The left side of **FIG. 3***f* corresponds to the right side of **FIG. 3***e*. The right side of **FIG. 3***f* shows the end state after a photolithographic process, lacquer layer **120** now having openings **122**, so that oxide layer **114**, **118** is partially exposed.

[0010] **FIG. 3***g* shows the first step of the plasma etching process for producing the contact holes in oxide layer **114**, **118**. The left side of **FIG. 3***g* corresponds to the right side of **FIG. 3***f*. Using a first isotropic plasma etching step, hollows **124** are etched into the surface of oxide layer **114**, **118** in the area of holes **122** in lacquer layer **120**.

[0011] **FIG. 3***h* illustrates a further plasma etching step. On the left side of **FIG. 3***h* the same situation is shown as on the right side of **FIG. 3***g*. The contact holes in oxide layer **114**, **118** are etched to completion by an anisotropic etching process, these now consisting of one isotropic part **124** and one anisotropic part **126**.

[0012] **FIG. 3***i* shows that the remaining lacquer layer **120** is removed by a plasma stripping process. The left side of **FIG. 3***i* corresponds to the right side of **FIG. 3***h*. Lacquer **120** is removed by the plasma stripping process, so that one obtains as a result an oxide layer **114**, **118** positioned on a metal layer **112**, which has partially flattened contact holes **124**, **126**. Because of the flattening of the upper hole edge in the region **124** of contact holes **124**, **126**, a good edge covering by the additional upper metal layer deposited later into each of the holes **124**, **126** is ensured.

[0013] The method shown in **FIG. 3** supplies a well planarized insulating layer; however, because of the large number of method steps, it is very costly. The upper hole edge of the contact holes is only partially planarized. In general, one would be afraid that, because of the large number of method steps, the probability of defects increases.

SUMMARY OF THE INVENTION

[0014] The present invention builds up on the method of the generic type according to claim 1 in that the overlayer material is structured subsequently to its application to the insulating layer, and in that subsequently to the structuring of the overlayer material a plasma etching process is carried out, whereby a structured and planarized insulating layer is created. Therefore, according to the present invention it is no longer necessary first to carry out a first plasma etching process after the application of the overlayer material to the insulating layer, then to rebuild again the oxide layer by a further oxide deposit, once more to apply a lacquer layer, and to structure this first, in order to introduce the desired structure into the oxide layer. Rather, it is possible to structure the overlayer material subsequently to its application onto the insulating layer, and to produce the desired structuring of the insulating layer in the subsequent plasma etching process. In this context it should be observed that the thickness of the oxide layer is sufficiently great before the application of the overlayer; for example, the thickness might correspond approximately to the sum of the thickness of the oxide layers separately applied in the related art.

[0015] Preferably lacquer is involved as far as the overlayer material is concerned. Lacquers are applied to an oxide layer in a simple manner, and they are especially suitable for representing a mask.

[0016] In this connection it is especially useful if the overlayer material is structured by photolithography. Hereby

it is possible to produce the most exact structures, which then positively enter into the precision of densely packed integrated circuits.

[0017] In the case of the insulating layer, preferably an oxide layer (TEOS) is involved. Oxide layers have come into their own as insulating layers in densely packed integrated circuits.

[0018] It may be of advantage if the plasma etching process is carried out in one step, the ratio of the overlayer material etching rate to the insulating material etching rate is 1 ±0.4. In the case of such an etching rate ratio and a suitable thickness of the applied layers, one may succeed in obtaining a desired result in a uniform process, i.e. a single production step.

[0019] On the other hand it may also be useful if the plasma etching process has several steps, in a first step at least one isotropic depression being etched into the insulating layer, in a second step at least one anisotropic depression being etched into the insulating layer, in a third step planarization takes place, and in a fourth step the anisotropic depression is finally etched to form a through hole. In this way, the contact holes may be formed in particularly controlled fashion. By a suitable selection of the layer thicknesses and the etching parameters, advantageously rounded contact holes are obtained at their surface.

[0020] It may also be useful if the plasma etching process has several steps, in a first step the ratio of the overlayer material etching rate to the insulating material etching rate being greater than 1, overlayer material primarily being etched and at least one step in the insulating layer being defined, in a second step the ratio of the overlayer material etching rate to the insulating material etching rate is 1 ±0.4, at least one depression in the insulating layer being etched and planarization taking place, in a third step the depression is etched further over a fixed period, and in a fourth step the depression is finally etched to a through hole. Thus, in the first step, first of all removal of overlayer material is provided, while in the second step etching of a depression in the insulating layer is begun, by a suitable selection of the ratio of the overlayer material etching rate to the insulating material etching rate, and planarization is carried out. In the third step, the ratio of the etching rates is then no longer decisively important, but the depression is is etched further over a fixed period. In the fourth step, in which the overlayer material may have already been completely removed, the etching rate ratio is unimportant, and the only thing that still matters is that the contact holes are etched to completion.

[0021] It may also be useful if the plasma etching process has several steps, in a first step the ratio of the overlayer material etching rate to the insulating material etching rate being less than 1, at least one step in the insulating layer being defined over a fixed period, in a second step the ratio of the overlayer material etching rate to the insulating material etching rate is greater than 1, primarily overlayer material being etched, in a third step the ratio of the overlayer material etching rate to the insulating material etching rate is 1 ±0.4, at least one depression being etched into the insulating layer and planarization taking place, in a fourth step the depression is further etched to a through hole over a fixed period, and in a fifth step the depression is etched to completion. In this specific embodiment, first of all a step in the insulating layer is defined over a fixed period, only a small quantity of overlayer material being removed by the plasma etching process. Thus, to begin with, clearly defined initial conditions are created for the further etching steps, which leads to especially exact results with respect to the surface structure of the insulating layer.

[0022] In one particularly advantageous variant of the method according to the present invention, the insulating material is applied by a one-time depositing. Even if it is possible, and, depending on the required quality and thickness of the insulating layer, if it may even be useful to undertake the depositing of the insulating material in several steps, it is still sometimes preferable, with regard to the economics of the method, to deposit the insulating material in one single step, in order to reduce the number of method steps.

[0023] Under certain circumstances it may be useful to remove overlayer material remaining behind after the plasma etching process by plasma stripping. Thus, with respect to the deposited layer thicknesses and the etching rate ratios, the actual plasma etching process may be arranged so variably that, even at the end of the plasma etching process, some overlayer material has still remained on the insulating layer. This is then removed by plasma stripping.

[0024] The method according to the present invention is then further refined in that an additional, upper metal layer is deposited on the finished system made of metal layer and insulating layer. The contact holes rounded at the surface are particularly suitable for the deposition of the additional metal layer, since they ensure good overlayer of the edges. Thus, in the final analysis, the method may be used in the production of a frequently needed multi-layer metallization having intermediate insulating layers.

[0025] The present invention is based on the surprising realization that a simplification of the production method may be achieved by the combination of the planarization process and the etching of the contact holes. Nevertheless, satisfactory results are obtained, particularly with regard to the shape of the contact holes. Because the number of method steps is decreased in the production of the integrated circuits, the number of defects is reduced, which results in a larger yield. The shape of the contact holes may be influenced, on the basis of the present invention, by the variation of the process parameters, for instance, the type of lacquer, the way of carrying out the photolithography, the thickness of the layers and the parameters of the plasma etching process, particularly with respect to the ratio of the etching rates. The desired rounding of the contact holes also results in their widening. This widening may be compensated by an adjustment of the measures of the exposure mask used in the lithography, which is used in the structuring of the resist mask.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026] The present invention shall now be clarified in terms of preferred specific embodiments by way of example, with reference to the accompanying drawings. The figures show:

[0027] **FIG. 1** cross sectional sketches of layer sequences which appear in a first specific embodiment of the method according to the present invention.

[0028] **FIG. 2** cross sectional sketches of layer sequences which appear in a second specific embodiment of the method according to the present invention.

[0029] **FIG. 3** cross sectional sketches of layer sequences which appear in a method of the related art.

DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

[0030] **FIG. 1** illustrates the method steps of a first specific embodiment of the method according to the present invention by various sketched layer constructions.

[0031] **FIG. 1***a* shows in cross section a substrate **10** having two structured metal strips **12**. This system shown on the left side of **FIG. 1***a*, by oxide deposition, turns into the system shown on the right side, in which an oxide layer **14** is additionally situated on substrate **10** and structured metal strips **12**. Comparison with the corresponding representation in **FIG. 3***a* shows that oxide layer **14** in Figure la has a greater thickness than oxide layer **114** in **FIG. 3***a*. For instance, the thickness of oxide layer **14** may correspond to the sum of the thicknesses of the two deposits of oxide layers in the related art according to **FIG. 3**.

[0032] **FIG. 1***b* shows the application of a lacquer layer **16**. The left part of **FIG. 1***b* corresponds to the right part of **FIG. 1***a*. In the right part of **FIG. 1***b* a lacquer layer **16** is shown, in addition to substrate **10**, metal strips **12** and oxide layer **14**.

[0033] This representation appears again on the left side of **FIG. 1***c*. As shown in the method according to the present invention, subsequently to the application of lacquer layer **16**, a lithography process is carried out. This is shown in **FIG. 1***c*. On the right side of **FIG. 1***c* one may recognize holes **22** in the lacquer layer, which expose the surface of oxide layer **14** in certain areas.

[0034] **FIG. 1***d* shows a first step of a plasma etching process. The left side of **FIG. 1***d* corresponds to the right side of **FIG. 1***c*. First an isotropic etching process takes place, which is selected to be a little shorter than the isotropic etching process of the related art, explained in connection with **FIG. 3***g*. The isotropic etching process, as a result, has depressions **24** in the surface of oxide layer **14** in the vicinity of through holes **22** through lacquer layer **16**.

[0035] As a further step of the plasma etching process, an anisotropic etching is shown in **FIG. 1***e*. The left side of **FIG. 1***e* corresponds to the right side of **FIG. 1***d*. On the right in **FIG. 1***e* there is additionally shown an anisotropic depression **26** as the continuation of hollows **24**.

[0036] **FIG. 1***f* shows an additional step of the plasma etching process for planarization and for the further forming of depressions **24**, **26** in oxide layer **14**. The left side of FIG. **1***f* corresponds to the right side of **FIG. 1***e*. On the right side of **FIG. 1***f* there is shown a planarized layer sequence made up of substrate **10**, metal strips **12** and oxide layer **14** having depressions **24**, **26**. It may already be seen that depressions **24**, **26** are rounded at the surface.

[0037] **FIG. 1***g* shows how the system is etched to completion. The left side of **FIG. 1***g* corresponds to the right side of **FIG. 1***f*. Depressions **24**, **26** are further developed by plasma etching in such a way that through holes **28** are created through oxide layer **14** having advantageously rounded edges.

[0038] The removal speed of each layer, or rather the ratio of the removal speeds is essentially a function of the parameters of the plasma etching process. By suitable selection and modification of these parameters, the layers may be removed selectively and in a controlled manner in the various method steps, which in the final analysis improves the precision during the production process.

[0039] **FIG. 2** shows an example of a multi-step plasma etching process as a part of the method according to the present invention, in which the parameters of the etching process are modified during the method. The left side of **FIG. 2***a* corresponds to the left side of **FIG. 1***d*. The planarization step shown in **FIG. 2***a* is carried out by plasma etching. In this context, the etching parameters are set in such a way that preferably lacquer layer **16** is etched. Into oxide layer **14**, only a step **30** is etched. On the right side of **FIG. 2***a* one may recognize that lacquer layer **16** has already been substantially removed, whereas in the oxide layer only the slight step **30** is present.

[0040] **FIG. 2***b* now shows how one proceeds further using other etching parameters. In this connection, the left illustration of **FIG. 2***b* corresponds to the right illustration in **FIG. 2***a*. Here, the etching parameters are selected in such a way that the lacquer etching rate is approximately equivalent to the oxide etching rate. As a result, one obtains a high degree of planarization and, at the same time, a further development of depressions **30** in oxide layer **14**.

[0041] **FIG. 2***c* shows a further step of the plasma etching process. The left side of **FIG. 2***c* corresponds to the right side of **FIG. 2***b*. Depressions **30** are further developed by additional etching; the result is shown on the right side of **FIG. 2***c*. Now the etching rates are no longer decisive. A fixed time may be set for the method step corresponding to **FIG. 2***c*.

[0042] In **FIG. 2***d*, depressions **30** are further developed to become through holes **28**. The left side of **FIG. 2***d* corresponds, in this case, to the right side of **FIG. 2***c*. The finished through hole **28** is shown on the right side of **FIG. 2***d*. The ratio of the etching rate of lacquer layer to oxide layer in this process step is unimportant.

[0043] The layer sequences shown on the right sides of **FIG. 1***g* and **FIG. 2***d* form the starting point for applying a further metallizing layer. The contact holes rounded at the surface are particularly suitable for the deposition of the additional metal layer, since they ensure good covering of the edges. Thus, in the final analysis, the method may be used in the production of a frequently needed multi-layer metallization having intermediate insulating layers.

[0044] The preceding description of the exemplary embodiments according to the present invention is used only for illustrative purposes, and not for the purpose of limiting the present invention. Various changes and modifications are possible within the context of the present invention, without departing from the scope of the invention and its equivalents.

What is claimed is:

1. A method for applying a structured insulating layer **(14)** onto a metal layer **(12)**, in which

insulating material **(14)** is applied onto the metal layer **(12)**,

overlayer material (**16**) is applied onto the insulating layer (**14**) and

insulating material (**14**) and the overlayer material (**16**) are etched in a plasma etching process, wherein,

the overlayer material (**16**) is structured subsequently to the application onto the insulating layer (**14**), and

subsequently to the structuring of the overlayer material (**16**), a plasma etching process is carried out, a structured and planarized insulating layer (**14**) being created.

2. The method as recited in claim 1, wherein, with respect to the overlayer material (**16**), lacquer is involved.

3. The method as recited in claim 1 or **2**, wherein the overlayer material (**16**) is structured by photolithography.

4. The method as recited in one of the preceding claims, wherein in the case of the insulating layer (**14**), an oxide layer (TEOS) is involved.

5. The method as recited in one of the preceding claims, wherein the plasma etching process is carried out in one step, the ratio of the overlayer material etching rate to the insulating material etching rate being 1 ±0.4.

6. The method as recited in one of the preceding claims, wherein the plasma etching process has a plurality of steps,

in a first step at least one isotropic depression (**24**) being etched into the insulating layer (**14**),

in a second step at least one anisotropic depression (**26**) being etched into the insulating layer (**14**),

in a third step a planarization taking place and

in a fourth step the anisotropic depression (**26**) being etched to a completed through hole (**28**).

7. The method as recited in one of the preceding claims, wherein the plasma etching process has a plurality of steps,

in a first step the ratio of the overlayer material etching rate to the insulating material etching rate being greater than 1, primarily the overlayer material (**16**) being etched, and at least one step (**30**) being defined in the insulating layer (**14**),

in a second step the ratio of the overlayer material etching rate to the insulating material etching rate being 1 ±0.4, at least one depression (**30**) being etched into the insulating layer (**14**) and planarization being carried out,

in a third step the depression (**30**) being etched further over a fixed period, and

in a fourth step the depression (**30**) being etched to a completed through hole (**28**).

8. The method as recited in one of the preceding claims, wherein the plasma etching process has a plurality of steps,

in a first step the ratio of the overlayer material etching rate to the insulating material etching rate being less than 1, at least one step being defined in the insulating layer over a fixed period,

in a second step the ratio of the overlayer material etching rate to the insulating material etching rate being greater than 1, primarily overlayer material being etched,

in a third step the ratio of the overlayer material etching rate to the insulating material etching rate being 1 ±0.4, at least one depression being etched into the insulating layer and planarization being carried out,

in a fourth step the depression being etched further over a fixed period, and

in a fifth step the depression being etched to a completed through hole.

9. The method as recited in one of the preceding claims, wherein the insulating material (**14**) is applied by a one-time depositing.

10. The method as recited in one of the preceding claims, wherein subsequently to the plasma etching process, remaining overlayer material (**16**) is removed by plasma stripping.

11. The method as recited in one of the preceding claims, wherein an additional metal layer is applied onto the finished set-up made up of the metal layer (**12**) and the insulating layer (**14**).

* * * * *