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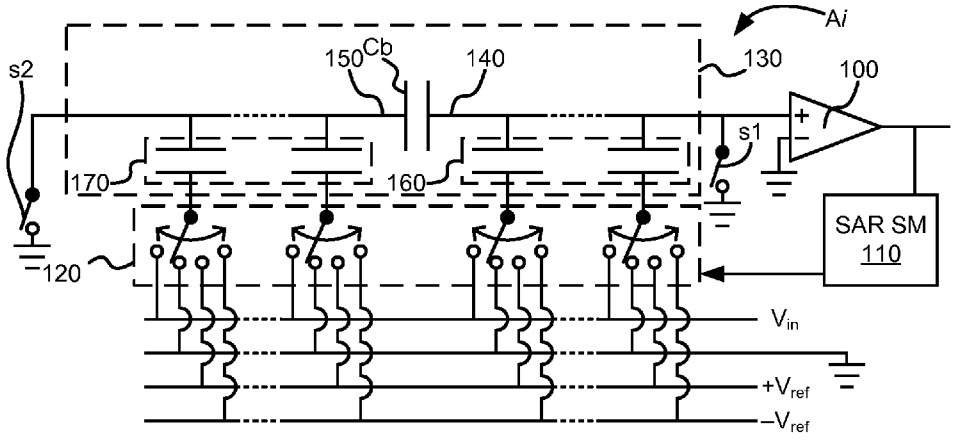

Fig. 9

(57) Abstract: Disclosed is a SAR (Ai) comprising an input for receiving an input voltage (Vin), a comparator (100), a first switch network (120) configured to be controlled by the SAR state machine (110) and connected to the input of the SAR ADC (Ai) and to reference voltage nodes, and a first capacitor network (130). The first capacitor network (130) comprises a first node (140) connected to an input of the comparator (100), a second node (150), and a bridge capacitor (Cb) connected between the first node (140) and the second node (150). Furthermore, the first capacitor network (130) comprises a first set (160) of capacitors having a first and a second terminal, wherein the first terminal of each capacitor in the first set is connected to the first node (140) and the second terminal of each capacitor in the first set is connected to the switch network (120). Moreover, the first capacitor network (130) comprises a second set (170) of capacitors having a first and a second terminal, wherein the first terminal of each capacitor in the second set is connected to the second node (150) and the second terminal of each capacitor in the first set is connected to the switch network (120). The SAR ADC (Ai) further comprises a second capacitor network (180) connected to the second node (150) of the first capacitor network and configured to control a gain of the SAR ADC (Ai).

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SUCCESSIVE-APPROXIMATION ANALOG-TO-DIGITAL CONVERTER

Technical field

The present invention relates to analog-to-digital converters (ADCs), in particular to successive-approximation (SAR) ADCs. Such SAR ADCs can, for instance, be used as sub ADCs in a time-interleaved ADC.

Background

An analog-to-digital converter (ADC) is an interface circuit between the analog and the digital signal processing domain that converts an input signal from an analog representation to a digital representation. ADCs are used in many different types of electronic circuits. For instance, ADCs can be used in receiver circuits for converting a received analog signal to a digital representation, which is then subject to further signal processing in a digital signal processor or the like.

One type of ADC that is commonly used to achieve relatively high sampling rates is the so-called time-interleaved ADC (TI-ADC). A TI-ADC comprises a number M of nominally identical sub ADCs that each operate on every M:th input sample in a time-interleaved manner. If the TI-ADC operates at a sampling rate f_s, each sub ADC operates at a considerably lower sampling rate $f_{s,sub} = f_s/M$.

A drawback with time-interleaving is the high matching requirement between sub ADCs in time (sampling moment), offset and gain. Estimation and correction for time mismatch can be avoided by having a sample-and-hold (S/H) circuit in-front of the ADC. The offset and gain mismatch can be handled in the digital domain, corrected by a subtraction and multiplication, respectively. In particular, the multiplication consumes power and silicon area, and alternative methods may therefore be preferred.

The sub ADC can for instance be implemented using a successive approximation (SAR) ADC with a capacitive digital-to-analog converter (DAC). A straight-forward implementation of the DAC utilizes a bank of binary-weighted, or radix-2, capacitors. The DAC converts a digital word of B bits into a voltage that is fed into a comparator for comparison with a sampled input voltage. The least significant bit (LSB) of that digital word has a corresponding capacitor with weight 1 (i.e. has a capacitance C, where C is some unit capacitance value) and the most significant bit (MSB) of that digital word has a corresponding capacitor with weight 2^{B-1} (i.e. has a capacitance $2^{B-1}C$).

US 6,720,903 B2 discloses a method of operating an SAR-type analog-to-digital converter to match the dynamic range of an input voltage signal to be converted with the full scale range of the converter, the converter including at least one array of binary weighted capacitors. The method includes the step of obtaining a digital gain code that represents the ratio between the full scale range and the dynamic range of the voltage signal to be converted, applying the voltage signal to be converted to the capacitor array so as to charge with the voltage signal to be converted only those array capacitors having the same binary weights as the bits of the gain code that have a selected binary value, and selectively coupling the capacitors of the array to one of a first and second predetermined reference voltage terminals according to an SAR technique, to obtain an output digital code corresponding to the input voltage signal. It should be noted that the gain control achieved by the SAR-ADC in US 6,720,903 B2 is relatively coarse. If used in a as a sub ADC in a TI-ADC, a finer degree of gain control may be needed, depending on requirements of a given application.

A problem with the binary-weighted capacitor bank is that the size grows exponentially with the number of bits. For large B, the DAC consumes a large power, silicon area and is complicated to layout due to matching requirements. Another side effect is that the circuit driving the ADC input needs to supply a large current to charge the large capacitors during the sampling phase.

To reduce the above-mentioned problems with a binary-weighted capacitor bank, the capacitor bank can be split into two sections with a bridge capacitor connected between them, resulting in a bridged capacitor bank. The two sections are commonly referred to as the main-DAC (MDAC) and sub-DAC (SDAC). The SDAC interpolates between the values of the MDAC. One may relate the MDAC and SDAC gains through a bridge ratio, here defined as the gain of the MDAC LSB to the comparator input divided by the gain of the SDAC MSB to the comparator input. To have a linear DAC transfer (equidistant quantization levels), it is important that the radix is 2 for all capacitors controlled by the digital word being converted. If the bridge ratio differs from its ideal value, the MDAC and SDAC may still be individually linear (radix-2), but the overall DAC transfer is nonlinear. To ensure a relatively accurate bridge ratio, the bridge capacitor should be matched with the other capacitors in the DAC. Different techniques for achieving relatively well-matched capacitors exist, such as implementing each capacitor as parallel connections of a number of smaller unit capacitors. However, perfect matching cannot be achieved in practice, and the bridge ratio will not be perfectly accurate. Parasitics also contribute to inaccuracy of the bridge ratio. Hence, an inaccuracy in the bridge ratio may therefore need to be estimated and corrected.

Summary

According to embodiments disclosed herein, bridged capacitor banks are utilized that have additional capacitors compared with conventional bridged capacitor banks. These additional capacitors can be used in various ways to compensate for matching problems, such as gain errors between sub ADCs or bridge-ratio inaccuracies.

According to a first aspect, there is provided SAR comprising an input for receiving an input voltage, a comparator, a SAR state machine connected to an output of the comparator, a first switch network configured to be controlled by the SAR state machine and connected to the input of the SAR ADC and to reference voltage nodes, and a first capacitor network. The first capacitor network comprises a first node connected to an input of the comparator, a second node, and a bridge capacitor connected between the first node and the second node. Furthermore, the first capacitor network comprises a first set of capacitors having a first and a second terminal, wherein the first terminal of each capacitor in the first set is connected to the first node and the second terminal of each capacitor in the first set is connected to the first switch network. Moreover, the first capacitor network comprises a second set of capacitors having a first and a second terminal, wherein the first terminal of each capacitor in the second set is connected to the second node and the second terminal of each capacitor in the first set is connected to the first switch network. The SAR state machine is configured to control the first switch network such that the input voltage is sampled on one or more of the capacitors in the union of the first and the second set during a first phase of a sampling clock period. Furthermore, the SAR state machine is configured to control the first switch network such that SAR A/D conversion is performed during a subsequent second phase of the sampling clock period. The SAR ADC further comprises a second capacitor network connected to the second node of the first capacitor network and configured to control a gain of the SAR ADC.

The second capacitor network may comprise a capacitor ladder. The capacitor ladder may comprise a set of k connection points, in the following numbered from 1 to k. The 1:st connection point may be connected to the second node of the first capacitor network. For each $j = 1, ..., k–1$, the capacitor ladder may comprise a bridge capacitor connected between connection point j and connection point $j+1$. For each $j = 1, ..., k$, the capacitor ladder may comprises a j:th capacitor having a first terminal connected to connection point j. The second capacitor network may comprise a capacitor connected between connection point k and a ground node. The second capacitor network may comprise a capacitor connected between connection point 1 and a ground node.

The SAR ADC may comprise a second switch network. For each $j = 1, ..., k$, the second switch network may comprise a j:th switch configured to connect a second terminal of the j:th capacitor of the second capacitor network to a ground node during the second phase of the sampling clock period, and to selectively connect the second terminal of the j:th capacitor of the second capacitor network to the ground node or the input of the SAR ADC during the first phase of the sampling clock period to control the gain of the SAR ADC. Furthermore, the SAR ADC may comprise a third switch network configured to connect the k connection points of the second capacitor network to the ground node during the first phase of the sampling clock period and to disconnect the k connection points of second capacitor network from the ground node during the second phase of the sampling clock period.

The SAR ADC may comprise a test sequence interface configured to provide a binary test sequence during a plurality of consecutive sampling clock periods. Each of the plurality of sampling clock periods may have an associated sample of the binary test sequence. The first capacitor network may comprise a first test-signal capacitor having a first and a second terminal, wherein the first terminal is connected to the first node of the first capacitor network. The first capacitor network may comprise a second test-signal capacitor having a first and a second terminal, wherein the first terminal is connected to the second node of the first capacitor network. For each of the plurality of consecutive sampling clock periods, the second terminal of the first test-signal capacitor may be configured to be supplied with a first voltage representing the associated sample of the binary test sequence, and the second terminal of the second test-signal capacitor may be configured to be supplied with a second voltage representing the associated sample of the binary test sequence, such that a contribution of the first voltage at the input of the comparator is counteracted.

The first voltage and the second voltage may be selected from a positive reference voltage and a negative reference voltage in response to the binary test sequence.

In some embodiments, the first test-signal capacitor is configured to be supplied with the first voltage in one of the first phase and the second phase of the sampling clock period, the second terminal of the second test-signal capacitor is configured to be supplied with the second voltage in the same one of the first phase and the second phase of the sampling clock period, and the first voltage and the second voltage have opposite polarity.

In some embodiments, the second terminal of the first test-signal capacitor is configured to be supplied with the first voltage in one of the first phase and the second phase of the sampling clock period, the second terminal of the second test-signal capacitor is configured to

be supplied with the second voltage in the other one of the first phase and the second phase of the sampling clock period, and the first voltage and the second voltage have the same polarity.

The binary test sequence may be a pseudo-random binary sequence.

The SAR ADC may comprise circuitry configured to estimate a bridge ratio based on output samples the SAR ADC generated during said plurality of sampling clock periods.

According to a second aspect, there is provided a time-interleaved ADC comprising a plurality of sub ADCs, each implemented as the SAR ADC according to the first aspect.

According to a third aspect, there is provided a receiver circuit comprising the SAR ADC of the first aspect or the time-interleaved ADC according to the second aspect.

According to a fourth aspect, there is provided an electronic apparatus comprising the SAR ADC of the first aspect, the time-interleaved ADC of the second aspect, or the receiver circuit of the third aspect. The electronic apparatus may be a communication apparatus, such as but not limited to a wireless communication device or a base station for a cellular communications system.

Further embodiments are defined in the dependent claims. It should be emphasized that the term "comprises/comprising" when used in this specification is taken to specify the presence of stated features, integers, steps, or components, but does not preclude the presence or addition of one or more other features, integers, steps, components, or groups thereof.

Brief description of the drawings

Fig. 1 illustrates a communication environment.

Fig. 2 illustrates a transceiver circuit.

Fig. 3 illustrates a TI-ADC.

Fig. 4 illustrates a bridged capacitor bank and an equivalent representation.

Fig. 5 shows plots of relations between capacitance values for a bridge ratio of 2.

Fig. 6 shows plots of relations between capacitance values for a bridge ratio of 1.

Figs. 7-8 illustrate different bridged capacitor banks.

Fig. 9 illustrates a SAR ADC.

Fig, 10 illustrates a sampling clock period.

Fig. 11 illustrates a capacitor network.

Fig. 12 illustrates a capacitor network and switches.

Fig. 13 illustrates circuitry for applying a test signal.

Detailed description

In this description, reference is made to various voltage levels. As is well known to a person skilled in the art of electronic design, what voltage level is considered to be zero volts, or "ground", can be arbitrarily selected. Often, ground is used to denote the lowest voltage level available in an integrated circuit, but this is not the case in this description. In this description, ground has been selected to be in the middle between two reference voltage levels. These reference voltage levels are referred to as a positive reference voltage $+V_{ref}$ and a negative reference voltage $-V_{ref}$.

Fig. 1 illustrates a communication environment wherein embodiments of the present invention may be employed. A wireless communication device 1, or wireless device 1 for short, of a cellular communications system is in wireless communication with a radio base station 2 of the cellular communications system. The wireless device 1 may be what is generally referred to as a user equipment (UE). The wireless devices 1 is depicted in Fig. 1 as a mobile phone, but may be any kind of device with cellular communication capabilities, such as a tablet or laptop computer, machine-type communication (MTC) device, or similar. Furthermore, a cellular communications system is used as an example throughout this disclosure. However, embodiments of the present invention may be applicable in other types of systems as well, such as but not limited to WiFi systems.

The radio base station 2 and wireless device 1 are examples of what in this disclosure is generically referred to as communication apparatuses. Embodiments are described below in the context of a communication apparatus in the form of the radio base station 2 or wireless device 1. However, other types of communication apparatuses can be considered as well, such as a WiFi access point or WiFi enabled device.

Fig. 2 is a block diagram of an embodiment of a transceiver circuit 10, which can be comprised in a communication apparatus, such as the radio base station 2 or the wireless device 1. In the embodiment illustrated in Fig. 2, the transceiver circuit 10 comprises a digital signal processing (DSP) circuit 15. The DSP circuit 15 may e.g. be what is commonly referred to as baseband processor. The DSP circuit 15 may e.g. be configured to perform various digital signal processing tasks, such as one or more of coding, decoding, modulation, demodulation, fast Fourier transform (FFT), inverse FFT (IFFT), mapping, demapping, etc.

Furthermore, in the embodiment illustrated in Fig. 2, the transceiver circuit 10 comprises a transmitter circuit 20. The transmitter circuit 20 comprises a digital-to-analog converter (DAC) 25. The DAC 25 is connected to the DSP circuit 15 and configured to receive, as an input signal of the DAC 25, a digital representation of a signal to be transmitted from the DSP

circuit 15. The DAC 25 is further configured to convert the signal to be transmitted to an analog representation, which is an output signal of the DAC 25. The transmitter circuit 20 also comprises a transmitter (Tx) frontend (FE) circuit 30 connected between the DAC 25 and an antenna 35. The Tx FE circuit 30 is configured to transform the output signal from the DAC 25 to a format suitable for transmission via the antenna 35. This may include operations such as frequency upconversion, filtering, and/or amplification. The Tx FE circuit 30 may comprise one or more mixers, filters, and/or amplifiers, such as power amplifiers (PAs), to perform such operations. The design of such Tx FE circuits is, per se, well known to a person skilled in the field of radio transceiver design, and is not discussed herein in any further detail.

Moreover, in the embodiment illustrated in Fig. 2, the transceiver circuit 10 comprises a receiver circuit 40. The receiver circuit 40 comprises a receiver (Rx) FE circuit 45 connected to the antenna 35. Furthermore, the receiver circuit 40 comprises an ADC 50. The ADC 50 is connected between the Rx FE circuit 45 and the DSP circuit 15. The Rx FE circuit is 45 is configured to is transform a signal received via the antenna 35 to a format suitable to be input to the ADC 50. This may include operations such as frequency downconversion, filtering, and/or amplification. The Rx FE circuit 45 may comprise one or more mixers, filters, and/or amplifiers, such as low-noise amplifiers (LNAs), to perform such operations. The design of such Rx FE circuits is, per se, well known to a person skilled in the field of radio transceiver design, and is not discussed herein in any further detail. The ADC 50 is configured to receive its (analog) input signal from the Rx FE circuit, and convert it to a digital representation to generate the digital output signal of the ADC 50. This digital output signal of the ADC 50 is input to the DSP circuit 15 for further digital signal processing.

Fig. 3 is a block diagram of the ADC 50 according to some embodiments. The ADC 50 may, for instance, be integrated on an integrated circuit. It comprises a plurality of sub ADCs A1-AM configured to operate in a time-interleaved manner. The integer M denotes the number of sub ADCs A1-AM. As illustrated in Fig. 3, the ADC 50 may comprise an S/H circuit 60 that is common to all sub ADCs A1-AM. In Fig. 3, the S/H circuit has an input 61 configured to receive an input voltage $v_{\text{in}}(t)$ representing the analog input signal of the ADC 50 at (continuous) time t. Furthermore, it has an output 63 configured to output a sampled input voltage $v_{\text{s}}(n)$ representing the analog input signal at sampling instants nT, where n is an integer valued sequence index and T is the sampling period time of the ADC 50. The ADC 50 may comprise an analog demultiplexer 70 configured to distribute samples of $v_{\text{s}}(n)$ to the correct sub ADC Ai. It should be noted that in some embodiments, the S/H circuit 60 may be omitted, for instance by having S/H circuits in the sub ADCs A1-AM instead. Moreover, the

ADC 50 may comprise a digital multiplexer 75 configured to interleave the outputs from the sub ADCs A1-A*M* in the correct order and output the interleaved output sequence on an output 76 as the digital output signal of the ADC 50.

Before going into more detailed embodiments of the sub ADCs A1-A*M*, some analyses of bridged capacitor banks are first discussed.

Fig. 4 shows, in the upper part, an example of a bridged capacitor bank with the SDAC part on the left and the MDAC part on the right. The bridge capacitor has the capacitance C_b, and the each of the other capacitors has a capacitance that is an integer multiple of a unit capacitance C. BM denotes the number of bits in the MDAC, and BS denotes the number of bits in the SDAC. The right-most node is connected to a comparator (not shown) and is referred to as the comparator node. The lower part of Fig. 4 shows an equivalent representation of the bridged capacitor bank. C_1 is the capacitance of the smallest capacitor (or LSB capacitor) of the MDAC and C_x is the sum of the capacitances of the other capacitors of the MDAC. C_2 is the capacitance of the largest capacitor (or MSB capacitor) of the SDAC and C_y is the sum of the capacitances of the other capacitors of the SDAC. It should be noted that the representation in the lower part of Fig. 4 is more general and may represent a bridged capacitor bank with other capacitance values than those shown in the upper part of Fig. 4. In the following, the letter C with an index is used interchangeably to represent a capacitance value and for the capacitor having that capacitance value. When the capacitor banks shown in drawings are in use, the bottom-nodes of the capacitors (other than C_b), which appear unconnected (or "floating") in the drawings such as Fig. 4, are to be connected voltage sources that can supply electrical charge to them. Such voltage sources can for instance be a S/H circuit that supplies a sampled input voltage, a reference voltage source that supplies a positive or negative reference voltage, or a source that provides a signal ground. The connections can be made via switches that can switch the nodes of the capacitors between different such voltage sources during the operation of the ADC in which the bridged capacitor bank is comprised. Such connections and voltage sources are omitted in drawings of capacitor banks for simplicity, but are assumed in the following analyses.

The bridge ratio is found by applying a step at the input of C_1 and C_2 and evaluating their contributions at the comparator node. The gain H_1 to the comparator node for C_1 is given by

$$H_1 = \frac{C_1(C_y + C_\mathrm{b} + C_2)}{C_y(C_\mathrm{x} + C_\mathrm{b} + C_1) + C_\mathrm{x}(C_\mathrm{b} + C_2) + C_\mathrm{b}(C_1 + C_2) + C_1C_2} \quad (1)$$

The gain H_2 to the comparator node for C_2 is given by

$$H_2 = \frac{C_2 C_\mathrm{b}}{C_y(C_\mathrm{x} + C_\mathrm{b} + C_1) + C_\mathrm{x}(C_\mathrm{b} + C_2) + C_\mathrm{b}(C_1 + C_2) + C_1 C_2} \tag{2}$$

The bridge ratio is given by the ratio

$$r = \frac{H_1}{H_2} = \frac{C_1(C_y + C_\mathrm{b} + C_2)}{C_2 C_\mathrm{b}} \tag{3}$$

For a given desired bridge ratio, the capacitance value of the bridge capacitor can be calculated as

$$C_\mathrm{b} = \frac{C_1(C_2 + C_y)}{C_2 r - C_1} \tag{4}$$

In the following, a normalized measure of capacitance is used where the unit capacitance $C = 1$ for simplicity, but without loss of generality. Suppose an extra capacitor C_e (not shown in Fig. 4) is added to the SDAC, the following holds for a binary weighted capacitor bank

$$\begin{aligned} C_1 &= 1 \\ C_2 &= 2^{BS-1} \\ C_\mathrm{y} &= (2^{BS-1} - 1) + C_e \end{aligned} \tag{5}$$

Inserting the above relations into the bridge capacitor equation, the capacitance C_e is given by

$$C_\mathrm{e} = C_\mathrm{b}(2^{BS-1}\mathrm{r} - 1) + 1 - 2^{BS} \tag{6}$$

C_e is the capacitance in the SDAC to (signal) ground in addition to the binary weighted part with BS bits. C_e is plotted for $BS = 3, 4, 5$ with $r = 2$ in Fig. 5 and $r = 1$ in Fig. 6, where the solutions for integer C_b and C_e are marked. It can be observed in Fig. 5 that for $r = 2$ and $C_b = 1$ (or, in other words, C_b is equal to the unit capacitance C, which is 1 in the normalized capacitance measure used in the analysis), $C_e = 0$. That is, no extra capacitor C_e should be added to achieve a bridge ratio of 2 when the bridge capacitor has the unit capacitance C. Furthermore, it can be observed from Fig. 6 that for $r = 1$, the minimum integer value of C_b that results in a non-negative value of C_e is 3. That is, if the bridge capacitor is implemented by parallel connection of an integer number of unit capacitors, each having the unit capacitance C, the number of parallel-connected unit capacitors need to be at least 3.

Exemplary capacitor banks are shown in Fig. 7 for $r = 2$ and in Fig. 8 for $r = 1$. Note again that, in use, the bottom nodes of the capacitors, including C_e, are not floating.

For $r = 2$, a bridge ratio of two is implemented, which means that all capacitors give a binary weighted contribution at the comparator input.

For $r = 1$, a bridge ratio of unity is achieved. This means that the capacitor with highest capacitance on the SDAC side and the capacitor with the lowest capacitance on the MDAC side have equal weight, while the other capacitors are binary weighted.

An insight that can be drawn as a conclusion of the analyses above is that, for a given desired bridge ratio, it is possible to add one or more additional capacitors (above represented by the additional capacitor C_e) by carefully selecting the capacitance of the bridge capacitor C_b. This insight is exploited in embodiments described below.

Fig. 9 illustrates part of a SAR-ADC according to some embodiments. To indicate that the SAR ADC may be used as any one of the sub ADC A1-A*M* in the TI-ADC 50 (Fig. 3), the reference sign A*i* is used for the SAR-ADC in Fig. 9. In Fig. 9, the SAR ADC A*i* comprises an input for receiving an input voltage V_{in}. Furthermore, it comprises a comparator 100 and an SAR state machine 110 connected to an output of the comparator 100. Moreover, it comprises a first switch network 120 configured to be controlled by the SAR state machine 110. The first switch network 120 is connected to the input of the SAR ADC A*i* and to reference voltage nodes $+V_{ref}$ and $-V_{ref}$. The SAR ADC A*i* further comprises a first capacitor network 130. The first capacitor network 130 is built up as a bridged capacitor bank as discussed above. It comprises a first node 140 connected to an input of the comparator 100 and a second node 150. It further comprises a bridge capacitor Cb connected between the first node 140 and the second node 150. Moreover, it comprises a first set 160 of capacitors and a second set 170 of capacitors. The capacitors in the first set 160 each has a first and a second terminal, wherein the first terminal is connected to the first node 140 and the second terminal is connected to the first switch network 120. In Fig. 9, the first terminal is directed up and the second terminal is directed down. The capacitors in the second set 170 each has a first and a second terminal, wherein the first terminal is connected to the second node 150 and the second terminal is connected to the first switch network 120. In Fig. 9, the first terminal is directed up and the second terminal is directed down. The SAR state machine (SM) 110 is configured to control the first switch network 120 such that the input voltage V_{in} is sampled on one or more of the capacitors in the union of the first and the second set 160, 170 during a first phase of a sampling clock period. In some embodiments, the SAR SM 110 is configured to control the switches in the first switch network 120 to connect the second terminal of each

capacitor in the first set 160 and the second set 170 to the input of the SAR ADC A*i* during the first phase of the sampling clock period. Thereby, the input voltage V_{in} is sampled on all of these capacitors. In some embodiments, the SAR SM 110 is configured to control the switches in the first switch network 120 to connect the second terminals of a subset of the capacitors in the first set 160 and the second set 170 to the input of the SAR ADC A*i* during the first phase of the sampling clock period. Furthermore, in these embodiments, the SAR SM 110 is configured to control the switches in the first switch network 120 to connect the second terminals of the remaining capacitors in the first set 160 and the second set 170 to a ground node during the first phase of the sampling clock period. By selecting which capacitors are part of the subset whose second terminals are connected to the input of the SAR ADC A*i*, a coarse gain control of the SAR ADC A*i* can be obtained, similar to what is described in US 6,720,903 B2. During the first phase of the sampling clock period, switches s1 and s2, shown in Fig. 9, may be controlled to connect the first node 140 and the second node 150, respectively, to ground nodes to allow a net flow of electrical charge to and from these nodes. Moreover, the SAR SM 110 is configured to control the switches in the first switch network 120 such that SAR analog-to-digital, A/D, conversion is performed during a subsequent second phase of the sampling clock period. For example, assuming a binary-weighted architecture, the second terminal of each capacitor is initially (i.e. at the start of the second phase of the sampling clock period) connected to ground. Furthermore, the first node 140 and the second node 150 are disconnected from ground by opening switches s1 and s2. The comparator is then allowed to settle. If the output of the comparator is 'high', or '1', the MSB of the output sample is set to '1' and the second terminal of the corresponding capacitor is connected to $-V_{ref}$. If the output of the comparator is 'low', or '0', the MSB of the output sample is set to '0' and the second terminal of the corresponding capacitor is connected to $+V_{ref}$. Subsequently, the comparator is again allowed to settle. If the output of the comparator is 'high', or '1', the second most significant bit, or "MSB–1" of the output sample is set to '1' and the second terminal of the corresponding capacitor is connected to $-V_{ref}$. If the output of the comparator is 'low', or '0', the MSB–1 of the output sample is set to '0' and the second terminal of the corresponding capacitor is connected to $+V_{ref}$. This procedure is iterated for each bit, in the order of decreasing significance, until all bits of the output sample have been determined. SAR A/D conversion procedures such as that outlined above are well known and therefore not described in any further detail herein.

Fig. 10 illustrates how the sampling clock period is divided into the first and the second phase, possibly with some guard interval in between them. Furthermore, it is illustrated how

the second phase is in turn divided into sub intervals in which the individual bits are determined. In Fig. 10, the bits MSB, MSB–1, LSB+1 (second least significant bit), and LSB are explicitly indicated. The dotted line represents all of the bits in between MSB–1 and LSB+1.

As described above, the capacitance value of the bridge capacitor C_b can be selected in such a way that an additional capacitive circuit (above referred to as capacitor C_e) can be connected to the second node 150.

In some embodiments, the SAR ADC A*i* further comprises a second capacitor network 180 connected to the second node 150 of the first capacitor network and configured to control a gain of the SAR ADC A*i*. This is illustrated in Fig. 11. As described in further detail below, this second capacitor network can be used for fine gain control of the SAR ADC A*i*. Coarse gain control can be obtained as outlined above with reference to US 6,720,903 B2.

In some embodiments, the second capacitor network 180 comprises a capacitor ladder. An example of this is illustrated in Fig. 12. In Fig. 12, the capacitor ladder comprises a set of k connection points, in the following numbered from 1 to k. In the example shown, $k = 3$, but any number of connection points may be used. In Fig. 12, the j:th connection point is labeled with the reference sign pj. The 1:st connection point p1 is connected to the second node 150 of the first capacitor network. For each $j = 1, ..., k–1$, the capacitor ladder comprises a bridge capacitor connected between the j:th connection point pj and the (j+1):th connection point p(j+1). Furthermore, for each $j = 1, ..., k$, the second capacitor network comprises a j:th capacitor having a first terminal connected to the j:th connection point pj. Furthermore, the second capacitor network 180 may comprise a capacitor connected between the k:th connection point pk and a ground node (i.e. the leftmost capacitor shown in Fig. 12). In the example shown in Fig. 12, the bridge capacitors have the capacitance 2C and the other capacitors in the capacitor ladder, including the capacitor connected between pk and ground, have capacitance C. This is a so called C-2C ladder structure. Regardless of how large the C-2C ladder is, i.e. how many connection points it has, the capacitance of the C-2C ladder seen from connection point p1 is 2C.

In order to get the desired total capacitance of the second capacitor network 180, an additional capacitor might need to be added, for example between p1 and ground. This is illustrated in Fig. 12 with an optional capacitor having the capacitance 5C. If this capacitance is included, the total capacitance of the second capacitor network 180 seen at connection point p1 is 7C. Hence, referring to Figs. 5 and 7, this particular example of the second capacitor network would be suitable for a 3-bit SDAC with Cb = 2C and a bridge ratio of 2 in the first

capacitor network 130 (see Fig. 5, lower graph, and Fig. 7, the topmost bridged capacitor bank). To be suitable in other scenarios, the capacitance value should be adjusted accordingly.

As illustrated in Fig. 12, the SAR ADC A*i* may comprise a second switch network 190. For each $j = 1, ..., k$, the second switch network comprises a *j*:th switch g*j*. The switch g*j* is configured to connect a second terminal of the *j*:th capacitor of the second capacitor network 180 to ground during the second phase of the sampling clock period. The switch g*j* is further configured to selectively connect the second terminal of the *j*:th capacitor of the second capacitor network to the ground node or the input of the SAR ADC A*i* during the first phase of the sampling clock period. By controlling which of the 1:st capacitor to the *k*:th capacitor of the capacitor ladder have its second node connected to the input of the SAR ADC A*i* during the first phase of the sampling clock period, the gain of the SAR ADC A*i* is controlled. as discussed above, this provides a finer control of the gain than controlling which of the capacitors in the first set 160 and the second set 170 (Fig. 9) are used to sample the input voltage V_{in} during the first phase of the sampling clock period. Increasing the total number *k* of connection points p*j* (i.e. increasing the size of the capacitor ladder) increases the resolution of the gain control.

As is also illustrated in Fig. 12, the SAR ADC may comprise a third switch network 195 configured to connect the *k* connection points p*j* of the second capacitor network 180 to ground during the first phase of the sampling clock period. Thereby, a net flow of electrical charge to and from these connection points is enabled during the first phase of the sampling clock period. Furthermore, the third switch network 195 is configured to disconnect the *k* connection points p1-p3 of second capacitor network 180 from ground during the second phase of the sampling clock period. Thereby, a net flow of electrical charge to and from these connection points is disabled during the second phase of the sampling clock period.

Above, embodiments are described with reference to Figs. 11-12 where the possibility to add additional capacitance to the second node 150 is utilized for controlling the gain of the SAR ADC A*i*. Alternatively or additionally, said possibility can be utilized for other purposes. One such purpose is to inject a test signal for estimating the bridge ratio of the first capacitor network. In essence, an additional capacitor is added to each side of the capacitor and a known test sequence $p[n]$ is injected into each of these capacitors in such a way that the contributions due to the test sequence $p[n]$ from these two capacitors counteract each other at the input of the comparator 100. The actual bridge ratio can be estimated by studying the digital output signal from the SAR ADC A*i* and estimating to what degree the test sequence $p[n]$ appears in said digital output signal from the SAR ADC A*i*. This can be done by

correlating the digital output signal of the SAR ADC A*i* with the test sequence $p[n]$. The resulting correlation can be used as an estimate of said degree to which the test sequence $p[n]$ appears in the output signal of the SAR ADC A*i*. The two capacitors may be designed such that said contributions cancel at the input of the comparator 100 if the bridge ratio has just the right value (i.e. the value it is intended to have). In that case, the test sequence $p[n]$ does not appear at all in the digital output signal from the SAR ADC A*i*. However, if there is a deviation from the intended bridge ratio, the contributions will not cancel perfectly at the input of the comparator 100, and a nonzero residue of the test sequence $p[n]$ remains in the output signal of the SAR ADC A*i*. A measure of how large this residue is, or in other words a measure of the aforementioned degree, such as said correlation, can be used to estimate how much the bridge ratio deviates from the intended value. Such embodiments are described below with reference to Fig. 13.

According to some embodiments, the SAR ADC A*i* comprises a test sequence interface 200 configured to provide a binary test sequence $p[n]$ during a plurality of consecutive sampling clock periods. In some embodiments, the binary test sequence $p[n]$ is provided at all time when the SAR ADC A*i* is in operation, whereby said plurality of consecutive sampling clock periods is, in some sense, all sampling clock periods. In other embodiments, the binary test sequence $p[n]$ is only applied during certain test intervals. In these cases, the plurality of consecutive sampling clock periods refers to the sampling clock periods within one such test interval. Each of the plurality of sampling clock periods, identified by the sequence index n, has an associated sample of the binary test sequence $p[n]$. In some examples below, where operation during a specific sampling clock period is described, the associated sample (i.e. associated with that sampling clock period) is sometimes referred to as the "current sample". In some embodiments, the SAR ADC A*i* comprises a test signal generator circuit 210 that is configured to generate the binary test sequence $p[n]$ and supply it to the test signal interface 200. In other embodiments, the binary test sequence $p[n]$ is supplied to the test signal interface by a test signal generator external to the SAR ADC A*i*. For example, the TI ADC 50 may comprise a test signal generation circuit that is common to all the sub ADCs A1-A*M*. In other embodiments, the test signal generation circuit may be external to the TI ADC 50. In some embodiments, the binary test sequence $p[n]$ is a pseudo-random binary sequence (PRBS). In such embodiments, the test signal generator circuit 210 may be implemented as a PRBS generator, for instance using a linear-feedback shift register. In some embodiments, the binary test sequence $p[n]$ may be pre-generated and stored in a memory of the test signal generator circuit 210. A PRBS is suitable for estimating the bridge ratio error during "normal

operation" of the SAR ADC A*i*, where an input signal that can have a significantly higher magnitude than the residue of the binary test sequence $p[n]$ (e.g. measured at the input of the comparator 100) is present. A PRBS is generally uncorrelated to the input signal, and its residue can therefore be recovered from the output signal of the SAR ADC A*i* by means of correlation.

According to some embodiments, the first capacitor network 130 comprises a first test-signal capacitor C_{T1} and a second test signal capacitor C_{T2}. The first test-signal capacitor C_{T1} has a first and a second terminal, wherein the first terminal is connected to the first node 140 of the first capacitor network 130. Similarly, the second test-signal capacitor C_{T2} has a first and a second terminal, wherein the first terminal is connected to the second node 150 of the first capacitor network 130. For each of the plurality of consecutive sampling clock periods, the second terminal of the first test-signal capacitor C_{T1} is configured to be supplied with a first voltage $V_1[n]$ in representing the associated sample of the binary test sequence $p[n]$, and the second terminal of the second test-signal capacitor C_{T2} is configured to be supplied with a second voltage $V_2[n]$, also representing the associated sample of the binary test sequence $p[n]$, such that a contribution of the first voltage $V_1[n]$ at the input of the comparator 100 is counteracted.

In the following, it is assumed that the sizes of the test signal capacitors are selected such the contribution from the second voltage $V_2[n]$ cancels the contribution from the first voltage $V_1[n]$ at the input of the comparator if the bridge ratio is just right, i.e. that the voltage gain from the second terminal of the second test signal capacitor C_{T2} to the input of the comparator 100 is equal to the voltage gain from the second terminal of the first test-signal capacitor C_{T1} to the input of the comparator 100. There are some different ways in which the first and second voltages $V_1[n]$ and $V_2[n]$ can be selected and supplied such that the above-mentioned counteraction is obtained. A few of these are mentioned below. For example, the first and second voltages $V_1[n]$ and $V_2[n]$ may have the same amplitude and the capacitors C_{T1} and C_{T2} may be designed to yield the same voltage gain to the comparator input. This can, for instance, be obtained by using the bridged capacitor bank second from the top of Fig. 8 (BS=4). Here, C_{T2} corresponds to the capacitance of 8C. C_{T1} does not have any corresponding capacitor in Fig. 8, but has to be added to the first node 140 with a capacitance of C. Adding capacitance to the first node 140 does not affect the bridge ratio. C_{T1} and C_{T2} present a unity weighted contribution at the input of the comparator and the remaining binary weighted capacitors present a binary weighted contribution at the input of the comparator. Part or all of

the additional capacitor with capacitance $6C$ can, in some embodiments, be realized as the second capacitor network 180.

In some embodiments, the first voltage $V_1[n]$ and the second voltage $V_2[n]$ are selected from a positive reference voltage $+V_{ref}$ and a negative reference voltage $-V_{ref}$ in response to the binary test sequence $p[n]$. A '0' sample in the sequence may correspond to one of $+V_{ref}$ and $-V_{ref}$. A '1' sample in the sequence may correspond to the other one of $+V_{ref}$ and $-V_{ref}$. Fig. 200 illustrates that the test signal interface may be configured to control switches to connect the second terminals of C_{T1} and C_{T2} to $+V_{ref}$ or $-V_{ref}$ in response to the test sequence $p[n]$.

In some embodiments, the second terminal of the first test-signal capacitor C_{T1} is configured to be supplied with the first voltage $V_1[n]$ in one of the first phase and the second phase of the sampling clock period and the second terminal of the second test-signal capacitor C_{T2} is configured to be supplied with the second voltage $V_2[n]$ in the same one of the first phase and the second phase of the sampling clock period. In these embodiments, the first voltage $V_1[n]$ and the second voltage $V_2[n]$ have opposite polarity in order to counteract each other's contributions at the input of the comparator 100. For example, if, for the first voltage $V_1[n]$, a '0' in the test sequence $p[n]$ corresponds to $V_1[n] = -V_{ref}$ and a '1' in the test sequence $p[n]$ corresponds to $V_1[n] = +V_{ref}$, then, for the second voltage $V_2[n]$, a '0' in the test sequence $p[n]$ corresponds to $V_2[n] = +V_{ref}$ and a '1' in the test sequence $p[n]$ corresponds to $V_2[n] = -V_{ref}$.

For instance, the second terminal of C_{T1} may be configured to be selectively (in response to the current sample of the test sequence $p[n]$) supplied with one of $+V_{ref}$ and $-V_{ref}$ and the second terminal of C_{T2} may be configured to be selectively supplied with the other one of $+V_{ref}$ and $-V_{ref}$ in the first phase of the sampling clock period, e.g. under control of the test signal interface 200. The second terminals of C_{T1} and C_{T2} may be configured to be connected to ground during the second phase of the sampling clock period. Fig. 13 illustrates this possibility with optional connections to ground in the switches connected to the second terminals of C_{T1} and C_{T2}. During the first phase of the sampling clock period, any deviation from the desired bridge ratio will manifest itself as a residue of the current sample of the test sequence $p[n]$ that is superpositioned onto the current sample of the input signal of the SAR ADC Ai, and remains so during the second phase of the sampling clock signal.

Alternatively, in some embodiments, the second terminal of C_{T1} may be configured to be selectively (in response to the current sample of the test sequence $p[n]$) supplied with one of $+V_{ref}$ and $-V_{ref}$ and the second terminal of C_{T2} may be configured to be selectively supplied

with the other one of $+V_{ref}$ and $-V_{ref}$ in the second phase of the sampling clock period, e.g. under control of the test signal interface 200. The second terminals of C_{T1} and C_{T2} may be configured to be connected to ground or to the receive the input voltage V_{in} during the first phase of the sampling clock period. In the latter case, C_{T1} and C_{T2} contributes to the sampling of the input voltage V_{in}, and may thus be utilized in the coarse gain control of the SAR ADC A*i*. Fig. 13 illustrates this latter possibility by including optional connections to V_{in} in the switches connected to the second terminals of C_{T1} and C_{T2}. In these embodiments, residue of the current sample of the test sequence $p[n]$ is superpositioned onto the current sample of the input signal of the SAR ADC A*i* in the second phase of the sampling clock signal (since this is when the test sequence $p[n]$ is applied).

In some embodiments, the second terminal of the first test-signal capacitor C_{T1} is configured to be supplied with the first voltage $V_1[n]$ in one of the first phase and the second phase of the sampling clock period and the second terminal of the second test-signal capacitor C_{T2} is configured to be supplied with the second voltage $V_2[n]$ in the other one of the first phase and the second phase of the sampling clock period. In these embodiments, the first voltage $V_1[n]$ and the second voltage have the same polarity in order to counteract each other's contributions at the input of the comparator 100. For example, if, for the first voltage $V_1[n]$, a '0' in the test sequence $p[n]$ corresponds to $V_1[n] = -V_{ref}$ and a '1' in the test sequence $p[n]$ corresponds to $V_1[n] = +V_{ref}$, then, for the second voltage, a '0' in the test sequence $p[n]$ also corresponds to $V_2[n] = -V_{ref}$ and a '1' in the test sequence $p[n]$ also corresponds to $V_2[n] = +V_{ref}$.

For instance, the second terminal of C_{T1} may be configured to be selectively (in response to the current sample of the test sequence $p[n]$) supplied with one of $+V_{ref}$ and $-V_{ref}$ in the first phase of the sampling clock period, and the second terminal of C_{T2} may be configured to be selectively supplied with the same one of $+V_{ref}$ and $-V_{ref}$ in the second phase of the sampling clock period, e.g. under control of the test signal interface 200. The second terminal of C_{T1} may be configured to be connected to ground during the second phase of the sampling clock period. The second terminal of C_{T2} may be configured to be connected to ground or to receive the input voltage V_{in} during the first phase of the sampling clock period. In the latter case, C_{T2} contributes to the sampling of the input voltage V_{in}, and may thus be utilized in the coarse gain control of the SAR ADC A*i*. During the first phase of the sampling clock period, a contribution from the first voltage $V_1[n]$ is superpositioned onto the current sample of the input signal of the SAR ADC A*i*. During the second phase of the sampling clock signal, a corresponding contribution from the second voltage $V_2[n]$ is subtracted therefrom, and a

residue of the current sample of the test sequence $p[n]$, which is indicative of the deviation from the intended bridge ratio, remains superpositioned onto the current sample of the input signal.

Alternatively, in some embodiments, the second terminal of C_{T1} may be configured to be selectively (in response to the current sample of the test sequence $p[n]$) supplied with one of $+V_{ref}$ and $-V_{ref}$ in the second phase of the sampling clock period, and the second terminal of C_{T2} may be configured to be selectively supplied with the same one of $+V_{ref}$ and $-V_{ref}$ in the first phase of the sampling clock period, e.g. under control of the test signal interface 200. The second terminal of C_{T2} may be configured to be connected to ground during the second phase of the sampling clock period. The second terminal of C_{T1} may be configured to be connected to ground or to the receive the input voltage V_{in} during the first phase of the sampling clock period. In the latter case, C_{T1} contributes to the sampling of the input voltage V_{in}, and may thus be utilized in the coarse gain control of the SAR ADC A*i*. During the first phase of the sampling clock period, a contribution from the second voltage $V_2[n]$ is superpositioned onto the current sample of the input signal of the SAR ADC A*i*. During the second phase of the sampling clock signal, a corresponding contribution from the first voltage $V_1[n]$ is subtracted therefrom, and a residue of the current sample of the test sequence $p[n]$, which is indicative of the deviation from the intended bridge ratio, remains superpositioned onto the current sample of the input signal.

As indicated in Fig. 13, the SAR ADC A*i* may comprise circuitry 220 configured to estimate the bridge ratio based on output samples the SAR ADC generated during said plurality of sampling clock periods. Alternatively, this circuitry 220 may be external to the SAR ADC A*i*. For instance, the TI ADC 50 (Fig. 3) may comprise such circuitry configured to estimate the bridge ratio that is common to all sub ADCs A1-A*M*. Alternatively, the bridge ratio estimation may be performed externally to the TI ADC 50, such as in the DSP circuit 15 (Fig. 2).

An example of how the bridge ratio estimation can be performed is provided in the following. If the two capacitors C_{T1} and C_{T2} have been designed to yield the same voltage gain to the comparator input the binary test sequence $p[n]$ is cancelled and not visible in the digital output data of the SAR ADC A*i*. On the other hand, if a residual of the binary test sequence $p[n]$ is present at the output, the bridge ratio must be corrected. The bridge ratio error can be estimated by means of correlating the SAR ADC A*i* output with the binary test sequence $p[n]$. The correlation output will be proportional to the bridge ratio mismatch. Below, the ADC output signal is $s_c[n] = s_{in}[n] + ws_{pn}[n](r_b - 1)$ where s_{in} is the output of

the SAR ADC Ai in the absence of the binary test sequence $p[n]$ and s_{pn} ($\in \{-1,1\}$) is a numerical equivalent of the binary test sequence $p[n]$ ($p[n]$ = '0' corresponds to $s_{pn}[n] = -1$, $p[n]$ = '1' corresponds to $s_{pn}[n] = 1$). The number r_b is a normalized bridge ratio quantity that ideally should be unity, in which case there will be no residue of $s_{pn}[n]$ in $s_c[n]$. The coefficient w is a weight of the binary test sequence $p[n]$, that indicates the nominal transfer of the sequence $s_{pn}[n]$ from the second terminal of the capacitor C_{T1} to the digital output of the SAR ADC Ai as well as from the second terminal of the capacitor C_{T2} to the digital output of the SAR ADC Ai. As an explanation of w, consider, for instance, a hypothetical situation where the sequence $s_{pn}[n]$ is input to the second terminal of C_{T1} in the form of the voltage $V_1[n] = V_{\text{ref}} s_{pn}[n]$, the second terminal of C_{T2} is kept grounded, and the input voltage v_{in} is held constantly 0. Furthermore, for this hypothetical situation, let us denote the output signal from the SAR ADC Ai $y[n]$ in order to not confuse it with the above defined output signal $s_c[n]$ when the SAR ADC Ai is in actual use. This digital output signal is $y[n] = w s_{pn}[n]$, or in other words $w = y[n]/s_{pn}[n]$.

The bridge ratio deviation $\Delta r_b = r_b - 1$ may be calculated by correlation as:

$$\Delta r_b = \frac{E[s_c s_{pn}]}{\sqrt{E[w^2 {s_{pn}}^2]}} = [E[{s_{pn}}^2] = 1] = E[s_c s_{pn}]/w$$

For estimation based on a finite set of N samples this bridge ratio deviation can be estimated as

$$\Delta \hat{r}_b = \frac{1}{wN} \sum_{n=1}^{N} s_c[n] s_{pn}[n]$$

The bridge capacitor C_b can be implemented as a variable capacitor configured to be controlled via a digital bridge ratio setting parameter r_s. For example, C_b can be implemented as a capacitor bank with a number of capacitors that can be selectively connected in parallel in response to r_s such that an increase in r_s leads to a decrease in C_b, and thus a larger bridge ratio, and a decrease in r_s leads to an increase C_b, and thus a smaller bridge ratio. Such digitally controllable variable capacitors are, per se, well known and not described in any further detail herein. For each estimation of the bridge ratio deviation $\Delta \hat{r}_b$, the bridge ratio setting r_s (not to be confused with the actual bridge ratio r_b) can be updated as $r_s = r_s/(1 + \alpha \Delta \hat{r}_b) \approx r_s(1 - \alpha \Delta \hat{r}_b)$ with $0 < \alpha \leq 1$. In other words, if the bridge ratio is found to be larger than the nominal value, i.e. $\Delta \hat{r}_b > 0$, the bridge ratio setting is reduced by a proportion of $|\Delta \hat{r}_b|$, and if the bridge ratio is found to be smaller than the nominal value, i.e. $\Delta \hat{r}_b < 0$, the

bridge ratio setting is increased by a proportion of $|\Delta\hat{r}_b|$. More generally, this may be viewed as an optimization problem based on a noisy metric ($\Delta\hat{r}_b$) and where the relation between the actual bridge ratio and the bridge ratio setting is not necessarily proportional or even linear. As such, there exist many established methods in the field of optimization and this is not further discussed herein.

C_{T2} may also be defined to have a value giving a weight different from that of C_{T1}. In this case, the binary test sequence $p[n]$ will not be fully cancelled, rather the correct bridge ratio will be obtained when there is a specific level of the binary test sequence $p[n]$ left at the digital output data of the SAR ADC Ai. Instead the cancellation of the binary test sequence $p[n]$ can be completed in digital domain. As the cancellation is not complete it will consume a small fraction of the full-scale range. One reason to give different weights to C_{T1} and C_{T2} is that C_{T1} has a smaller capacitance than C_{T2} and thus will have a larger capacitance variation in fabrication (mismatch). A larger C_{T1} will lead to a smaller relative capacitance variance and thus will improve accuracy.

The bridge ratio error may be calibrated in the analog domain, e.g. by adjusting the bridge capacitor C_b as described above. Alternatively, the bridge ratio error may be compensated for in the digital domain by digital post processing of the output signal from the SAR ADC Ai. For instance, let d_j denote the bits of the output $Y = \sum_j w_j d_j$ from the SAR ADC Ai with nominal weights w_j, for instance $w_j = 2^{j-1}$ for a binary-weighted architecture with a nominal bridge ratio of 2. A compensated output $\hat{Y}$ can be calculated as $\sum_j \hat{w}_j d_j$, where $\hat{w}_j$ are compensated bit weights computed in response to the estimated bridge ratio. For instance, the compensated bit weights can be computed as $\hat{w}_j = c_{\mathrm{SDAC}} w_j$ for bits d_j of the SDAC and as $\hat{w}_j = c_{\mathrm{MDAC}} w_j$ for bits d_j of the MDAC, where c_{SDAC} and c_{MDAC} are compensation factors derived from the estimated bridge ratio $\hat{r}_b = 1 + \Delta\hat{r}_b$ such that $\frac{c_{\mathrm{SDAC}}}{c_{\mathrm{MDAC}}} = \hat{r}_b$. In some embodiments, either c_{SDAC} or c_{MDAC} is set to 1.

The SAR ADC Ai may be comprised in a receiver circuit 40, either as a stand-alone ADC or as a sub ADC in another ADC, such as the TI ADC 50. Furthermore, the SAR ADC Ai, may be comprised in an electronic apparatus, either as a separate component or as a part of another circuit, such as the receiver circuit 40 or the TI ADC 50. The electronic apparatus can e.g. be a communication apparatus, such as the wireless communication device 1 or the base station 2 for a cellular communications system.

The disclosure above refers to specific embodiments. However, other embodiments than the above described are possible within the scope of the invention. The different features of

the embodiments may be combined in other combinations than those described. For instance, some embodiments described above provides gain-control functionality by means of the second capacitor network 180. Furthermore, some embodiment described above provides test-sequence injection functionality by means of test signal capacitors C_{T1} and C_{T2}. It should be noted that some embodiments can include only one of these functionalities, whereas some embodiments can include both of the functionalities in combination.

CLAIMS

1. A successive-approximation, SAR, analog-to-digital converter, ADC, (A*i*) comprising

an input for receiving an input voltage (V_{in});

a comparator (100);

a SAR state machine (110) connected to an output of the comparator (100);

a first switch network (120) configured to be controlled by the SAR state machine (110) and connected to the input of the SAR ADC (A*i*) and to reference voltage nodes; and

a first capacitor network (130); wherein

the first capacitor network (130) comprises

a first node (140) connected to an input of the comparator (100);

a second node (150);

a bridge capacitor (Cb) connected between the first node (140) and the second node (150);

a first set (160) of capacitors having a first and a second terminal, wherein the first terminal of each capacitor in the first set is connected to the first node (140) and the second terminal of each capacitor in the first set is connected to the first switch network (120); and

a second set (170) of capacitors having a first and a second terminal, wherein the first terminal of each capacitor in the second set is connected to the second node (150) and the second terminal of each capacitor in the first set is connected to the first switch network (120); wherein

the SAR state machine (110) is configured to control the first switch network (120) such that

- the input voltage (V_{in}) is sampled on one or more of the capacitors in the union of the first and the second set (160, 170) during a first phase of a sampling clock period; and

- SAR analog-to-digital, A/D, conversion is performed during a subsequent second phase of the sampling clock period; and

the SAR ADC (A*i*) further comprises a second capacitor network (180) connected to the second node (150) of the first capacitor network and configured to control a gain of the SAR ADC (A*i*).

2. The SAR ADC (A*i*) of claim 1, wherein the second capacitor network (180) comprises a capacitor ladder.

3. The SAR ADC (A*i*) of claim 2, wherein the capacitor ladder comprises a set of *k* connection points (p1-p3), in the following numbered from 1 to *k*, wherein

the 1:st connection point (p1) is connected to the second node (150) of the first capacitor network;

for each *j* = 1, ..., *k*–1, the capacitor ladder comprises a bridge capacitor connected between connection point *j* (p*j*) and connection point *j*+1 (p(*j*+1)); and

for each *j* = 1, ..., *k*, the capacitor ladder comprises a *j*:th capacitor having a first terminal connected to connection point *j* (p*j*).

4. The SAR ADC (A*i*) of claim 3, wherein the second capacitor network (180) comprises a capacitor connected between connection point *k* and a ground node.

5. The SAR ADC (A*i*) of claim 3 or 4, wherein the second capacitor network (180) comprises a capacitor connected between connection point 1 (p1) and a ground node.

6. The SAR ADC (A*i*) of any one of claims 3 to 5, comprising a second switch network (190), wherein

for each *j* = 1, ..., *k*, the second switch network comprises a *j*:th switch (g*j*) configured to

- connect a second terminal of the *j*:th capacitor of the second capacitor network to a ground node during the second phase of the sampling clock period; and

- selectively connect the second terminal of the *j*:th capacitor of the second capacitor network to the ground node or the input of the SAR ADC during the first phase of the sampling clock period to control the gain of the SAR ADC.

7. The SAR ADC (A*i*) of claim 6, wherein the SAR ADC comprises a third switch network (195) configured to connect the *k* connection points (p1-p3) of the second capacitor network (180) to the ground node during the first phase of the sampling clock period and to disconnect the *k* connection points (p1-p3) of second capacitor network (180) from the ground node during the second phase of the sampling clock period.

8. The SAR ADC (A*i*) of any preceding claim, comprising

a test sequence interface (200) configured to provide a binary test sequence (*p*[*n*]) during a plurality of consecutive sampling clock periods, wherein

each of the plurality of sampling clock periods has an associated sample of the binary test sequence ($p[n]$);

the first capacitor network (130) comprises a first test-signal capacitor (C_{T1}) having a first and a second terminal, wherein the first terminal is connected to the first node (140) of the first capacitor network (130); and

the first capacitor network (130) comprises a second test-signal capacitor (C_{T2}) having a first and a second terminal, wherein the first terminal is connected to the second node (150) of the first capacitor network (130); and wherein, for each of the plurality of consecutive sampling clock periods

the second terminal of the first test-signal capacitor (C_{T1}) is configured to be supplied with a first voltage ($V_1[n]$) representing the associated sample of the binary test sequence ($p[n]$); and

the second terminal of the second test-signal capacitor (C_{T2}) is configured to be supplied with a second voltage ($V_2[n]$) representing the associated sample of the binary test sequence ($p[n]$), such that a contribution of the first voltage ($V_1[n]$) at the input of the comparator (100) is counteracted.

9. The SAR ADC (A*i*) of claim 8, wherein the first voltage ($V_1[n]$) and the second voltage ($V_2[n]$) are selected from a positive reference voltage ($+V_{ref}$) and a negative reference voltage ($-V_{ref}$) in response to the binary test sequence ($p[n]$).

10. The SAR ADC (A*i*) of claim 8 or 9, wherein the second terminal of the first test-signal capacitor (C_{T1}) is configured to be supplied with the first voltage ($V_1[n]$) in one of the first phase and the second phase of the sampling clock period , the second terminal of the second test-signal capacitor (C_{T2}) is configured to be supplied with the second voltage ($V_2[n]$) in the same one of the first phase and the second phase of the sampling clock period, and the first voltage ($V_1[n]$) and the second voltage ($V_2[n]$) have opposite polarity.

11. The SAR ADC (A*i*) of claim 8 or 9, wherein the second terminal of the first test-signal capacitor (C_{T1}) is configured to be supplied with the first voltage ($V_1[n]$) in one of the first phase and the second phase of the sampling clock period , the second terminal of the second test-signal capacitor (C_{T2}) is configured to be supplied with the second voltage ($V_2[n]$) in the other one of the first phase and the second phase of the sampling clock period, and the first voltage ($V_1[n]$) and the second voltage ($V_2[n]$) have the same polarity.

12. The SAR ADC (A*i*) of any one of the claims 8-12, wherein the binary test sequence (*p*[*n*]) is a pseudo-random binary sequence.

13. The SAR ADC (A*i*) of any one of the claims 8-13, comprising circuitry (220) configured to estimate a bridge ratio based on output samples the SAR ADC generated during said plurality of sampling clock periods.

14. A time-interleaved ADC (50) comprising a plurality of sub ADCs (A1-A*M*), each implemented as the SAR ADC (A*j*) according to any preceding claim.

15. A receiver circuit (40) comprising the SAR ADC (A*i*) of any one of the claims 1-13 or the time-interleaved ADC (50) according to claim 14.

16. An electronic apparatus (1, 2) comprising the SAR ADC (A*i*) of any one of the claims 1 - 13, the time-interleaved ADC (50) of claim 14, or the receiver circuit (40) of claim 15.

17. The electronic apparatus (1, 2) of claim 16, wherein the electronic apparatus is a communication apparatus.

18. The electronic apparatus (1) of claim 17, wherein the communication apparatus (1) is a wireless communication device (1) for a cellular communications system.

19. The electronic apparatus (2) of claim 17, wherein the communication apparatus (2) is a base station (2) for a cellular communications system.

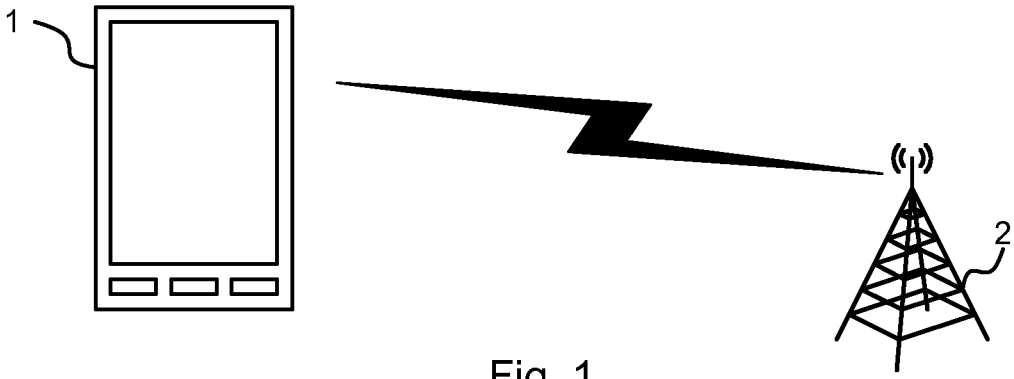

Fig. 1

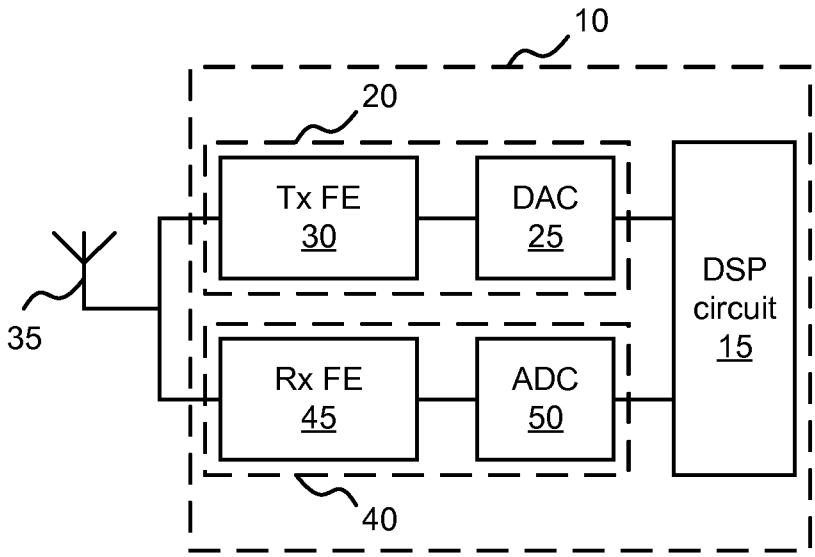

Fig. 2

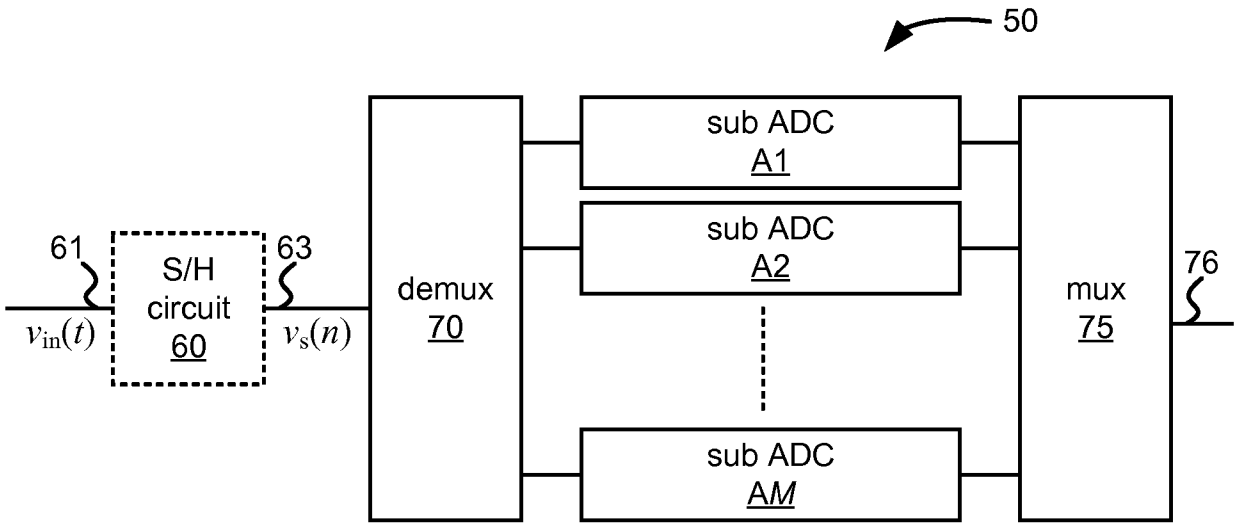
50
61
S/H
circuit
60
63
$v_{in}(t)$
$v_s(n)$
demux
70
sub ADC
A1
sub ADC
A2
sub ADC
AM
mux
75
76

Fig. 3

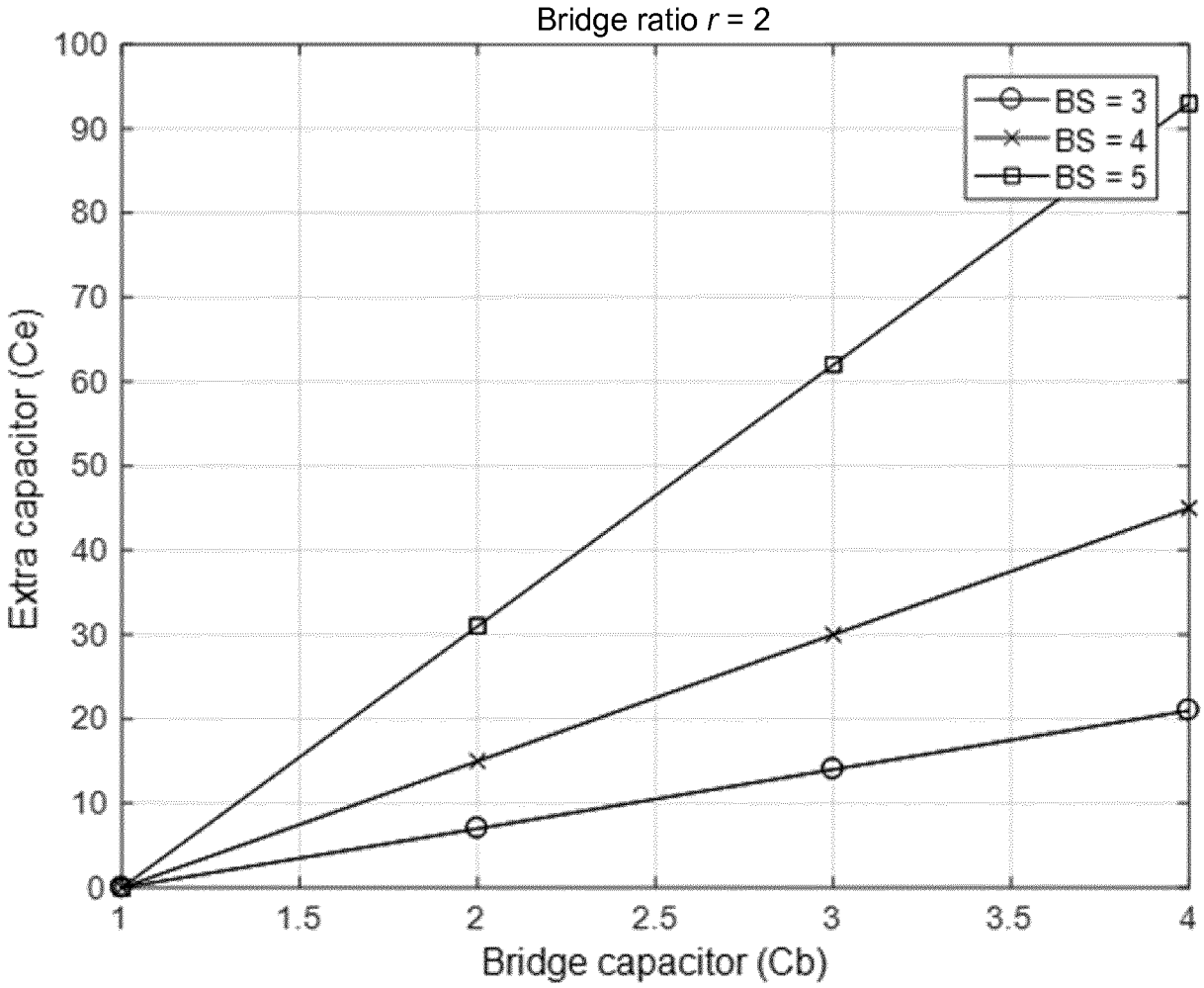
Bridge ratio r = 2
BS = 3
BS = 4
BS = 5
Extra capacitor (Ce)
Bridge capacitor (Cb)
0
10
20
30
40
50
60
70
80
90
100
1
1.5
2
2.5
3
3.5
4

Fig. 5

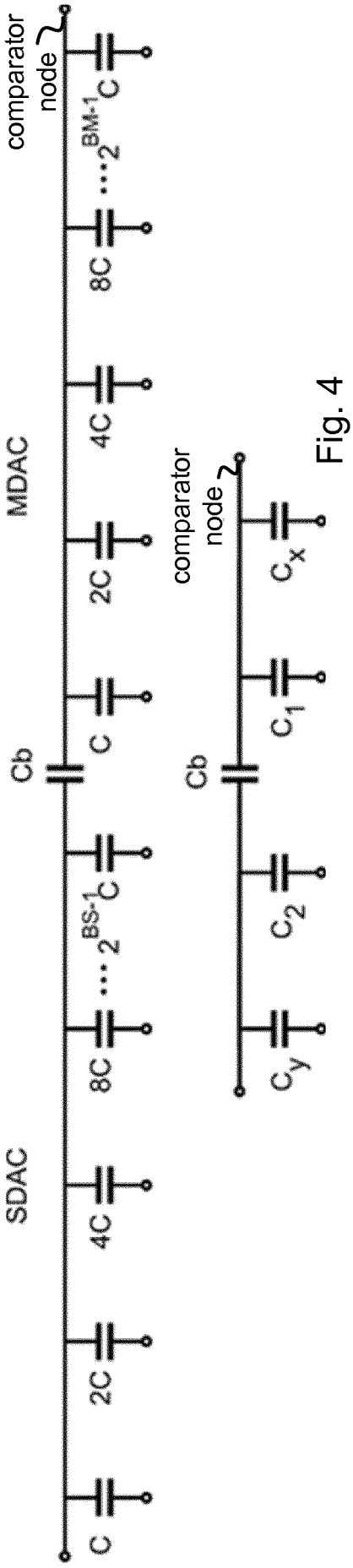
comparator node
MDAC
SDAC
Cb
C
2C
4C
8C
$2^{BS-1}C$
$2^{BM-1}C$

Fig. 4

comparator node
Cb
C_1
C_2
C_x
C_y

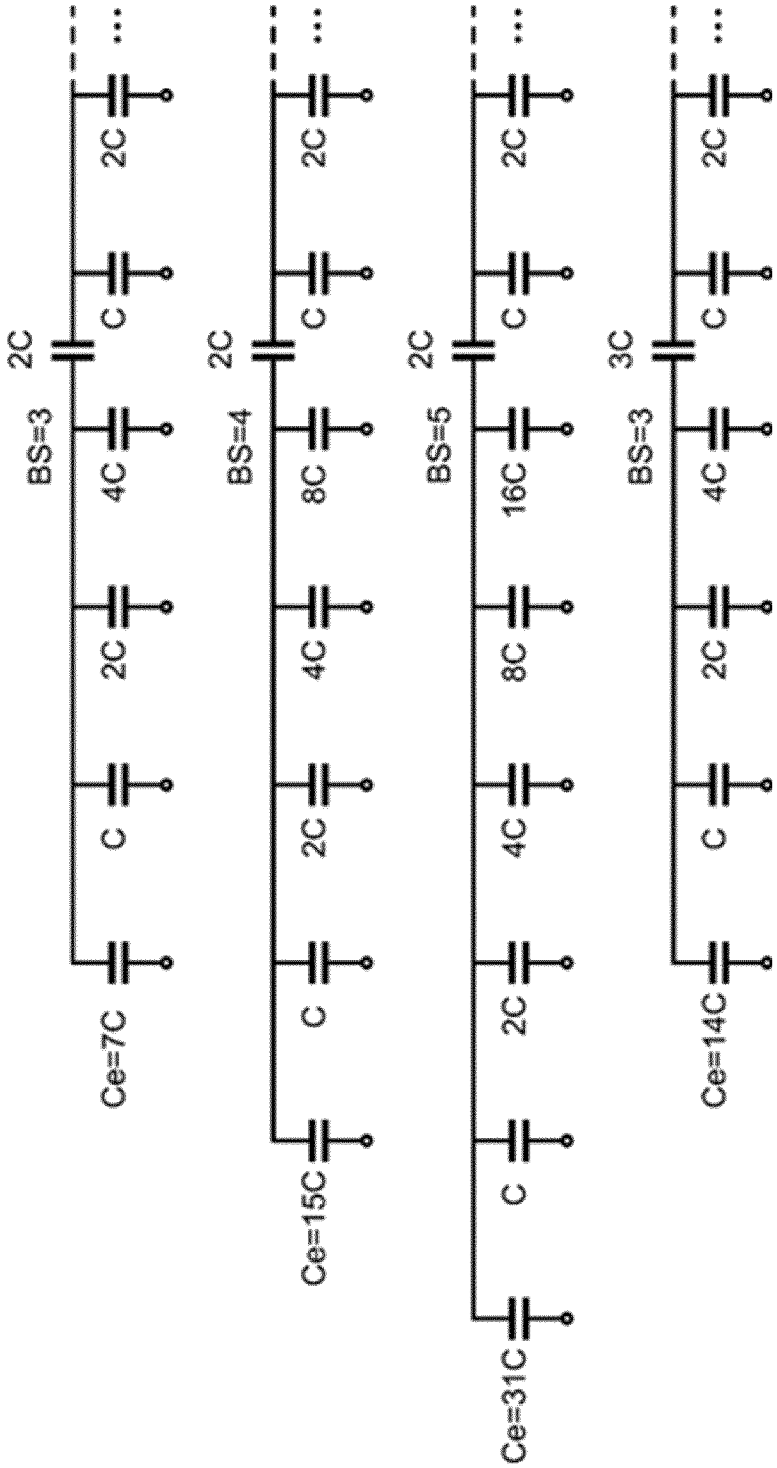
BS=3
BS=4
BS=5
BS=3
2C
3C
C
4C
8C
16C
Ce=7C
Ce=15C
Ce=31C
Ce=14C

Fig. 7

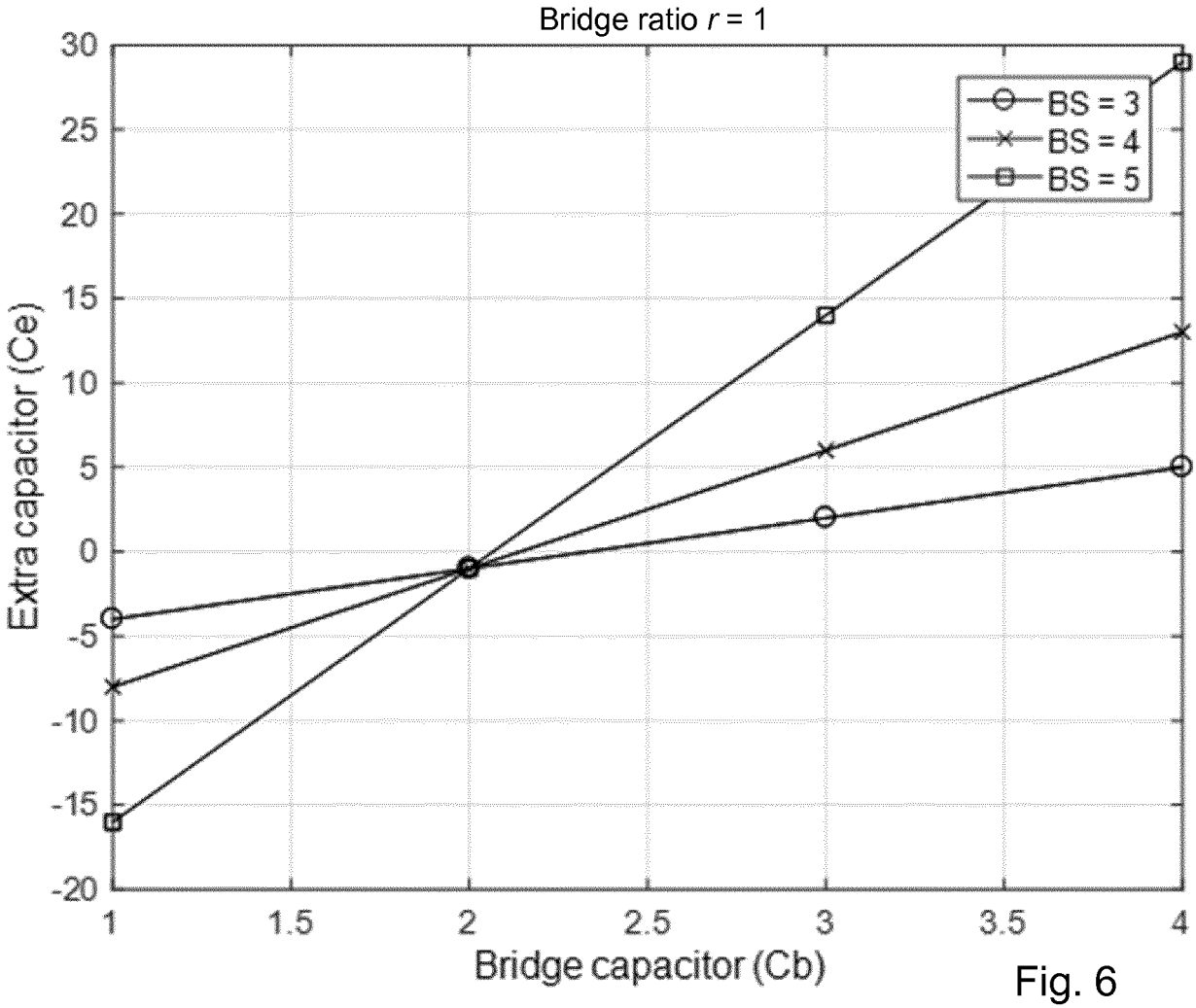
Bridge ratio r = 1
BS = 3
BS = 4
BS = 5
Extra capacitor (Ce)
Bridge capacitor (Cb)
30
25
20
15
10
5
0
-5
-10
-15
-20
1
1.5
2
2.5
3
3.5
4

Fig. 6

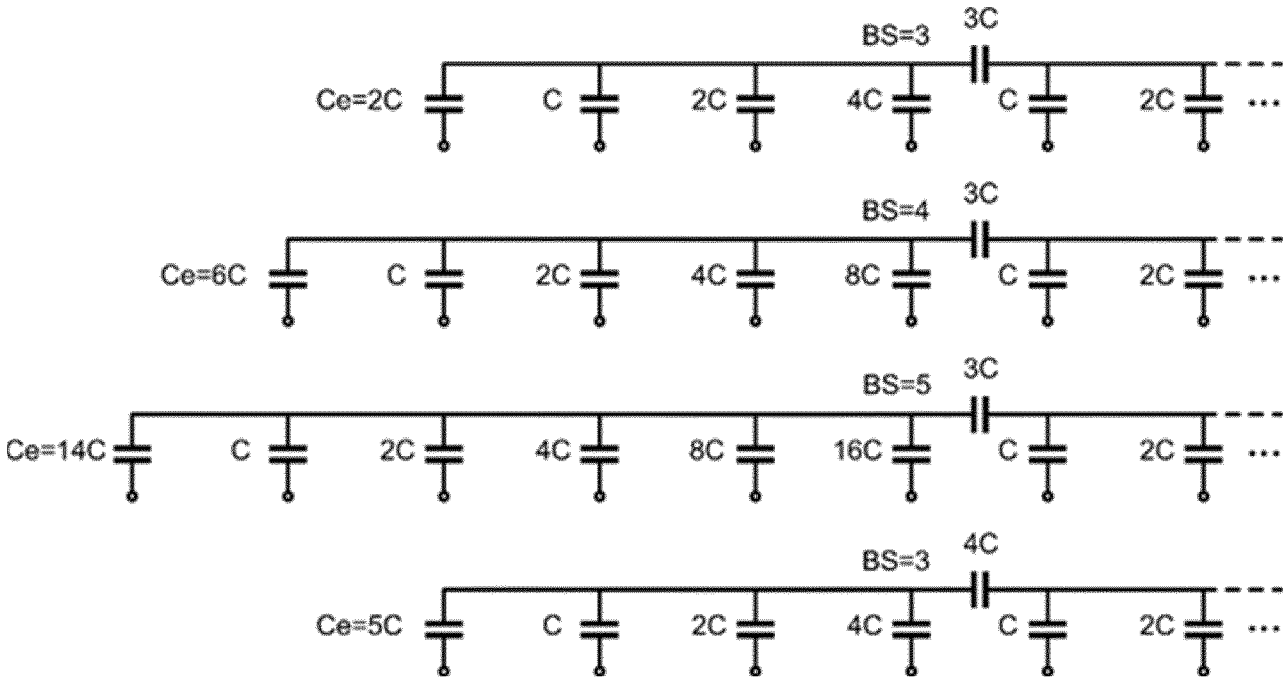
BS=3
3C
Ce=2C
C
2C
4C
C
2C
BS=4
3C
Ce=6C
C
2C
4C
8C
C
2C
BS=5
3C
Ce=14C
C
2C
4C
8C
16C
C
2C
BS=3
4C
Ce=5C
C
2C
4C
C
2C

Fig. 8

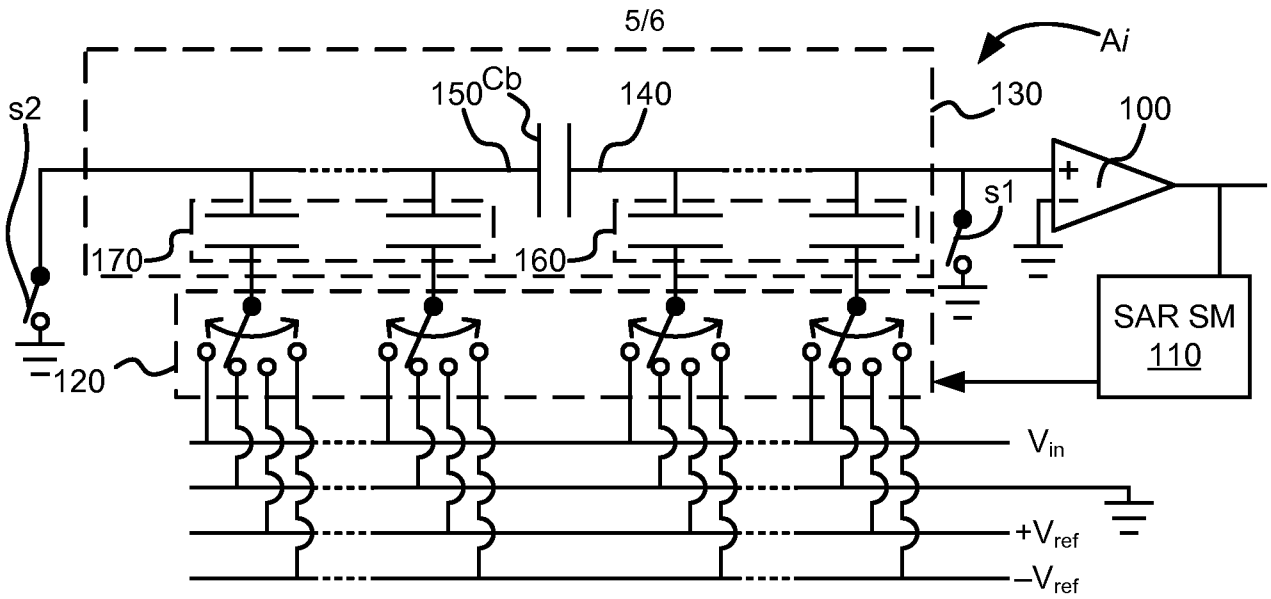

Fig. 9

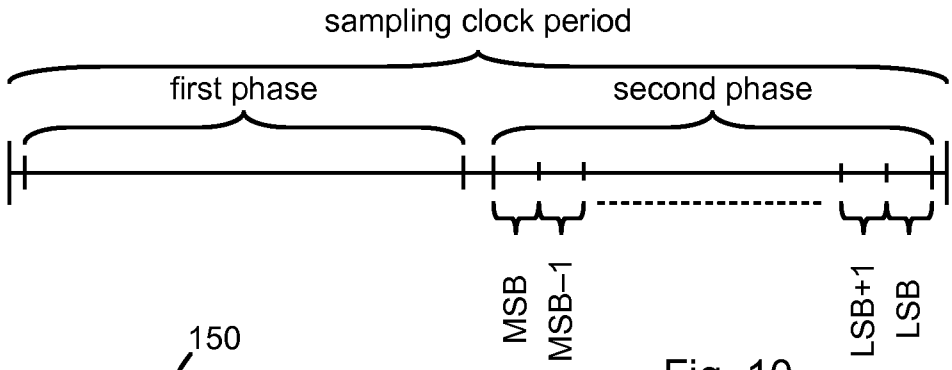

Fig. 10

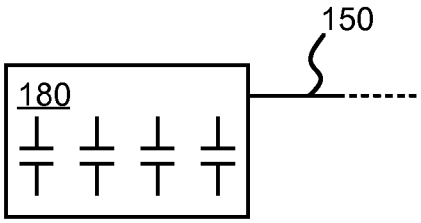

Fig. 11

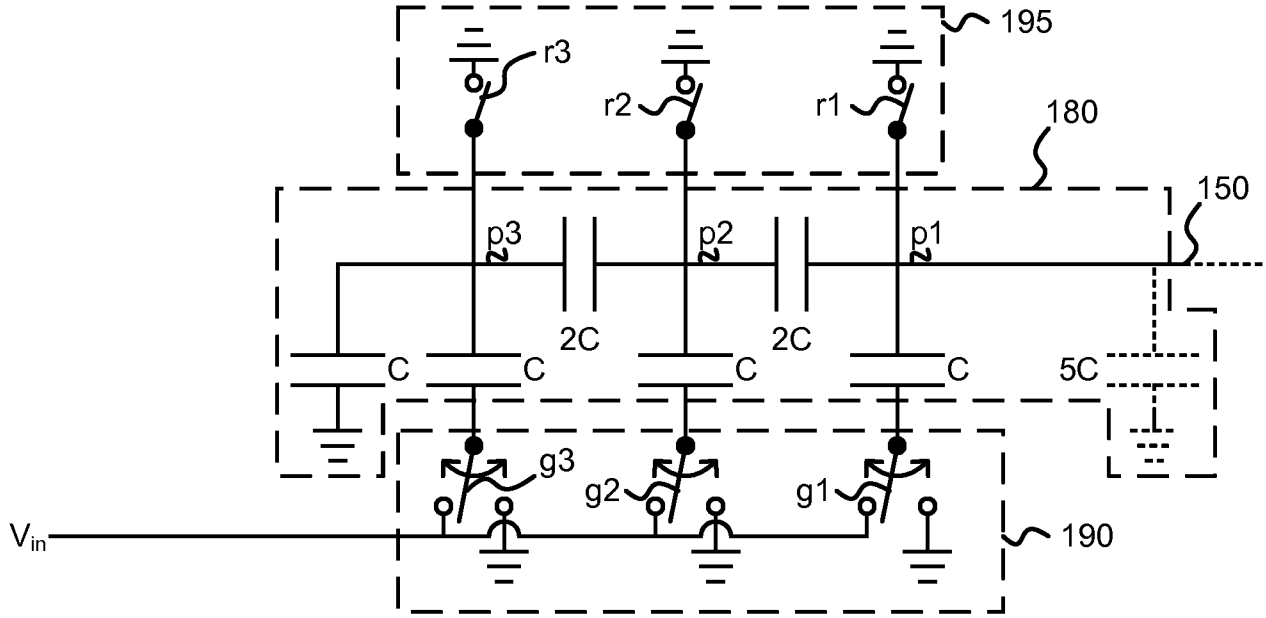

Fig. 12

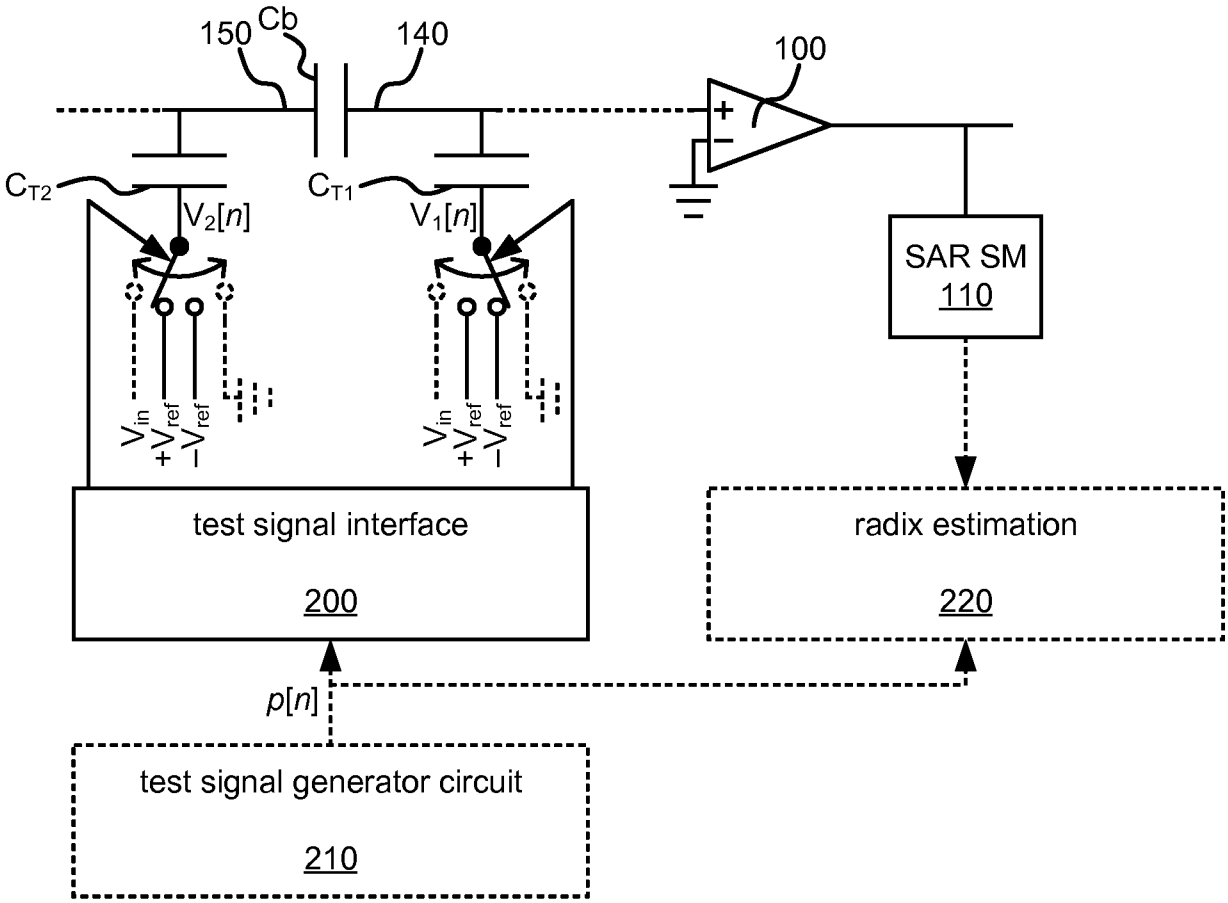
150
Cb
140
100
C_{T2}
C_{T1}
$V_2[n]$
$V_1[n]$
V_{in}
$+V_{ref}$
$-V_{ref}$
SAR SM
110
test signal interface
200
radix estimation
220
$p[n]$
test signal generator circuit
210

Fig. 13

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2018/056826

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03M1/18
ADD. H03M1/46 H03M1/78 H03M1/80

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data, COMPENDEX, INSPEC, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2012/001781 A1 (SCANLAN ANTHONY GERARD [IE]) 5 January 2012 (2012-01-05) abstract; figure 10	1-7, 14-19

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
7 February 2019	18/02/2019

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Galardi, Leonardo

5

Form PCT/ISA/210 (second sheet) (April 2005)

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	Frank Ohnhäuser: "ADCs Based on Successive Approximation" In: "Analog-Digital Converters for Industrial Applications Including an Introduction to Digital-Analog Converters", 1 January 2015 (2015-01-01), Springer Berlin Heidelberg, Berlin, Heidelberg, XP055524313, ISBN: 978-3-662-47020-6 pages 51-118, DOI: 10.1007/978-3-662-47020-6_2, sections 2.2.1; section 2.2.2.2;; figures 2.8-2.11 figure 2.18	1-7, 14-19

X	LING DU ET AL: "Self-calibrated SAR ADC based on split capacitor DAC without the use of fractional-value capacitor", IEEJ TRANSACTIONS ON ELECTRICAL AND ELECTRONIC ENGINEERING, vol. 8, no. 4, 1 July 2013 (2013-07-01), pages 408-414, XP055524396, US ISSN: 1931-4973, DOI: 10.1002/tee.21872 section 4; figure 1	1-7, 14-19

A	RUOYU XU ET AL: "Digitally Calibrated 768-kS/s 10-b Minimum-Size SAR ADC Array With Dithering", IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE SERVICE CENTER, PISCATAWAY, NJ, USA, vol. 47, no. 9, 1 September 2012 (2012-09-01), pages 2129-2140, XP011457915, ISSN: 0018-9200, DOI: 10.1109/JSSC.2012.2198350 section III.A; figures 3-6	8-19

A	ZHE LI ET AL: "Calibration for split capacitor DAC in SAR ADC", 2013 IEEE 10TH INTERNATIONAL CONFERENCE ON ASIC, IEEE, 28 October 2013 (2013-10-28), pages 1-4, XP032594058, ISSN: 2162-7541, DOI: 10.1109/ASICON.2013.6811966 ISBN: 978-1-4673-6415-7 [retrieved on 2014-05-07] abstract section 4; figure 3a	8-19

INTERNATIONAL SEARCH REPORT

International application No.
PCT/EP2018/056826

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☒ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-7(completely); 14-19(partially)

   SAR Analog-to-digital converter having an additional capacitor ladder for controlling the gain of the SAR during sampling.

   ---

2. claims: 8-13(completely); 14-19(partially)

   Sar Analog-to-digital converter equipped with a test sequence interface.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2018/056826

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2012001781 A1	05-01-2012	NONE	