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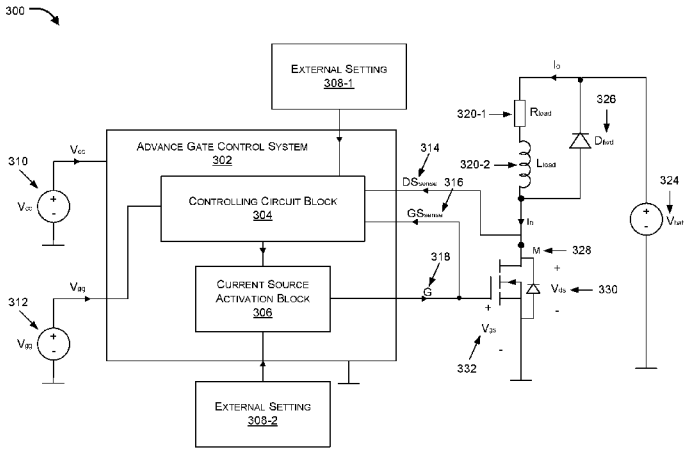


FIG. 3

(57) Abstract: The present disclosure provides a gate control system and a method thereof for controlling voltage and current transition during switching sequence. A circuit arrangement for turning-on and turning-off an inductive load (L_{load}) using the gate control system is also described. Systems and methods provide optimal trade-off between switching loss dissipation and electromagnetic emissions. The system includes a current source activation block (306) configured to include a plurality of current sources for selectively driving a power gate (G, 318), wherein each of the plurality of current sources can be activated for different time intervals, and a controlling circuit block (304) configured to receive a sensed drain-source voltage (DS_{sense}, 314), a sensed gate-source voltage (GS_{sense}, 316), and a voltage source signal (V_{gg}, 312) as a control signal, and determine borders between different time intervals for activation of each of the plurality of current sources in preconfigured sequential manner to drive the power gate, wherein amplitude of each of plurality of current sources can be different.

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GATE CONTROL SYSTEM AND METHOD THEREOF FOR PROVIDING CONTROL OVER VOLTAGE AND CURRENT TRANSITION

TECHNICAL FIELD

[0001] The present disclosure relates to the field of power electronics. More particularly, the present disclosure relates to gate control system and method thereof for providing control over voltage and current transition during power switching.

BACKGROUND

[0002] Background description includes information that may be useful in understanding the present invention. It is not an admission that any of the information provided herein is prior art or relevant to the presently claimed invention, or that any publication specifically or implicitly referenced is prior art.

[0003] Consumer electronic devices and electronic appliances of a modern home include some form of electronic or electromechanical control systems to control ON and OFF operation for the electronic devices or appliances. During transition state i.e. when the appliance, also referred interchangeably as load, needs to go from ON state to OFF state, or needs to go from OFF state to ON state, there is some transition delay and electromagnetic emissions. Though, in last few years, electronics have greatly improved the functionality and convenience of these devices/appliances, having electronic controls makes these devices susceptible to interference from ambient electromagnetic signals or electromagnetic emissions generated during transition state. Hence, there is a requirement for circuits that can minimize magnitude of electromagnetic interference generated, or radiated, by each device during the transition state. The device/appliance incorporating such electronic circuit can become a good neighbour to other electrical and electronic devices/appliances in its vicinity.

[0004] In power electronics, inductive loads, for example motor winding, switcher coil, etc., are common loads that are usually driven by a power MOSFET, IGBT or any other kind of a semiconductor switch that is designed in various topologies (half bridge, full bridge etc.). Inductive loads have special switching behaviour and introduce several engineering trade-offs that have to be addressed during power circuit design in order to develop an efficient and reliable application. One of the most significant trade-off that needs to be considered while designing semiconductor switches is trade-off between switching loss dissipation and generation of electromagnetic emissions during transition state between ON and OFF.

[0005] Most of the known semiconductor switches of present day consider trade-off that is required to design electronic circuit for safe operation of inductive load. During transition state, a switching sequence takes places to avoid high emission or to minimize switching loss. A switching sequence in most of the known systems includes current transition that is carried out at full voltage on transistor, and similarly, voltage transition that is carried out at full current that results in high energy dissipation on the transistor. The energy dissipation is also referred as switching losses. Setting fast transitions of current and voltage indeed reduces switching losses, but on the other hand, results in steep current and voltage slopes that cause electromagnetic emissions. An optimal point of the trade-off is therefore sought by adapting current and voltage slopes during transition state, i.e. turn-on and turn-off switching sequence. The goal is to find the steepest slopes possible that don't cause excessive electromagnetic emissions in order to meet strict electromagnetic compatibility (EMC) standards.

[0006] To overcome some the problems highlighted as above, gate control systems have been proposed in the past. The typical gate control system includes power transistors with isolated gates, for example MOSFETs and IGBTs, that can be driven via series gate resistor. An optimal point of the above-mentioned trade-off is sought by adapting or changing resistance of the serial gate resistors. However, using these arrangements and methods optimal point is hardly achievable, as changing the resistance value has, in turn, a bearing on transition times of both, current and voltage. In such cases, it is necessary to, say, slow down current transition to meet EMC standards, by changing gate resistance, at the same time voltage transition also slows down, resulting in generation of excessive switching losses.

[0007] Therefore there is a requirement in the art for a gate control system and method thereof that can provide more control over voltage and current transitions, providing optimal trade-off between switching loss dissipation and electromagnetic emissions so as to minimize both of them.

[0008] In some embodiments, numerical parameters set forth in the written description are approximations that can vary depending upon the desired properties sought to be obtained by a particular embodiment. In some embodiments, the numerical parameters should be construed in light of the number of reported significant digits and by applying ordinary rounding techniques. Notwithstanding that, the numerical ranges and parameters setting forth the broad scope of some embodiments of the invention are approximations, the numerical values set forth in the specific examples are reported as precisely as practicable. The numerical values presented in some embodiments of the invention may contain certain errors

necessarily resulting from the standard deviation found in their respective testing measurements.

[0009] As used in the description herein and throughout the claims that follow, the meaning of "a," "an," and "the" includes plural reference unless the context clearly dictates otherwise. Also, as used in the description herein, the meaning of "in" includes "in" and "on" unless the context clearly dictates otherwise.

[0010] The recitation of ranges of values herein is merely intended to serve as a shorthand method of referring individually to each separate value falling within the range. Unless otherwise indicated herein, each individual value is incorporated into the specification as if it were individually recited herein. All methods described herein can be performed in any suitable order unless otherwise indicated herein or otherwise clearly contradicted by context. The use of any and all examples, or exemplary language (e.g. "such as") provided with respect to certain embodiments herein is intended merely to better illuminate the invention and does not pose a limitation on the scope of the invention otherwise claimed. No language in the specification should be construed as indicating any non-claimed element essential to the practice of the invention.

[0011] Groupings of alternative elements or embodiments of the invention disclosed herein are not to be construed as limitations. Each group member can be referred to and claimed individually or in any combination with other members of the group or other elements found herein. One or more members of a group can be included in, or deleted from, a group for reasons of convenience and/or patentability. When any such inclusion or deletion occurs, the specification is herein deemed to contain the group as modified thus fulfilling the written description of all groups used in the appended claims.

SUMMARY

[0012] Embodiments of the present disclosure provide a gate control system and method thereof for controlling voltage and current transition during switching sequence. Systems and methods of present disclosure provide optimal trade-off between switching loss dissipation and electromagnetic emissions. Systems and methods of present disclosure provide an advanced gate control that can minimize switching loss and electromagnetic emission. An embodiment of present disclosure provides a semiconductor switch that can be configured to use the method of present disclosure to drive a power gate to provide efficient switching.

[0013] An embodiment of the present disclosure provides a gate control system that can drive a power gate to perform switching operation, wherein the system can include a current

source activation block that can be configured to include plurality of current sources for selectively driving the gate, wherein each of the plurality of current sources can be activated for different time intervals, and a controlling circuit block that can be configured to receive a sense voltage between drain and source DSsense, a voltage between gate and source GSsense, a voltage source Vgg signal, and determine borders between different time intervals for activation of each of the plurality of current sources in preconfigured sequential manner.

[0014] In an exemplary embodiment, the gate control system can include a controlling circuit block that can be configured to receive a sense voltage between drain and source DSsense, a voltage between gate and source GSsense, and a voltage source Vgg signal, to process the received DSsense, GSseense and Vgg for performing voltage division, subsequently filtering DSsense and GSsense, to provide conditioned 'DSsense2', 'DSsense', GSsense' and Vgg' that can be used to determine interval borders between different time intervals at which each of the plurality of current sources, one at a time, can respectively be activated in a preconfigured sequential manner, and to generate ON/OFF control signal for activating each of the plurality of current sources, one at a time, and a current source activation block configured to receive the ON/OFF control signal and activate the each of the plurality of current sources for respective time intervals in the preconfigured sequential manner based on the ON/OFF control signal for supplying current to the power gate during a switching operation.

[0015] In an exemplary embodiment, the current source activation block can be configured to include a plurality of current sources that can be activated sequentially, one at a time, based on the ON/OFF signal for the determined time intervals. In an exemplary embodiment, amplitude of each of the plurality of current sources can be configured manually by the user or can be configured automatically using an aspect of the present disclosure. The amplitude of each of the plurality of current sources can be configured through a current source amplitude manager. Based on ON/OFF signal received from the gate control system, current source selected from the plurality of current can be activated at borders between the time intervals.

[0016] In an exemplary embodiment, the controlling circuit block can be configured to include a signal processing block, intervals border detection block and logic circuitry for controlling current sources. In an exemplary embodiment, the signal processing block can be configured to include circuitry to receive sense voltage between drain and source DSsense, voltage between gate and source GSsense, and a voltage source Vgg signal, and include voltage dividers to divide the received DSsense, Gssense, and Vgg to meet voltage range of

the controlling circuit block and filters to subsequently filter the DSsense and GSsense eliminate high-frequency oscillations that may occur during power transistor switching. In an exemplary embodiment, division ratio to be used by the voltage dividers, and filter properties to be used by the filters can be configured by the user to match the requirement of specific system where the gate control system is about to be implemented. The signal processing unit can include a voltage supply Vcc, a resistor R and diode D connected in series to avoid loss of resolution that could have occurred in system due to voltage divider and filters. The signal processing unit can provide conditioned 'DSsense2', 'DSsense', GSsense' and Vgg', which can be used by the interval borders detection block for determining the borders between the different time intervals.

[0017] In an exemplary embodiment, the interval borders detection block can be configured to receive the DSsense2', DSsense', GSsense' and Vgg' and generate signal S2, signal S3, and signal S4, which in combination with Vgg' can be used to determine the borders between the different time intervals. Borders, also referred as points, for example N2, N3 and N4 for turn-on sequence and F4, F3, and F2 for turn-off sequence can be determined based on signal S2, S3 and S4 respectively.

[0018] Further, in an exemplary embodiment, the logic circuitry for controlling current sources can be configured to receive Vgg', S2, S3 and S4 and determine the ON/OFF control signals that can be sent to the current sources activation block.

[0019] In an exemplary implementation, signal S2, or point N2 or point F2 can be indicative of a situation when voltage between the gate and source Vgs 332 crosses a predefined threshold Vth, signal S3, or point N3can be indicative of a situation during turn-on sequence when voltage between drain and source Vds 330 starts falling or signal S3 or point F3 can be indicative of situation during turn-off sequence when the Vds 330 reaches a desired value, and signal S4, or point N4 can be indicative of a situation during turn-on sequence when the Vds 330 reaches a desired value or signal S4 or point F4 can be indicative of a situation during turn-off sequence when the Vds 330 starts rising, wherein for the turn-on sequence, the desired value is voltage Vbat 324 that is required to run the load 320, and for the turn-off sequence the desired value is near to zero.

[0020] In an exemplary embodiment, a turn-on switching sequence can start at time T0 at which a first current source of the plurality of current sources can be active for time interval T1. On receiving signal S2, which is indicative of point N2, a second current source of the plurality of current sources can be activated for time interval T2 and the first current source can be turned-off. Further, on receiving signal S3, which is indicative of point N3, a third

current source of the plurality of current sources can be activated for time interval T3, and the second current source can be turned-off. Further, on receiving signal S4, which is indicative of point N4, a fourth current source of the plurality of current sources can be activated.

[0021] In an exemplary embodiment, a turn-off switching sequence can start at time T0 at which the fourth current source of the plurality of current sources can be active for time interval T4'. On receiving signal S4, which is indicative of point F4, the third current source of the plurality of current sources can be activated for time interval T3' and the fourth current source can be turned-off. Further, on receiving signal S3, which is indicative of point F3, the second current source of the plurality of current sources can be activated for time interval T2', and the third current source can be turned-off. Further, on receiving signal S2, which is indicative of point F2 the first current source of the plurality of current sources can be activated.

[0022] Various objects, features, aspects and advantages of the inventive subject matter will become more apparent from the following detailed description of preferred embodiments, along with the accompanying drawing figures in which like numerals represent like components.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] In the Figures, similar components and/or features may have the same reference label. Further, various components of the same type may be distinguished by following the reference label with a second label that distinguishes among the similar components. If only the first reference label is used in the specification, the description is applicable to any one of the similar components having the same first reference label irrespective of the second reference label.

[0024] FIG. 1 illustrates an exemplary circuit for inductive load switching that can be used in accordance with an embodiment of present disclosure.

[0025] FIG. 2 illustrates exemplary graphs of inductive load switching circuit in accordance with an embodiment of the present disclosure.

[0026] FIG. 3 illustrates an exemplary block diagram of a gate control system for providing efficient inductive load switching in accordance with an embodiment of the present disclosure.

[0027] FIG. 4 illustrates an exemplary circuit that can be used by the current source block 306 in accordance with an embodiment of the present disclosure.

[0028] FIG. 5 illustrates exemplary graphs observed during switching activity of an inductive load switching using gate control system in accordance with an embodiment of the present disclosure.

[0029] FIG. 6 illustrates exemplary functional blocks of a controlling circuit block 304 in accordance with an embodiment of the present disclosure.

[0030] FIG. 7A illustrates exemplary graph highlighting interval borders associated with events in accordance with an embodiment of the present disclosure.

[0031] FIG. 7B illustrates exemplary points that are marked in graphs as shown in FIG. 7A.

[0032] FIG. 8 illustrates functional blocks of a signal processing block that can used to determine the drain source voltage in accordance with an embodiment of present disclosure.

[0033] FIG. 9 illustrates an exemplary circuit that can be used for interval borders detection in accordance with an embodiment of the present disclosure.

[0034] FIG. 10 illustrates exemplary border intervals determined in accordance with an embodiment of the present disclosure.

[0035] FIG. 11 illustrates an exemplary logic circuit for controlling current sources in accordance with an embodiment of the present disclosure.

[0036] FIG. 12 illustrates an exemplary flow of a method for driving a power gate to perform switching operation in accordance with an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0037] The following is a detailed description of embodiments of the disclosure depicted in the accompanying drawings. The embodiments are in such detail as to clearly communicate the disclosure. However, the amount of detail offered is not intended to limit the anticipated variations of embodiments; on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the present disclosure as defined by the appended claims.

[0038] Each of the appended claims defines a separate invention, which for infringement purposes is recognized as including equivalents to the various elements or limitations specified in the claims. Depending on the context, all references below to the "invention" may in some cases refer to certain specific embodiments only. In other cases it will be recognized that references to the "invention" will refer to subject matter recited in one or more, but not necessarily all, of the claims.

[0039] Various terms as used herein are shown below. To the extent a term used in a claim is not defined below, it should be given the broadest definition persons in the pertinent art have given that term as reflected in printed publications and issued patents at the time of filing.

[0040] Embodiment of the present disclosure provides a gate control system and method thereof for controlling voltage and current transition during switching sequence. The systems and methods of present disclosure provide optimal trade-off between switching loss dissipation and electromagnetic emissions. The system and methods of present disclosure provides an advanced gate control system that can minimize the switching loss and the electromagnetic emission. An embodiment of present disclosure provides a semiconductor switch that can be configured to use the method of present disclosure to drive a power gate to provide efficient switching.

[0041] An embodiment of the present disclosure provides a gate control system that can drive a power gate to perform switching operation, the system includes a current source activation block configured to include plurality of current sources for selectively driving the gate, wherein each of the plurality of current sources can be activated for different time intervals, and a controlling circuit block configured to receive a sense voltage between drain and source DSsense, a voltage between gate and source GSsense, a voltage source Vgg signal and determine borders between different time intervals for activation of each of the plurality of current sources in preconfigured sequential manner.

[0042] In an exemplary embodiment, the gate control system can include a controlling circuit block configured to receive a sense voltage between drain and source DSsense, a voltage between gate and source GSsense, and a voltage source Vgg signal, to process the received DSsense , GSseense and Vgg for performing voltage division, subsequently filtering DSsense and GSsense, to provide conditioned 'DSsense2', 'DSsense', GSsense' and Vgg' that can be used to determine interval borders between different time intervals at which each of the plurality of current sources, one at a time, can respectively be activated in a preconfigured sequential manner, and to generate ON/OFF control signal for activating the each of the plurality of current sources, and a current source activation block configured to receive the ON/OFF control signal and activate the each of the plurality of current sources for respective time intervals in the preconfigured sequential manner based on the ON/OFF control signal for supplying current to the power gate during a switching operation.

[0043] In an exemplary embodiment, the current source activation block can be configured to include plurality of current sources, which can be activated sequentially, one at

a time, based on the ON/OFF signal for the determined time intervals. In an exemplary embodiment, amplitude of each of the plurality of current sources can be configured manually by the user or can be configured automatically using an aspect of the present disclosure. The amplitude of each of the plurality of current sources can be configured through a current source amplitude manager. Based on ON/OFF signal received from the gate control system, current source selected from the plurality of current can be activated at borders between the time intervals In an exemplary embodiment, the controlling circuit block can be configured to include a signal processing block, intervals border detection block and logic circuitry for controlling current sources. In an exemplary embodiment, the signal processing block can be configured to include circuitry to receive the sense voltage between drain and source DSsense, the voltage between gate and source GSsense, and a voltage source Vgg signal, and include voltage dividers to divide the received DSsense, GSsense and Vgg to meet voltage range of the controlling circuit block and filters to subsequently filter the DSsense and GSsense eliminate high-frequency oscillations that may occur during power transistor switching. In an exemplary embodiment, division ratio to be used by the voltage dividers, and filter properties to be used by the filters can be configured by the user to match the requirement of specific system where the gate control system is about to be implemented. The signal processing unit can include a voltage supply Vcc, a resistor R and diode D connected in series to avoid loss of resolution that could have occurred in system due to voltage divider and filters. The signal processing unit can provide conditioned DSsense2', DSsense', GSsense' and Vgg' which can be used by the interval borders detection block for determining the borders between the different time intervals.

[0044] In an exemplary embodiment, the interval borders detection block can be configured to receive the DSsense2', DSsense', GSsense' and Vgg' and generate signal S2, signal S3, and signal S4, which in combination with Vgg' can be used to determine the borders between the different time intervals. Borders, also referred as points, for example N2, N3 and N4 for turn-on sequence and F4, F3, and F2 for turn-off sequence can be determined based on signal S2, S3 and S4 respectively.

[0045] Further in an exemplary embodiment, the logic circuitry for controlling current sources can be configured to receive Vgg', S2, S3 and S4 and determine the ON/OFF control signals that can be sent to the current sources activation block.

[0046] In an exemplary implementation, signal S2, or point N2 or point F2 can be indicative of a situation when voltage between the gate and source Vgs 332 crosses a predefined threshold Vth, signal S3, or point N3can be indicative of a situation during turn-on

sequence when voltage between drain and source Vds 330 starts falling or signal S3 or point F3 can be indicative of situation during turn-off sequence when the Vds 330 reaches a desired value, and signal S4, or point N4 can be indicative of a situation during turn-on sequence when the Vds 330 reaches a desired value or signal S4 or point F4 can be indicative of a situation during turn-off sequence when the Vds 330 starts rising , wherein for the turn-on sequence the desired value is voltage Vbat 324 that is required to run the load 320, and for the turn-off sequence the desired value is near to zero.

[0047] In an exemplary embodiment, a turn-on switching sequence can start at time t0 at which a first current source of the plurality of current sources can be active for time interval T1. On receiving signal S2, which is indicative of point N2, a second current source of the plurality of current sources can be activated for time interval T2 and the first current source can be turned-off. Further, on receiving signal S3, which is indicative of point N3, a third current source of the plurality of current sources can be activated for time interval T3, and the second current source can be turned-off. Further, on receiving signal S4, which is indicative of point N4, a fourth current source of the plurality of current sources can be activated.

[0048] In an exemplary embodiment, a turn-off switching sequence can start at time t0 at which the fourth current source of the plurality of current sources can be active for time interval T4'. On receiving signal S4, which is indicative of point F4, the third current source of the plurality of current sources can be activated for time interval T3' and the fourth current source can be turned-off. Further, on receiving signal S3, which is indicative of point F3, the second current source of the plurality of current sources can be activated for time interval T2', and the third current source can be turned-off. Further, on receiving signal S2, which is indicative of point F2 the first current source of the plurality of current sources can be activated.

[0049] FIG. 1 illustrates exemplary circuit for inductive load switching that can be used in accordance with an embodiment of present disclosure. The inductive load switching circuit 100 can include a power gate, for example a MOSFET M 102, inductive load(s) such as Rload 104-1and Lload 104-2, collectively and interchangeably referred as inductive load as Rload 104-1 and Lload 104-2, collectively and interchangeably referred as load104, freewheeling diode Dfwd 106, and a driving circuit for driving the power gate. In an exemplary embodiment, the driving circuit can include a voltage source Vgg 108 and a resistor Rg 110, intrinsic capacitors such as Cgs 114 and Cgd 112 and supply voltage Vbat 116 connected in the manner as shown in FIG. 1. In an exemplary embodiment, the inductive

load switching circuit can be operated to turn-on or turn-off power supply to the inductive load 104 using turn-on switching sequence or turn-off switching sequence respectively.

[0050] In an exemplary embodiment, turn-on and turn-off switching sequences can include different time intervals at which resistance of the resistor Rg 110 can be varied. For example, turn-on switching sequence interval can have four intervals of different durations, referred hereinafter as T1, T2, T3 and T4, and turn-off switching sequence can similarly have four intervals of different durations referred hereinafter T1', T2', T3' and T4'. In an exemplary embodiment, the turn-on switching sequence interval and turn-off switching sequencing interval can be symmetrical.

[0051] As the turn-off switching sequence is symmetric to the turn-on switching sequence, and as the switching loss and the electromagnetic emission is same in both these situations, different embodiments of the present disclosure will be explained with reference to turn-on switching sequence. As one may appreciate, turn-off switching sequence can similarly be performed. The switching sequence for the turn-on can be as below. Before time T0, the circuit 100 can already have been excited and Lload 104-2 can be driving a current I0 through the diode Dfwd 106. As the diode Dfwd 106 is forwardly biased, voltage between drain and source, referred hereinafter as Vds 118 can be equal to Vbat 116, i.e. vds=~Vbat before T0. In the interval T1 at t=T0, power source Vgg 108 turns on and starts charging input capacitances Cgs 114 and Cgd 112 via resistor Rg 110. Interval T1 lasts till voltage between ground and source referred hereafter Vgs 120 reaches a threshold voltage Vth. As output conditions at the MOSFET M 102 remains same, the interval T1 is known as turn-on delay. There can be no switching losses on MOSFET M 102 during the interval T1. As soon as the Vgs 120 reaches a threshold voltage Vth, the interval T1 ends and interval T2 starts. At the beginning of interval T2, as the Vgs may have reached Vth, the MOSFET M 102 starts conducting and taking over load current I0 from the Dfwd 106.When total current starts flowing through MOSFET M 102, the diode Dfwd 106 can be reverse-biased and so reverse-recovery process can be carried out on the diode Dfwd 106, manifesting itself as drain current overshot. Increasing drain current id and Vds =~ Vbat can cause notable power dissipation on MOSFET M 102 that can cause switching losses. At the end of interval T2, switching losses can reach their maximum value.

[0052] Once the diode Dfwd 106 is reverse-biased and as the Cgd 112 may have started discharging, Vds 118 can start dropping during interval T3.Soon after start of interval T3, the Vgs can reach Vmu, i.e. Vgs = Vmu, which is also referred as Miller plateau. Discharging process for Cgs 114 can continue at constant vgs=Vmu (Miller plateau) for full duration of

interval T3.During interval T3, the Vds 118 starts dropping at full drain current (id=I0) that can produce high power dissipation on MOSFET M 102 and can cause second part of switching losses. When the capacitor Cgd 112 is fully discharged, interval T3 ends and interval T4 start. During interval T4, Vgs 120 starts rising again to the final value and achieve Vgs equal to Vgg. Turn-on switching sequence is completed at a point when Vgs 120 reaches Vgg (and switching losses are transformed into conductive ones).Similar switching sequence except the reverse recovery phenomena can be performed for turn-off switching sequence.

[0053] FIG. 2 illustrates exemplary graphs of inductive load switching circuit 100 in accordance with an embodiment of the present disclosure. FIG. 2 illustrates different graphs of voltage and current at different point of circuit 100 during turn-on switching sequence and turn-off switching sequence. First half of each graph shows turn-on switching sequence and second half shows turn-off switching sequence. Graph (a) illustrates waveform 210for voltage at input power source Vgg and waveform 202 for voltage between gate and source Vgs during entire turn-on switching sequence and turn-off switching sequence. Graph(b) illustrates waveform204 for current Id during entire turn-on switching sequence and turn-off switching sequence. Graph(c) illustrates waveform 206 for voltage between drain and source Vds during entire turn-on switching sequence and turn-off switching sequence. Graph(d) illustrates waveform 208 that represent switching loss during turn-on switching and switching loss turn-off switching. As illustrated in waveform 202, during interval T1 at t=T0, power source Vgg 108 turns on and starts charging input capacitances Cgs114 and Cgd112 via resistor Rg 110 and hence Vgs 120 starts increasing. Interval T1 lasts till Vgs120reaches a threshold voltage Vth. As soon as the Vgs 120 reaches a threshold voltage Vth, the interval T1 ends and interval T2 starts. At the beginning of interval T2, as the Vgs 120 has reached Vth,MOSFET M102 starts conducting and taking over load current I0 from the Dfwd.

[0054] As shown in waveform 206, Vds 118 during interval T1 and T2 remains equal to Vbat and the Vds 118can start dropping during interval T3 as shown in steep slope on waveform 206. When total current starts flowing through MOSFET M 102, the diode Dfwd106 can be reverse-biased and so reverse-recovery process can be carried out on the diode Dfwd 106, manifesting itself as drain current overshot. Increasing drain current id and Vds =~ Vbat may cause notable power dissipation on MOSFET M 102 that can cause switching losses as shown in waveform208. At the end of interval T2, switching losses can reach their maximum value.

[0055] Once the diode Dfwd 106 is reverse-biased and as the Cgd 112may have started discharging, Vds118 can start dropping duringinterval T3 as shown in waveform 206.Soon

after start of interval T3, Vgs120 can reach Vmu, i.e. Vgs = Vmu as shown in waveform 202. Discharging process for Cgs 112 can continue at constant vgs=Vmu (Miller plateau) for full duration of interval T3.During interval T3, Vds118 starts dropping at full drain current (id=I0) that canproduce high power dissipation on MOSFET M 102 and cancause second part of switching losses. When the capacitor Cgd 112is fully discharged, interval T3 ends and interval T4 starts. During interval T4, Vgs 120starts rising again towards the final value and achieve Vgs 114 equal to Vgg108 as shown by intersection of waveform 210 with waveform 202. Turn-on switching sequence is completed at a point when Vgs reaches Vgg.Similar switching sequence except the reverse recovery phenomena can be performed for turn-off switching sequence.

[0056] As shown in waveform204, current I0 during the interval T1 remains near to zero, starts increasing suddenly during interval T2 and reaches the peak by end of interval T2. As presented, switching losses dissipate in intervals T2 and T2' where drain current transition can be carried out at full drain-source voltage on MOSFET M 102 and similarly in T3 and T3' where drain-source voltage transition can be carried out at full drain current. Generally, switching losses peak could reach several kilowatts in certain systems and could present an important source of losses.To reduce switching losses,shorter intervals T2, T3 and T2', T3' possible can be used to minimize surface below PM curve 208. However, this may result in steep current and voltage slopes which on the other hand can be main source of electromagnetic emissions in power systems. Emissions, of course, must be kept in certain range to meet strict EMC standard. The optimum point of the presented switching losses and electromagnetic emissions trade-off would therefore be to set shortest intervals T2, T3 and T2', T3' possible (i.e. steepest current and voltage slopes possible) that do not generate excessive electromagnetic emissions.

[0057] The trade-off however can hardly be achieved by using conventional driving method for power MOSFETs or IGBTs with series gate resistor Rg 110. The problem is that adapting Rg110, influence the duration of all intervals (i.e. on all slopes) of the turn-on or turn-off switching sequence and it is not possible to trim a single transition of current or voltage individually.So, in case it is necessary to, say, slow down current transition at turn-on (i.e. to extend T2)to meet EMC standards, by changing (increasing) gate resistance of Rg 110, voltage transitionis also slowed down (i.e. we also extend T3) which results in generation of excessive switching losses.Increasing resistance of resistor Rg110 also extends delay (T1 and T4') and reaches final value (T4 and T1')intervals, which may complicate control algorithm implementation and decrease system reliability.

[0058] FIG. 3 illustrates an exemplary block diagram of gate control system for providing efficient inductive load switching in accordance with an embodiment of the present disclosure. The inductive load switching circuit 300 can include a power gate 328, for example a MOSFET M328, inductive load(s), such as Rload 320-1 and Lload 320-2, collectively and interchangeably referred as inductive load 320, a freewheeling diode Dfwd 326, a gate control system 302 that includes a driving circuit for driving the power gate 328. In an exemplary embodiment, the gate control system 302 can be configured to drive the power gate 328 to perform switching operation for turning-on or turning-off the load 320. The system 302 can include a current source activation block 306 configured to include plurality of current sources for selectively driving the power gate 328, wherein each of the plurality of current sources can be activated for different time intervals, and a controlling circuit block 304 configured to receive a sense voltage between drain and source DSsense 314, a voltage between gate and source GSsense 316, a voltage source Vgg signal 312 and determine borders between different time intervals for activation of each of the plurality of current sources in preconfigured sequential manner to drive the power gate 328.

[0059] In an exemplary embodiment, the controlling circuit block 304 can be figured to receive the sense voltage between drain and source DSsense 314, the voltage between gate and source GSsense 316, and the voltage source Vgg 312 signal, to process the received DSsense 314 and GSsense 316 for performing voltage division and filtering, to determine interval borders between different time intervals at which each of the plurality of current sources, one at a time, can respectively be activated in a preconfigured sequential manner, and to generate ON/OFF control signals for activating the each of the plurality of current sources for driving the power gate 328. In an exemplary embodiment, the current source activation block 306 can be configured to receive the ON/OFF control signals and activate each of the plurality of current sources, one at a time, for respective time intervals in the preconfigured sequential manner based on the ON/OFF control signals for supplying current to the power gate 328 during a switching operation. Using the system 302, the power gate 328 will not face any steep rise and fall of voltage or current.

[0060] In an exemplary embodiment, the current source activation block 306 can be configured to include plurality of current sources, which can be activated sequentially, one at a time for the determined time intervals, based on the ON/OFF control signals.

[0061] In an exemplary embodiment, amplitude of each of the plurality of current sources can be configured manually by the user or can be configured automatically using an aspect of the present disclosure. The amplitude of each of the plurality current sources can be

configured through a current sources amplitude manager. Border between the time intervals or point at which each of the current sources of the plurality of current sources can be switched on or off can be determined based on the ON/OFF control signals.

[0062] In an exemplary embodiment, the controlling circuit block 304 can be configured to include a signal processing block, an intervals boarder detection block, and a logic circuitry for controlling current sources.

[0063] In an exemplary embodiment, the signal processing block can be configured to receive the sense voltage between drain and source DSsense 314, the voltage between gate and source GSsense 316, a voltage source Vgg signal 312, and include voltage dividers to divide the received DSsense 314, GSsense 316, andVgg 312 to meet voltage range of the controlling circuit block 304. In another aspect, the signal processing block 602 (Ref to FIG. 6) can be configured to have filters to eliminate high-frequency oscillations that may occur during power transistor/gate switching in the divided DSsense 314 and GSsense 316. Such filters are not required for Vgg 312 which is supposed to be a logic signal.

[0064] In an exemplary embodiment, division ratio to be used by the voltage dividers, and filter properties to be used by the filters can be configured by the user to match the requirement of specific purpose where the advanced gate control system 302 is about to be implemented. The signal processing block can provide conditioned DSsense2', DSsense', GSsense' and Vgg' which can be used by the interval border detection block for determining the border between the different time intervals.

[0065] In an exemplary embodiment, the interval border detection block can be configured to receive the DSsense2', DSsense', GSsense' and Vgg' and generate signal S2, signal S3, and signal S4, that, in combination with Vgg', can be used to determine the border between the different time intervals. Borders, also referred as points, for example N2, N3 and N4 for turn-on sequence and F4, F3, and F2 for turn-off sequence can be determined based on signals S2, S3 and S4 respectively.

[0066] Further, in an exemplary embodiment, the logic circuitry for controlling current sources can be configured to receive Vgg', S2, S3 and S4 and determine the ON/OFF control signals to send to the current source activation block.

[0067] In an exemplary implementation, signal S2, or point N2 or point F2 can be indicative of a situation when voltage between the gate and source Vgs 332crosses a predefined threshold Vth, signal S3, or point N3can be indicative of a situation during turn-on sequence when voltage between drain and source Vds 330 starts falling or signal S3 or point F3 can be indicative of situation during turn-off sequence when the Vds330 reaches a desired

value, and signal S4, or point N4 can be indicative of a situation during turn-on sequence when the Vds330 reaches a desired value or signal S4 or point F4 can be indicative of a situation during turn-off sequence when the Vds 330 starts rising, wherein for the turn-on sequence, the desired value is voltage Vbat 324that is required to run the load 320, and for the turn-off sequence the desired value is near to zero.

[0068] In an exemplary embodiment, a turn-on switching sequence can start at time t0 at which a first current source of the plurality of current sources can be active for time interval T1. On receiving signal S2, which is indicative of point N2, a second current source of the plurality of current sources can be activated for time interval T2 and the first current source can be turned-off. Further, on receiving signal S3, which is indicative of point N3, a third current source of the plurality of current sources can be activated for time interval T3, and the second current source can be turned-off. Further, on receiving signal S4, which is indicative of point N4, a fourth current source of the plurality of current sources can be activated.

[0069] In an exemplary embodiment, a turn-off switching sequence can start at time t0' at which the fourth current source of the plurality of current sources can be active for time interval T4'. On receiving signal S4, which is indicative of point F4, the third current source of the plurality of current sources can be activated for time interval T3' and the fourth current source can be turned-off. Further, on receiving signal S3, which is indicative of point F3, the second current source of the plurality of current sources can be activated for time interval T2'3, and the third current source can be turned-off. Further, on receiving signal S2, which is indicative of point F2 the first current source of the plurality of current sources can be activated.

[0070] In an exemplary embodiment, selective current sources are activated based on ON/OFF signals to drive the power gate 328 that in turn can turn-on or turn-off power supply to the inductive load 320 using turn-on switching sequence or turn-off switching sequence respectively.

[0071] In an exemplary embodiment, turn-on and turn-off switching sequences can include different time intervals at which different current sources of varied amplitude can drive the power gate 328. For example, turn-on switching sequence interval can have four intervals of different durations, referred hereinafter as T1, T2, T3 and T4, and turn-off switching sequence can similarly have four intervals of different durations referred hereinafter T1', T2', T3' and T4'. In an exemplary embodiment, the turn-on switching sequence interval and turn-off switching sequencing interval can be symmetrical.

[0072] As the turn-off switching sequence is symmetric to the turn-on switching sequence, and as the switching loss and the electromagnetic emission is same for the designed system, different embodiments of the present disclosure will be explained with reference to turn-on switching sequence. As one may appreciate, turn-off switching sequence can similarly be performed.

[0073] The system can be configured to drive the power gate 328 by using a selected current source that can be turned-on and turned-off in a selected order at different time intervals during a switching sequence.

[0074] FIG. 4 illustrates an exemplary circuit that can be used by the current source block 306 in accordance with an embodiment of the present disclosure. As shown in FIG. 4, the current circuit block 306 can include a plurality of current sources, for example, 8 current sources, namely Ig1, Ig2, Ig3, Ig4, and Ig4', Ig3', Ig2' and Ig1'. Each current source is supposed to be active only in specified interval during the switching sequence, for example current source Ig1, Ig2, Ig3, Ig4 can be active during time interval T1, T2, T3, T4 respectively for turn-on sequence, and similarly current sources Ig4', Ig3', Ig2', Ig1' can be active in time interval T4', T3', T2', T'1 respectively for turn-off sequence. The current sources are turned on and off based on ON/OFF control signal 402received from the controlling circuit block 304. In an exemplary embodiment, amplitude of current of each source can be set individually by the current sources amplitude manager 404.

[0075] Amplitude values for each current source can be configured externally by user per requirements of the load. In an exemplary embodiment, the current source block 306 can have a programmable memory for programming the amplitude of different current sources.

[0076] In different embodiments, current sources and current sources amplitude manager 404 can be realized in various ways. For example, current sources could be implemented as current mirrors, and current sources amplitude manager 404 can be current mirror's reference MOSFETs. The reference current can be then set via external resistor and so an external amplitude setting can be enabled.. More sophisticated amplitude manager 404 could be realized with extensive digital and analogue circuitry that would first establish communication interface (SPI for instance) to message the desired amplitude values and secondly set the corresponding reference current for current mirror.

[0077] In an exemplary embodiment, current sources block 306 can also be realized with less than 8 sources, employing some of them in multiple intervals of the switching sequence. For instance, we can remove Ig1' from the block and use Ig2' also in T1' to simplify overall design. Furthermore, current sources activity can overlap in certain intervals in order to sum

currents to the power transistor gate. For example, say that demanded current in interval T3 is higher than that in T2, in such cases the set source Ig2 can be active in both intervals (T2 and T3) and adjust Ig3's amplitude to only supply the difference between Ig2's amplitude and demanded current in T3.

[0078] FIG. 5 illustrates exemplary graphs observed during switching activity of an inductive load switching using advanced gate control system 302 in accordance with an embodiment of the present disclosure. As can be seen, waveform 502, in graph 'a', indicates current at load during different time intervals, waveform 504 in graph 'b' indicates voltage between drain and source Vds during different time interval, and waveform 506 in graph'c' shows current at gate during different time intervals. Influence of the Ig2 amplitude manipulation on current slope graph 502 can be observed during interval T2.

[0079] FIG. 6 illustrates exemplary functional blocks of a controlling circuit block 304 in accordance with an embodiment of the present disclosure. In an exemplary embodiment, the controlling circuit block 304 can be configured to include a signal processing module 602, an interval detection module 604, and a logic circuitry for controlling current sources 606.

[0080] In an exemplary embodiment, the signal processing block 602 can be configured to receive sense voltage between drain and source DSsense 314, the voltage between gate and source GSsense 316, a voltage source Vgg signal 312, and include voltage dividers to divide the received DSsense 314, GSsense 316, and Vgg 312 to meet voltage range of the controlling circuit block andto subsequently filter the DSsense 314and GSsense 316to eliminate high-frequency oscillation that may occur during power transistor switching. The signal processing block 602 can provide conditioned DSsense2', DSsense', GSsense' and Vgg', which can used by the interval border detection block 604.

[0081] The interval border detection block 604 can be configured to receive the DSsense2', DSsense', GSsense' and Vgg' and generate signal S2, signal S3, and signal S4, which in combination with Vgg' can be used to determine the borders between the different time intervals. Borders, also referred as points, for example N2, N3 and N4 for turn-on sequence and F4, F3, and F2 for turn-off sequence can be determined based on signal S2, S3 and S4 respectively.

[0082] Further in an exemplary embodiment, the logic circuitry for controlling current sources 606 can be configured to receive Vgg', S2, S3 and S4 and determine the ON/OFF control signals 402 to be sent to the current source activation block 306.

[0083] Functionalities of the controlling circuit block 304 can be explained with help of graphs of FIG. 7A that illustrate interval borders associated with events.FIG. 7A illustrates

exemplary graph highlighting interval borders associated with events in accordance with an embodiment of the present disclosure and FIG. 7B illustrates exemplary points that are marked in graphs as shown in FIG. 7A.

[0084] In an exemplary embodiment, borders between intervals can be associated with special events, or points as shown in FIG. 7A and FIG. 7B. The points N0 710, N2 712, N3 714 and N4 716 for turn-on sequence and F0, F4, F3 and F2 for turn-off sequence are shown in FIG. 7A. By sensing these points, the system can recognize borders between intervals and subsequently turn current sources on or off. An important thing to mention is that all points are located exclusively on voltage signals (vds and vgg) and so we don't have to measure current through the power transistor. This functionality allows the present system to be used in high current environments, as it doesn't require current sensing for determining the interval borders.

[0085] As shown in FIG. 7A and described in FIG. 7B, point N0 710 on waveforms 702 of Vgs indicates start of turn-on sequence when Vgg starts rising, N2712 indicates a point on waveform 702 when the Vgs reaches the threshold voltage Vth, N3 714 indicates a point on waveform 706 when Vds starts falling, and N4 716 indicates a point on waveforms 706 when Vds falls to the final value so as to complete the turn on sequence. Similarly, point F0 on waveform 702 indicates start of turn-off sequence when Vgg starts falling, F4 on waveform 706 indicates a point when Vds starts rising, F3 on waveform 706 indicates a point when Vds reaches to final value, and F2indicates a point when Vgs falls to the threshold values.

[0086] FIG. 8 illustrates functional blocks of a signal processing block602 that can be used to determine the drain source voltage in accordance with an embodiment of present disclosure. In an exemplary embodiment, the signal processing block 602 can be configured to receive the DSsense 314, the GSsense 316, the Vgg signal 312, and include voltage dividers 806 to divide the received DSsense 314, GSsense 316and Vgg signal 312 to meet voltage range of the controlling circuit block and filters 808 to subsequently filter the DSsense 314 and GSsense 316to eliminate high-frequency oscillation that may occur during power transistor switching. The signal processing block 602 can provide conditioned DSsense2' 810, DSsense' 812, GSsense' 814 and Vgg' 816 which can used by the interval border detection block 604, wherein the Vgg 312 can be a logic signal.

[0087] In an exemplary embodiment, division ratio to be used by the voltage dividers 806 can be externally set by the user. Filter properties to be used by the filters 808 can also be externally set by the user to match requirements of specific system where advanced gate control system is about to be implemented.

[0088] In an exemplary embodiment, Vds can be sensed from DSsense signal using a suitable arrangement. At its highest value DSsense can be equal to Vbat, and hence can reach several tens or even hundreds of volts in some systems. This can result in high voltage division ratio and therefore the system can lose resolution that on the other hand may be crucial to detect points N3 and F3.To solve above problem, a special circuit as shown in FIG. 8 with series connection of diode D 802, resistor R 804 and voltage supply Vcc310 can be used. For DSsense<Vcc, node voltage DSsense2 can just follow DSsense 314, wherein DSsense2 can be equal to DSsense 314 plus voltage drop on diode D 802. For higher values, where DSsense 314 is greater than Vcc 310, the diode D 802 enters in blocking mode and node voltage DSsense2remains at Vcc level.Since Vcc can be the highest value of DSsense2,a lower dividing ratio would be required and so resolution of Vds can be retained. The signal processing block 602 outputs filtered DSsense2' 810, DSsense' 812, GSsense'814 and Vgg' 816.

[0089] FIG. 9 illustrates an exemplary circuit that can be used for intervals border detection in accordance with an embodiment of the present disclosure. FIG. 10 illustrates exemplary border intervals determined in accordance with an embodiment of the present disclosure. In an exemplary embodiment, the interval border detection block 604 can receive DSsense2' 810, DSsense' 812, GSsense' 814 and Vgg' 816 and generate logic signals S2 912-3, signal S3 912-3 and signal S4 912-1. The logic signals S2 912-3, S3 912-2 and S4 912-1are shown in graph(d) of the FIG. 10.Start of the logic signals can indicate interval borders between intervals and current state of power transistor. The logic signal S2, S3, S4 along with Vgg' 816 provides enough information for adequate control of current sources. As mentioned above, borders are indicated by points N0, N2, N3 and N4 for turn-on sequence and F0, F4, F3, F2 for turn-off sequence as shown in FIG.10. Border, is also shown in FIG. 10 graphs d as line S2 1002, line S3, 1004, and line 1006, wherein start and end of line S2 1002 indicates point N2 and point F2 respectively. Start and end of line 1004 indicates point N3 and pint F3 respectively. Similarly, start and end of line 1006 indicates point N4 and point F4 respectively.

[0090] In an exemplary embodiment, detection of these points can be achieved by a suitable circuit, for example as shown in FIG. 9. To simplify the explanation, we will only describe detection of points N4 and F4 and generation of output signal S4. However, explanation applies to detection of all points and generation of signals S2 and S3 as well.

[0091] Signals S2, S3 and S4 are set and reset with complementary point pairs: N2 – F2 for S2, N3 – F3 for S3 and N4 – F4 for S4. Points within a pair describe similar voltage level

crossing of corresponding signals. N2 and F2 indicate Vgs (via GSsense') crossing threshold voltage, N3 and F3 indicate start of Vds falling and end of Vds rising (via DSsense') and lastly, for the case describing, N4 and F4 indicate the end of Vds falling at turn-on and start of Vds rising at turn-off (via DSsesnse2').

[0092] In an exemplary embodiment, transition of Vds across N4 and F4 can be detected with comparators U1 902 and U2 904 (via DSsense2', divided and filtered Vds)followed by AND gate U3 906 and AND gate U4 908 respectively as shown in FIG. 9. In an exemplary implementation, reference values Vref for detection of point N4 and different Vref for detection of F4 can be set externally by a user.

[0093] Using the exemplary circuit as shown in FIG. 9, different points such as N0, N2, N3 and N4 for turn-on sequence and F0, F4, F3 and F2 for turn-off sequence can be determined and can be used to match transitions of selected inductive load circuit and power transistor. Determining the different points, or in other words interval borders and controlling the current supply to the power gate based on the determined time interval can enable efficient switching.

[0094] Since both comparators U1 902 and U2 904 switch at each DSsense2' crossing of their reference values, wherein the crossings appear once at turn-on and once at turn-off, the interval border detection block can employ AND gates U3 906 and U4 908 with applied Vgg' and Vgg' inverted to indicate whether turn-on or turn-off sequence is currently on. By doing so, interval border detection block 604 can create a window where N4 and F4 can be detected (N4 during turn-on on comparator U1 902 and F4 during turn-off on comparator U2 904). In an exemplary embodiment, the AND gates U3 906 and U4 908, outputs of which indicate detection of N4 and F4, can be followed by a SR cell 910, wherein when N4 is detected, SET (S) of SR cell 910 can be triggered and s4 can be set to 1. Similarly, when F4 is detected, RESET (R) can be triggered and S4 can be set to 0. With simple modification, similar circuit can be used to generate other signals, such as S3 and S2.

[0095] FIG. 11 illustrates an exemplary logic circuit for controlling current sources in accordance with an embodiment of the present disclosure. As shown in FIG. 11, logic circuitry for controlling current sources 606 implements logic functions that transform signals S2, S3, S4 and Vgg' to turn-on and turn-off signals for each current source in the current sources block. As one may appreciate, block contents and number of output signals can depend on number of current sources being used by the current source block and their desired operation.

[0096] FIG. 12 illustrates an exemplary flow of a method for driving a power gate to perform switching operation in accordance with an embodiment of the present disclosure. As shown in FIG. 12, the method includes steps of, at 1202,sensing a sense voltage between drain and source Vds, a voltage between gate and source Vgs, and a voltage source Vgg signal. The method can further include, at step 1204, activating a first current source selected from plurality of current sources at a time t0,and at 1206, turning off the first current source and activating a second current source selected from the plurality of current sources at end of time interval T1. At step 1208, the method can include, turning off the second current source and activating a third current source selected from the plurality of current sources at end of time interval T2, and at step 1210, turning off the third current source and activating a fourth current source selected from the plurality of current sources at end of time interval T3, wherein the end of time interval T1, the end of time interval T2, and the end of time interval T3 can be determined based on the Vds, Vgs and the Vgg, and wherein amplitude of plurality of current sources can be different and preconfigured.

[0097] In an exemplary embodiment, the end of time interval T1, also referred as N2, is a point when voltage between the gate and a source Vgs reaches a predefined threshold voltage, the end of time interval T2, also referred as N3, is a point when voltage between drain and the source Vds starts falling, and the end of time interval T3, also referred as N4 is a point when the Vds reaches to a desired value, during a turn-on switching sequence.

[0098] While the foregoing describes various embodiments of the invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof. The scope of the invention is determined by the claims that follow. The invention is not limited to the described embodiments, versions or examples, which are included to enable a person having ordinary skill in the art to make and use the invention when combined with information and knowledge available to the person having ordinary skill in the art.

CLAIMS

We Claim:

1. A gate control system to drive a power gate to perform switching operation, the system comprising:

a controlling circuit block comprising circuitary to receive a sense voltage between drain and source (DSsense), a sense voltage between gate and source (GSsense), and a voltage source (Vgg) signal, and determine borders between the different time intervals based on the DSsense, GSsense, and Vgg to generate a control signal;

a current source activation block comprising a plurality of current sources for selectively driving the power gate based on the control signal, wherein each of the plurality of current sources are selectively activated for driving the power gate, one at a time, for different time intervals; and

wherein amplitude of each of the plurality of current sources are different and are preconfigured.

2. The system claim 1, wherein the amplitude of each of the plurality of current sources are preconfigured through a current source amplitude manager that allows a user or an application program to configure the amplitude of each of the plurality of current sources.

3. The system of claim 1, wherein the controlling circuit block comprises

a signal processing block configured to divide and filter the DSsense, the GSense, and the Vgg,

an interval border detection block configured to determine the borders between the different time intervals; and

a logic circuitry for controlling current sources configured to generate the control signal.

4. The system of claim 3, wherein the signal processing block comprises

a suitable circuitry to receive the DSsense, the GSsense, the Vgg signal;

one or more voltage dividers to divide the received Dssense, the received GSsense, and the Vgg to meet voltage range of the controlling circuit block;

one or more filters to filter the DSsense and the GSsense to eliminate high-frequency oscillations, and generate conditioned DSsense2', DSsense', GSsense' and Vgg' to be used by the interval border detection block.

5. The system of claim 4, wherein the signal processing block comprises a voltage supply Vcc, a resister R, and a diode D connected in series to avoid loss of resolution that occurrs due to the one or more voltage dividers or the one or more filters.
6. The system of claim 4, wherein the interval border detection block is configured to receive the DSsense2', DSsense', GSsense' and Vgg' and generate signal S2, signal S3, and signal S4, which in combination with Vgg' is used to determine the borders between the different time intervals.
7. The system of claim 6, wherein the logic circuitry for controlling current sources is configured to receive the Vgg', the S2, the S3, and the S4 to determine the control signal that is sent to the current source activation block.
8. The system of claim 6, wherein the interval border detection block is configured to generate the signal S2, the signal S3, and the signal S4 using one or more of comparators, AND gates, and a SR logic cell.
9. The system of claim 6, wherein the signal S2 is indicative of a situation when voltage between the gate and source Vgs reaches a predefined threshold Vth, the signal S3 is indicative of a situation when voltage between drain and source Vds starts falling, and the signal S4 is indicative of a situation when the Vds reaches a desired value during a turn-on sequence.
10. The system of claim 6, wherein the signal S2 is indicative of a situation when voltage between the gate and source Vgs reaches the predefined threshold Vth, the signal S4 is indicative of a situation when the Vds starts rising, and the signal S3 is indicative of a situation when the Vds reaches a desired value during a turn-off sequence.
11. A circuit for driving an inductive load, the circuit comprising:

a main voltage source Vbat;

a power gate;

a freewheeling diode Dfwd connected in parallel with the inductive load; and

a gate control system for driving the power gate, wherein the gate control system comprises:

a controlling circuit block comprising circuitary to receive a sense voltage between drain and source (DSsense), a sense voltage between gate and source (GSsense), and a voltage source (Vgg) signal, and determine borders between the different time intervals based on the DSsense, GSsense, and Vgg to generate a control signal;

a current source activation block comprising a plurality of current sources for selectively driving the power gate based on the control signal, wherein each of the plurality of current sources are selectively activated for driving the power gate, one at a time, for different time intervals; and

wherein amplitude of each of the plurality of current sources are different and are preconfigured.

12. A method for driving a power gate to turn-on or turn off an inductive load, the method comprising the steps of:

sensing a sense voltage between drain and source Vds, a sense voltage between gate and source Vgs, and a voltage source Vgg signal;

activating a first current source selected from a plurality of current sources at time T0;

turning off the first current source and activating a second current source selected from the plurality of current sources at end of time interval T1;

turning off the second current sources and activating a third current source selected from the plurality of current sources at end of time interval T2; and

turning off the third current source and activating a fourth current source selected from the plurality of current sources at end of time interval T3;

wherein the end of time interval T1, the end of time interval T2, and the end of time interval T3 can be determined based on the Vds, Vgs and the Vgg, and wherein amplitude of the plurality of current sources are different and are preconfigured.

13. The method of claim 12, wherein the end of time interval T1 is a point when the Vgs reaches a predefined threshold voltage, the end of time interval T2 is a point when the Vds starts falling, and the end of time interval T3 is a point when the Vds reaches to a desired value during a turn-on switching sequence.

14. The method of claim 12, wherein the end of time interval T1 is a point when the Vgs reaches a predefined threshold voltage, the end of time interval T2 is a point when the Vds starts rising, and the end of time interval T3 is a point when the Vds reaches to a desired value, during a turn-off switching sequence.

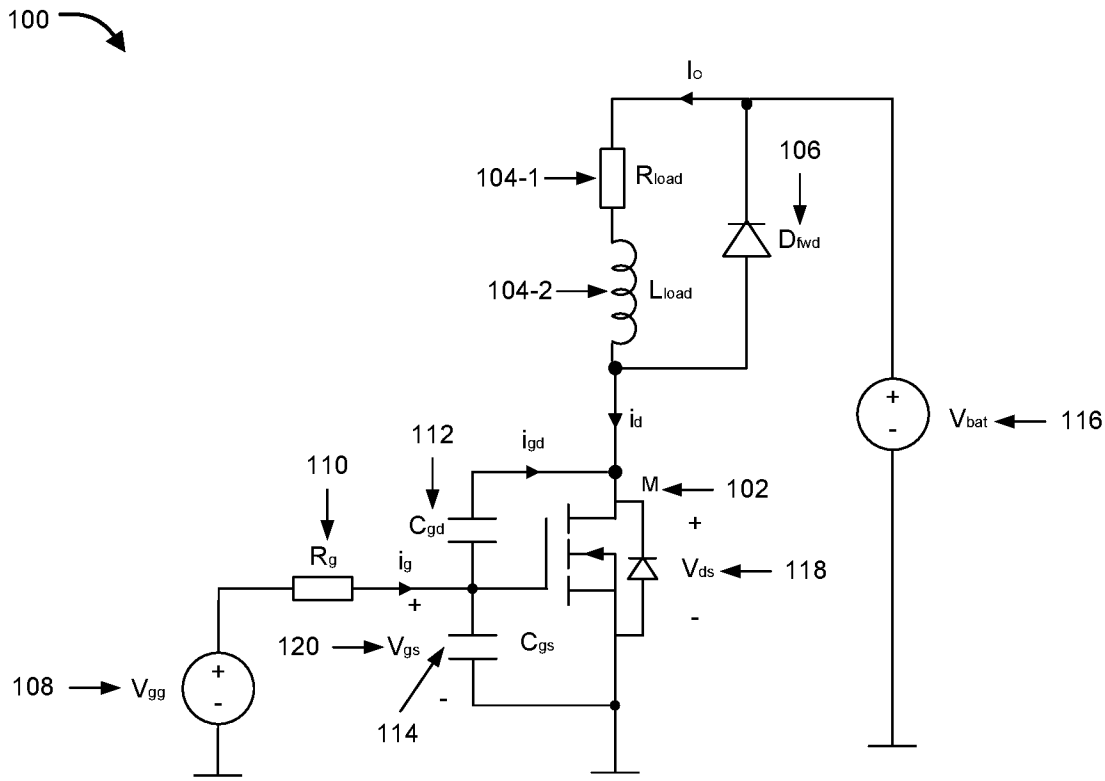

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I_O
104-1
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D_{fwd}
104-2
L_{load}
i_d
V_{bat}
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112
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110
M
102
C_{gd}
+
R_g
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118
-
+
120
V_{gs}
C_{gs}
108
V_{gg}
-
114

FIG. 1

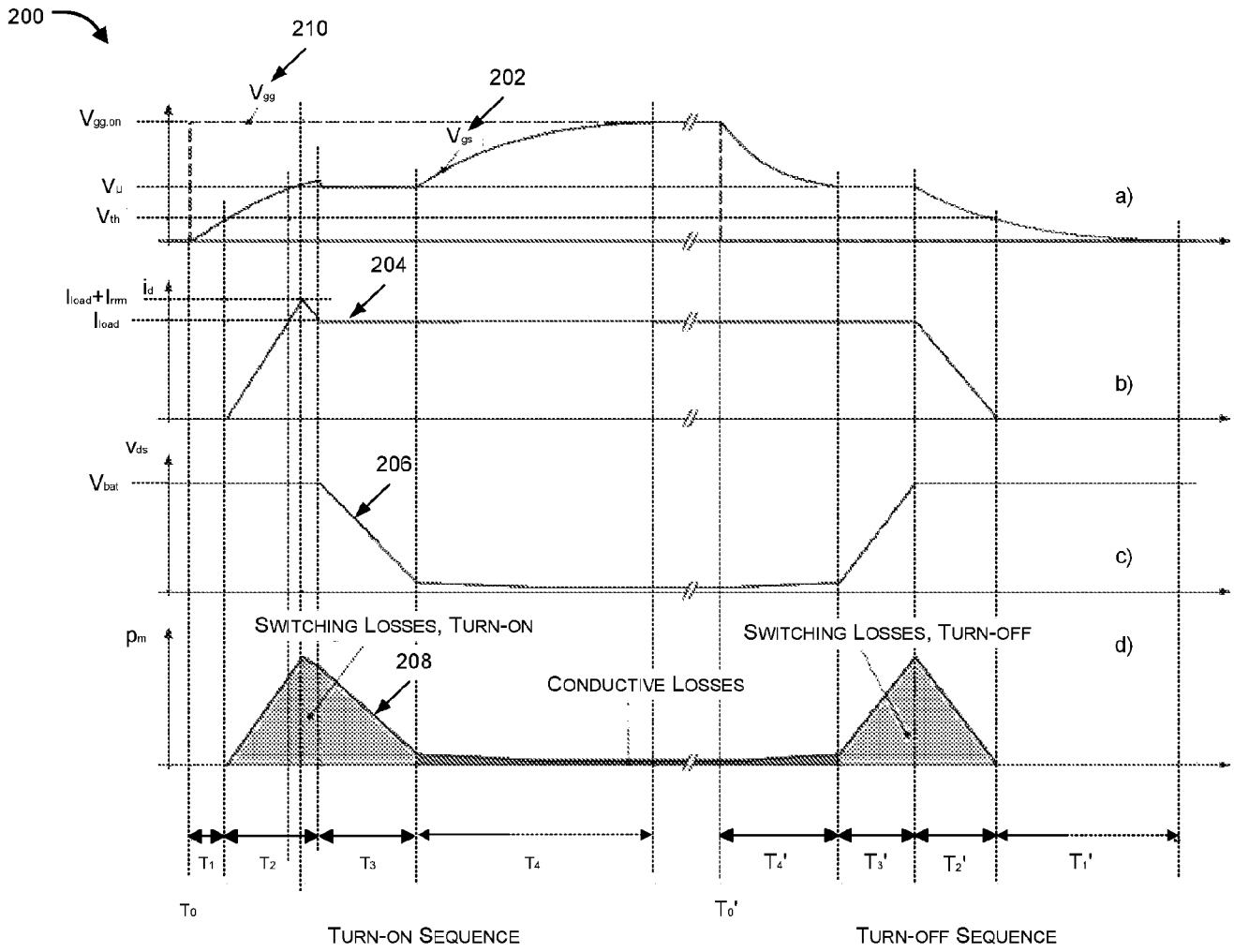

200
210
V_{gg}
202
V_{gs}
$V_{gg,on}$
V_u
V_{th}
a)
204
$I_{load}+I_{rrm}$
i_d
I_{load}
b)
v_{ds}
V_{bat}
206
c)
p_m
SWITCHING LOSSES, TURN-ON
208
CONDUCTIVE LOSSES
SWITCHING LOSSES, TURN-OFF
d)
T_1
T_2
T_3
T_4
T_4'
T_3'
T_2'
T_1'
T_0
T_0'
TURN-ON SEQUENCE
TURN-OFF SEQUENCE

FIG. 2

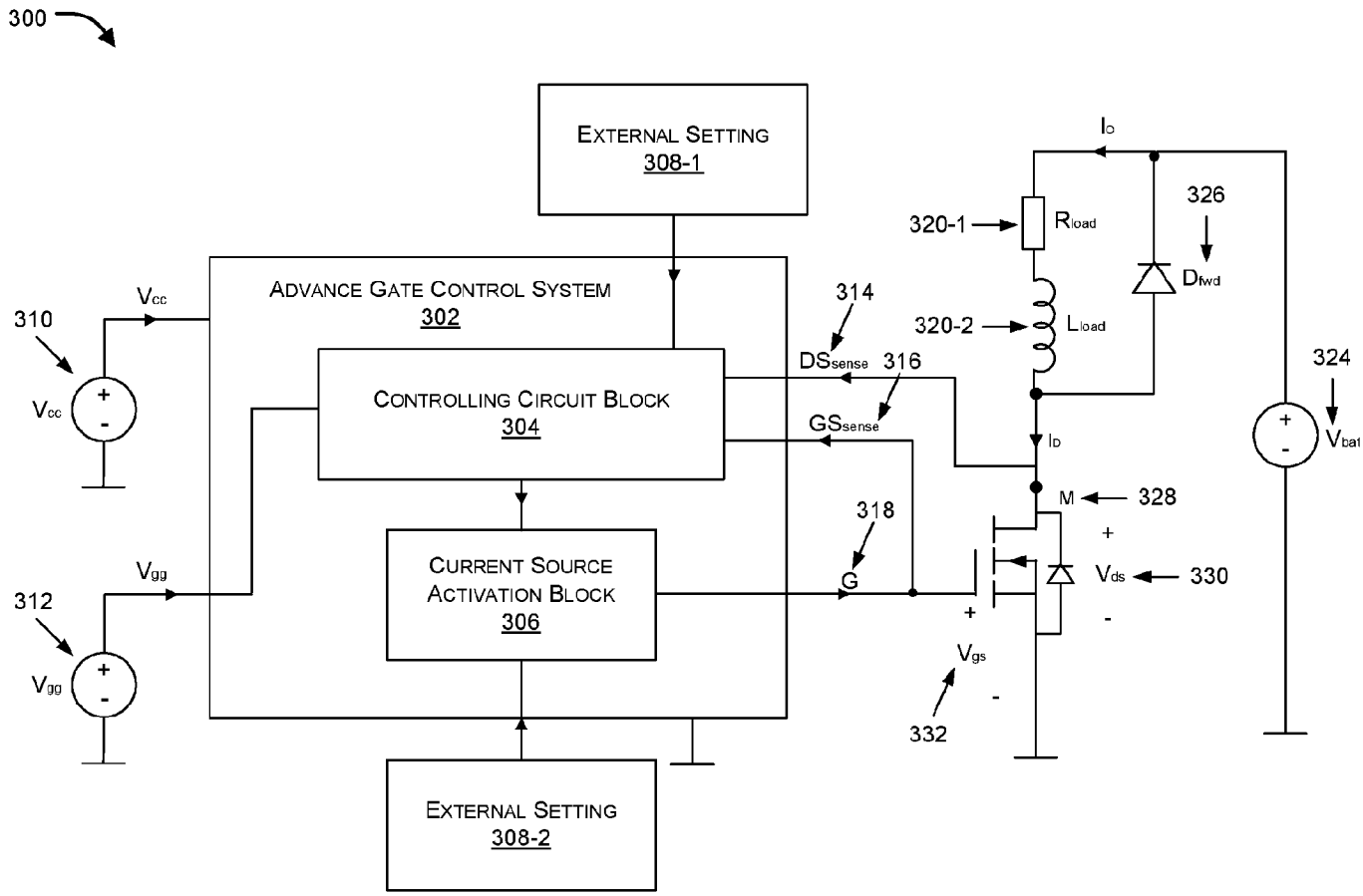

300
EXTERNAL SETTING
308-1
ADVANCE GATE CONTROL SYSTEM
302
CONTROLLING CIRCUIT BLOCK
304
CURRENT SOURCE
ACTIVATION BLOCK
306
EXTERNAL SETTING
308-2
310
Vcc
312
Vgg
314
DSsense
316
GSsense
318
G
320-1
Rload
320-2
Lload
326
Dfwd
Io
ID
M
328
Vds
330
Vgs
332
324
Vbat

FIG. 3

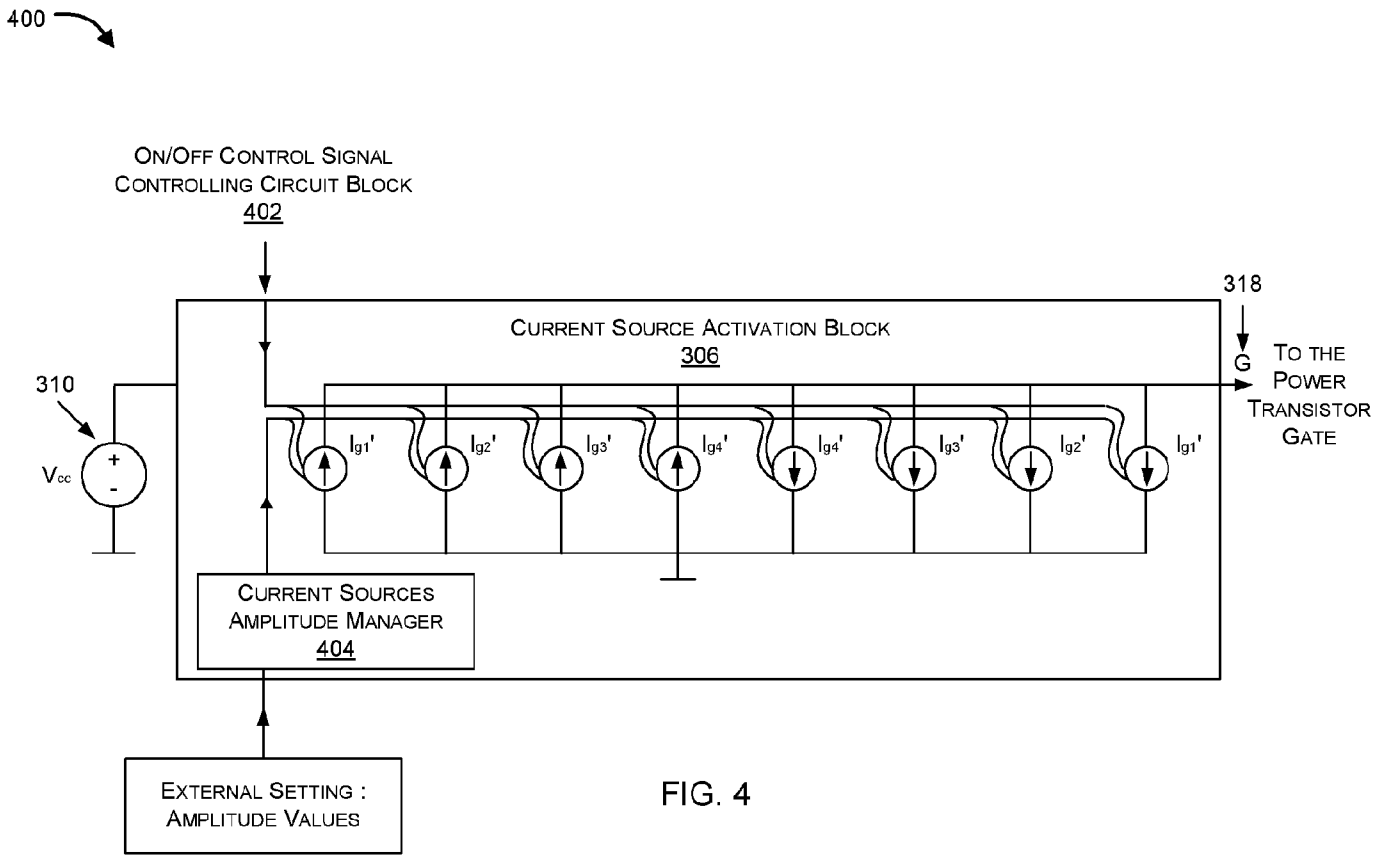

400
ON/OFF CONTROL SIGNAL CONTROLLING CIRCUIT BLOCK
402
318
CURRENT SOURCE ACTIVATION BLOCK
306
G
TO THE POWER TRANSISTOR GATE
310
Vcc
+
-
Ig1'
Ig2'
Ig3'
Ig4'
Ig4'
Ig3'
Ig2'
Ig1'
CURRENT SOURCES AMPLITUDE MANAGER
404
EXTERNAL SETTING : AMPLITUDE VALUES

FIG. 4

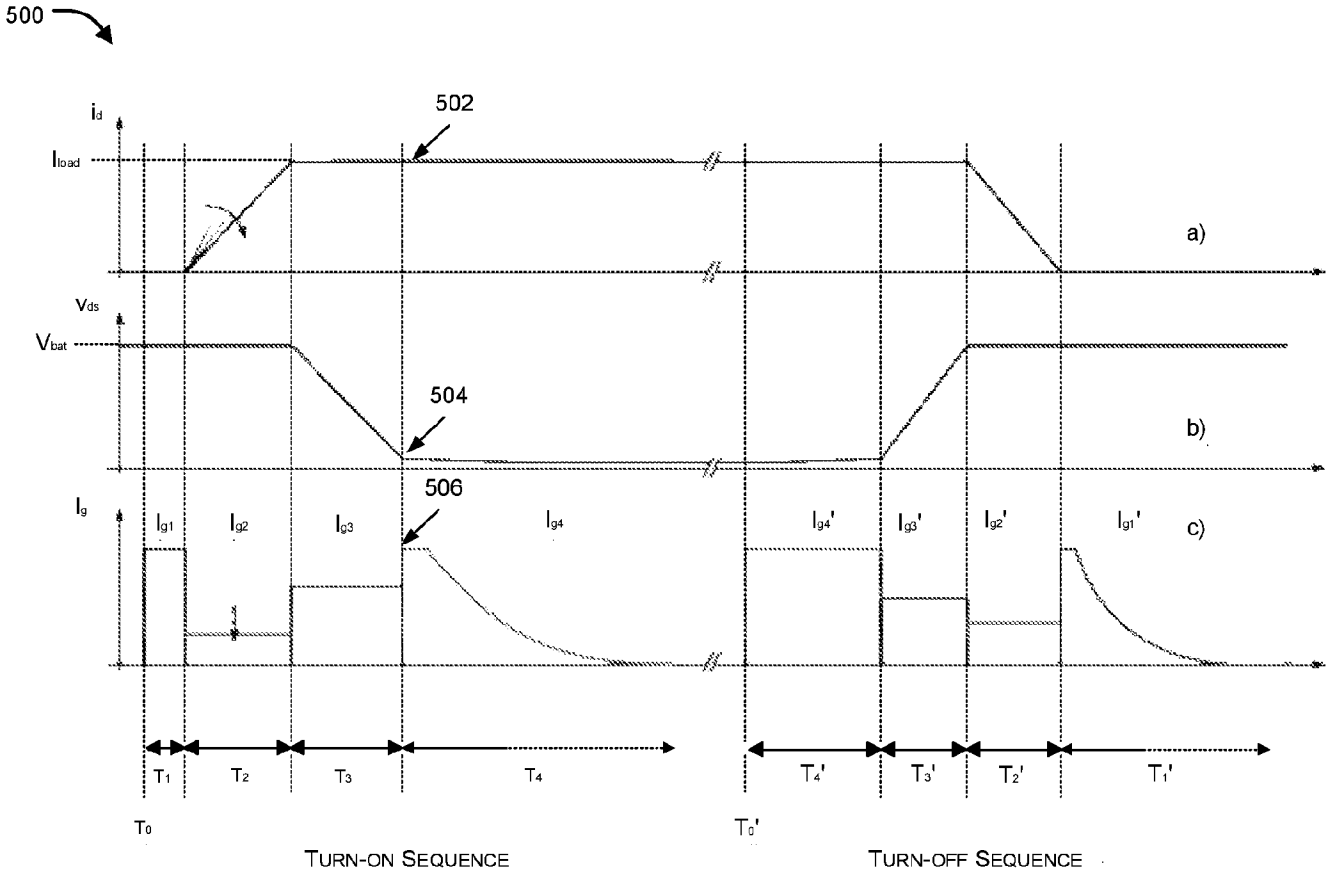

500
i_d
I_{load}
502
a)
V_{ds}
V_{bat}
504
b)
I_g
506
I_{g1}
I_{g2}
I_{g3}
I_{g4}
I_{g4}'
I_{g3}'
I_{g2}'
I_{g1}'
c)
T_1
T_2
T_3
T_4
T_4'
T_3'
T_2'
T_1'
T_0
T_0'
TURN-ON SEQUENCE
TURN-OFF SEQUENCE

FIG. 5

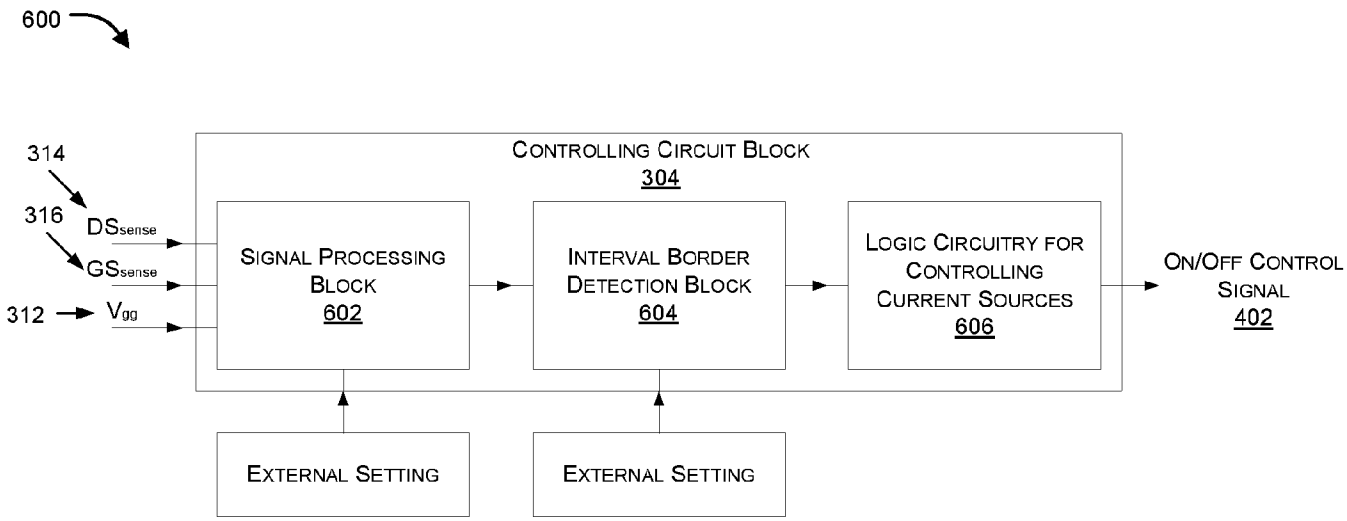

600
314
316
DSsense
GSsense
312
Vgg
CONTROLLING CIRCUIT BLOCK
304
SIGNAL PROCESSING BLOCK
602
INTERVAL BORDER DETECTION BLOCK
604
LOGIC CIRCUITRY FOR CONTROLLING CURRENT SOURCES
606
ON/OFF CONTROL SIGNAL
402
EXTERNAL SETTING
EXTERNAL SETTING

FIG. 6

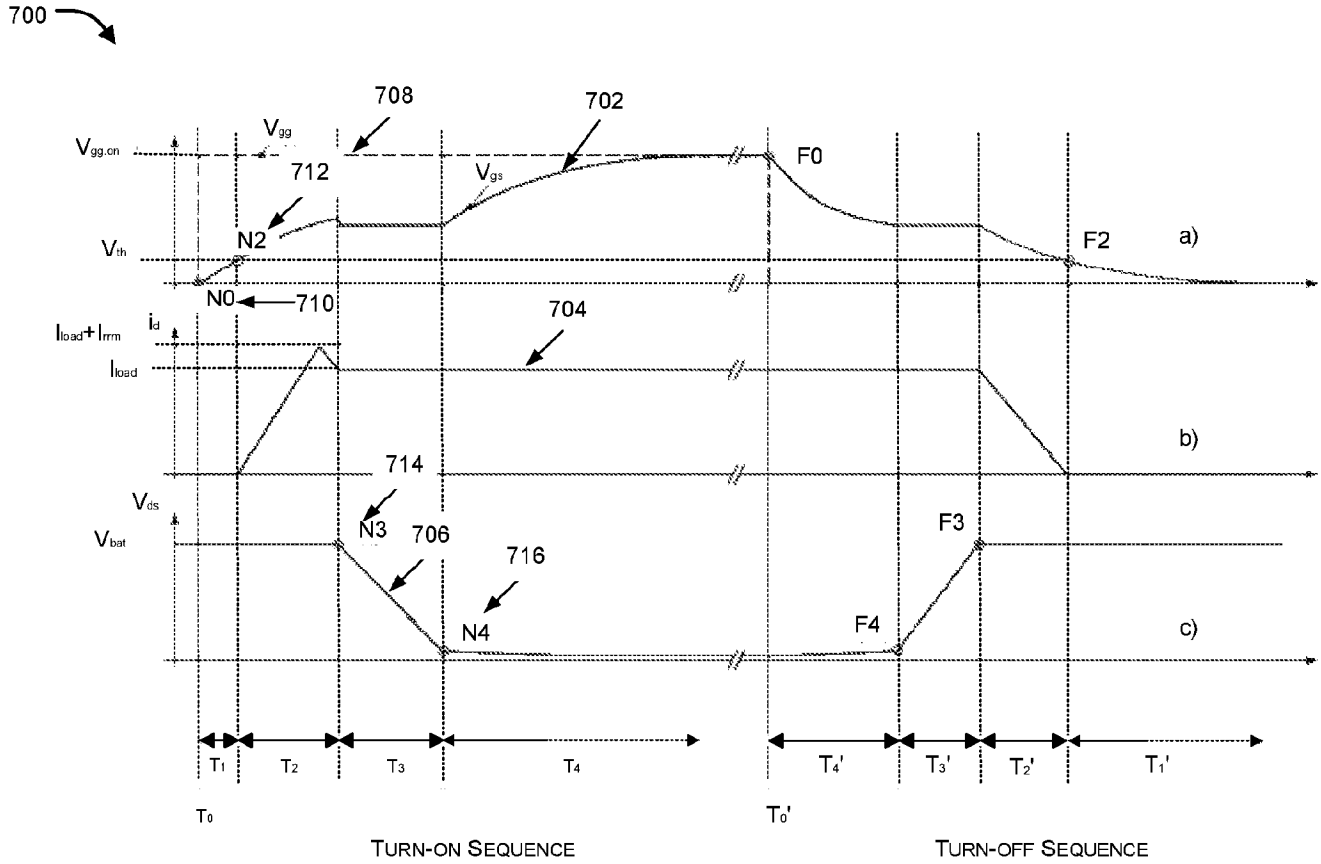

700
708
702
V_{gg}
$V_{gg,on}$
712
V_{gs}
F0
N2
V_{th}
F2
a)
N0
710
704
$I_{load}+I_{rrm}$
i_d
I_{load}
b)
714
V_{ds}
N3
706
F3
V_{bat}
716
N4
F4
c)
T_1
T_2
T_3
T_4
T_4'
T_3'
T_2'
T_1'
T_0
T_0'
TURN-ON SEQUENCE
TURN-OFF SEQUENCE

FIG. 7A

750

Point	Start of Interval	Associated Event
N0	T1	Start of TURN-ON Sequence, Vgg Starts Rising
N2	T2	VGS reaches threshold voltage
N3	T3	VDS Starts Falling
N4	T4	VDS Falls to the Final Value
Power Transistor is On		
F0	T4	Start of TURN-OFF Sequence Vgg Starts Falling
F4	T3	VDS Starts Rising
F3	T2	VDS Rises to the Final Value
F2	T1	VGS Falls to the Threshold Voltage
Power Transistor is Off		

FIG. 7B

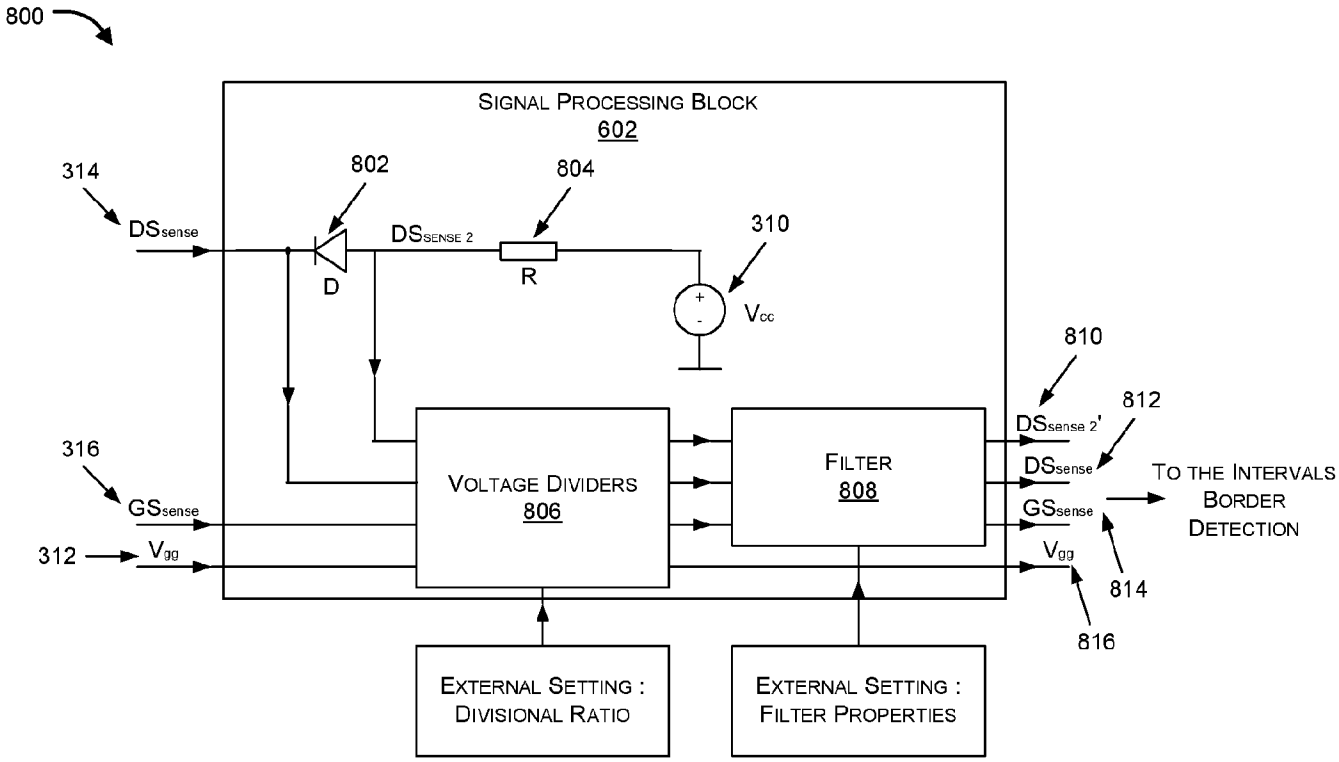

800
SIGNAL PROCESSING BLOCK
602
314
DSsense
802
D
DSSENSE 2
804
R
310
Vcc
316
GSsense
312
Vgg
VOLTAGE DIVIDERS
806
FILTER
808
810
DSsense 2'
812
DSsense
GSsense
Vgg
TO THE INTERVALS BORDER DETECTION
814
816
EXTERNAL SETTING : DIVISIONAL RATIO
EXTERNAL SETTING : FILTER PROPERTIES

FIG. 8

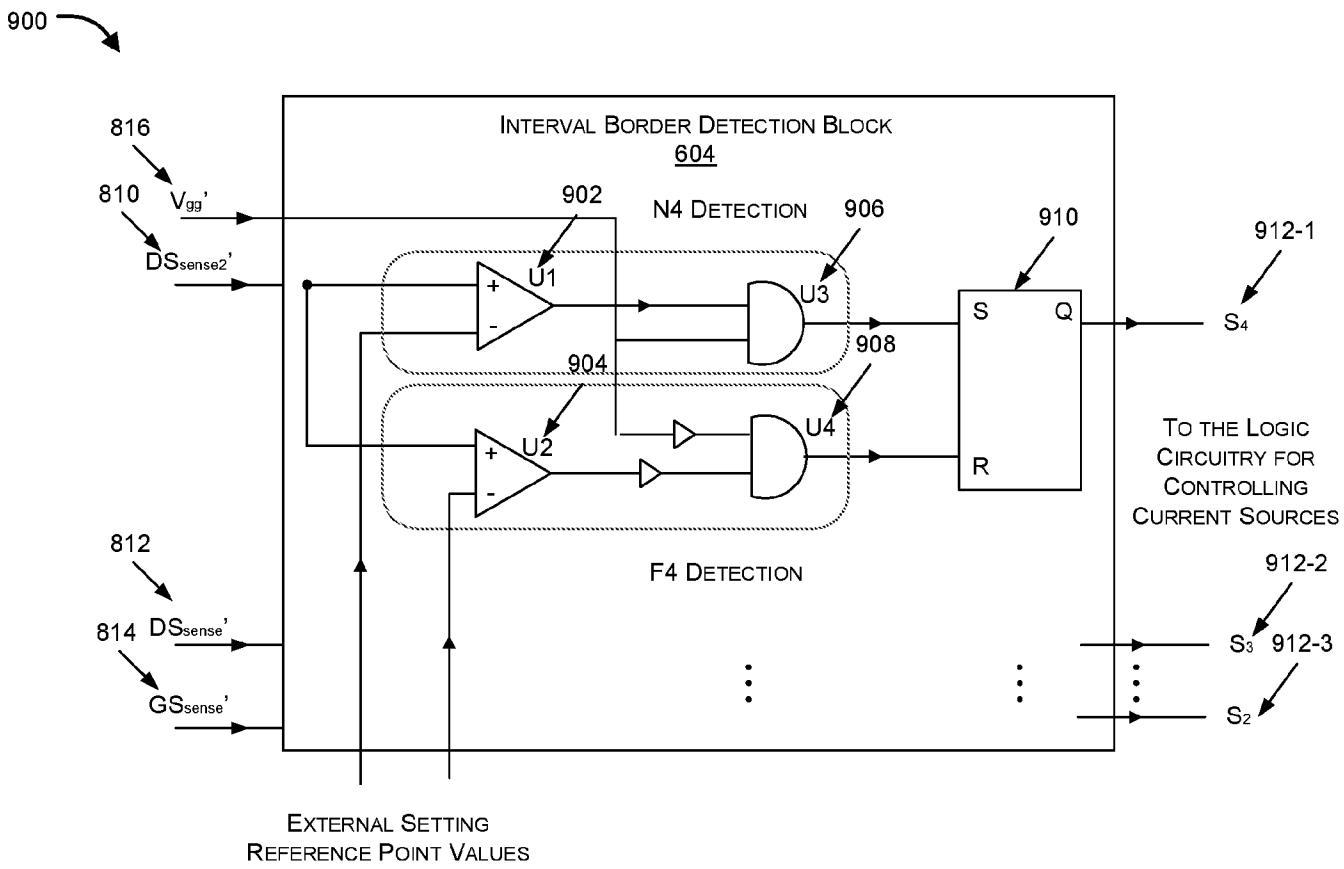

900
816
810
V_{gg}'
DS_{sense2}'
INTERVAL BORDER DETECTION BLOCK
604
902
N4 DETECTION
906
910
912-1
U1
U3
S
Q
S_4
908
904
U2
U4
R
TO THE LOGIC CIRCUITRY FOR CONTROLLING CURRENT SOURCES
812
814
DS_{sense}'
GS_{sense}'
F4 DETECTION
912-2
S_3
912-3
S_2
EXTERNAL SETTING REFERENCE POINT VALUES

FIG. 9

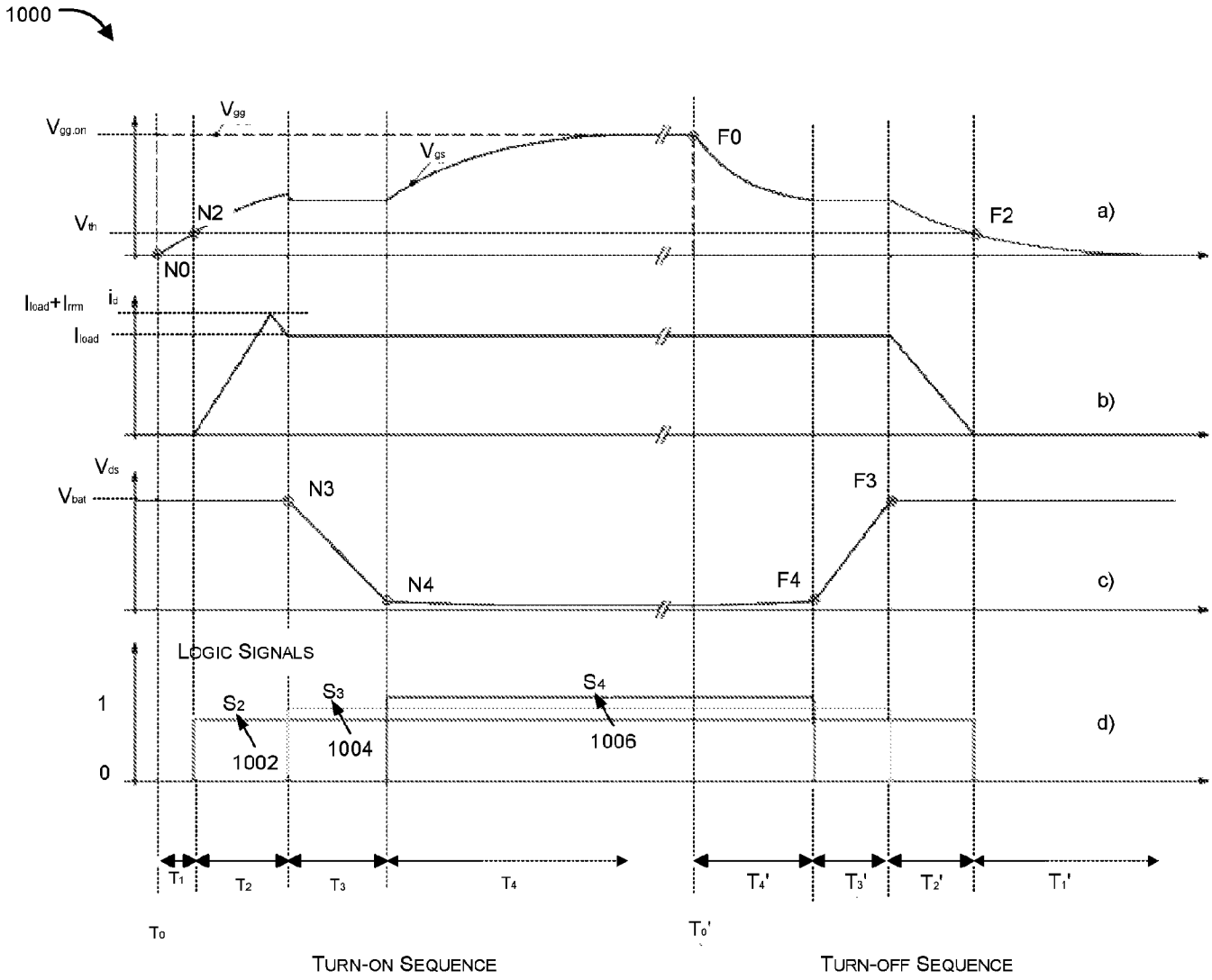

1000
Vgg
Vgg,on
Vgs
F0
Vth
N2
F2
a)
N0
Iload+Irrm
id
Iload
b)
Vds
Vbat
N3
F3
N4
F4
c)
LOGIC SIGNALS
S2
S3
S4
1
0
1002
1004
1006
d)
T1
T2
T3
T4
T4'
T3'
T2'
T1'
T0
T0'
TURN-ON SEQUENCE
TURN-OFF SEQUENCE

FIG. 10

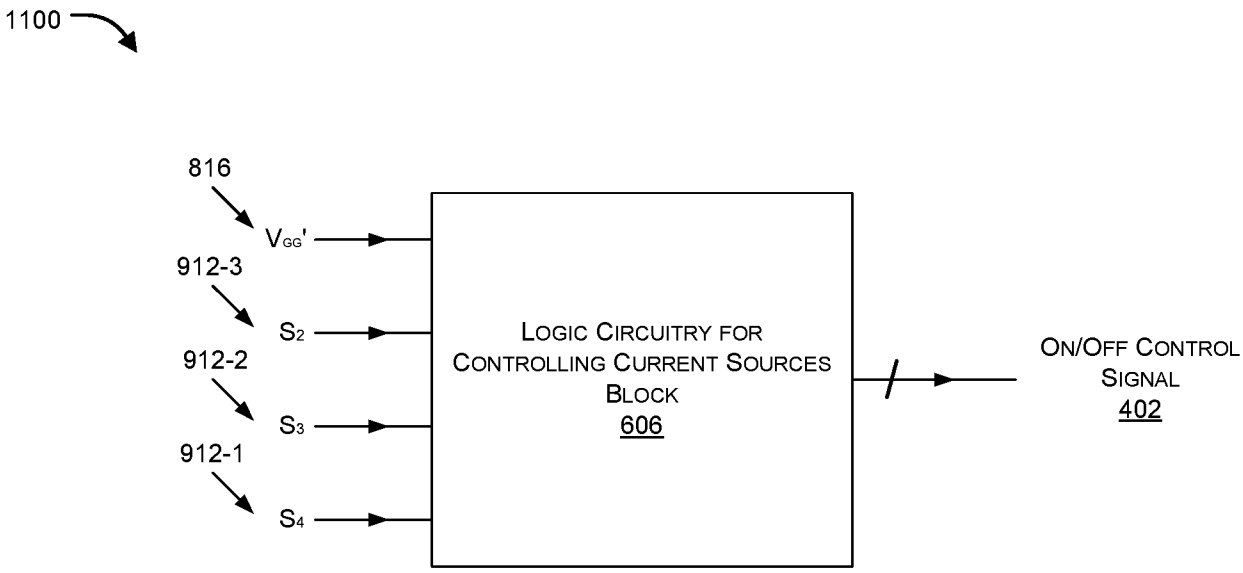

1100
816
V_{GG}'
912-3
S_2
912-2
S_3
912-1
S_4
LOGIC CIRCUITRY FOR CONTROLLING CURRENT SOURCES BLOCK
606
ON/OFF CONTROL SIGNAL
402

FIG. 11

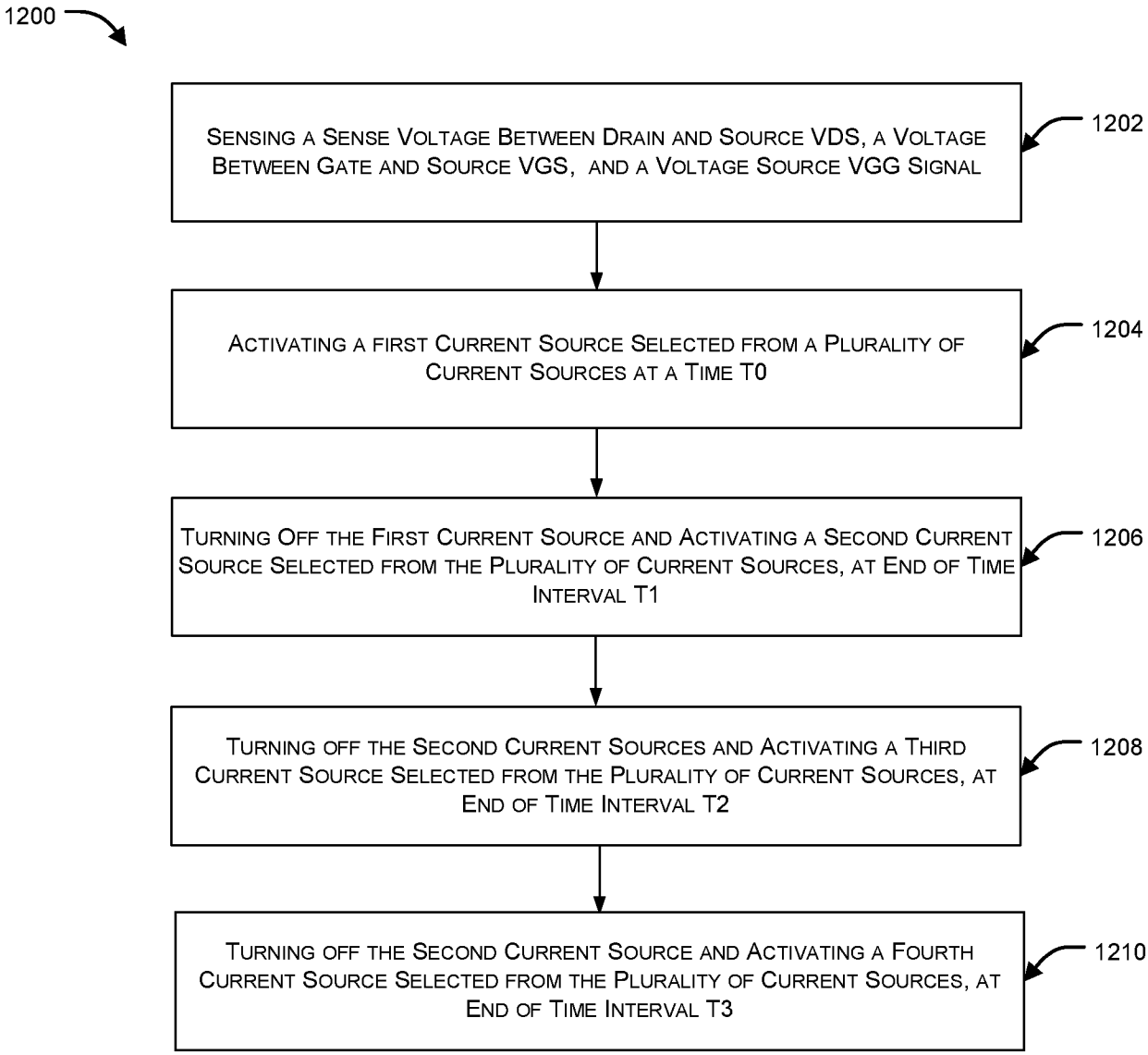

1200
SENSING A SENSE VOLTAGE BETWEEN DRAIN AND SOURCE VDS, A VOLTAGE BETWEEN GATE AND SOURCE VGS, AND A VOLTAGE SOURCE VGG SIGNAL
1202
ACTIVATING A FIRST CURRENT SOURCE SELECTED FROM A PLURALITY OF CURRENT SOURCES AT A TIME T0
1204
TURNING OFF THE FIRST CURRENT SOURCE AND ACTIVATING A SECOND CURRENT SOURCE SELECTED FROM THE PLURALITY OF CURRENT SOURCES, AT END OF TIME INTERVAL T1
1206
TURNING OFF THE SECOND CURRENT SOURCES AND ACTIVATING A THIRD CURRENT SOURCE SELECTED FROM THE PLURALITY OF CURRENT SOURCES, AT END OF TIME INTERVAL T2
1208
TURNING OFF THE SECOND CURRENT SOURCE AND ACTIVATING A FOURTH CURRENT SOURCE SELECTED FROM THE PLURALITY OF CURRENT SOURCES, AT END OF TIME INTERVAL T3
1210

FIG. 12

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2016/050211

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03K17/16
ADD. H03K17/64

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/021498 A1 (SCHEIKL ERICH [AT]) 5 February 2004 (2004-02-05) figures 5,6A,6B -----	1-14
X	WO 00/10243 A1 (ABB DAIMLER BENZ TRANSP [DE]; BELWON WALDEMAR A [SE]) 24 February 2000 (2000-02-24) figures 2,3,4,6 page 12, line 9 - page 13, line 22 page 17, line 27 - page 18, line 20 -----	1-14

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
14 September 2016	22/09/2016

Name and mailing address of the ISA/	Authorized officer
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2016/050211

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		US 6337799 B1	08-01-2002
		WO 0010243 A1	24-02-2000