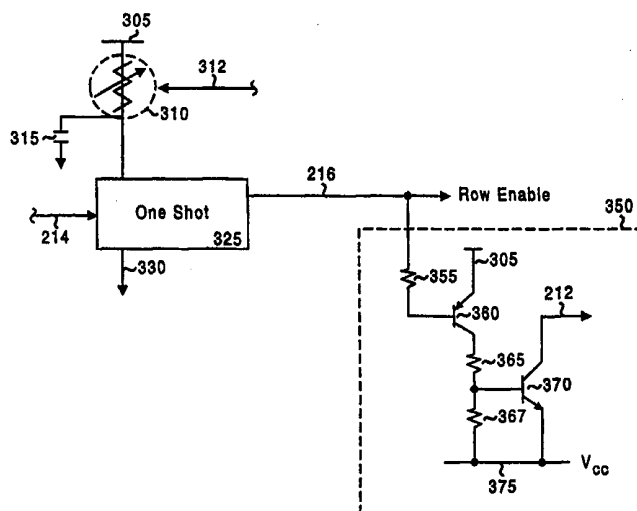




INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶ : G09G 3/22	A1	(11) International Publication Number: WO 99/12148 (43) International Publication Date: 11 March 1999 (11.03.99)
(21) International Application Number: PCT/US98/08540 (22) International Filing Date: 27 April 1998 (27.04.98) (30) Priority Data: 08/920,675 29 August 1997 (29.08.97) US (71) Applicant: CANDESCENT TECHNOLOGIES CORPORATION [US/US]; 6580 Via Del Oro, San Jose, CA 95119 (US). (72) Inventor: HANSEN, Ronald, L.; 10941 Miguelito Road, San Jose, CA 95127 (US). (74) Agents: GALLENSON, Mavis, S. et al.; Ladas & Parry, Suite 2100, 5670 Wilshire Boulevard, Los Angeles, CA 90036-5679 (US).		(81) Designated States: JP, KR, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published <i>With international search report.</i>

(54) Title: CIRCUIT AND METHOD FOR CONTROLLING THE BRIGHTNESS OF AN FED DEVICE IN RESPONSE TO A LIGHT SENSOR



(57) Abstract

A circuit and method for controlling the brightness of a display screen implemented using a field emission display (FED) screen (200). In an automatic brightness adjustment embodiment, an ambient light sensor (580) supplies the brightness signal that changes in proportion to the light sensed. The FED screen brightness is increased in response to increases in the light sensor output and decreased in response to decreases in the light sensor output. Another embodiment uses the light sensor (580) for brightness normalization where the FED screen (200) is used as the reference light level and the FED screen brightness is compensated for due to variations caused by age and manufacturing differences. A manual brightness adjustment (override) and automatic brightness on/off switch are also provided.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	ES	Spain	LS	Lesotho	SI	Slovenia
AM	Armenia	FI	Finland	LT	Lithuania	SK	Slovakia
AT	Austria	FR	France	LU	Luxembourg	SN	Senegal
AU	Australia	GA	Gabon	LV	Latvia	SZ	Swaziland
AZ	Azerbaijan	GB	United Kingdom	MC	Monaco	TD	Chad
BA	Bosnia and Herzegovina	GE	Georgia	MD	Republic of Moldova	TG	Togo
BB	Barbados	GH	Ghana	MG	Madagascar	TJ	Tajikistan
BE	Belgium	GN	Guinea	MK	The former Yugoslav Republic of Macedonia	TM	Turkmenistan
BF	Burkina Faso	GR	Greece	ML	Mali	TR	Turkey
BG	Bulgaria	HU	Hungary	MN	Mongolia	TT	Trinidad and Tobago
BJ	Benin	IE	Ireland	MR	Mauritania	UA	Ukraine
BR	Brazil	IL	Israel	MW	Malawi	UG	Uganda
BY	Belarus	IS	Iceland	MX	Mexico	US	United States of America
CA	Canada	IT	Italy	NE	Niger	UZ	Uzbekistan
CF	Central African Republic	JP	Japan	NL	Netherlands	VN	Viet Nam
CG	Congo	KE	Kenya	NO	Norway	YU	Yugoslavia
CH	Switzerland	KG	Kyrgyzstan	NZ	New Zealand	ZW	Zimbabwe
CI	Côte d'Ivoire	KP	Democratic People's Republic of Korea	PL	Poland		
CM	Cameroon	KR	Republic of Korea	PT	Portugal		
CN	China	KZ	Kazakstan	RO	Romania		
CU	Cuba	LC	Saint Lucia	RU	Russian Federation		
CZ	Czech Republic	LI	Liechtenstein	SD	Sudan		
DE	Germany	LK	Sri Lanka	SE	Sweden		
DK	Denmark	LR	Liberia	SG	Singapore		
EE	Estonia						

**CIRCUIT AND METHOD FOR CONTROLLING THE BRIGHTNESS OF
AN FED DEVICE IN RESPONSE TO A LIGHT SENSOR**

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates to the field of flat panel display screens. More specifically, the present invention relates to the field of flat panel field emission displays (FEDs).

RELATED ART

In the field of flat panel display devices, it is often necessary to adjust the brightness of the display screen. Active matrix liquid crystal devices (AMLCDs) typically contain one or more backlighting lamps that project light through the active matrix of liquid crystal cells. The brightness adjustment of AMLCD devices alters the gray-scale resolution of the pixels. These flat panel display screens alter the brightness of the display by controlling the electrical drive to, and hence the intensity of, the backlighting lamp. However, by its nature, the color and the uniformity produced by an AMLCD device degrade as the backlighting lamp is moved away from an optimum brightness point. The optimum brightness point is typically factory set. By altering the gray-scale resolution of the pixels when performing brightness adjustment, this prior art method of altering the brightness of a flat panel display has the unfortunate side effect of degrading the quality of the displayed image. It is desirable to provide a brightness adjustment for a flat panel display screen that does not compromise the gray-

scale quality of the pixels.

In another prior art mechanism for altering the brightness of an AMLCD, the image data used to render an image on the screen is altered as it is fed to the display. A function composed of a gain and an offset value is programmed into the display and all image data is then passed through the function which multiplies the data by the gain value and then adds the programmed offset value. The values of the above function are then altered as the brightness needs to be increased or decreased. This prior art mechanism for altering screen brightness is disadvantageous because it requires relatively complex circuitry for altering the large volume of image data. Secondly, this prior art mechanism degrades the gray-scale quality of the image by altering the gray-scale resolution of the flat panel display. It is desirable to provide a brightness adjustment for a flat panel display screen that does not alter the image data nor compromise the gray-scale resolution of the image.

Flat panel field emission displays (FEDs) do not use backlighting lamps. Flat panel FEDs utilize emitters each having an anode and a cathode and a gate. The voltage applied across an individual emitter (gate to cathode) causes it to release electrons toward a phosphor spot located on a display screen. Many emitters are associated with a single phosphor spot. A pixel is composed of three (e.g., red, green and blue) independently controlled phosphor spots. The gray-scale content of a pixel within a flat panel FED screen is represented by the voltages applied to the red, green and blue emitters that constitute the pixel. However, a brightness adjustment mechanism

that alters the relative voltages applied to the emitters of the red, green and blue phosphor spots will vary the gray-scale quality of the pixels within a flat panel FED screen. It is desirable to provide a brightness adjustment for a flat panel FED screen that does not compromise the gray-scale resolution of the pixels.

One prior art mechanism for altering the brightness of an FED alters the high voltage (e.g., several kilovolts) applied to the emitter's anode. This method is disadvantageous because it requires a variable output high voltage power supply which is more complex and hence more expensive than a constant voltage output power supply. Secondly, this prior art mechanism requires that the brightness adjustment circuitry be implemented with high voltage components rather than less expensive, simpler low voltage components. It is desirable to provide a brightness adjustment for a flat panel FED screen that does not require altering high voltage levels nor that requires high voltage components.

Accordingly, the present invention provides a mechanism and method for controlling the brightness of a flat panel display screen that does not compromise the gray-scale resolution of the pixels of the display screen and that is responsive to a light sensor. The present invention also provides a mechanism for altering the brightness of a flat panel display screen that does not alter the image data. Further, the present invention provides a mechanism and method for controlling the brightness of a flat panel FED screen that does not compromise the gray-scale resolution of the pixels of the display screen. The

present invention provides a brightness adjustment mechanism and method for a flat panel FED screen that alters low voltage control signals. These and other advantages of the present invention not specifically mentioned above will become clear within discussions of the present invention presented herein.

SUMMARY OF THE INVENTION

A circuit and method are described herein for controlling the brightness of a display screen implemented using a flat panel field emission display (FED) screen. Within the flat panel FED screen, a matrix of rows and columns is provided and emitters are situated within each row-column intersection. Rows are activated sequentially and separate gray scale information is presented to the columns. In one embodiment, rows are activated sequentially from the top most row down to the bottom row with only one row asserted at a time. When the proper voltage is applied across the cathode and gate of the emitters, they release electrons toward a phosphor spot, e.g., red, green, blue, causing an illumination point. Therefore, each pixel contains one red, one green and one blue phosphor spot.

In one embodiment, the present invention includes specialized circuitry common to all the row drivers for altering the applied voltage to the rows to cause a change in brightness cross the FED screen. The applied voltage can be pulse width modulated or amplitude modulated to alter the brightness of the flat panel FED screen. Because the relative column voltages remain constant within this embodiment of the present invention, gray scale resolution is not compromised as brightness is

altered. In one embodiment, the enable lines of the row drivers are turned on and off to modulate the pulse width ("on-time") of the row voltage. In a second embodiment, the row driver power supply is interrupted to modulate the pulse width ("on-time") of the row voltage. Within one implementation, it is more efficient to alter the row voltage than the column voltage. This is the case because there is no increase in CV^2 loss with row modulation. However, an alternative embodiment of the present invention includes circuitry for varying the column voltage in amplitude or pulse width to alter the brightness of the FED screen.

The brightness circuitry of the present invention can be made responsive to a manual brightness control or can be made responsive to an ambient light sensor positioned near the flat panel FED screen. In an automatic brightness adjustment embodiment of the present invention, a light sensor supplies the brightness signal that changes in proportion to the ambient light sensed. Using the above mechanisms and methods, the FED screen brightness is increased in response to increases in the light sensor output and decreased in response to decreases in the light sensor output. Another embodiment uses the light sensor for brightness normalization where the FED screen is used as the reference light level and the FED screen brightness is compensated for due to variations caused by age and manufacturing differences. A manual brightness adjustment (override) and automatic brightness on/off switch are also provided.

Specifically, embodiments of the present invention include a display system comprising: a light sensor for generating an

output signal proportional to an amount of sensed light; a manual brightness adjustment device; a reference circuit for generating a reference signal, the reference signal responsive to the manual brightness adjustment device; a converter circuit coupled to receive the output signal and the reference signal and for generating a brightness signal indicating a brightness level; a brightness control circuit coupled to receive the brightness signal and for generating a row on-time pulse having a width that is proportional to the brightness signal; and a field emission display screen having rows and column lines coupled, respectively, to row and column drivers, the row drivers coupled to receive the row on-time pulse and wherein the field emission display screen automatically varies in brightness in proportion to the width of the row on-time pulse.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross section structural view of part of a flat panel FED screen that utilizes a gated field emitter situated at the intersection of a row and a column line.

Figure 2 is a plan view of internal portions of the flat panel FED screen of the present invention and illustrates several intersecting rows and columns of the display.

Figure 3 illustrates a plan view of an flat panel FED screen in accordance with the present invention illustrating row and column drivers and numerous intersecting rows and columns.

Figure 4 is a circuit schematic illustrating circuitry utilized by the present invention for altering the brightness of the flat panel FED screen of the present invention.

Figure 5 illustrates timing diagrams of the signals produced by the circuit of Figure 4 and used by the row drivers of the flat panel FED screen of Figure 3.

Figure 6 is an illustration of brightness controlled column drivers of the flat panel FED screen of the present invention.

Figure 7 is a perspective view of a computer system utilizing an ambient light sensor in accordance with one embodiment of the present invention.

Figure 8 is a block diagram of circuitry of a general purpose computer system including an FED screen of the present invention having an ambient light sensor.

Figure 9 is a logical block diagram of a circuit of the present invention for utilizing an ambient light sensor for automatically adjusting the brightness of an flat panel FED screen.

Figure 10 is a logical block diagram of a circuit of the present invention utilizing an ambient light sensor and feed-back for automatically adjust the brightness of a flat panel FED screen for brightness normalizing.

DETAILED DESCRIPTION OF THE INVENTION

In the following detailed description of the present invention, a method and mechanism to alter the brightness of a flat panel FED screen without altering the gray-scale content of the display pixels, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be recognized by one skilled in the art that the present invention may be practiced without these

specific details or with equivalents thereof. In other instances, well known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention.

A discussion of an emitter of a field emission display (FED) is presented. Figure 1 illustrates a multi-layer structure 75 which is a portion of an FED flat panel display. The multi-layer structure 75 contains a field-emission backplate structure 45, also called a baseplate structure, and an electron-receiving faceplate structure 70. An image is generated by faceplate structure 70. Backplate structure 45 commonly consists of an electrically insulating backplate 65, an emitter (or cathode) electrode 60, an electrically insulating layer 55, a patterned gate electrode 50, and a conical electron-emissive element 40 situated in an aperture through insulating layer 55. One type of electron-emissive element 40 is described in United States Patent Number 5,608,283, issued on March 4, 1997 to Twichell et al. and another type is described in United States Patent Number 5,607,335, issued on March 4, 1997 to Spindt et al., which are both incorporated herein by reference. The tip of the electron-emissive element 40 is exposed through a corresponding opening in gate electrode 50. Emitter electrode 60 and electron-emissive element 40 together constitute a cathode of the illustrated portion 75 of the FED flat panel display 75. Faceplate structure 70 is formed with an electrically insulating faceplate 15, an anode 20, and a coating of phosphors 25. Electrons emitted from element 40 are received by phosphors portion 30.

Anode 20 of Figure 1 is maintained at a positive voltage

relative to cathode 60/40. The anode voltage is 100-300 volts for spacing of 100-200 um between structures 45 and 70 but in other embodiments with greater spacing the anode voltage is in the kilovolt range. Because anode 20 is in contact with phosphors 25, the anode voltage is also impressed on phosphors 25. When a suitable gate voltage is applied to gate electrode 50, electrons are emitted from electron-emissive element 40 at various values of off-normal emission angle θ 42. The emitted electrons follow non-linear (e.g., parabolic) trajectories indicated by lines 35 in Figure 1 and impact on a target portion 30 of the phosphors 25. The phosphors struck by the emitted electrons produce light of a selected color and represent a phosphor spot. A single phosphor spot can be illuminated by thousands of emitters.

Phosphors 25 are part of a picture element ("pixel") that contains other phosphors (not shown) which emit light of different color than that produced by phosphors 25. Typically a pixel contains three phosphor spots, a red spot, a green spot and a blue spot. Also, the pixel containing phosphors 25 adjoins one or more other pixels (not shown) in the FED flat panel display. If some of the electrons intended for phosphors 25 consistently strike other phosphors (in the same or another pixels), the image resolution and color purity can become degraded. As discussed in more detail below, the pixels of an FED flat panel screen are arranged in a matrix form including columns and rows. In one implementation, a pixel is composed of three phosphor spots aligned in the same row, but having three separate columns. Therefore, a single pixel is uniquely

identified by one row and three separate columns (a red column, a green column and a blue column).

The size of target phosphor portion 30 depends on the applied voltages and geometric and dimensional characteristics of the FED flat panel display 75. Increasing the anode/phosphor voltage to 1,500 to 10,000 volts in the FED flat panel display 75 of Figure 1 requires that the spacing between the backplate structure 45 and the faceplate structure 70 be much greater than 100-200 μm . Increasing the interstructure spacing to the value needed for a phosphor potential of 1,500 to 10,000 causes a larger phosphor portion 30, unless electron focusing elements (e.g., gated field emission structures) are added to the FED flat panel display of Figure 1. Such focusing elements can be included within FED flat panel display structure 75 and are described in United States Patent Number 5,528,103 issued on June 18, 1996 to Spindt, et al., which is incorporated herein by reference.

Importantly, the brightness of the target phosphor portion 30 depends on the voltage potential applied across the cathode 60/40 and the gate 50. The larger the voltage potential, the brighter the target phosphor portion 30. Secondly, the brightness of the target phosphor portion 30 depends on the amount of time a voltage is applied across the cathode 40/60 and the gate 50 (e.g., on-time window). The larger the on-time window, the brighter the target phosphor portion 30. Therefore, within the present invention, the brightness of FED flat panel structure 75 is dependent on the voltage and the amount of time (e.g., "on-time") the voltage is applied across cathode 60/40 and

the gate 50.

As shown in Figure 2, the FED flat panel display is subdivided into an array of horizontally aligned rows and vertically aligned columns of pixels. A portion 100 of this array is shown in Figure 2. The boundaries of a respective pixel 125 are indicated by dashed lines. Three separate emitter lines 230 are shown. Each emitter line 230 is a row electrode for one of the rows of pixels in the array. The middle row electrode 230 is coupled to the emitter cathodes 60/40 (Figure 1) of each emitter of the particular row associated with the electrode. A portion of one pixel row is indicated in Figure 2 and is situated between a pair of adjacent spacer walls 135. A pixel row is comprised of all of the pixels along one row line 250. Two or more pixels rows (and as much as 24-100 pixel rows), are generally located between each pair of adjacent spacer walls 135. Each column of pixels has three gate lines 250: (1) one for red; (2) a second for green; and (3) a third for blue. Likewise, each pixel column includes one of each phosphor stripes (red, green, blue), three stripes total. Each of the gate lines 250 is coupled to the gate 50 (Figure 1) of each emitter structure of the associated column. This structure 100 is described in more detail in United States Patent Number 5,477,105 issued on December 19, 1995 to Curtin, et al., which is incorporated herein by reference.

The red, green and blue phosphor stripes 25 are maintained at a positive voltage of 1,500 to 10,000 volts relative to the voltage of the emitter-electrode 60/40. When one of the sets of electron-emission elements 40 is suitably excited by adjusting

the voltage of the corresponding row (cathode) lines 230 and column (gate) lines 250, elements 40 in that set emit electrons which are accelerated toward a target portion 30 of the phosphors in the corresponding color. The excited phosphors then emit light. During a screen frame refresh cycle (performed at a rate of approximately 60 Hz in one embodiment), only one row is active at a time and the column lines are energized to illuminate the one row of pixels for the on-time period. This is performed sequentially in time, row by row, until all pixel rows have been illuminated to display the frame. Frames are presented at 60 Hz. Assuming n rows of the display array, each row is energized at a rate of $16.7/n$ ms. The above FED 100 is described in more detail in the following United States Patents: US Patent No. 5,541,473 issued on July 30, 1996 to Duboc, Jr. et al.; US Patent No. 5,559,389 issued on September 24, 1996 to Spindt et al.; US Patent No. 5,564,959 issued on October 15, 1996 to Spindt et al.; and US Patent No. 5,578,899 issued November 26, 1996 to Haven et al., which are incorporated herein by reference.

Figure 3 illustrates an FED flat panel display screen 200 in accordance with the present invention. Region 100, as described with respect to Figure 2, is also shown in Figure 3. The FED flat panel display screen 200 consists of n row lines (horizontal) and x column lines (vertical). For clarity, a row line is called a "row" and a column line is called a "column." Row lines are driven by row driver circuits 220a-220c. Shown in Figure 3 are row groups 230a, 230b and 230c. Each row group is associated with a particular row driver circuit; three row driver circuits are shown 220a-220c. In one embodiment of the present

invention there are over 400 rows and approximately 5-10 row driver circuits. However, it is appreciated that the present invention is equally well suited to an FED flat panel display screen having any number of rows. Also shown in Figure 3 are column groups 250a, 250b, 250c and 250d. In one embodiment of the present invention there are over 1920 columns. However, it is appreciated that the present invention is equally well suited to an FED flat panel display screen having any number of columns. A pixel requires three columns (red, green, blue), therefore, 1920 columns provides at least 640 pixel resolution horizontally.

Row driver circuits 220a-220c are placed along the periphery of the FED flat panel display screen 200. In Figure 3, only three row drivers are shown for clarity. Each row driver 220a-220c is responsible for driving a group of rows. For instance, row driver 220a drives rows 230a, row driver 220b drives rows 230b and row driver 220c drives rows 230c. Although an individual row driver is responsible for driving a group of rows, only one row is active at a time across the entire FED flat panel display screen 200. Therefore, an individual row driver drives at most one row line at a time, and when the active row line is not in its group during a refresh cycle it is not driving any row line. A supply voltage line 212 is coupled in parallel to all row drivers 220a-220c and supplies the row drivers with a driving voltage for application to the cathode 60/40 of the emitters. In one embodiment, the row driving voltage is negative in polarity.

An enable signal is also supplied to each row driver 220a-220c in parallel over enable line 216 of Figure 3. When the

enable line 216 is low, all row drivers 220a-220c of FED screen 200 are disabled and no row is energized. When the enable line 216 is high, the row drivers 220a-220c are enabled.

A horizontal clock signal is also supplied to each row driver 220a-220c in parallel over clock line 214 of Figure 3. The horizontal clock signal or synchronization signal pulses upon each time a new row is to be energized. The n rows of a frame are energized, one at a time, to form a frame of data. Assuming an exemplary frame update rate of 60 Hz, all rows are updated once every 16.67 milliseconds. Assuming n rows per frame update, the horizontal clock signal pulses once every $16.67/n$ milliseconds. In other words a new row is energized every $16.67/n$ milliseconds. If n is 400, the horizontal clock signal pulses once every 41.67 microseconds.

All row drivers of FED 200 are configured to implement one large serial shift register having n bits of storage, one bit per row. Row data is shifted through these row drivers using a row data line 212 that is coupled to the row drivers 220a-220c in serial fashion. During sequential frame update mode, all but one of the bits of the n bits within the row drivers contain a "0" and the other one contains a "1". Therefore, the "1" is shifted serially through all n rows, one at a time, from the upper most row to the bottom most row. Upon a given horizontal clock signal pulse, the row corresponding to the "1" is then driven for the on-time window. The bits of the shift registers are shifted through the row drivers 220a-220c once every pulse of the horizontal clock as provided by line 214. In interlace mode, the odd rows are updated in series followed by the even rows. A

different bit pattern and clocking scheme is therefore used.

The row corresponding to the shifted "1" becomes driven responsive to the horizontal clock pulse over line 214. The row remains on during a particular "on-time" window. During this on-time window, the corresponding row is driven with the voltage value as seen over voltage supply line 212 if the row drivers are enabled. During the on-time window, the other rows are not driven with any voltage. As discussed more fully below, the present invention varies the size of the on-time window to alter the brightness of the FED flat panel display screen 200 of Figure 3. To increase the brightness, the on-time window is expanded. To decrease the brightness, the on-time window is decreased. Since the relative voltage amplitudes are not altered on the column drivers, the present invention does not degrade gray-scale resolution by altering brightness in the above fashion. Alternatively, in another embodiment, the present invention alters the amplitude of the voltage value applied to line 212 to alter the brightness of the FED screen 200 of Figure 3. In one embodiment, the rows are energized with a negative voltage.

As shown by Figure 3, there are three columns per pixel within the FED flat panel display screen 200 of the present invention. Column lines 250a control one column of pixels, column lines 250c control another column line of pixels, etc. Figure 3 also illustrates the column drivers 240 that control the gray-scale information for each pixel. The column drivers 240 drive amplitude modulated voltage signals over the column lines. In an analogous fashion to the row driver circuits, the column drivers 240 can be broken into separate circuits that each drive

groups of column lines. The amplitude modulated voltage signals driven over the column lines 250a-250e represent gray-scale data for a respective row of pixels. Once every pulse of the horizontal clock signal at line 214, the column drivers 240 receive gray-scale data to independently control all of the column lines 250a-250e of a pixel row of the FED flat panel display screen 200. Therefore, while only one row is energized per horizontal clock, all columns 250a-250e are energized during the on-time window. The horizontal clock signal over line 214 synchronizes the loading of a pixel row of gray-scale data into the column drivers 240. Column drivers 240 receive column data over column data line 205 and column drivers 240 are also coupled in common to a column voltage supply line 207.

Different voltages are applied to the column lines by the column drivers 240 to realize different gray-scale colors. In operation, all column lines are driven with gray-scale data (over column data line 205) and simultaneously one row is activated. This causes a row of pixels of illuminate with the proper gray-scale data. This is then repeated for another row, etc., once per pulse of the horizontal clock signal of line 214, until the entire frame is filled. To increase speed, while one row is being energized, the gray-scale data for the next pixel row is simultaneously loaded into the column drivers 240. Like the row drivers, 220a-220c the column drivers assert their voltages within the on-time window. Further, like the row drivers 220a-220c, the column drivers 240 have an enable line. In one embodiment, the columns are energized with a positive voltage.

BRIGHTNESS CONTROL CIRCUITRY

Figure 4 illustrates brightness control circuitry 300 utilized by embodiments of the present invention for adjusting the brightness of the FED flat panel display screen 200 of Figure 3. This brightness control circuitry 300 can be situated adjacent to the row drivers 220a-220c and column drivers 240 of FED flat panel display screen 200. In a first embodiment of the present invention, the display average brightness is controlled by pulse width modulating the row voltage. The present invention utilizes pulse width modulation of the supply voltage to the row drivers 220a-220c, e.g., modulating the on-time window of the row drivers 220a-220c. In this first embodiment, the gray-scale generation is controlled by amplitude modulation of the column drivers 240, e.g., by controlling the magnitude of the column driver voltages. In this case, the average brightness is linearly proportional to the row on-time window.

As the brightness is to be increased, the row on-time window is increased and as the brightness is to be decreased, the row on-time window is decreased. An advantage of this type of brightness control is that the gray-scale resolution of the pixels of the FED screen 200 is not degraded as the on-time window is varied. This is the case because in this first embodiment of the present invention, neither the column data nor the column driver output voltages are altered.

Brightness control circuitry 300 of Figure 4 includes a one shot circuit 325 coupled to a resistor and capacitor network (RC network) consisting of a voltage controlled resistor 310 and a capacitor 315. Line 330 is tied to ground or -Vcc. In

accordance with the present invention, the one shot circuit 325 determines the length of the on-time period of the row drivers 220a-220c (Figure 3). Therefore, within the present invention, the on-time period of the row drivers 220a-220c is variable and depends on the desired brightness of the FED flat panel display screen 200. The resistance of the voltage controlled resistor 310 varies depending on the voltage over line 312 which carries a brightness signal. The voltage over line 312 varies and represents a brightness signal which is a setting indicative of the desired brightness of the FED flat panel display screen 200. The voltage over line 312 can be controlled as a result of a manual knob made user-assessable or from a circuit that performs automatic compensation or normalization (described further below). Alternatively, the voltage over line 312 can be a result of a mixture of manual and automatic origin. One end of the voltage controlled resistor 310 is coupled at node 305 to a logical level (e.g., 3.3 or 5 volts DC).

In this configuration, the RC network of Figure 4 determines the pulse width of the one shot circuit 325 using well known mechanisms. In one embodiment, the output 216 of the one shot circuit 325 is low when active and high otherwise. Therefore, the on-time window as determined by the one shot circuit 325 is measured by its low output value in this embodiment. Also, the one shot circuit 325 is coupled to receive the horizontal synchronization pulse over line 214. Therefore, the length of the on-time window is determined by the RC network and it starts in synchronization with the horizontal clock signal received over line 214. The output of the one shot circuit 325 is coupled to

drive the row enable line 216. In the first embodiment of the present invention, the circuitry 350 is not used and line 212 is directly coupled to the row driving voltage source, -Vcc 375.

Because the row driver circuits 220a-220c (Figure 3) are enabled low, when the one shot 325 generates its low signal over line 216 to define the on-time window, all row driver circuits 220a-220c of Figure 3 are enabled. However, only one row driver circuit will contain the "1" in the serial shift register. Therefore, for each pulse of the horizontal synchronization clock signal, one on-time pulse is generated to enable the row driver circuits 220a-220c for its duration.

Figure 5 illustrates a timing diagram of signals used in accordance with the present invention. Signals 410, 415 and 440 are transistor-transistor level (TTL) logic signals. Signal 410 illustrates the vertical synchronization signal and each pulse 410a indicates the start of a new frame. Generally, frames are presented at 60 Hz. In non-interlaced refresh mode, pulse 410a indicates that the first row of FED 200 is ready to be energized. Signal train 415 represents the horizontal synchronization clock signal and pulses 415a-415c represent the start timing for energizing (e.g., refreshing) the first three exemplary row lines. Each pulse of 415a-415c indicates that a new row is to be energized (e.g., a new row of pixels are refreshed). In non-interlaced refresh mode, pulses 415a, 415b and 415c correspond to the start of energizing of row one, row two and row three, respectively, of the rows of the FED flat panel display screen 200 (Figure 3).

With reference to Figure 5, signal 440 represents the row

enable signal generated by the one shot circuit 325 and transmitted over line 216 (Figure 4) for the first three exemplary rows. Low asserted variable length pulses 440a-440c represent the on-time windows for all the row drivers 220a-220c. Variable length on-time window pulses 440a-440c correspond, respectively, to the horizontal row synchronization clock pulses 415a-415c. During each variable length on-time window 440a-440c, only one row line of FED flat panel display screen 200 is active, as shown by the signals 420, 425 and 430. Signals 420, 425 and 430 correspond to the voltages seen over the three exemplary row lines. Driving voltage signal 420 corresponds to the first row, driving voltage signal 425 corresponds to the second row, and driving voltage signal 430 corresponds to the third row.

The dashed lines within signal 440 indicate that the on-time window is variable in pulse width depending on the value of the RC network of the one shot circuit 325. For instance, signal 420 illustrates the voltage applied to an exemplary row line that is to be energized in synchronization with enable pulse 440a. Pulse 420a is the on-time window. The absolute maximum length of the on-time window can be the length of time between pulses of signal 415, e.g., from pulse 415a to pulse 415b, but can be arbitrarily set to a value less than this amount. In the example of Figure 5, the maximum length of pulse 420a is arbitrarily set to about half of the period between pulses of signal 415. This on-time window (pulse 420a) is variable as indicated by the different periods 2, 4, 6, 8, and 10 of Figure 5. Brightness magnitude is linearly related to the length of the on-time window within the present invention. Therefore, period 10 (in this example)

represents the full application of $-V_{cc}$ to the exemplary row and corresponds to the maximum brightness of the FED flat panel display screen 200. Period 8 represents $6/7$ of the full $-V_{cc}$ application and represents an amount $6/7$ of the full brightness. Period 6 represents $5/7$ of the full $-V_{cc}$ application and represents an amount $5/7$ of the full brightness. Lastly, Period 2 represents $3/7$ of the full $-V_{cc}$ application and represents an amount $3/7$ of the full brightness. It is appreciated that only one period, of periods 2-10, is selected per on-time pulse and that periods 2-10 of Figure 5 are all shown as an example of the possible brightness levels of this embodiment of the present invention. It is appreciated further that in other examples, the maximum on-time window 420a can be increased to the entire period between pulses of signal 415.

As the brightness is to be increased, a signal over line 312 (Figure 4) alters the RC network of the one shot circuit 325 such that pulse width of pulse 420a increases in size from a minimum pulse width 2. Alternatively, as the brightness is to be decreased, a signal over line 312 (Figure 4) alters the RC network of the one shot circuit 325 such that pulse width of pulse 420a decreased in size from a maximum of pulse width 10. The same is true for the pulses 425a and 430a. Therefore, the particular pulse width (e.g., of the on-time window) of pulses 420a, 425a and 430a depends on the value of the voltage controlled resistor 310 of Figure 4 which is controlled by the brightness signal over line 312.

Figure 5 also illustrates signals 425 and 430 corresponding to two other exemplary row lines that are energized in

synchronization with enable pulses 440b and 440c, respectively. Similar to pulse 420a, the pulse widths of pulses 425a and 430a are variable and depend on the pulse width of enable pulses 440b and 440c, respectively. For non-interlaced refresh mode, the row lines corresponding to pulses 420a, 425a and 430a are adjacent to each other on the FED flat panel display screen 200.

With reference to Figure 4, a second embodiment of the present invention is provided that is applicable in cases where the row driver circuits 220a-220c of Figure 3 do not have enable lines. In this second embodiment, circuit 250 of Figure 4 is used, in conjunction with one shot circuit 325, to interrupt the voltage supplied over the voltage supply line 212 that feeds the row drivers 220a-220c. In circuit 350, the TTL row enable signal 216 is coupled to a resistor 355 and used to control the gate of transistor 360. In circuit 350, transistor 360 is coupled to a logic voltage level 305 and coupled to resistor 365 which is coupled in series to resistor 367 which is coupled to -Vcc or node 375. Voltage level -Vcc is the driving voltage level for the row lines of the FED flat panel display screen 200. The node between resistor 365 and resistor 367 is coupled to control the gate of transistor 370. Transistor 370 is coupled to node 375 (-Vcc) and also coupled to line 212. Therefore, in the second embodiment of the present invention, line 212 is not directly coupled to -Vcc 375.

When the row enable line 216 is low, transistor 360 turns on causing a voltage at the gate of transistor 370 which turns on transistor 370. This causes line 212 to be coupled to -Vcc through transistor 370. Under this condition, -Vcc is supplied

to all of the row drivers 220a-220c of the FED flat panel display screen 200. When the row enable line 216 is high, transistor 360 turns off causing transistor 370 to also turn off. This decouples line 212 from -Vcc. Under this condition, -Vcc is disconnected from the row drivers 220a-220c of the FED flat panel display screen 200.

Under the first embodiment of the present invention, the voltage, -Vcc, is constantly supplied to the row drivers 220a-220c, but the enable line 216 is controlled on and off to implement the proper on-time window. Under the second embodiment of the present invention, the voltage, -Vcc, is directly controlled on and off to implement the proper on-time window. It is appreciated that the signals shown in Figure 5 are equally applicable to the second embodiment of the present invention. In the second embodiment, however, the enable line 216 does not directly control the row drivers 220a-220c, as in the first embodiment, but controls the application of the supply voltage over line 212 to the row drivers 220a-220c.

Figure 6 illustrates a third embodiment of the present invention for adjusting the brightness of an FED flat panel display screen 200. With respect to the third embodiment of the present invention, the on-time window of the column drivers 240a-240c are adjusted and a constant on-time window is used for the row drivers 220a-220c. Figure 6 illustrates three exemplary column drivers 240a-240c of FED flat panel display screen 200 that drive exemplary columns 250f-250h, respectively. These three columns 250f-250h correspond to the red, green and blue lines of a column of pixels. Gray-scale information is supplied

over data bus 250 to the column drivers 240a-240c. The gray-scale information causes the column drivers to assert different voltage amplitudes (amplitude modulation) to realize the different gray-scale contents of the pixel. Different gray-scale data for a row of pixels are presented to the column drivers 240a-240c for each pulse of the horizontal clock signal.

Each column driver 240a-240c of Figure 6 also has an enable input that is coupled to enable line 510 which is supplied in parallel to each column driver 240a-240c. Further, each column driver 240a-240c is also coupled to a column voltage line 515 which carries the maximum column voltage. The column drivers 240a-240c also receive a column clock signal for clocking in the gray-scale data for a particular row of pixels. According to the third embodiment of the present invention, pulse width modulation is applied to the column drivers 240a-240c to implement brightness control. The longer the pulse width, the brighter the display in linear fashion. The shorter the pulse width, the darker the display.

Within this embodiment, a column enable signal is generated by circuitry analogous to that shown in Figure 4 and this column enable signal is coupled to column driver enable line 510. The column enable line 515 causes the on-time window for the column drivers 240a-240c to become variable, depending on the desired brightness of the FED flat panel display screen 200. In the third embodiment, the column drivers 240a-240c utilize voltage amplitude modulation to realize the gray-scale content, but also use pulse width modulation to vary the brightness of the FED flat panel display screen 200. The third embodiment of the present

invention does not degrade the gray-scale resolution of the image.

A fourth embodiment of the present invention is applicable for column drivers 240a-240c that do not have an enable input. In this case, a circuit is used analogous to circuit 350 of Figure 4 to interrupt, e.g., turn on and off, the maximum column voltage supplied over line 515 in synchronization with the column on-time. In effect, a circuit analogous to circuit 350 is used to couple and decouple the maximum column voltage, V_{cc} , from line 515 and is controlled from an enable line analogous to enable line 216.

It is appreciated that the first and second embodiments of the present invention consume less power than the third and fourth embodiments because pulse width modulation of the column drivers 240a-240c requires driving against the capacitance of all the columns simultaneously whereas pulse width modulation of the row drivers 220a-220c only drives against the capacitance of a single row at a time. This is the case because during refresh, only one row is on at a time, but all columns are on so that an entire row of pixels are energized. It is further appreciated that performing brightness control using pulse width modulation, rather than using amplitude modulation, is advantageous because it does not degrade the gray-scale resolution available to the FED flat panel display screen 200.

BRIGHTNESS SENSOR AND AUTOMATIC ADJUSTMENT

Figure 7 illustrates another embodiment of the present invention which includes an ambient light sensor 580 (Figure 8) integrated within a general purpose computer system 550 having the FED flat panel display screen 200 therein. An exemplary portable computer system 550 in accordance with the present invention includes a keyboard or other alphanumeric data entry device 565. Computer system 550 also includes a cursor directing device 570 (e.g., a mouse, roller ball, finger pad, track pad, etc.) for directing a cursor across the FED flat panel display screen 200. The exemplary computer system 550 shown in Figure 7 contains a base portion 590b and a retractable display portion 590a that optionally pivots about axis 572. The ambient light sensor 580 can be placed within a number of positions within the present invention and positions 580a and 580b are exemplary only. As described further below, for brightness normalization position 580b is advantageous and for automatic brightness adjustment position 580a is advantageous.

Refer to Figure 8 which illustrates a block diagram of elements of computer system 550. Computer system 550 contains an address/data bus 500 for communicating address and data information, one or more central processors 501 coupled to the bus 500 for processing information and instructions. Computer system 550 includes a computer readable volatile memory unit 502 (e.g., random access memory, static RAM, dynamic, RAM, etc.) coupled with the bus 500 for storing information and instructions for the central processor(s) 501 and a computer readable non-volatile memory unit (e.g., read only memory, programmable ROM,

flash memory, EPROM, EEPROM, etc.) 503 coupled with the bus 500 for storing static information and instructions for the processor(s) 501.

Computer system 550 of Figure 8 also includes a mass storage computer readable data storage device 504 such as a magnetic or optical disk and disk drive coupled with the bus 500 for storing information and instructions. The FED flat panel display screen 200 is coupled to bus 500 and alphanumeric input device 565, including alphanumeric and function keys, is coupled to the bus 500 for communicating information and command selections to the central processor(s) 501. Ambient light sensor 580 is coupled to FED flat panel display screen 200. Also coupled to FED flat panel display screen 200 is a manual brightness adjustment knob 520 and a switch 530 that controls whether or not automatic brightness adjustment features of the present invention are enabled or disabled. In one embodiment of the present invention, the manual brightness adjustment knob 520 directly controls the voltage level of the brightness signal of line 312 (Figure 3).

The cursor control device 570 of Figure 8 is coupled to the bus 500 for communicating user input information and command selections to the central processor(s) 501. Computer system 500 optionally includes a signal generating device 508 coupled to the bus 500 for communicating command selections to the processor(s) 501. Elements within 552 are generally internal to computer system 550.

The present invention utilizes the ambient light sensor 580 in two embodiments. In one embodiment, as the ambient light detected by the light sensor 580 increases, the brightness of the

FED screen 200 is automatically increased. Likewise, as the ambient light detected by the light sensor 580 decreases, the brightness of the FED screen 200 is automatically decreased to maintain image viewing quality. This is done to maintain image viewing quality in a setting where the ambient light intensity is changing over time or if the display is transported to different settings having different ambient light intensities. The average brightness of the FED screen 200 is adjusted according to the circuitry described with respect to Figure 4 herein. In this first embodiment, the manual adjustment knob 530 can be used as an override and allows the user to manually adjust the FED screen's brightness level.

In a second embodiment of the present invention that uses the light sensor 580, the sensor is used to provide brightness normalization for the FED screen 200 over the FED screen's useful lifetime. This embodiment is useful for brightness correcting of the FED screen 200 over age. In this case, the light sensor 580 is positioned such that it is exposed to a substantial amount of the FED screen's own light emission. As the light detected by the light sensor 580 falls below a predetermined threshold level, the average brightness of the FED screen 200 is increased. Likewise, as the light detected by the light sensor 580 rises above the predetermined threshold level, the average brightness of the FED screen 200 is decreased. Both of the above are performed in an attempt to bring the FED screen 200 to a factory preset brightness amount over the lifetime of the FED screen 200. In this embodiment, the average brightness of the FED screen 200 is adjusted according to the circuitry described with respect to

Figure 4 herein.

Figure 9 illustrates a block diagram of the first embodiment 600 of the present invention that utilizes the ambient light sensor 580 which is sensitive to ambient light 620. In this embodiment 600, it is advantageous that the light sensor 580 not receive a substantial amount of light from the FED screen 200 itself since the light sensor 580 is to receive and respond to the ambient light in the surroundings of computer system 550. In this case, the sensor 580 can be placed in position 580a (Figure 7) so that it is exposed to the ambient light but not substantially exposed to direct light from the FED screen 200.

A number of different ambient light sensors 580 can be used in accordance with the present invention. One well known line of light sensors is commercially available from Texas Instruments and another is commercially available from Burr-Brown. Light sensors 580 used in accordance with the present invention generate a variable output signal in response to and in proportion to the light detected. Depending on the light sensor used, the output signal 585 can vary in current amount, voltage amount, oscillation frequency, and in pulse width with a fixed frequency. Another type of light sensor 580 is passive and varies in resistance as the light is varied.

A comparison circuit 590 is used that receives a reference voltage signal 635 and also the output signal 585 of the sensor 580. The comparison circuit contains circuitry that generates the brightness voltage signal 312 in response to the values of signal 585 and 635. Using well known methods and components, the comparison circuit converts the sensor output signal 585 (e.g.,

variable current, variable frequency, variable pulse width, or variable voltage, etc.) into a converted variable voltage signal that varies in proportion to the amount of light received by sensor 580. Well known circuits and components are used at this stage. Within comparison circuit 590, if switch 530 is "OFF" then the sensor output signal 585 and the converted variable voltage signal are ignored by the comparison circuit 590. In this case, comparison circuit 590 outputs the reference voltage signal 635 over line 312. However, if switch 530 is "ON," then the converted variable voltage signal is then electrically added to the reference voltage level by the comparison circuit 590 to yield the brightness voltage signal the is output over line 312.

The reference voltage signal 635 of Figure 9 is generated by a reference circuit 630 that is coupled to the manual brightness adjustment knob 520. In one embodiment, the manual brightness adjustment knob 520 controls a potentiometer element within circuit 630 that alters the reference voltage 635. As the manual adjustment knob 520 is adjusted to increase brightness, the reference voltage 635 is increased and as the manual adjustment knob 520 is adjusted to decrease brightness, the reference voltage 635 is decreased by circuit 630. The brightness voltage signal 312 controls circuit 300 of Figure 9 as discussed above. In accordance with the present invention, circuit 300 can use pulse width modulation of the on-time window to control either the row drivers 220a-220c or the column drivers 240 to adjust the brightness of the FED flat panel display screen 200 as discussed in the embodiments above.

In operation, the embodiment 600 of Figure 9 performs as

follows. If switch 530 is OFF and knob 520 is adjusted for more brightness, then brightness voltage signal 312 increases in amplitude causing the on-time window of circuit 300 to increase. If switch 530 is OFF and knob 520 is adjusted for less brightness, then brightness voltage signal 312 decreases in amplitude causing the on-time window of circuit 300 to decrease. If switch 530 is ON and manual adjust 520 is constant, then brightness voltage signal 312 automatically increases in voltage in direct proportion to any increase in detected ambient light from the light sensor 580. If switch 530 is ON and manual adjust 520 is constant, then brightness voltage signal 312 automatically decreases in voltage in direct proportion to any decrease in detected ambient light 620 from the ambient light sensor 580.

Because the converted variable voltage of circuit 590 is added to the reference voltage signal 635, if switch 530 is ON and manual adjustment knob 520 is increased, the brightness voltage signal 312 increases assuming no change in ambient light 620. If switch 530 is ON and manual adjustment knob 520 is decreased, the brightness voltage signal 312 decreases assuming no change in ambient light 620. As discussed above, as the brightness signal 312 increases, the on-time window increases and the brightness of the FED screen 200 increases. Likewise, as the brightness signal 312 decreases, the on-time window decreases and the brightness of the FED screen 200 decreases.

Figure 10 illustrates a block diagram of the second embodiment 700 of the present invention that utilizes a light sensor 580 and this embodiment performs brightness normalization for FED screen 200. Brightness normalization samples the

brightness of the FED screen 200 and alters the brightness of the FED screen 200 if the sampled amount varies from a predetermined preferred level. This embodiment 700 is used to maintain the average brightness of the FED screen 200 over its useful life and also to compensate for variations in manufacturing and variations in the FED screen 200 that occur over time. In embodiment 700, it is advantageous that the light sensor 580 receive a substantial amount of light from the FED screen 200 itself as a reference source and not receive significant light from the ambient sources. In this case, the sensor 580 can be placed in position 580b (Figure 7) so that it is exposed to direct light emitted from the FED screen 200 but not substantially exposed to the ambient light.

In the system 700 of Figure 10, a negative feedback loop 730 exists between the light sensor 380 and the light emitted from flat panel FED screen 200. Therefore, the brightness control circuitry 300 adjusts the brightness at flat panel screen 200 automatically in response to the light detected by sensor 380. Also, reference circuit 630' also adjusts the reference voltage over line 635 in response to the manual adjustment knob 520. In the mode of operation where both manual adjustment and automatic screen normalization are active at the same time, manual adjustment has override priority. In operation, as the light sensor 580 detects brighter light emitted from the FED screen 200 that exceeds a factory set threshold, circuit 300 causes the on-time pulse width to decrease, thereby causing the FED screen 200 to become less bright. Likewise, as the light sensor 580 detects less bright light emitted from the FED screen 200 that is below

the factory set threshold, circuit 300 causes the on-time pulse width to increase, thereby causing the FED screen 200 to become brighter. Embodiment 700 also contains the full range of manual adjustment features as described with respect to embodiment 600. That is, increasing or decrease the reference voltage over line 635 also alters the brightness displayed on flat panel FED screen 200 in the manner described with reference to Figure 9.

System 700 is useful for automatically compensating for variations in the manufacturing of FED screens 200 and also for automatically compensating for FED screens 200 that become less bright over time as a result of age, frequency of use, prolonged use, temperature, etc. It is appreciated that the electronics required to implement system 600 and system 700 can be fabricated in the same support electronics that are used by FED screen 200 and typically situated along the periphery of the pixel array or behind the pixel array.

The preferred embodiment of the present invention, a method and mechanism to alter the brightness of an FED flat panel screen without altering the gray-scale content of the display pixels, is thus described. While the present invention has been described in particular embodiments, it should be appreciated that the present invention should not be construed as limited by such embodiments, but rather construed according to the below claims.

CLAIMS

What is claimed is:

1. A device comprising:

a light sensor generating an output signal proportional to sensed light;

a converter circuit for generating a brightness signal responsive to said output signal; and

a brightness control circuit coupled to receive said brightness signal, said brightness control circuit for generating a row on-time pulse having a width that is in proportion to said brightness signal and generated in synchronization with said horizontal synchronization clock signal.

2. The device of claim 1 wherein the device is a field emission display device further comprising:

a plurality of column drivers each coupled to a respective column line, said column drivers for driving amplitude modulated voltage signals over column lines;

a plurality of row drivers each coupled to a respective row line, said plurality of row drivers for driving a first voltage signal over one row line at a time, wherein a pixel is comprised of intersections of one row line and at least three column lines;

a horizontal synchronization clock signal for synchronizing the refresh of individual row lines, said brightness control circuit coupled to enable said plurality of row drivers and having a width that varies in proportion to said brightness

signal.

3. The device as described in Claim 2 further comprising:
a manual adjustment;

a reference circuit for generating a reference signal, said reference signal responsive to said manual adjustment; and

wherein said converter circuit is for generating a smaller brightness signal upon said light sensor sensing a larger amount of brightness from said field emission display device and wherein said converter circuit is for generating a larger brightness signal upon said light sensor sensing a smaller amount of brightness from said field emission display device.

4. The device of claim 1 wherein the device is a display system further comprising:

a manual brightness adjustment device;

a reference circuit for generating a reference signal, said reference signal responsive to said manual brightness adjustment device;

said converter circuit coupled to receive said output signal and said reference signal, said brightness signal indicating a brightness level; and

a field emission display screen having pixels at intersections of row and column lines which are coupled, respectively, to row and column drivers, said row drivers coupled to receive said row on-time pulse and wherein said pixels of said field emission display screen automatically vary in brightness in proportion to said width of said row on-time pulse.

5. The device of claim 1 wherein said device is coupled to a bus which is coupled to a processor and memory unit to form a computer system, said device being a display system further comprising a field emission display screen having pixels at intersections of row and column lines which are coupled, respectively, to row and column drivers, said row drivers coupled to receive said row on-time pulse and wherein said pixels of said field emission display screen automatically vary in brightness in proportion to said width of said row on-time pulse.

6. The device as described in Claim 1, 2, 4 or 5 wherein said converter circuit is for generating a larger brightness signal upon said light sensor sensing a larger amount of light and wherein said converter circuit is for generating a smaller brightness signal upon said light sensor sensing a smaller amount of light.

7. The device as described in Claim 4 wherein said converter circuit is for generating a larger brightness signal upon said light sensor sensing a larger amount of light and wherein said converter circuit is for generating a smaller brightness signal upon said light sensor sensing a smaller amount of light;

said field emission display screen further comprising a horizontal synchronization clock signal for synchronizing the refresh of individual row lines and wherein:

said column drivers are each coupled to a respective column line and are for driving amplitude modulated voltage signals over

said column lines;

said row drivers are each coupled to a respective row line and are for driving a first voltage signal over one row line at a time, wherein a pixel is comprised of intersections of one row line and at least three column lines; and

said plurality of row drivers are enabled by said row on-time pulse and wherein said row on-time pulse is generated in synchronization with said horizontal synchronization clock signal.

8. The device as described in Claim 6 or 7 further comprising a plurality of multi-layer structures situated at respective intersections of respective row lines and respective column lines, each multi-layer structure for illuminating at a brightness that is linearly proportional to said width of said row on-time pulse.

9. The device as described in Claim 8 wherein said brightness control circuit comprises:

a network comprising a voltage controlled resistor coupled to said brightness signal and a capacitor, said network for defining said width of said row on-time pulse; and

a one shot circuit coupled to said network and coupled to said horizontal synchronization clock signal for generating said row on-time pulse in synchronization with said horizontal synchronization clock signal.

10. The device as described in Claim 8 wherein there are

at least three column lines of a respective pixel which comprise a red column line, a green column line and a blue column line.

11. The device as described in Claim 8 wherein each multi-layer structure comprises:

a high voltage anode;

phosphors coated on said high voltage anode;

a gate coupled to a corresponding column line; and

a cathode comprising an electron-emissive element and an emitter electrode, said emitter electrode coupled to a corresponding row line wherein said electron-emissive element releases electrons into said phosphors upon said first voltage signal driven on said corresponding row line and a second voltage signal driven on said corresponding column line.

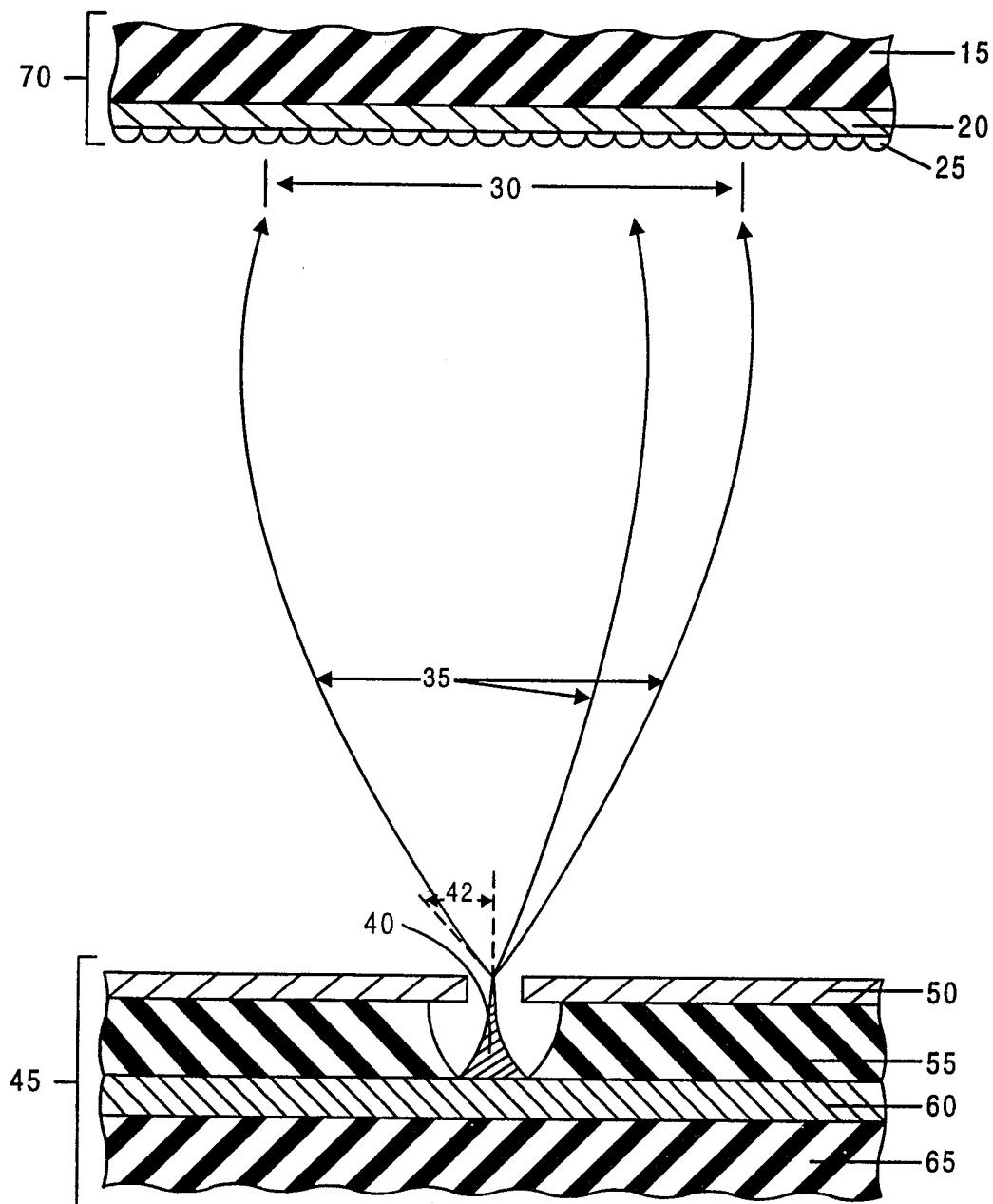
75

FIG. 1

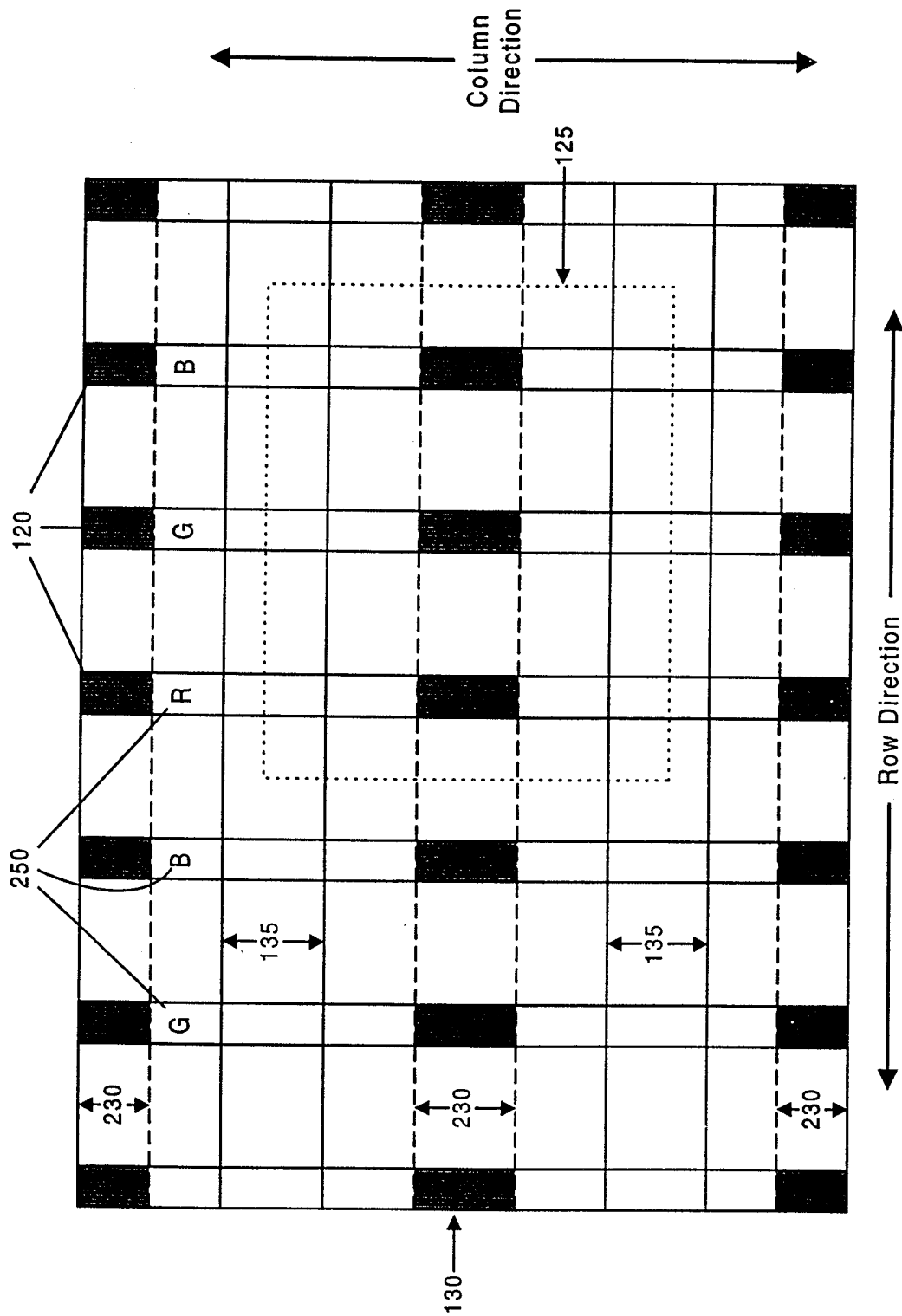


FIG. 2

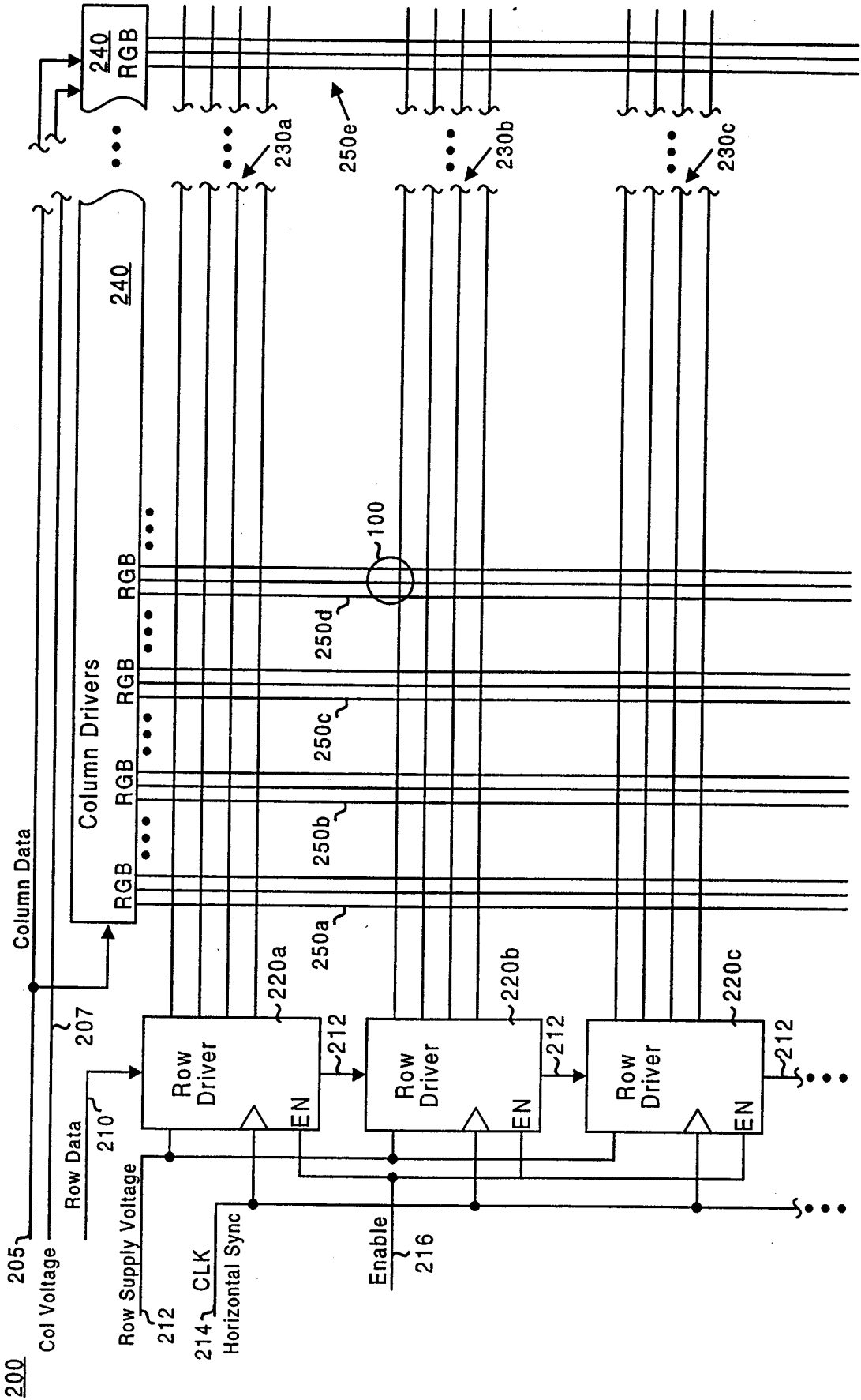


FIG. 3

300

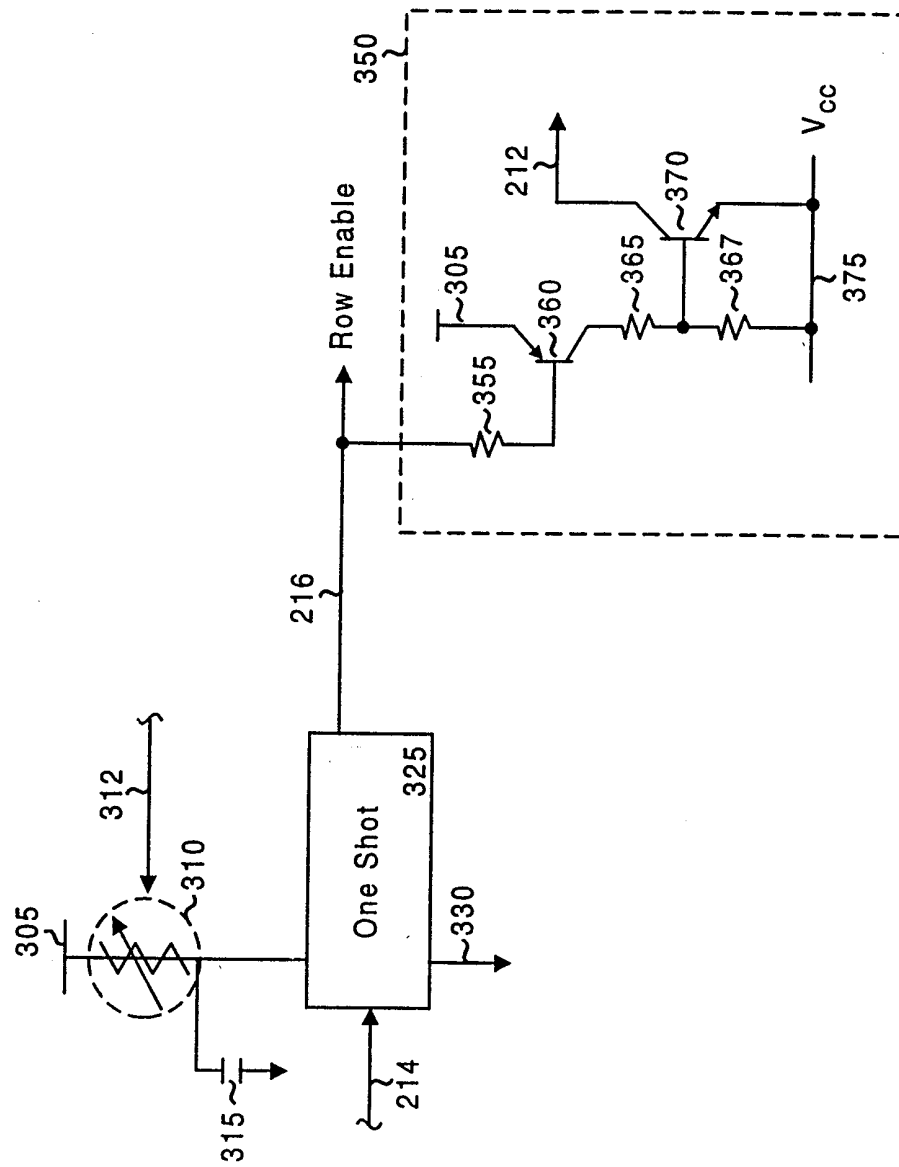


FIG. 4

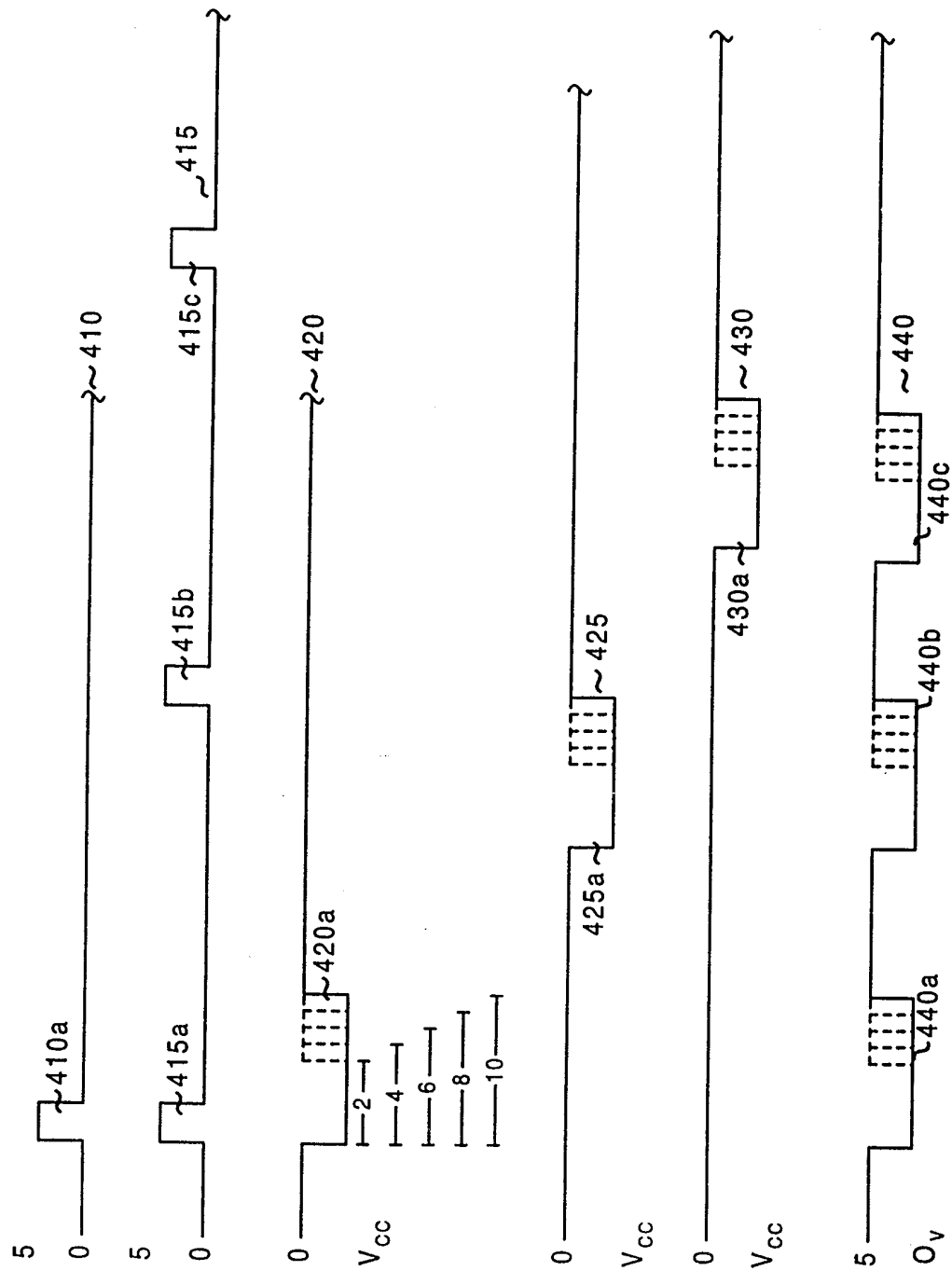


FIG. 5

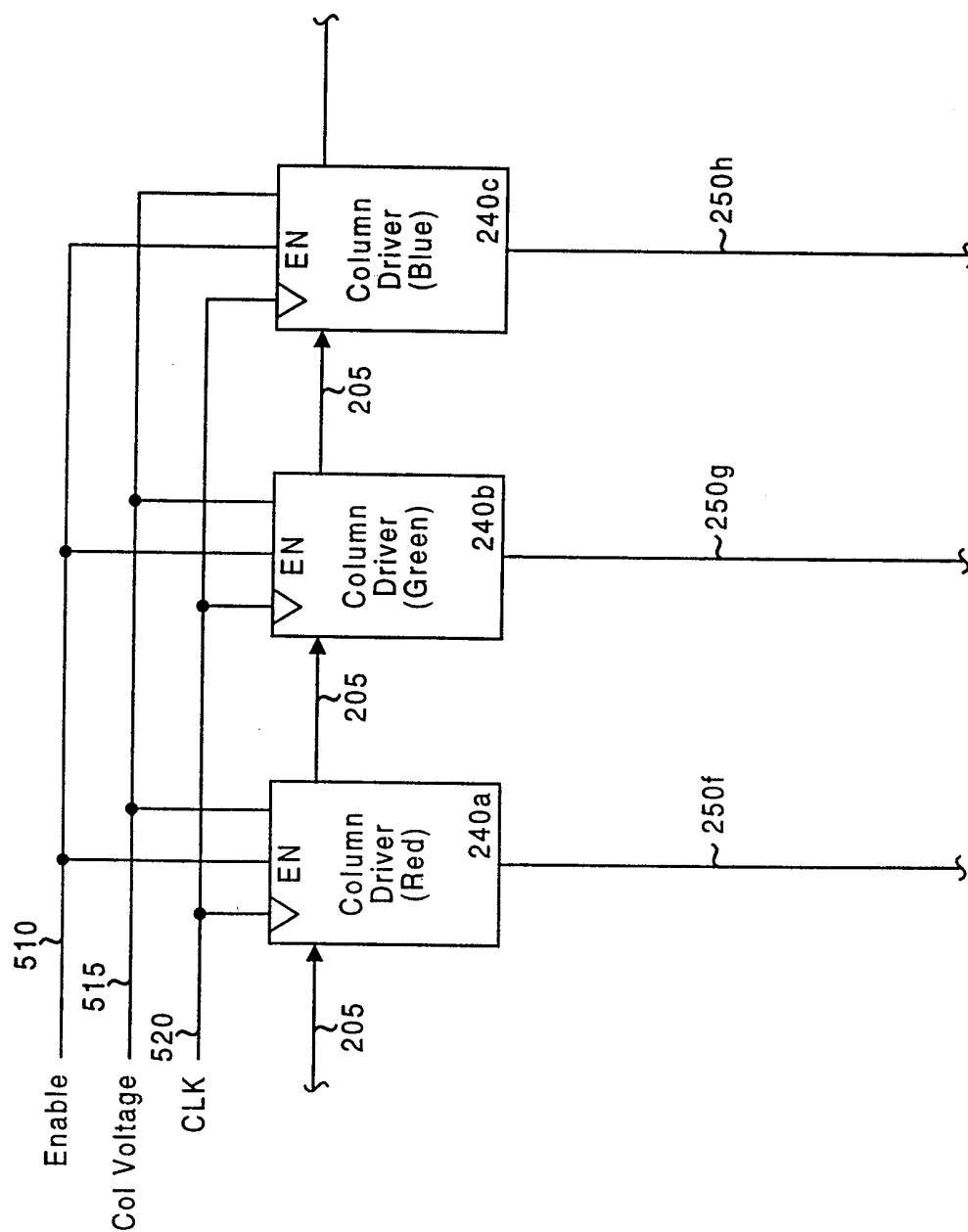


FIG. 6

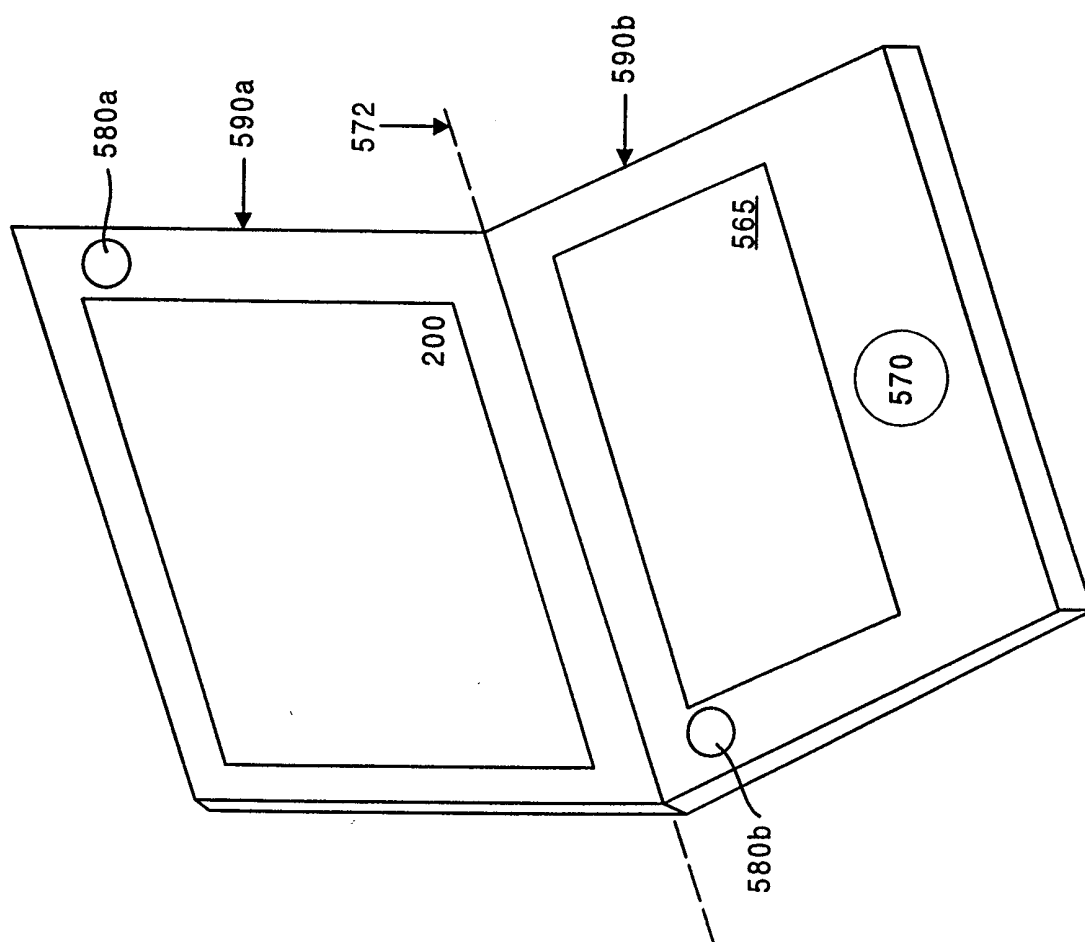


FIG. 7

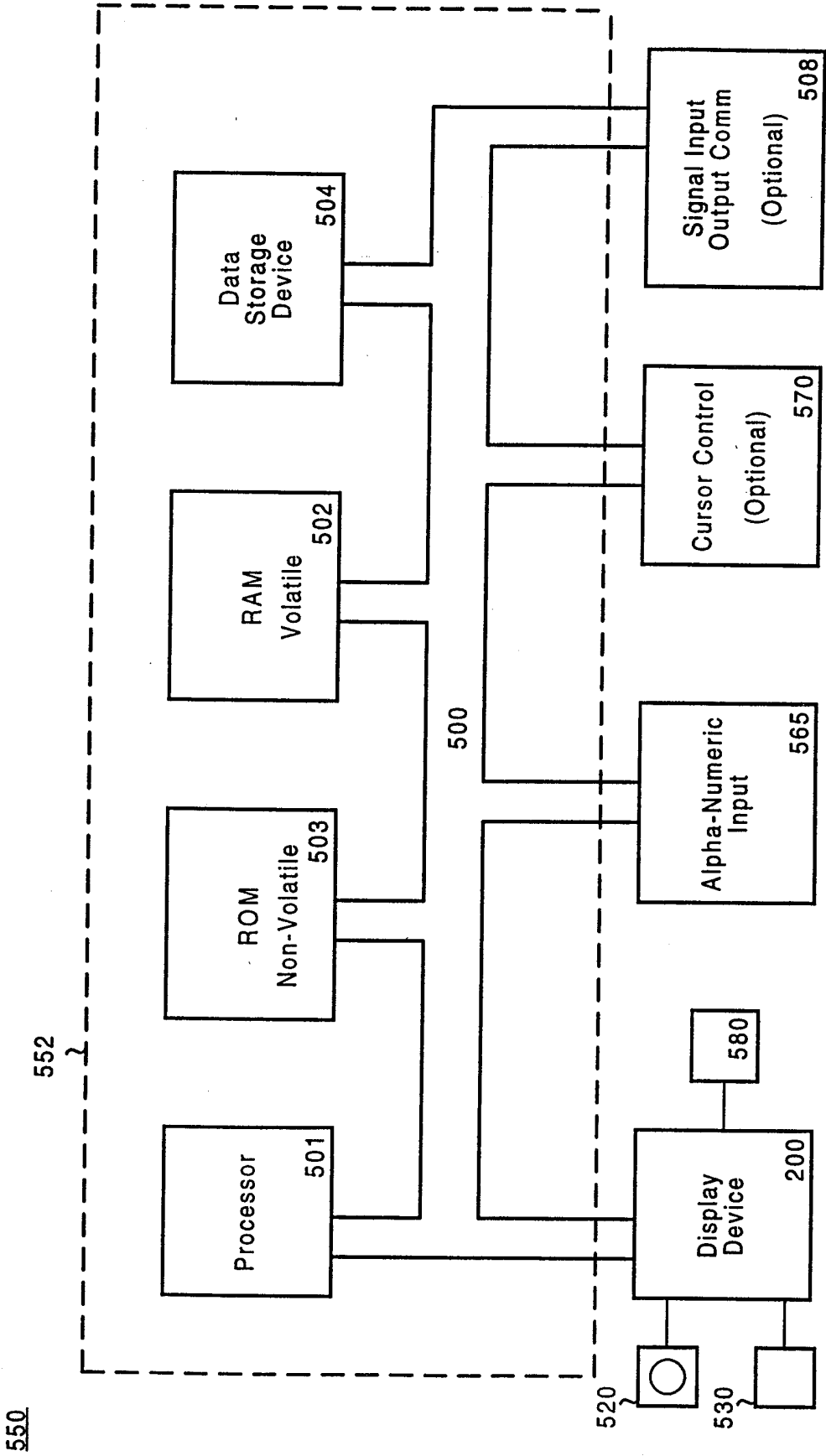
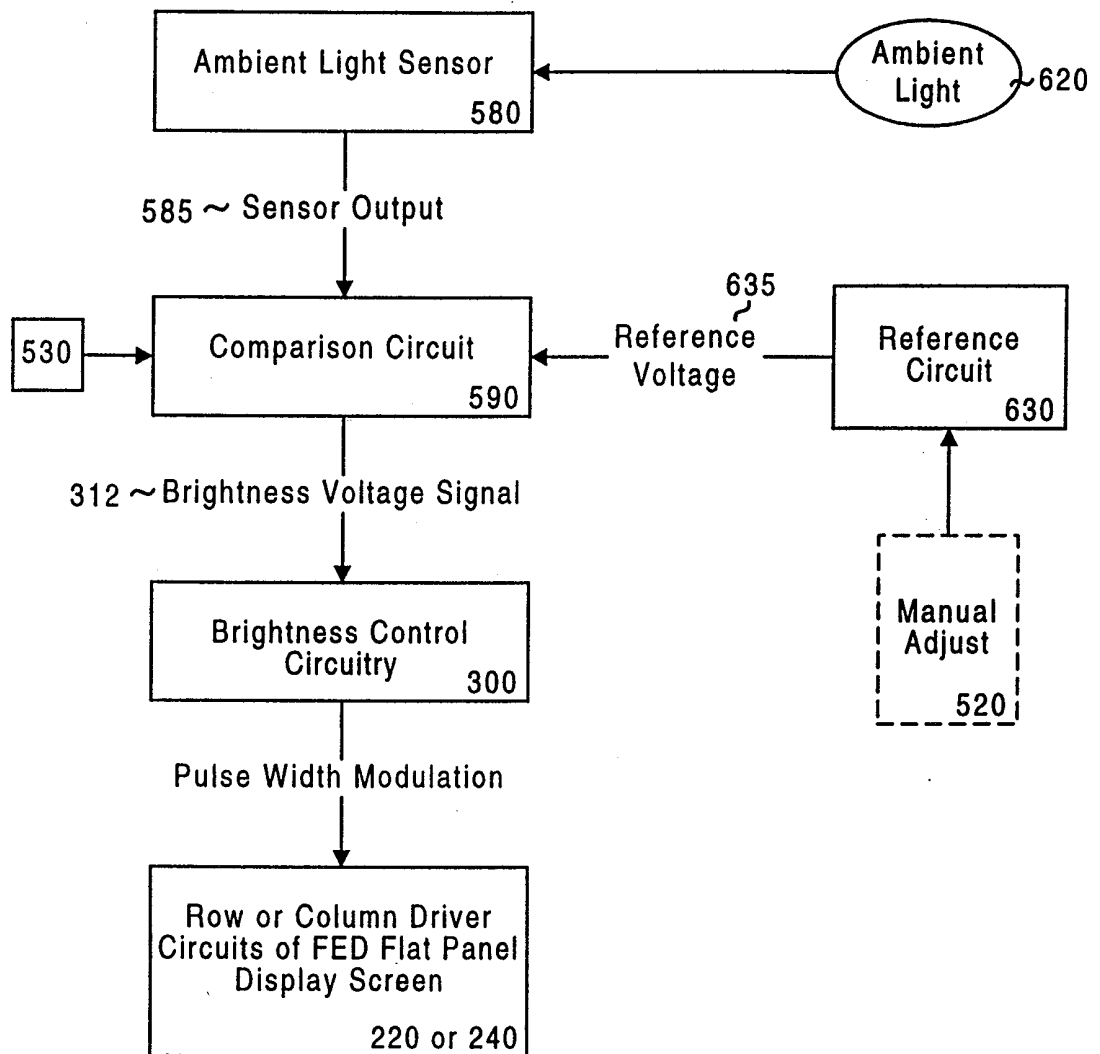


FIG. 8

600**FIG. 9**

10/10

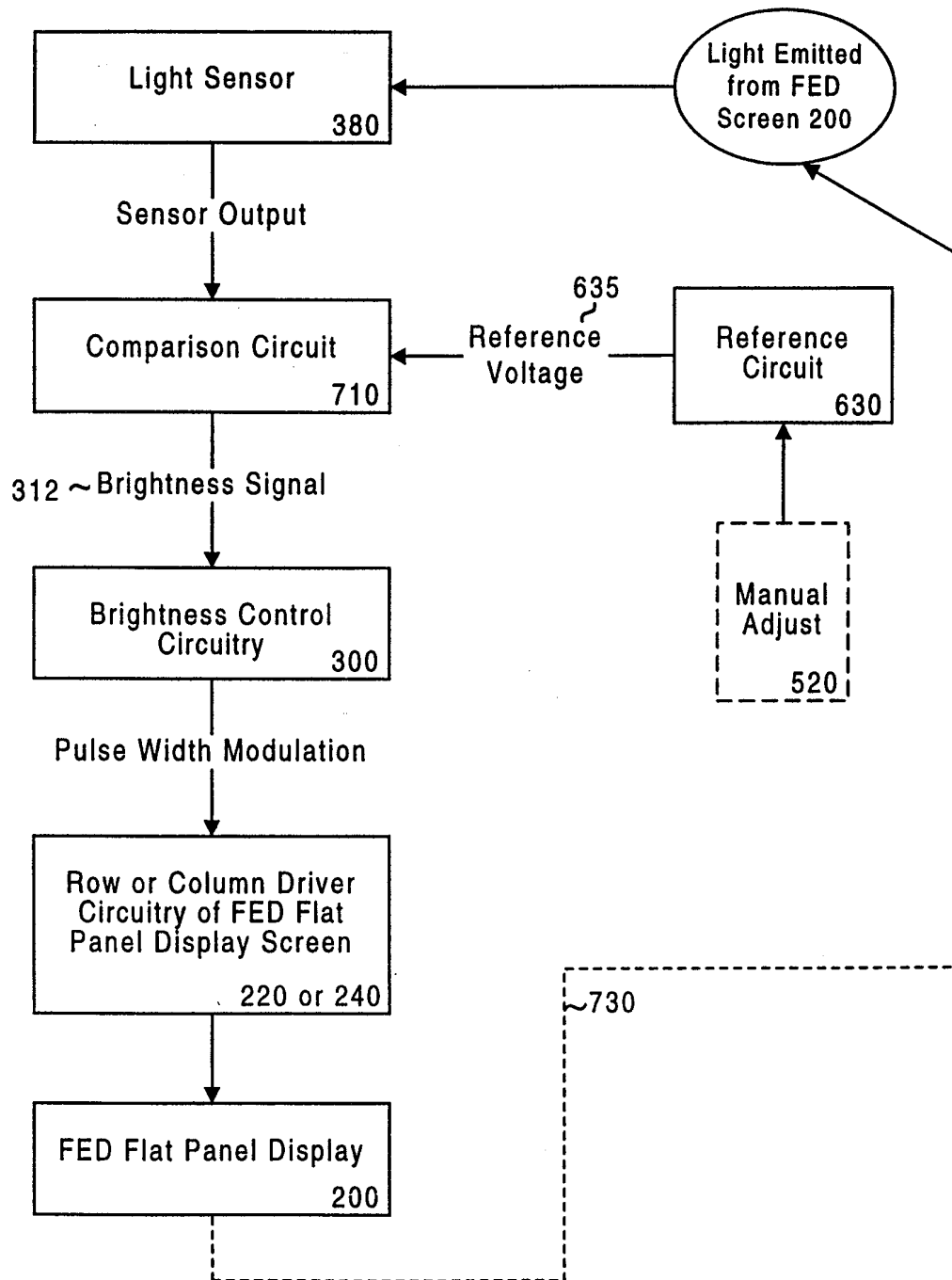
700

FIG. 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/08540

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :G09G 3/22

US CL :345/75, 147; 348/602

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 345/75, 147, 74, 20, 47, 213, 212; 348/602

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,262,698 A (DUNHAM) 16 November 1993, see the entire document.	1
--		-----
Y		2-11
Y	US 4,589,022 A (PRINCE et al.) 13 May 1986, see the entire document.	2-11

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:	*T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
A document defining the general state of the art which is not considered to be of particular relevance	*X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
E earlier document published on or after the international filing date	*Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
L document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	*G* document member of the same patent family
O document referring to an oral disclosure, use, exhibition or other means	
P document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search

26 AUGUST 1998

Date of mailing of the international search report

OCT 13 1998

Name and mailing address of the ISA/US
Commissioner of Patents and Trademarks
Box PCT
Washington, D.C. 20231

Facsimile No. (703) 305-3230

Authorized officer

DENNIS-DOON CHOW

Telephone No. (703) 305-4398