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DC/DC CONVERTER

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(57) Claim

1. A DC to DC voltage converter for converting an input signal to an output signal and including an input circuit with a gating circuit to apply said input signal threat, an output circuit generating said output signal, and a waveform generating circuit which is controlled by said input and output signals and which generates a control pulse waveform which is a function of said input and output signals and which is used to control said gating circuit, wherein said waveform generating circuit includes a pulse generator circuit controlled by said output signal to generate a pulse stream having an average frequency which is a function of said output signal, and wherein the pulse stream is applied to a pulse width modulator circuit controlled by the input signal, whereby the pulse width modulator converts each pulse of the pulse stream into a PWM pulse having a width which is a function of the input signal, the PWM pulses forming the control pulse waveform.

613102

ORIGINAL

COMMONWEALTH OF AUSTRALIA

PATENTS ACT 1952-1969

COMPLETE SPECIFICATION FOR THE INVENTION ENTITLED

"DC/DC CONVERTER"

The following statement is a full description of this invention, including the best method of performing it known to us:-

The present invention relates to a DC to DC voltage/current electric converter for converting an input signal to an output signal and including an input circuit with a gating circuit to apply said DC input signal therat, an output circuit generating said DC output signal, and a converter circuit which is controlled by said input and output signals and which generates a control pulse waveform which is function of said input and output signals and which is used to control said gating circuit.

Such a converter is already known from the book "Design of Solid-State Power Supplies, Second Edition", by E.R. Hnatek, Van Nostrand Reinhold Company, pp. 562-581. In this known converter the frequency of the control pulses is constant, whereas their width and amplitude are variable and function of both the input and output signals. Indeed, therein a generator periodically generates a ramp voltage which exponentially increases towards a first voltage which is function of the input signal voltage and this ramp voltage is each time compared with a second voltage which is function of the output signal voltage. The comparator each time provides a control pulse as long as the ramp voltage does not exceed this second voltage.

Because the control pulses are function of both the input and output signals and are periodically generated, it is clear that such a control pulse may for instance be generated even when the output signal is sufficiently high. In this case electric power is unnecessarily supplied to the output circuit and has to be consumed in the load coupled therewith, so that the efficiency of the converter is then low. Moreover, because the gating circuit is periodically operated, electric power is each time consumed therein.

An object of the present invention is to provide an electric converter of the above type, but which consumes less electric power in the gating circuit and enables a better control, in function of the needs, of the electric power supplied to the output circuit.

According to the invention this object is achieved by including in said converter circuit a pulse generator circuit controlled by said output signal and generating a pulse stream having an average frequency which is a function of the output signal, and a pulse width modulator circuit, controlled by said input signal and by said pulse stream, which converts each pulse of said pulse stream into a pulse having a width which is a function of said input signal and forms part of said control pulse waveform.

Hence, the input and output signals control two separate parameters of the control pulse waveform, i.e. the pulse width and the average frequency thereof respectively. As a consequence, when for instance the output signal is sufficiently high the average frequency of this control pulse waveform is changed by interrupting the control pulses thereby stopping the supply of electric power and the operation of the gating circuit.

It should be noted that the MAX630, a Step-Up Switching Regulator, manufactured by Maxim Integrated Products, Sunnyvale, California, may be used in an electric converter for converting a DC input signal to a DC output signal. Indeed, when the input of this circuit is controlled by this output signal a pulse stream having an average frequency which is only function of the output signal is generated at the output of the circuit. A gating circuit in the input circuit of the converter may then be controlled by means of this pulse stream. Hence, in this case the gating circuit is not controlled by the input signal.

The above mentioned and other objects and features of the invention will become more apparent and the invention itself will be best understood by referring to the following description of an embodiment taken in conjunction with the accompanying drawings wherein :

Fig. 1 represents an electric converter according to the invention;

Fig. 2 shows switching regulator circuit SR of Fig. 1 in more detail;

Fig. 3 represents timing circuit TC of Fig. 1 in more detail;

Fig. 4 shows pulse waveforms appearing at various points of the converter;

The converter shown in Fig. 1 includes an input circuit IC, an output circuit OC, a pulse frequency modulator circuit PFM, a pulse width modulator circuit PWM and an operation start circuit SC. It is built up by means of :

- a switching regulator circuit SR of the above MAX 630 type. This circuit is schematically shown in Fig. 2. It has terminals SR1 to SR8 and includes a bandgap reference generator BRG, an oscillator OSC, a flipflop FF1 comprising two cross-coupled NOR gates NOR1 and NOR2, two comparators COMP1 and COMP2 constituted by operational amplifiers, and two NMOS transistors NM1 and NM2;
- a timing circuit TC of the type ICM7555 also manufactured by Maxim. This circuit is schematically shown in Fig. 3. It has terminals TC1 to TC8 and includes a flipflop FF2 comprising two cross-coupled NOR gates NOR3 and NOR4, comparators COMP3 and COMP4 constituted by operational amplifiers, NMOS transistor NM3, inverters INV1 to INV3 and resistances R1 to R3 of equal value;
- Schmitt trigger NAND gates G1, G2 ~~and G3~~. A chip with 4 such gates and manufactured by Hitachi.
- a transformer TR;
- further NMOS transistors NM4 and NM5;
- further resistors R4 to R10;
- capacitors C1 to C10;
- diodes D1 to D3;
- Zener diodes Z1 and Z2;

The input circuit IC has input terminals I1 and I2 which are interconnected by the primary winding of transformer TR in series with the drain-

to-source path of NMOS transistor NM4 which constitutes a gating circuit or electronic switch.

The output circuit OC has output terminals O1 and O2 which are interconnected by the secondary winding of transformer TR in series with rectifier diode D1. Capacitor C1, capacitor C2 and Zener diode Z1 are branched in parallel across the output terminals O1 and O2. Terminals O2 and I2 are interconnected.

The operation start circuit SC includes NMOS transistors NM5 whose drain-to-source path is connected between input terminal I1 and a common supply lead SL and whose gate is connected to the junction point of resistance R4 and Zener diode Z2 which is connected in series between the input terminals I1 and I2.

The pulse frequency modulator circuit PFM includes the switching regulator circuit SR whose terminals SR1 to SR8 are connected as follows:-

- terminal SR1 is connected to tapping point A of a resistive voltage divider which comprises resistances R6, R7, R8 coupled in series between output terminal O2 and ground lead GL;
- terminal SR1 is connected to ground lead GL through capacitor C3 which determines the frequency of the oscillator OSC forming part of SR;
- terminals SR3 and SR8 constitute output terminals of SR and will be considered later;
- terminal SR4 is the ground terminal of SR and is directly connected to ground lead GL;
- terminals SR5 and SR6 are both connected, on the one hand directly to the supply lead SL and on the other hand to ground lead GL in series with capacitor C4;
- terminal SR7 is connected to the tapping point B of the voltage divider R6/R8.

As shown in Fig. 2, inside the switching regulator SR terminal SR1 is connected to the inverting input of comparator COMP1 whose non-inverting input is connected to the output VBG of the bandgap reference generator BRG. The output of COMP1 controls the gate of NMOS transistor NM1 whose drain-to-source path is connected between terminal SR8 and ground terminal SR4. Terminal SR2 is connected to the input of oscillator OSC whose output is coupled to input F7 of flipflop FF1. Another input F8 of this flipflop is connected to the output of comparator COMP2 whose inverting and non-inverting inputs are coupled to terminal SR7 and output VBG of BRG respectively. Terminal SR3 is connected to ground terminal SR4 through the drain-to-source path of NMOS transistor NM2 whose gate is controlled by the output F9 of the flipflop FF1. Finally, terminals SR5 and SR6 are connected to inputs of the bandgap reference circuit BRG.

The abovementioned output terminal SR3 of the circuit SR is directly connected to the first input M1 of gate G1 which is fed between supply lead SL and ground lead GL and whose second input N1 is directly connected to SL which is further coupled to input M1 through resistance R9. The output P1 of G1 is connected to the first input M2 of gate G2 via a differentiator circuit comprising series capacitor C5 and shunt resistance R10 which is connected between M2 and ground lead GL. The input N2 of G2 which is fed between SL and GL is directly connected to SL and the output P2 of this gate constitutes the output of the pulse frequency modulator circuit PFM.

The pulse width modulator circuit PWM includes the timing circuit TC whose terminals TC1 to TC8 are connected as follows :

- ground terminal TC1 is connected to input terminal I2, output terminal O1 and ground lead GL;
- output P2 of gate G2 is connected to trigger terminal TC2;
- terminal TC3 is connected to the gate of NMOS transistor NM4;
- output P1 of gate G1 is connected to terminal TC4;

- terminal TC5 is connected to ground lead GL via capacitor C6;
- terminals TC6 and TC7 are both connected to the output G of an integrator circuit comprising resistance R5 connected to input terminal I1 and capacitor C7 connected to ground lead GL. This output G is moreover connected to supply lead SL through clamping diode D3 and to terminal SR8 of SR via capacitor C10;
- terminal TC8 is connected on the one hand directly to supply lead SL and on the other hand to ground lead GL via capacitor C8.

As shown in Fig. 3, inside the timing circuit TC terminal TC1 is connected to terminal TC8 via a resistive voltage divider comprising the series connected equal resistances R1 to R3 and having tapping points D and E. Terminal TC2 is connected to the inverting input of comparator COMP3 whose non-inverting input is connected to the tapping point D of R1/3 and whose output constitutes input F5 of the flipflop FF2. The output F4 of this flipflop FF2 is connected to terminal TC3 via the series connected inverters INV1 and INV2. Terminal TC4 is connected to input F1 of flipflop FF2 through inverter INV3 and the input F2 of this flipflop is constituted by the output of comparator COMP4. Terminal TC5 is connected to the inverting input of this comparator COMP4 and to tapping point E of voltage divider R1/3, whilst terminal TC6 is connected to the non-inverting input of this comparator. Finally, terminal TC7 is connected to the drain electrode of discharge NMOS transistor NM3 whose source electrode is connected to terminal TC1 and whose gate is coupled to the junction point F6 of inverters INV1 and INV2.

The above described DC to DC converter operates as follows.

When an input voltage V1 is applied across the input terminals I1 and I2 of the input circuit IC a current is able to flow from I1 to I2 which is connected to the ground lead GL through resistance R4 and Zener diode Z2 in series. When this current is sufficiently high a Zener voltage of e.g. 5.6

Volts is established at the junction point of these components due to which transistor NM5 whose source is grounded via resistors R3 to R1 becomes conductive. As a consequence current is then able to flow from input terminal I1 to the ground lead GL through the drain-to-source path of NM5, supply lead SL and a plurality of parallel connected circuits. Thus both the supply lead SL and the terminal TC8 of TC are brought at a voltage VSL equal to the Zener voltage less the threshold voltage of NM5.

As a consequence and when assuming that the values of the resistances R1 to R3 are equal, voltages VD = VSL/3 and VE = 2VSL/3 are established at the respective tapping points D and E of the voltage divider R1/3 and therefore also at the non-inverting input of comparator COMP3 and at the inverting input of comparator COMP4 respectively. Because terminal TC2 is normally activated the output F5 of COMP3 is deactivated. Also the output F2 of COMP4 is normally deactivated because the voltage at terminal G or TC6, TC7 is smaller than VE. The flipflop FF2 is in a condition wherein the outputs F4 and F3 of its gates NOR3 and NOR4 are de-activated and activated respectively. The inputs F1, F2 and F3 of gate NOR3 are de-activated (due to terminal TC4 being activated), de-activated and activated respectively Terminal TC3 is de-activated thus blocking transistor NM4 of the input circuit IC, whereas terminal F6 is activated so that the transistor NM3 is conductive and thus connects G and TC6, TC7 to the ground at terminal TC1 via its drain-to-source path. This means that as long as the flipflop FF2 is in the reset condition wherein its output F4 is de-activated a voltage is prevented from being built up at terminal G or TC6, TC7, due to which the input F2 of this flipflop remains in the de-activated condition.

The above mentioned supply voltage VSL is also applied to the Schmitt trigger gates G1 and G2 as well as to the terminals SR3 and SR5, SR6 of the switching regulator SR forming part of the circuit PFM, i.e. to SR3 via resistance R9 and directly to SR5 and SR6. As a consequence the reference generator BRG generates the bandgap reference voltage VBG on its like named

output VBG. Because initially no current flows in the output circuit OC the output terminal 02 is at ground potential so that the voltages VSR1 and VSR7 on terminals SR1 and SR7 of the switching regulator SR are both smaller than this bandgap reference voltage VBG. As a consequence the outputs of comparators COMP1 and COMP2 are both activated due to which transistor NM1 becomes conductive, thus connecting capacitor C10 in parallel with capacitor C7, and flipflop FF2 is triggered to its set condition wherein the output F9 of its gate NOR2 is de-activated. Due to this the pulses OS (Fig. 4) of a square pulse waveform with period 2T1 generated by the oscillator OSC are allowed to pass through this gate NOR2 wherein they are inverted before being supplied to the gate of transistor NM2. In this transistor the pulses are again inverted and appear at the output SR3 of SR as a pulse stream SR3 (Fig. 4) whose pulses vary between VSL and ground. This pulse stream SR3 is inverted and shaped in the Schmitt trigger gate G1 and is then supplied as a pulse stream P1, TC4 (Fig. 4) from the output P1 of G1 to the differentiator circuit C5, R10 as well as to the input TC4 of the timing circuit TC. In this differentiator circuit C5, R10 the pulses of P1, TC4 are differentiated and in the subsequent Schmitt trigger gate G2 the resultant pulses are clamped, shaped and inverted so that a pulse stream P2, TC2 (Fig. 4) comprising negatively directed pulses is generated at the output P2 of gate G2. As shown in Fig. 4 these pulses occur at the beginning of each of the positively directed pulses of P1, TC4. From P2 they are supplied to terminal TC2 of the timing circuit TC.

In this timing circuit TC the pulse stream P1, TC4 is inverted in the inverter INV3 so that it is applied as a pulse stream F1 (Fig. 4) to the like named input F1 of flipflop FF2. Each of the negatively directed pulses of P2, TC2 applied to terminal TC2 brings the comparator COMP3 in a condition wherein the output F5 (Fig. 4) thereof is temporarily activated. Hence, a pulse stream F5 is constituted by positively directed pulses each

occurring after the end of a positively directed pulse of F1 is applied to input F5 of the flipflop FF2.

The effect of the pulse streams F1, F2 and F5 on the flipflop FF2 is that a control pulse waveform TC3 and a pulse stream F6 are generated, as explained hereinafter and shown in Fig. 4.

Indeed, each time the input F1 is activated the flipflop FF2 is reset to the condition wherein its output F4 and terminal TC3 are both de-activated, whereas terminal F6 is activated. As a consequence transistor NM4 is then blocked whereas transistor NM3 is conductive and thus prevents a voltage from being built up on terminal G or TC6, TC7, as already described above. Each time the input F5 is activated the flipflop FF2 is triggered to its set condition wherein its output F4 and terminal TC3 are both activated, whereas terminal F6 is de-activated. As a consequence transistor NM4 then becomes conductive, whereas transistor NM3 is blocked so that on the one hand the input voltage V1 is applied to the primary winding of transformer TR thus storing electric energy therein and that, on the other hand, a current starts flowing through the integrator circuit R5, C7, C10 and so that an exponentially increasing voltage VG is generated on the terminal G or TC6, TC7. When this voltage VG reaches the threshold voltage VE after a time interval T2 the output F2 of comparator COMP4 becomes activated so that flipflop FF2 is then triggered back to its reset condition wherein output F4 and terminal TC4 are both de-activated and terminal F6 is activated. As a consequence transistor NM4 is then blocked, whereas transistor NM3 becomes conductive. Due to this the current flow in the primary winding of transformer TR is interrupted, but a current then starts flowing in the secondary winding thereof via the then conductive diode D1 so that an output voltage V2 is built up across output terminals 02 and 01. This voltage is filtered by capacitor C1. Meanwhile, capacitor C7 is discharged to ground through the conductive transistor NM3, and when the

voltage on terminal G or TC6, TC7 decreases below the threshold voltage VE the output F2 of COMP4 again becomes de-activated.

From the above it is clear that each time transistor NM4 is conductive a current flows in the primary winding of transformer TR, whilst a current is supplied to a load, connected across the output terminals 01, 02, through the secondary winding of this transformer when transistor NM4 is blocked and diode D1 is conductive. It should moreover be noted that during the time intervals wherein NM4 is conductive and diode D1 is blocked current is supplied to the load by the reservoir capacitor C2. Thus the output voltage V2 is gradually built up.

From the above it also follows that the flipflop FF2 in combination with the comparator COMP4 and the integrator circuit R5, C7, C10 in fact is a monostable circuit which is triggered to its unstable condition for a time interval T2 by the pulses of pulse stream F5. If it were not reset before the end of time interval T1 this flipflop is anyhow reset by a pulse of pulse stream F1.

The integrator circuit R5, C7, C10 provides a voltage VG approximately given by the relation :

$$VG = \frac{t}{T} V1 \qquad (1)$$

with $T = R5.(C7+C10)$ (2)

Hence, this voltage is directly proportional to the input voltage V1. Because this voltage is supposed to reach the threshold voltage VE after a time interval T2 the latter is given by the following relation :

$$T2 = \frac{VE.T}{V1} \qquad (3)$$

Because VE.T is a constant the time interval T2 which is also the (variable) width of each of the pulses of the control pulse waveform TC3, F4 (Fig. 4) is inversely proportional to the input voltage V1. Hence the circuit PWM really modifies the width of the pulses of F5 in function of the input voltage V1.

It should also be noted that the peak value of the current flowing in the primary winding of the transformer is a constant. Indeed, this peak value which is reached at the end of the time interval T2 is given by:

$$ip = \frac{V1.T2}{L} \qquad (4)$$

or, when taking the relation (3) into account by:

$$ip = \frac{VE.T}{L} \qquad (5)$$

wherein L is the self inductance of this primary winding.

Considering again the pulse frequency modulator circuit PFM, as soon as the output voltage V2 exceeds the voltage VSL by the voltage drop in diode D2 the voltage VSL is determined by this output voltage V2 and blocks transistor NM5 is blocked. This voltage is filtered by capacitor C9.

As soon as this output voltage V2 reaches a value such that the voltage VA at the tapping point A of the voltage divider R6/8, i.e. at terminal SR1, exceeds the bandgap reference voltage VBG the output of comparator COMP1 of the switching regulator SR becomes de-activated due to which transistor NM1 is blocked. As a consequence capacitor C10 is then no longer connected across capacitor C7 so that the time constant T is then decreased and becomes

$$T' = R5.C7 \qquad (6)$$

whilst the time interval T2 is reduced to

$$T'2 = \frac{VE.T'}{V1} \qquad (7)$$

Hence, at the start of the operation of the converter pulses of the control pulse waveform have a maximum width T2 and afterwards a reduced width T'2. This means that at the start much electric energy is supplied to the output unit DC.

When the output voltage V2 reaches a still higher value such that the voltage VB at the tapping point B of the voltage divider R6/8, i.e. at terminal SR7, exceeds the bandgap reference voltage VBG and the output F8 of

comparator COMP2 becomes de-activated. Due to this the flipflop FF1 is triggered to its set condition wherein its output F9 is activated and terminal SR3 de-activated (Fig. 4). Thus the passage of oscillator pulses through gate NOR2 and towards timing circuit TC is inhibited.

This situation continues as long as the voltage at terminal SR7 exceeds the reference voltage VBG, but as soon as this is no longer so the flipflop FF1 is again triggered to its reset condition to again allow the flow of the pulse streams P1, TC4 and P2, TC2 to the timing circuit TC. Because the flow of these pulse streams is directly controlled by the output voltage V2 it is clear that their average frequency is function of V2, the pulses themselves having a constant width.

From the above it follows that the converter :

- generates a pulse stream F5 the pulses of which have a constant width and an average frequency which is solely function of the output voltage V2;
- converts each of the pulses of this pulse stream F5 to a control pulse whose width T2 is solely function (inversely proportional) of the input voltage V1 and which forms part of a control pulse waveform TC3, F4. Only at the start of an operation this width is also function of the output voltage V2.

Hence, the control pulse waveform TC3, F4 has two parameters, i.e. its average frequency and the width of its pulses, which are normally solely function of this output and input voltages V2 and V1 respectively. Thus the electric power supplied by the converter can be regulated independently in function of the input and output voltage values.

While the principles of the invention have been described above in connection with specific apparatus, it is to be clearly understood that

this description is made only by way of example and not as a limitation on the scope of the invention.

The claims defining the invention are as follows:

1. A DC to DC voltage converter for converting an input signal to an output signal and including an input circuit with a gating circuit to apply said input signal threat, an output circuit generating said output signal, and a waveform generating circuit which is controlled by said input and output signals and which generates a control pulse waveform which is a function of said input and output signals and which is used to control said gating circuit, wherein said waveform generating circuit includes a pulse generator circuit controlled by said output signal to generate a pulse stream having an average frequency which is a function of said output signal, and wherein the pulse stream is applied to a pulse width modulator circuit controlled by the input signal, whereby the pulse width modulator converts each pulse of the pulse stream into a PWM pulse having a width which is a function of the input signal, the PWM pulses forming the control pulse waveform.

2. A converter as claimed in claim 1, further including a transformer whose primary and secondary windings form part of said input and output circuits respectively, said output circuit further including a rectifier-filter circuit providing said output signal.

3. A converter as claimed in claim 1, including a first control circuit whereby said pulse stream generated by said pulse generator circuit is interrupted when said output signal or a function thereof exceeds a predetermined reference value, said converter further including a monostable circuit, with a set input to which said pulse stream is supplied and with an output on which said control pulse waveform is generated, said monostable circuit having a time constant which is a function of said input signal.

4. A converter as claimed in claim 3, including a time constant modifying circuit to make said time constant also a function of said output signal as long as said output signal or a function thereof does not exceed said predetermined reference value.

5. A converter as claimed in claim 4, wherein said monostable circuit, includes an integrator circuit which is constituted by the series connection of a resistance and a first capacitance and which is fed by said input signal, said resistance and said first capacitance determining said time constant, and wherin said time constant modifying circuit, is able to detect when said input signal or a function thereof does not exceed or exceeds said predetermined reference value and to then connect or disconnect a second capacitance across or from said first capacitance respectively.

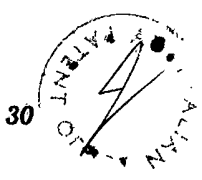
6. A converter as claimed in claim 3, wherein said pulse generator circuit also generates a second pulse stream which is also interrupted when said output signal or

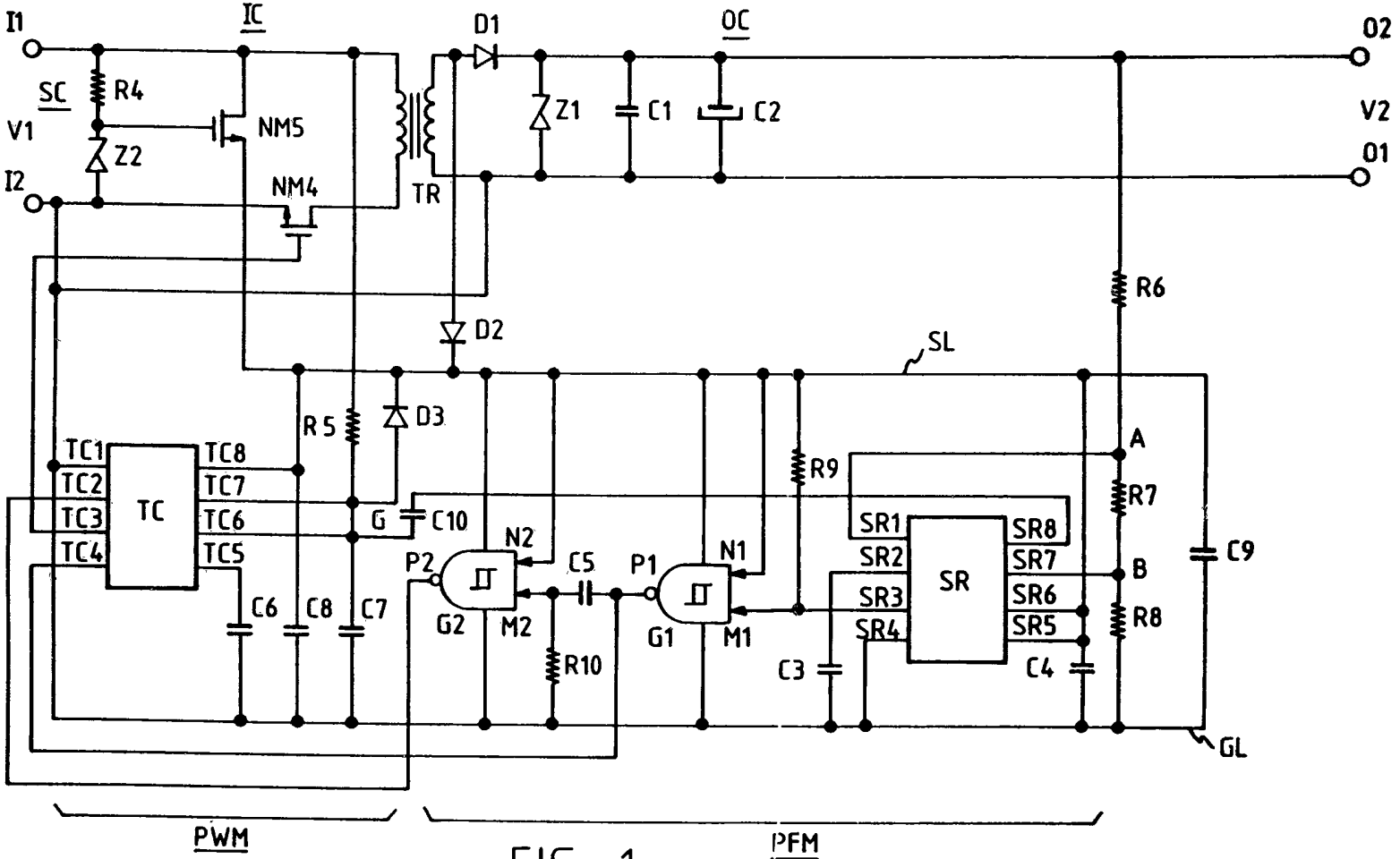
a function thereof exceeds said predetermined reference value and which is supplied to a reset input of said monostable circuit to reset this circuit for a predetermined time interval immediately preceeding each pulse of said first mentioned pulse stream.

7. A DC to DC voltage/current converter substantially as herein described with reference to Figs. 1 to 4 of the accompanying drawings.

DATED THIS FIRST DAY OF MAY, 1991

ALCATEL N.V.

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R4
V1
NM5
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C1
C2
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TR
R6
D2
SL
R5
D3
A
TC1
TC2
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C5
P1
N1
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R10
C3
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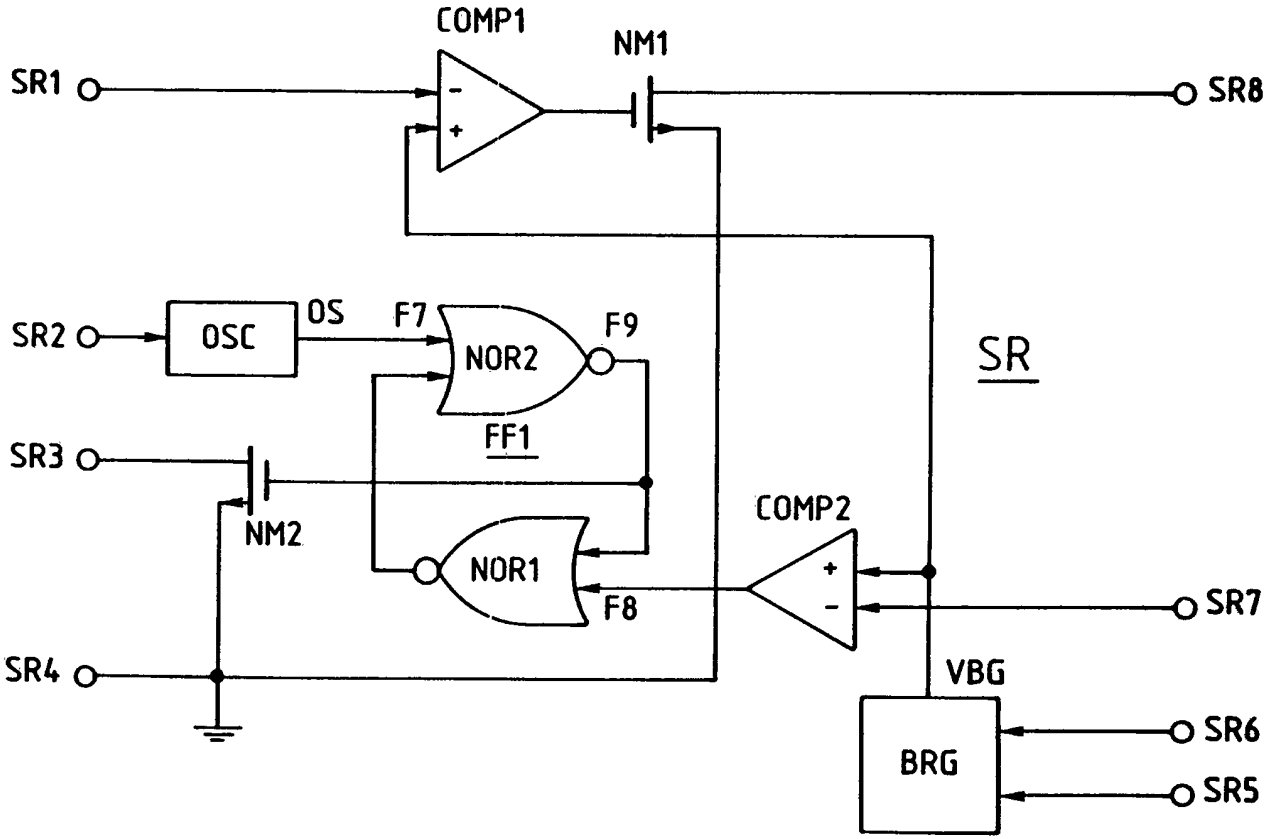
GL
PWM
PFM

FIG. 1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SR8
SR2
OSC
OS
F7
NOR2
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NM2
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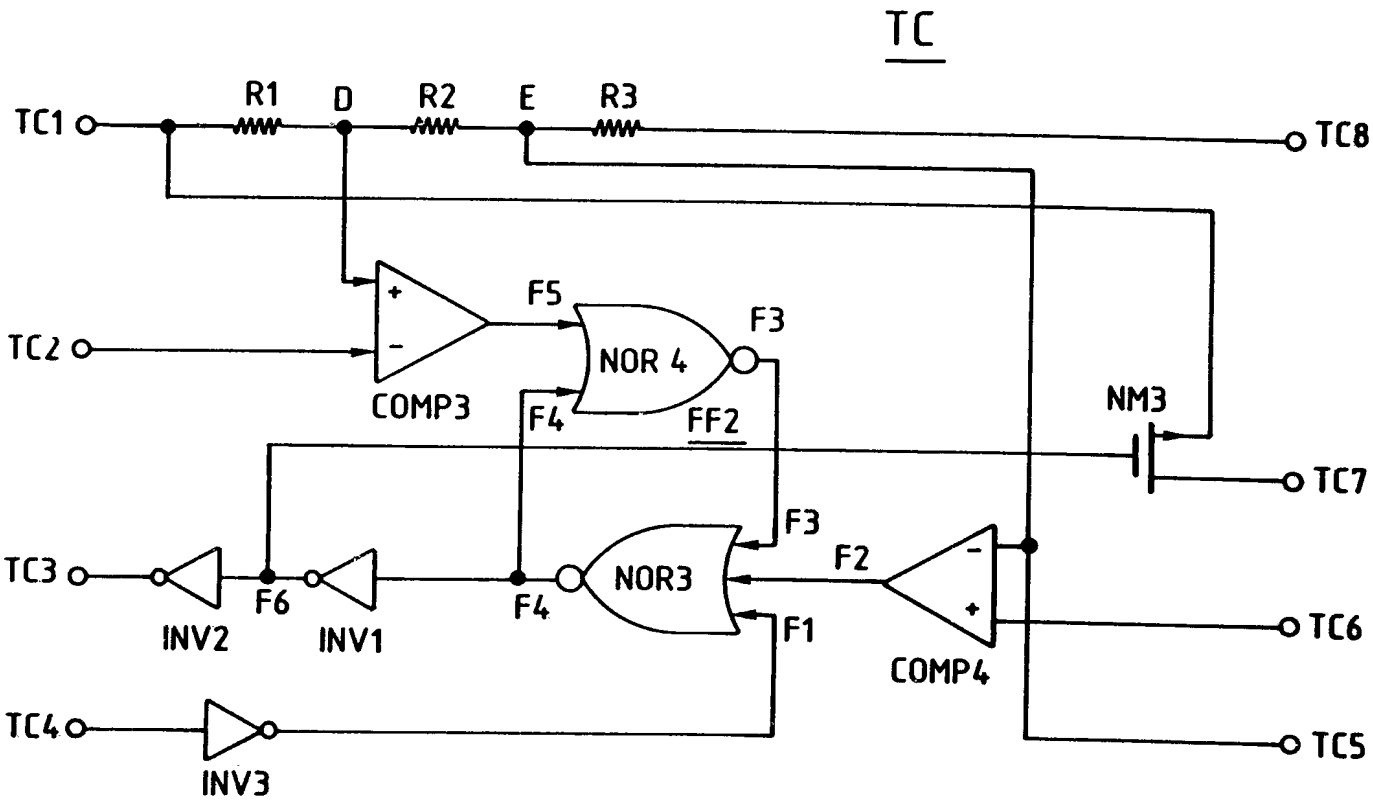
SR7
SR4
VBG
BRG
SR6
SR5

FIG. 2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R2
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R3
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TC8
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F4
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TC3
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TC5
INV3

FIG. 3

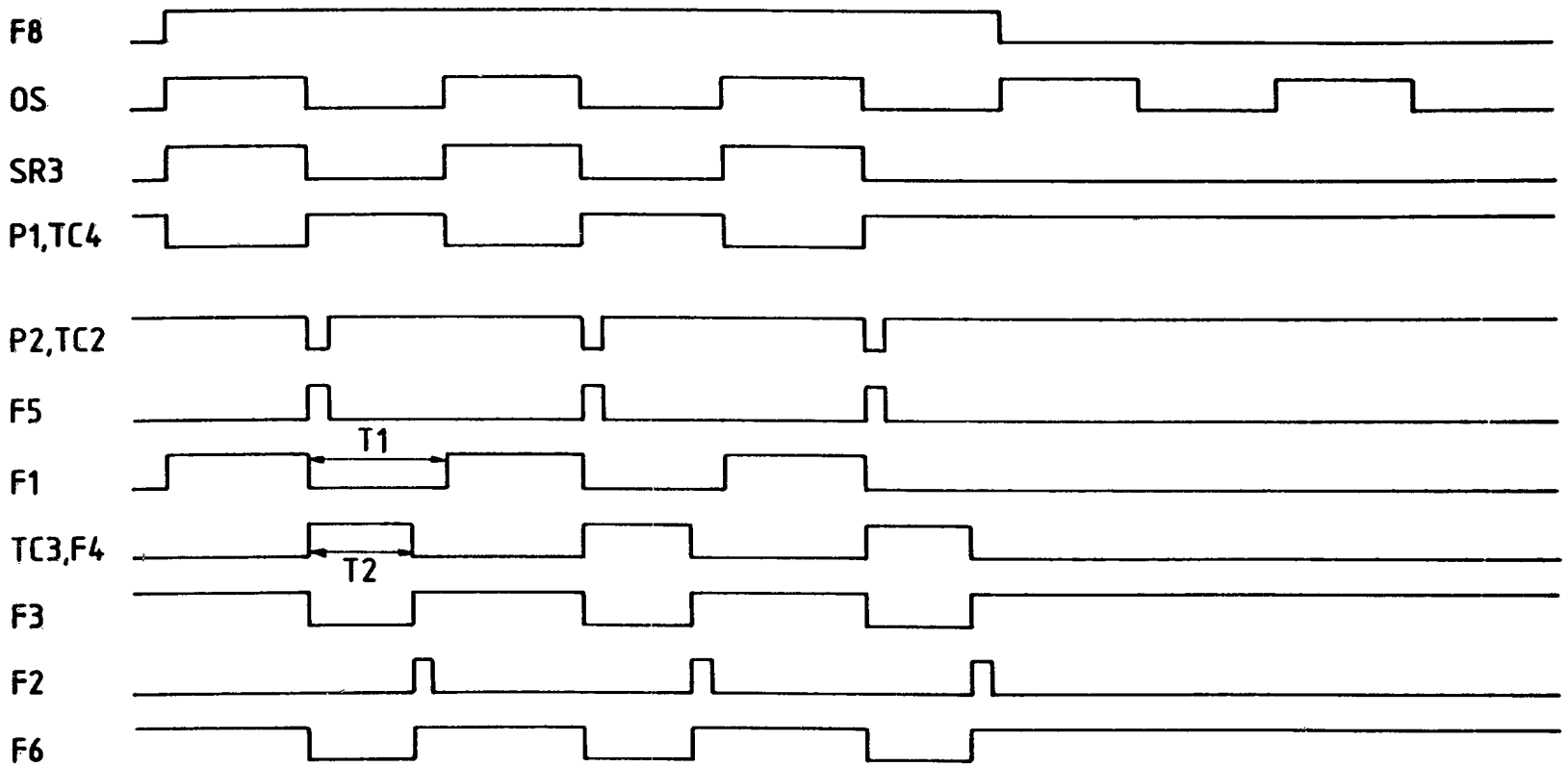

FIG.4