(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
23 May 2013 (23.05.2013)

(10) International Publication Number
WO 2013/074496 A1

(51) International Patent Classification:
H01L 29/737 (2006.01) ***H01L 33/00*** (2010.01)
H01L 29/778 (2006.01)

(21) International Application Number:
PCT/US2012/064778

(22) International Filing Date:
13 November 2012 (13.11.2012)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/629,181 14 November 2011 (14.11.2011) US
61/629,175 14 November 2011 (14.11.2011) US

(71) Applicant: **QUANTUM ELECTRO OPTO SYSTEMS SDN. BHD.** [MY/MY]; Melaka Media House Mitc City, 75450 Ayer Keroh, Melakia (MY).

(72) Inventor; and
(71) Applicant *(for AL only)*: **WALTER, Gabriel** [MY/US]; 5015 Sheboygan Ave, Madison, WI 5370 (US).

(74) Agent: **NOVACK, Martin**; 16355 Vintage Oaks Lane, Delray Beach, FL 33484 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report (Art. 21(3))*

(54) Title: OPTICAL TILTED CHARGE DEVICES AND METHODS

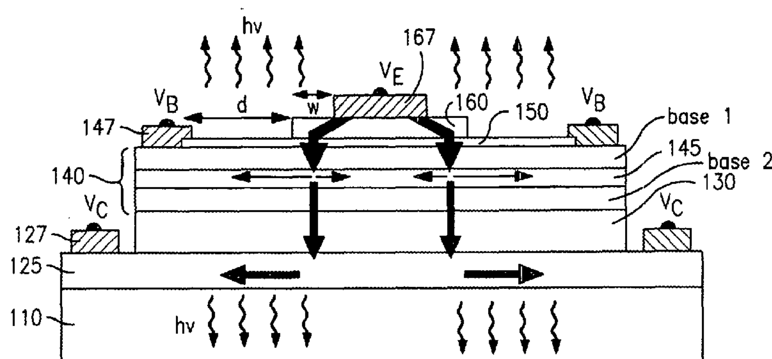


FIG. 1

(57) Abstract: A method for producing optical signals with improved efficiency, including the following steps: providing a layered semiconductor structure that includes a substrate, a semiconductor collector region of a first conductivity type, a semiconductor base region of a second conductivity type disposed on the collector region, and a semiconductor emitter region of the first semiconductor type disposed as a mesa over a portion of a surface of the base region; providing, in the base region, at least one region exhibiting quantum size effects; providing collector, base, and emitter electrodes, respectively coupled with the collector, base and emitter regions; providing a tunnel barrier layer over at least the exposed portion of the surface of the base region; and applying signals with respect to the collector, base, and emitter electrodes to produce optical signals from the base region. Also disclosed is an optical tilted charge device with an InGaAsN quantum well.

WO 2013/074496 A1

OPTICAL TILTED CHARGE DEVICES AND METHODS

FIELD OF THE INVENTION

This invention relates to the field of semiconductor light emitting devices and techniques and, more particularly, to tilted charge light emitting devices and methods.

BACKGROUND OF THE INVENTION

Included in the background of the present invention are technologies relating to heterojunction bipolar transistors (HBTs, which are electrical tilted charge devices) and light-emitting transistors, transistor lasers, and tilted charge light-emitting diodes (respectively, LETs, TLs, and TCLEDs, all of which are optical tilted charge devices). A tilted charge device gets its name from the energy diagram characteristic in the device's base region, which has, approximately, a descending ramp shape from the emitter interface to the collector (or drain, for a two terminal device) interface. This represents a tilted charge population of carriers that are in dynamic flow - "fast" carriers recombine, and "slow" carriers exit via the collector (or drain).

Regarding optical tilted charge devices and techniques, which typically employ one or more quantum size regions in the device's base region, reference can be made, for example, to U.S. Patent Numbers 7,091,082, 7,286,583, 7,354,780, 7,535,034, 7,693,195, 7,696,536, 7,711,015, 7,813,396, 7,888,199, 7,888,625, 7,953,133, 7,998,807, 8,005,124, 8,179,937, and 8,179,939; U.S. Patent Application Publication Numbers US2005/0040432, US2005/0054172, US2008/0240173, US2009/0134939, US2010/0034228, US2010/0202483, US2010/0202484, US2010/0272140, US2010/0289427, US2011/0150487, and US2012/0068151; and to PCT International Patent Publication Numbers WO/2005/020287 and WO/2006/093883 as well as to the publications referenced in U.S. Patent Application Publication Number US2012/0068151.

An optical tilted charge device includes an active region with built-in free majority carriers of one polarity. At one input to this active region, a single species of minority carriers of opposite polarity are injected and allowed to diffuse across the

active region. This active region has features that enable and enhance the conduction of majority carriers and the radiative recombination of minority carriers. On the output side of the region, minority carriers are then collected, drained, depleted or recombined by a separate and faster mechanism. Electrical contacts are coupled to this full-featured region.

In early 2004, a publication described an optical tilted charge device incorporating a quantum well in the base region of the device in order to enhance radiative recombination (see M. Feng, N. Holonyak Jr., and R. Chan, Quantum-Well-Base Heterojunction Bipolar Light-Emitting Transistor, Appl. Phys. Lett. 84, 1952, 2004). In that paper, it was demonstrated that the optical signal followed the sinusoidal electrical input signal at speeds of up to 1 GHz. More than five years later, after further work and fundamental developments (relating, among other developments, to operation methods, active area design, and epilayer structure), it was reported that high speed tilted charge devices as spontaneous emission light emitters, operated at bandwidths of 4.3 GHz (LET) and later at 7 GHz (TCLED). (See G. Walter, C.H. Wu, H.W. Then, M. Feng, and N. Holonyak Jr., Titled-Charge High Speed (7 GHz) Light Emitting Diode, Appl. Phys. Lett. 94, 231125, 2009.) Further improvements have been achieved since that time, but additional advances in efficiency and bandwidth are desirable for achieving commercially practical opto-electronic devices and techniques.

Tilted charge light-emitting devices, for example of the types disclosed in documents listed above (for example, in the form of light-emitting transistors and tilted charge light-emitting transistors and tilted charge light-emitting diodes) can produce spontaneous light emission at relatively high speed and bandwidths. For some applications, however, it would be desired to have tilted charge spontaneous light emitting devices and techniques that can operate at much higher speeds and bandwidths, and the achievement of such devices and techniques are among the objectives of one of the aspects of the present invention.

In the U.S. Patent Application Publication No. US2010/202484, there is shown, as background, a QW-heterojunction bipolar light emitting transistor (QW-HBLET) with a deep QW design and homogeneous doped base region. Reference can be made, for example, to the patents referenced above. The relatively deep QW assists captured carriers to spread laterally and recombine away from the optical cavity. In addition to that, as the carriers spread laterally, the carriers can also

rethermalize and carriers that rethermalize towards the emitter (back diffusion) are mostly lost in to non-radiative recombination. As an improvement thereto, an asymmetrical base region was set forth, having a relatively wider bandgap base sub-region on the emitter side the QW as compared to a relatively narrow bandgap sub-region on the collector side. Also, one or more shallow quantum wells were used for reasons that include limiting diffusion of captured carriers and increasing speed.

Applicant's research has indicated that the use of heavily doped high composition alloy (e.g. ternary or quaternary material) in the base region of an optical tilted charge device (OTCD), can result in significantly higher non-radiative recombination ($\eta_{non-rad}$ ~ 30% to 90% of base recombination). Some of this research has been focused on the use of a relatively shallow InGaAs quantum well (ΔE, the quantum well depth energy, is a small multiple of kT, $\Delta E \sim kT$) with emission photon energies that can be coupled to InP/InGaAs based photodetectors. (See also the above-referenced Published Application US 2010/0202484.) The use of a shallow quantum well allows the utilization of phonons as a method to increase the speed of the optical tilted charge device. However, there are certain applications of optical tilted charge devices where a deep quantum well ($\Delta E >> kT$) is advantageous, and device speed is of a lesser concern; for example, in optical devices that require high base current density operations and stable current gain under varying bias current characteristics or temperature. For such applications, use of a high composition alloyed base (e.g. AlGaAs), with its attendant disadvantage, would appear inevitable.

It is among the further objects of the present invention to provide improvements in optical tilted charge devices that need to use relatively deep quantum wells, while avoiding concomitant drawbacks.

SUMMARY OF THE INVENTION

The question can be posed: How does one design an efficient, high speed spontaneous emission tilted charge device? For example, how does one progress from 0.1 GHz to a 10 GHz bandwidth? One approach might be to make the device area smaller and narrower to result in smaller resistances (R), smaller capacitances (C) and smaller inductances (L), or to merely utilize the design rules of the fastest InGaP/GaAs heterojunction bipolar transistor (HBT). This would not achieve the objective.

Despite their origin from transistor technology, optical tilted charge devices share few common design traits with the high speed HBT transistor (an electrical tilted charge device). An optical tilted charge device has a quantum size region (typically, one or more quantum wells) in its base region. The addition of a quantum well in the base of a transistor, does not merely introduce another element or defect to assist in recombination, but also a structure which is capable of storing charge, lateral transport, and re-thermalizing of captured carriers. Furthermore, with significantly lower electrical gain (higher base current ratios), problems associated with base sheet resistance (heating, emitter crowding) and base current densities (reliability) is amplified and the importance of base transit time, a big issue in design of HBT's, is dwarfed by concerns of lateral resistance and emitter crowding at low emitter current densities. When designing a high speed optical tilted charge device, optical extraction, beam shape and optical power output can be as important as the electrical gain and electrical bandwidth of the device. Even the design rules which the HBT community has followed with some success, that the speed of an HBT can be increased by continuously shrinking the dimensions of the base-emitter junction and base collector junction, cannot be utilized for a tilted charge light emitter, since the physical dimensional reduction results in increasingly smaller radiative recombination efficiency. Thus, it will be understood that design rules suitable for a purely electrical input/output tilted charge device are not necessarily suitable for devices that require also the optimization of an optical output.

Similarly, the high speed tilted optical charge device shares few common design traits with charge storage light emitters (i.e., diode lasers or light emitting diodes). For example, although both use structures such as a quantum well, the design rules of an optical charge storage device necessitate methods of maximizing confinement or storage of carriers (to improve the probability of stimulated emission process where captured carriers “wait” to be stimulated by a photon field or recombine by spontaneous emission), whereas the design rules of an optical tilted charge device necessitate the minimization of stored carriers. Even design rules for light extraction used in charge storage devices do not simply apply to tilted charge devices due to the physical design restrictions imposed on the tilted charge device (different geometry) and high speed application (e.g. compatibility with a high speed interconnect).

Accordingly, design considerations for an optical tilted charge device are not about finding a balance between the design rules for an HBT and those for a diode light emitter; in other words, not about deciding whether the device should be more like an HBT or like a diode light emitter. Rather, the design paradigm for a tilted charge light emitting device should depend on the particular charge dynamics, geometry, optical characteristics, and applications that are unique to the device. As will be disclosed, an aspect of the invention involves reducing non-radiative recombination associated with base surface recombination. Another aspect of the invention involves reduction of base charge capacitance associated with the lateral transport and unintentional confinement of electrons in the quantum well.

The use of a quantum well (QW) in a heterojunction bipolar transistor (HBT) in conjunction with a thin base layer thickness (the “base 1” region) between the QW and the base surface (e.g. a layer thickness of less than about 300 Angstroms) introduces the problem of carriers tunneling from the quantum well into the surface states where they recombine non-radiatively. Use of an asymmetric base region as a technique for reducing thermalization of captured electrons in QW towards the surface has previously been disclosed (see U.S. Patent Application Publication No. US2010/0202484). This helps in reducing non-radiative recombination and since electron re-thermalization is preferred toward the collector, it also assists in reducing lateral transport of electrons. The larger bangap region of the asymmetric base region also acts to reduce surface recombination.

In accordance with principles of an aspect hereof, when it is necessary to keep the base 1 region thickness to ~300 Angstroms or less, a tunneling barrier structure comprising, for example, a low doped (1E-16 cm^{-3} to 5E-17 cm^{-3}) or unintentionally doped n-type layer structure of thickness preferably between about 15 to 50 nm, can be used to increase the spatial distance from the quantum well to the surface, thereby reducing tunneling of captured carriers in the quantum well to the surface states without having to physically increase the p-type base region between the quantum well and emitter region. The tunnel barrier structure material should preferably have an energy gap greater than the fundamental states of the quantum well, and should be selectively removable by an etching process that will not affect the base 1 region. For a base 1 region comprising GaAs or a low % (< 20%) Al, AlGaAs layer, the tunnel barrier can, for example, be made of relatively higher Al % (>35%), AlGaAs or lattice matched or be a strained InAlGaP alloy layer.

An asymmetric base design, with increasingly higher energy barrier, can also be employed in conjunction with the above-described ledge to increase the tunneling barrier height, to generate preferential conditions of carrier re-thermalization towards the collector, and to increase the barrier height, which also reduces tunneling.

In accordance with a form of the invention, a method is set forth for producing optical signals with improved efficiency, including the following steps: providing a layered semiconductor structure that includes a substrate, a semiconductor collector region of a first conductivity type, a semiconductor base region of a second conductivity type disposed on said collector region, and a semiconductor emitter region of said first semiconductor type disposed as a mesa over a portion of a surface of said base region; providing, in said base region, at least one region exhibiting quantum size effects; providing collector, base, and emitter electrodes, respectively coupled with said collector, base and emitter regions; providing a tunnel barrier layer over at least the exposed portion of said surface of said base region; and applying signals with respect to said collector, base, and emitter electrodes to produce optical signals from said base region. In an embodiment of this form of the invention, the step of providing said electrodes includes providing at least a portion of said base electrode as being disposed on said surface of said base region and spaced from said emitter mesa, and said step of providing said tunnel barrier layer comprises providing said tunnel barrier layer on said surface of said base region between said mesa and said base electrode. In this embodiment said step of providing said at least one region exhibiting quantum size effects comprises providing a discontinuous or non-planar quantum size region; that is, quantum dots and/or quantum wires (discontinuous), or a corrugated quantum well (non-planar). Also in this embodiment, said step of providing said base region comprises providing a base region that includes a first base sub-region on the emitter side of said quantum size region, and a second base sub-region on the collector said of said quantum size region, and said first and second base sub-regions are provided with asymmetrical band structures with respect to each other.

In accordance with a further form of the invention, a method is set forth for producing a tilted-charge light-emitting device, including the following steps: forming a layered semiconductor structure that includes a substrate, a semiconductor collector region of a first conductivity type, a semiconductor sub-base region of a second conductivity type, a quantum size region, and a further semiconductor sub-

base region of said second conductivity type; depositing a tunnel barrier layer on said further sub-base region; forming a semiconductor emitter mesa of said first conductivity type on a portion of the surface of said barrier layer; and providing collector, base, and emitter electrodes respectively coupled with said collector, base, and emitter regions. In an embodiment of this form of the invention, said barrier layer is deposited over a non-peripheral portion of a surface of said further sub-base region, and said step of forming said base electrode comprises forming said base electrode on a peripheral portion of said further sub-base region, spaced from said emitter mesa. Also in this embodiment, said step of forming said base sub-region and said further base sub-region comprises forming said base sub-region and further base sub-region as having asymmetrical band structures with respect to each other. This can be implemented by forming said further base sub-region with higher bandgap semiconductor material than the semiconductor material of said sub-base region. In an embodiment of this form of the invention, said further base sub-region is formed with a thickness of less than about 30 nm.

In accordance with another form of the invention, there is set forth a tilted-charge light-emitting semiconductor device, comprising: a layered semiconductor structure that includes a substrate, a semiconductor collector region of a first conductivity type, a semiconductor base region of a second conductivity type disposed on said collector region, and a semiconductor emitter region of said first semiconductor type disposed as a mesa over a portion of a surface of said base region; said base region including at least one region exhibiting quantum size effects; collector, base, and emitter electrodes, respectively coupled with said collector, base and emitter regions; and a tunnel barrier layer disposed over at least the exposed portion of said surface of said base region; whereby, signals applied with respect to said collector, base, and emitter electrodes can produce optical signals from said base region. In an embodiment of this form of the invention, at least a portion of said base electrode is disposed on said surface of said base region and spaced from said emitter mesa, and said tunnel barrier layer is disposed on said surface of said base region between said mesa and said base electrode. In an embodiment of this form of the invention, said at least one region exhibiting quantum size effects comprises a discontinuous or non-planar quantum size region.

In accordance with still another form of the invention, a method is set forth for producing optical signals with improved efficiency, including the following steps:

providing a layered semiconductor structure that includes a substrate, a semiconductor drain region of a first conductivity type, a semiconductor base region of a second conductivity type disposed on said drain region, and a semiconductor emitter region of said first semiconductor type disposed as a mesa over a portion of a surface of said base region; providing, in said base region, at least one region exhibiting quantum size effects; providing a base/drain electrode coupled with said base and drain regions, and providing an emitter electrode coupled with said emitter region; providing a tunnel barrier layer over at least the exposed portion of said surface of said base region; and applying signals with respect to said base base/drain and emitter electrodes to produce optical signals from said base region. In an embodiment of this form of the invention, said step of providing said electrodes includes providing at least a portion of said base/drain electrode as being disposed on said surface of said base region and spaced from said emitter mesa, and wherein said step of providing said tunnel barrier layer comprises providing said tunnel barrier layer on said surface of said base region between said mesa and said base/drain electrode.

The design of a practical optical tilted charge device includes several complex considerations including achievement of high internal quantum efficiency, manufacturability, compatibility and reliability. Therefore, transitioning from an existing design of an optical tilted charge device to another presents challenges. In accordance with another aspect of the present invention, there is provided an optical tilted charge device with a deep quantum well (with ΔE at least about 0.25 eV $\gg$ kT) while maintaining a heavily doped base region that is substantially binary. The optical tilted charge device with these features is still capable of incorporating etch stop layers that selectively stop etching at one type of semiconductor material, to assist in the definition of the emitter mesa, base mesa and collector mesa which benefits manufacturability. In addition, for reliability reasons, the base region can still be doped with carbon (p-type, NPN structure) or silicon (n-type, PNP). Compatibility is maintained, since the emission photon energies of the optical tilted charge device can still be coupled to existing InP/InGaAs based photodetectors. A further advantage is that the disclosed GaAs based optical tilted charge device hereof is compatible with the use of silicon-based substrates and lenses.

In accordance with still another form of the invention, a method is provided for making an optical tilted-charge device that is substantially matched to GaAs lattice constant, including the following steps: providing a layered semiconductor structure that includes: a GaAs substrate; a semiconductor collector region; a semiconductor base region that includes a doped GaAs second base sub-region, an InGaAsN quantum size region, and a doped GaAs first base sub-region; and a semiconductor emitter region; and providing collector, base, and emitter electrodes respectively coupled with said collector region, said base region, and said emitter region. Electrical signals, applied with respect to said collector, base, and emitter electrodes, produces light emission from said base region. In an embodiment of this form of the invention, the step of providing said collector and emitter regions comprises providing said regions as substantially GaAs, and the step of providing said second and first base sub-regions comprises providing said second and first base sub-regions as being heavily doped p-type (where, as used herein, heavily doped means at least about $10^{18}cm^{-3}$ for p-type and $10^{17}cm^{-3}$ for n-type). Also in this embodiment, the step of providing said InGaAsN quantum size region comprises providing an InGaAsN quantum well between GaAs barrier layers. Alternatively, the step of providing said InGaAsN quantum size region can comprise providing a plurality of InGaAsN quantum wells, each between GaAs barrier layers. Also in this embodiment, the method includes growing said layered semiconductor structure with intervening InAlGaP alloy etch stop layers for defining base and emitter mesas using an etchant that selectively removes arsenide-based materials. (The InAlGaP alloy for this etch stop application also includes the use of InGaP or InAlAs etch stop layers.) In a form of this embodiment, the layered semiconductor structure is deposited on a GaAs-on-Si substrate, and a Si lens is formed from said substrate.

In still another form of the invention, a method is set forth for making a two-terminal optical tilted-charge device that is substantially matched to GaAs lattice constant, including the following steps: providing a layered semiconductor structure that includes: a GaAs substrate; a semiconductor drain region; a semiconductor base region that includes a doped GaAs second base sub-region, an InGaAsN quantum size region, and a doped GaAs first base sub-region; and a semiconductor emitter region; and providing a base/collector electrode coupled with said collector and base regions, and an emitter electrode coupled with said emitter region.

Electrical signals, applied with respect to said base/drain and emitter electrodes, produces light emission from said base region.

In a further form of the invention, there is set forth an optical tilted-charge device that is substantially matched to GaAs lattice constant, comprising: a layered semiconductor structure that includes: a GaAs substrate; a semiconductor collector region; a semiconductor base region that includes a heavily doped GaAs second base sub-region, an InGaAsN quantum size region, and a heavily doped GaAs first base sub-region; and a semiconductor emitter region; said collector and emitter regions being of opposite conductivity type to the conductivity type of said base sub-regions; and collector, base, and emitter electrodes respectively coupled with said collector region, said base region, and said emitter region; whereby application of electrical signals with respect to said collector, base, and emitter electrodes will produce light emission from said base region. In an embodiment of this form of the invention, the InGaAsN quantum size region in said base region comprises a quantum well having a depth of at least about 0.25 eV. In this embodiment, the InGaAsN quantum size region comprises an InGaAsN quantum well between GaAs barrier layers. Preferably, the InGaAsN quantum size region comprises $In_xGa_{1-x}AsN$ with x at least about 0.3. Also in this embodiment, the GaAs substrate is disposed on silicon, and said silicon is in the form of a lens.

Further features and advantages of the invention will become more readily apparent from the following detailed description when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross-sectional view of an optical tilted charge device, in the form of a light-emitting transistor, in accordance with an embodiment of the invention and which can be used in practicing an embodiment of the method of the invention.

Figure 2 is a table showing the epilayer structure of an example of the Figure 1 device wherein the quantum well is within tunneling distance to the surface of the base. A tunnel barrier of the same material as the emitter is used. An asymmetric base is used to favor re-thermalization towards the collector and increase the barrier height. The tilted charge device epilayers are designed to be compatible with HBT foundry processes.

Figure 3 is a table showing the processed device DC characteristics for devices fabricated using the structure of Figures 1 and 2.

Figure 4 is a graph of light output as a function of base current for the devices of Figures 1 and 2. The distance between emitter mesa edge and base metal edge was varied from 1.5 μm to 7 μm while keeping all other dimensions the same. Increasing the distance d, equivalently increases base resistance (hole resistance) and therefore promotes, comparatively, the lateral transport of electrons in the quantum well towards the base contact. Light was measured using a large area detector via the bottom substrate and plotted vs base current (recombination current). The measured data showed that radiative recombination efficiency did not change as the distance was varied, as can be seen in Figure 4, in which the four plotted curves, for distances d ranging from 1.5 μm to 7 μm, substantially overlap and appear as a single curve.

Figure 5 is a graph which plots the capacitance C_D versus the distance d. AC analysis indicates that as the distance d is varied from 1.5 um to 7 um, the capacitance associated with the electron dynamics (i.e. charge storage capacitance, diffusion capacitance), increases. As only the lateral dimensions (d) were altered, this indicates that the capacitance area has increased due to the lateral travel of electrons via the QW, thus populating a larger area of the quantum well.

Figure 6 is a cross-sectional view of another optical tilted charge device similar to the device of Figure 1 (with like reference numerals representing similar elements), but with the device base region having a discontinuous quantum structure in the form of quantum dots, in the base region.

Figure 7 is a table showing the epilayer structure of a device in accordance with another embodiment of the invention. An asymmetric base and discontinuous quantum structure are incorporated into the design. Re-thermalization toward the collector is favored.

Figure 8 is a table showing epilayer structure of a device in accordance with another embodiment of the invention, wherein a corrugated quantum well is employed.

Figure 9 is a table showing the epilayer structure of a device in accordance with another embodiment of the invention, wherein a narrow quantum well is used in combination with a discontinuous quantum structure.

Figure 10 is a cross-sectional view of an optical tilted charge device, in the form of a light-emitting transistor, in accordance with another embodiment of the invention and which can be used in practicing another embodiment of the method of the invention.

Figure 11 is a table showing the epilayer structure of an example of the Figure 10 embodiment of the invention.

Figure 12 is a table showing the epilayer structure of a device in accordance with another embodiment of the invention.

Figure 13 is a cross-sectional view of another optical tilted charge device, in the form of a two-terminal tilted charge light-emitting diode, in accordance with a further embodiment of the invention and which can be used in practicing a further embodiment of the method of the invention.

DETAILED DESCRIPTION

Referring to Figure 1, there is shown a cross-sectional view of an optical tilted charge device, in the form of a light-emitting transistor, in accordance with an embodiment of the invention and which can be used in practicing an embodiment of the method of the invention. In Figure 1, a subcollector region 125 is disposed on an undoped substrate 110. A mesa on subcollector 125 includes a base region 140 disposed between a collector region 130 and an emitter region 160 formed on a further mesa. The base region includes one or more quantum wells 145 between an upper base region (base 1) and a lower base region (base 2). In this embodiment, a collector electrode 127 contracts a surface of subcollector region 125, a base electrode 147 contacts a surface of base region 140, and an emitter electrode 167 contacts a surface of emitter region 160. A tunnel barrier layer 150 is disposed over the top surface of the base region 140, between the base region and emitter region 160, covering, inter alia, the exposed portion of the surface of the base region.

The table of Figure 2 shows an example of a representative epilayer structure for the embodiment of Figure 1. Except where otherwise indicated, the epilayer structure can be made using existing MOCVD (metalorganic vapor deposition) and/or MBE (molecular beam epitaxy) deposition techniques, and the devices formed using existing photolithography techniques.) In this example there are two $In_{0.2}Ga_{0.8}As$ quantum wells (layers 7 and 9) within GaAs barriers. The upper quantum well (layer 9) is within tunneling distance (24 um) to the surface of base 140

(i.e., the surface of base 1 – layer 12). In this example, a tunneling barrier 150 (layer 13) of the same material as the emitter 160 (layer 14) us used; namely $In_{0.49}Ga_{0.51}As$. An asymmetric base is used to favor re-thermalization toward the collector and increase the barrier height. The tunnel barrier structure increases the distance (and reduces tunneling probability) between the carriers in the quantum well to the surface states. Without the tunnel barrier, as indicated, the tunneling distance between the quantum well and the surface state is 24 nm. With the tunnel barrier, this distance is increased to 78 nm (~3 times). Tunneling probability may also be reduced by increasing the thicknesses of layer 11 and 12 (base 1) of the epi-structure. The use of the tunnel barrier allows design that does not require a thick base 1 region (e.g. for base transit time reasons or material reasons). In the table (and other tables hereof), the third column includes, for some layers, the designation “ELDL”, which stands for the optional use of engineered long diffusion length material for these layers. In this regard reference can be made to U.S. Patent Application Publication US 2012/006815, which describes the use of such material. It will be understood, however, that the present invention does not require the use of this optional material. The third column of the tables hereof also lists a characteristic emission wavelength associated with the material system and quantum size regions.

In Figure 1, the photon (wavy) arrows indicate that usable light can be extracted either from the top or from the bottom side. In this embodiment base contact (Ti-Pt-Au) is made to layer 12, emitter contact (Au-Ge) is made to layer 15, and collector contact (Au-Ge) is made to layer 1. The device is operated with the base-emitter junction in forward bias (e.g. $V_{BE} > 1.2$ volts) and the base-collector junction in high impedance mode (not necessary reversed bias – e.g. -2.5 volts < $V_{BC} < 0.5$ volts). Carrier movement is depicted by solid arrows.

In the present embodiment, because the material of the tunnel barrier is the same as or similar to the emitter, the total effective tunnel barrier thickness, where emitter is present, is accordingly greater. If desired, the use of dissimilar materials for the emitter and tunnel barrier, for example AlGaAs emitter and InAlGaP tunnel barrier, can allow the layers to be separated during processing.

In the present embodiment, a thin 21 nm doped AlGaAs graded layering (layers 11 and 12, with Al content of 0.5% to 5%) are used to increase the barrier height and to favor re-thermalization toward the collector. A 3 nm undoped GaAs

buffer layer (layer 10) is added to reduce the contamination of dopants into the quantum well. The tilted charge device epilayers are designed to be compatible with HBT foundry processes. The processed device DC characteristics are shown in the table of Figure 3. Fabricated devices were lapped to 150 μm, and measured.

A study was performed on the effects of varying the distance between the base contact and emitter mesa (distance d in Figure 1). The distance between emitter mesa edge and base metal edge was varied from 1.5 μm to 7 μm while keeping all other dimensions the same. Increasing the distance d equivalently increases base resistance (hole resistance) and therefore promotes, comparatively, the lateral transport of electrons in the quantum well towards the base contact. Light was measured using a large area detector via the bottom substrate and plotted vs. base current (recombination current). The measured data showed that radiative recombination efficiency did not change as the distance was varied between from about 1.5 μm to 7 μm. This can be seen in Figure 4, in which the four plotted curves, for distances d ranging from 1.5 μm to 7 μm, substantially overlap and appear as a single curve. This indicates that the technique hereof, involving use of the described tunnel barrier, was successful in isolating captured electrons in the quantum well from non-radiative surface recombination. The limiting of non-radiative recombination at the surface also assists in reducing the formation of heat spots at the surface (which is an amplified issue in a low current gain transistor such as a light emitting transistor), that could lead to base-emitter leakage and reliability issues.

Further studies indicated, however, that the preservation of charge in the QW due to the previously described technique resulted in an increase of capacitance, C_D, related to the electron dynamics (i.e., base stored capacitance, diffusion capacitance). This can be seen from the graph of Figure 5, which plots the capacitance C_D versus the distance d. AC analysis indicates that as the distance d is varied from 1.5 um to 7 um, the capacitance associated with the electron dynamics (i.e. charge storage capacitance, diffusion capacitance), increases. As only the lateral dimensions (d) were altered, this indicates that the capacitance area has increased due to the lateral travel of electrons via the quantum well, thus populating a larger area of the quantum well.

In applications where it's desirable to reduce C_D, an embodiment hereof utilizes a discontinuous quantum structure (DQS) as the quantum size region in the

device's base region. The DQS, such as the quantum dots or quantum wires, provides energy gap discontinuities along the lateral axis. The physical discontinuities and the associated energy gap discontinuities (energy barriers) confine or discourage the movement of captured carriers to within the boundaries of the discontinuous quantum structure. This is shown in Figure 6, which illustrates a device similar to the device of Figure 1 (with like reference numerals representing similar elements), but with the device base region (designated 140') having a discontinuous quantum structure, in the form of quantum dots 645, in the base region. The DQS structure may be incorporated during growth of epitaxial layers (see the table of Figure 7), or by patterning of quantum structures followed by a re-growth method.

As represented in the table of Figure 7, thin n-type InGaAs layers (less than 100 nm) were used in order to enable use of non-alloy contact which is optically smoother compared to alloyed contacts such as AuGe. The resulting smoother contact layer will improve light extraction from the bottom of the substrate by reflecting photons downward. For designs of the Figure 6 embodiment where only bottom emission is desired, the exposed emitter mesa width (W) may be reduced or eliminated (e.g. by self-aligned methods) so that the entire emitter mesa width is covered by the reflecting non-alloy contact, in order to increase bottom light extraction. The thickness of the InGaAs layers are preferably thin enough to reduce photon self-absorption, but thick enough to enable the use of non-alloy contacts.

As seen in the table of Figure 7, an asymmetric DQS is incorporated into the design to favor re-thermalization toward the collector. As indicated above, other DQSs, such as quantum wires, may also be used instead of quantum dots. Relatively thin tellerium doped InGaAs sub-emitter layers are used to enable the use of Ti-Pt-Au contacts for the emitter. Ti-Pt-Au provides better reflectivity as compared to Au-Ge alloy contacts, and will offset the photon absorption loss due to the use of low bandgap InGaAs sub-emitter layers.

In the Figure 6 embodiment, as indicated, the discontinuous quantum structure is used to prevent the lateral transport of electrons towards the base contact. The edge recombination process is this Figure is exaggerated to indicate that the tilted charge device is an edge recombination device. It will be evident that by shrinking the emitter mesa dimensions it is possible to eventually obtain a "uniform" recombination distribution under the emitter mesa. Photon arrows indicate

that usable light can be extracted either from the top or from the bottom side. Base contact (Ti-Pt-Au) is made to layer 13, emitter contact (Ti-Pt-Au) is made to layer 18, and collector contact (Au-Ge) is made to layer 1 (referencing the table of Figure 7). As was noted, relatively thin tellurium doped InGaAs sub-emitter layers (layers 17 and 18) are used to enable the use of Ti-Pt-Au contacts for the emitter. Ti-Pt-Au better reflectivity vs Au-Ge alloy contacts will offset the photon absorption loss due to the use of low bandgap InGaAs sub-emitter layers. As in the Figure 1 embodiment, the device is operated with the base-emitter junction in forward bias and the base-collector junction in high impedance mode (not necessary reversed bias). A partial DBR or full DBR cavity may also be incorporated into this structure. This embodiment, and others hereof, can also be operated as a laser by providing a suitable resonant optical cavity.

In a further embodiment hereof, lateral conduction of minority carrier is reduced by the use of single or multiple highly strained corrugated (non-planar) quantum wells (C-QW) (for example, InGaAs QW in a InGaP/GaAs LET, with indium composition of more than about 20%), where the quantum well width is defined as the distance between the two barriers confining the fundamental recombination state of the quantum well. Indium composition and corrugation of quantum well can be verified using methods such as SIMS (secondary ion mass spectrometry) analysis, AFM (atomic force microscopy), FIB (focused electron beam), or high resolution TEM (transmission electron microscope). The highly strained surfaces result in growth of non-planar (corrugated) QW surfaces. (Reference can be made for example, to T. Chung, G. Walter, and N. Holonyak, Jr., “Coupled Strained Layer InGaAs Quantum Well Improvement of an InAs Quantum Dot AlGaAs-GaAs-InGaAs-InAs Heterostructure Laser,” Appl. Phys. Lett. 79, 4500-4502 (2001); G. Walter, T. Chung, and N. Holonyak, Jr., “High Gain Coupled InGaAs Quantum Well InAs Quantum Dot AlGaAs-GaAs-InGaAs-InAs Heterostructure Diode Laser Operation,” Appl. Phys. Lett. 80, 1126-1128 (2002); G. Walter, T. Chung, and N. Holonyak, Jr., “Coupled-Stripe Quantum-Well-Assisted AlGaAs-GaAs-InGaAs-InAs Quantum-Dot Laser,” Appl. Phys. Lett., 80, 3045 (2002)). Growth of corrugated QWs can be enhanced with the use of off axis substrates or pre-patterned substrates (for example, selective crystal planes or by photolithography/etching processes). A corrugated or non-planar surface provides optical and electrical wave function perturbations which distorts carrier mobility.

The epilayer structure set forth in the table of Figure 8 is for an embodiment of a tilted charge device wherein a corrugated quantum well (C-QW) is embedded with a main emission peak designed around 1020 nm. A 1020 nm emission peak light emitter may be used with high-OH (UV/VIS) fibers. (Designs for other emission wavelengths can alternativey be employed.) An asymmetric C-QW is used in this embodiment to favor re-thermalization toward the collector and to increase tunneling distance. If needed, aluminum composition in layer 6, 10 and/or 11 may be increased to reduce the emission wavelength from 1020 nm to, say, 1000 nm without having to reduce indium composition.

In a further embodiment, the epilayer structure of which is shown in the table of Figure 9, a narrow quantum well (planar QW or C-QW) is used in combination with a DQS to provide improved carrier capture ability and to assist in material growth of the DQS. As set forth in Figure 9, the tilted charge device includes a thin planar quantum well (QW) coupled via a tunneling barrier to a 5 mono layer (ML) DQS with a main emission peak designed around (but not necessarily) 1020 nm. The quantum well may be designed to have a peak emission wavelength of 1020 nm (~same energy) or 980 nm (~higher energy). A 1020 nm emission peak light emitter may be used with high-OH fibers. An asymmetric DQS is used in this design to favor re-thermalization toward the collector and to increase tunneling distance.

In a further embodiment, the features of the invention are employed in a two terminal tilted-charge light-emitting diode, of the general type disclosed in U.S. Patent Application Publication No. US2010/0202483 or U.S. Patent Application Publication No. US2012/0068151. In this device, the structure of the Figure 1 or 6 embodiments is varied, with the region beneath the base region being designated a drain region, and a peripheral base/drain electrode is coupled with the base region and the drain region. The base region, including at least one quantum size region that is preferably discontinuous or corrugated, is provided as in the prior descriptions, and the emitter mesa and emitter contact can also substantially correspond with the prior description. As before, a tunnel barrier layer is advantageously provided over the exposed portion of the base region.

Figure 10 shows a device in accordance with another embodiment of the invention, and which can be used in practicing another embodiment of the method of the invention. The semiconductor layering shown in Figure 10, from the bottom up, includes: a GaAs substrate 1110; a GaAs buffer region 1120; a sub-collector region

1130; a collector region 1140; a base region 1160 that includes a base sub-region 1162 called “base-2”, a quantum size region 1150 (one or more quantum wells or other suitable quantum size regions such as quantum dots or quantum wires), a base sub-region 1167 called “base-1”, an emitter region 1170, and a sub-emitter region 1180. In accordance with a feature hereof, an InGaAsN quantum size region is employed in the base region. The collector, base, and emitter electrodes are shown respectively as metal collector contact 1135 (which contacts the subcollector region), metal base contact 1165 (which contacts the base-1 region), and metal emitter contact 1185 (which contacts the sub-emitter region). A collimator or focusing lens 1105 can be molded to or affixed to the GaAs substrate 1110. The collimator or lens 1105 can be advantageously formed of silicon. When the device is grown on a GaAs-on-Si substrate, the lens can be formed by etching the silicon. Although a bottom light emitter is shown, the device can also be configured as a top emitter.

The table of Figure 11 shows the more detailed semiconductor epilayers of an example of the Figure 10 embodiment. The epilayer structure can be made using existing MOCVD (metalorganic vapor deposition) and/or MBE (molecular beam epitaxy) deposition techniques, and the devices formed using existing photolithography techniques. The base-2 region includes a p-type GaAs layer (layer 6), followed by a lower doped p-type GaAs material (layer 7) to complete the base-2 region. The dopant is reduced closer to the quantum well to reduce the diffusion of dopants into the quantum well region. The dopant for the p-type base region is preferably carbon, which has a relatively abrupt diffusion tail compared to most other p-type dopants such as zinc. Then, a quantum well structure including an unintentionally doped GaAs layer (layer 8) is grown to form the first barrier layer, followed by a thin (~120 A) lower bandgap InGaAsN layer, which is substantially lattice matched to GaAs (layer 9), and then completed with another thin GaAs layer as the second barrier layer (layer 10). A multiple quantum well structure may alternatively be implemented by using repetitious layers of InGaAsN and GaAs barrier layers, as shown in the table of Figure 12. The active base region of the device is then completed with the growth of the base-1 structure, including lower doped p-type GaAs layer (layer 11) and a higher doped GaAs contact layer (layer 12). Layer 14 is shown in the table as having a possibility of aluminum content, such as for index step or confinement using lateral oxidation.

InGaAsN semiconductor material, advantageously used for the quantum well hereof, is a quaternary material which uses smaller nitrogen atoms to compensate for the strain induced by the larger indium atoms, allowing the material to remain substantially matched to GaAs lattice constant. This allows higher incorporation of indium to lower the energy gap of the InGaAsN layer, resulting in a deeper quantum well, without having to increase the energy gap of the barrier layers which would require resorting to ternary composition.

The use of InGaAsN material for the quantum well also allows for the design of devices with emission peak longer than 1100 nm, which has relatively high transmission through silicon. This allows the optical tilted charge devices to be advantageously coupled to high index silicon lenses (as in Figure 10). Since the entire OTCD structure is substantially lattice matched to GaAs lattice constants, and the emission wavelength can be tailored to enable the use of silicon lenses, the disclosed devices can be directly grown on GaAs-on-Si substrates, and the lens etched from the Si. Also, for GaAs substrates, an alternative is to etch a lens in the GaAs.

In the present embodiment, low doped, and substantially matched to GaAs lattice constant, InAlGaP alloy (e.g. $In_{0.49}Ga_{0.51}P$) etch stop layers are placed in Layer 1, 4 and 13, which also define the boundaries for the base contact layer (layer 13), the collector contact layer (layer 3) and the boundary (layer 1) between the doped and undoped buffers. Layer 1 can be used to assist in the GaAs substrate removal or device isolation by allowing all conducting material to be removed and therefore electrically decoupling one device from another adjacent device. These phosphide based materials (e.g. InGaP or InAlGaP) are stable relative to etchant used to remove the arsenide based materials such as GaAs and InGaAs. Likewise, the phosphide based materials can be removed using etchant that is stable against arsenide based material. Accordingly, the phosphide based materials can be removed without affecting the arsenide materials and vice versa. A partial DBR or full DBR cavity may also be incorporated into this structure. This embodiment, and others hereof, can also be operated as a laser by providing a suitable resonant optical cavity.

In a further embodiment, the features of the invention are employed in a two terminal tilted-charge light-emitting diode, of the general type disclosed in U.S. Patent Application Publication No. US2010/0202483 or U.S. Patent Application

Publication No. US2012/0068151. In this device, the structure of the Figure 10 embodiment is varied, with the region beneath the base region being designated a drain region, and a peripheral base/drain electrode being coupled with the base region and the drain region. An example is shown in Figure 13, in which lens 1105, substrate 1110, buffer region 1120, base-1 region 1162, quantum size region 1150, base-2 region 1167, emitter region 1170, sub-emitter region 1180, and emitter contact 1185 are similar to elements of like reference numerals in Figure 10. Instead of subcollector and collector, regions, however, the Figure 13 device has subdrain region 1430 and drain region 1440. Also, instead of base and collector electrodes, the device of this embodiment has a base/drain electrode 1465. As described in the above-referenced Patent Application Publications, application of electrical signals to said base/drain and emitter electrodes produces light emission from the base region. The tilted-charge light-emitting diode of this embodiment has the same advantages in fabrication and operation as the three terminal optical tilted charge device of the Figure 10 embodiment.

The invention has been described with reference to particular preferred embodiments, but variations within the spirit and scope of the invention will occur to those skilled in the art. For example, while npn light-emitting transistors have been described, it will be understood that certain principles hereof will apply as well to pnp light-emitting transistors.

CLAIMS:

1. A method for producing optical signals with improved efficiency, comprising the steps of:

providing a layered semiconductor structure that includes a substrate, a semiconductor collector region of a first conductivity type, a semiconductor base region of a second conductivity type disposed on said collector region, and a semiconductor emitter region of said first semiconductor type disposed as a mesa over a portion of a surface of said base region;

providing, in said base region, at least one region exhibiting quantum size effects;

providing collector, base, and emitter electrodes, respectively coupled with said collector, base and emitter regions;

providing a tunnel barrier layer over at least the exposed portion of said surface of said base region; and

applying signals with respect to said collector, base, and emitter electrodes to produce optical signals from said base region.

2. The method as defined by claim 1, wherein said step of providing said electrodes includes providing at least a portion of said base electrode as being disposed on said surface of said base region and spaced from said emitter mesa, and wherein said step of providing said tunnel barrier layer comprises providing said tunnel barrier layer on said surface of said base region between said mesa and said base electrode.

3. The method as defined by claim 1or 2, wherein said step of providing said at least one region exhibiting quantum size effects comprises providing a discontinuous or non-planar quantum size region.

4. The method as defined by claim 3, wherein said step of providing said discontinuous or non-planar quantum size region comprises providing a region of quantum dots and/or quantum wires.

5. The method as defined by claim 3, wherein said step of providing said discontinuous or non-planar quantum size region comprises providing a corrugated quantum well.

6. The method as defined by claim 1 or 2, wherein said step of providing said base region comprises providing a base region that comprises substantially GaAs and AlGaAs, and said step of providing said tunnel barrier comprises providing a tunnel barrier comprising InGaP.

7. The method as defined by claim 1 or 2, wherein said step of providing said base region comprises providing a base region that includes a first base sub-region on the emitter side of said quantum size region, and a second base sub-region on the collector said of said quantum size region, and providing said first and second base sub-regions with asymmetrical band structures with respect to each other.

8. The method as defined by claim 1 or 2, further comprising disposing said base region in an optical resonant cavity, and wherein said optical signals are laser signals.

9. A method for producing a tilted-charge light-emitting device, comprising the steps of:

forming a layered semiconductor structure that includes a substrate, a semiconductor collector region of a first conductivity type, a semiconductor sub-base region of a second conductivity type, a quantum size region, and a further semiconductor sub-base region of said second conductivity type;

depositing a tunnel barrier layer on said further sub-base region;

forming a semiconductor emitter mesa of said first conductivity type on a portion of the surface of said barrier layer; and

providing collector, base, and emitter electrodes respectively coupled with said collector, base, and emitter regions.

10. The method as defined by claim 9, wherein said barrier layer is deposited over a non-peripheral portion of a surface of said further sub-base region, and wherein said step of forming said base electrode comprises forming said base

electrode on a peripheral portion of said further sub-base region, spaced from said emitter mesa.

11. The method as defined by claim 9 or 10, wherein said step of forming said quantum size region comprises forming a discontinuous or non-planar quantum size region.

12. The method as defined by claim 9, wherein said further base sub-region is formed with a thickness of less than about 30 nm.

13. A tilted-charge light-emitting semiconductor device, comprising:

a layered semiconductor structure that includes a substrate, a semiconductor collector region of a first conductivity type, a semiconductor base region of a second conductivity type disposed on said collector region, and a semiconductor emitter region of said first semiconductor type disposed as a mesa over a portion of a surface of said base region;

said base region including at least one region exhibiting quantum size effects;

collector, base, and emitter electrodes, respectively coupled with said collector, base and emitter regions; and

a tunnel barrier layer disposed over at least the exposed portion of said surface of said base region;

whereby, signals applied with respect to said collector, base, and emitter electrodes can produce optical signals from said base region.

14. The device as defined by claim 13, wherein said at least one region exhibiting quantum size effects comprises a discontinuous or non-planar quantum size region.

15. A method for producing optical signals with improved efficiency, comprising the steps of:

providing a layered semiconductor structure that includes a substrate, a semiconductor drain region of a first conductivity type, a semiconductor base region of a second conductivity type disposed on said drain region, and a

semiconductor emitter region of said first semiconductor type disposed as a mesa over a portion of a surface of said base region;

providing, in said base region, at least one region exhibiting quantum size effects;

providing a base/drain electrode coupled with said base and drain regions, and providing an emitter electrode coupled with said emitter region;

providing a tunnel barrier layer over at least the exposed portion of said surface of said base region; and

applying signals with respect to said base base/drain and emitter electrodes to produce optical signals from said base region.

16. The method as defined by claim 15, wherein said step of providing said at least one region exhibiting quantum size effects comprises providing a discontinuous or non-planar quantum size region.

17. A method for making an optical tilted-charge device that is substantially matched to GaAs lattice constant, comprising the steps of:

providing a layered semiconductor structure that includes: a GaAs substrate; a semiconductor collector region; a semiconductor base region that includes a doped GaAs second base sub-region, an InGaAsN quantum size region, and a doped GaAs first base sub-region; and a semiconductor emitter region; and

providing collector, base, and emitter electrodes respectively coupled with said collector region, said base region, and said emitter region.

18. The method as defined by claim 17, further comprising the step of applying electrical signals with respect to said collector, base, and emitter electrodes to produce light emission from said base region.

19. The method as defined by claim 17 or 18, wherein said step of providing said InGaAsN quantum size region comprises providing an InGaAsN quantum well between GaAs barrier layers.

20. The method as defined by claim 19, further comprising growing said layered semiconductor structure with intervening InAlGaP alloy etch stop layers for defining base and emitter mesas using an etchant that selectively removes arsenide-based materials.

21. The method as defined by claim 17 or 18, further comprising forming said layered semiconductor structure on a GaAs-on-Si substrate, and further comprising forming a Si lens from said substrate.

22. A method for making a two-terminal optical tilted-charge device that is substantially matched to GaAs lattice constant, comprising the steps of:

providing a layered semiconductor structure that includes: a GaAs substrate; a semiconductor drain region; a semiconductor base region that includes a doped GaAs second base sub-region, an InGaAsN quantum size region, and a doped GaAs first base sub-region; and a semiconductor emitter region; and

providing a base/collector electrode coupled with said collector and base regions, and an emitter electrode coupled with said emitter region.

23. The method as defined by claim 22, further comprising the step of applying electrical signals with respect to said emitter and base/drain electrodes to produce light emission from said base region.

24. The method as defined by claim 22 or 23, wherein said step of providing said InGaAsN quantum size region comprises providing an InGaAsN quantum well between GaAs barrier layers.

25. The method as defined by claim 22 or 23, further comprising forming said layered semiconductor structure on a GaAs-on-Si substrate, and further comprising forming a Si lens from said substrate.

26. An optical tilted-charge device that is substantially matched to GaAs lattice constant, comprising:

a layered semiconductor structure that includes: a GaAs substrate; a semiconductor collector region; a semiconductor base region that includes a heavily

doped GaAs second base sub-region, an InGaAsN quantum size region, and a heavily doped GaAs first base sub-region; and a semiconductor emitter region; said collector and emitter regions being of opposite conductivity type to the conductivity type of said base sub-regions; and

collector, base, and emitter electrodes respectively coupled with said collector region, said base region, and said emitter region;

whereby application of electrical signals with respect to said collector, base, and emitter electrodes will produce light emission from said base region.

27. The optical tilted-charge device as defined by claim 26, wherein said InGaAsN quantum size region in said base region comprises a quantum well having a depth of at least about 0.25 eV.

28. The optical tilted-charge device as defined by claim 26 or 27, wherein said InGaAsN quantum size region comprises an InGaAsN quantum well between GaAs barrier layers.

29. The optical tilted-charge device as defined by claim 26, wherein said GaAs substrate is disposed on silicon, and wherein said silicon is in the form of a lens.

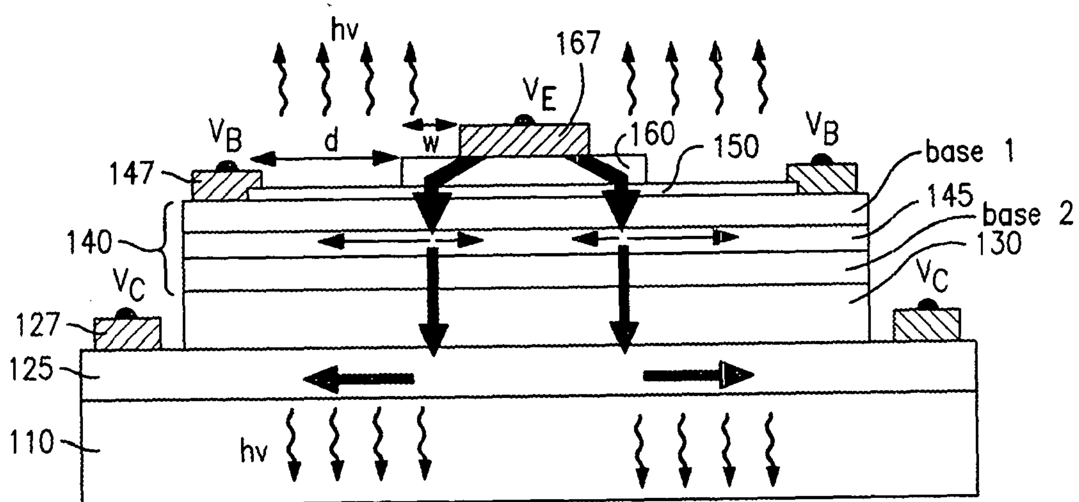


FIG. 1

Layer	Comment	Character	Material	x	Thickness (Å)	Type	Dopant	Level (/cm^3)
16	Sub-Emitter		In(x)Ga(1-x)As	0.500	50	N	Si	1.0E+19
15	Sub-Emitter		In(x)Ga(1-x)As	0.000	2730	N	Si	5.0E+18
14	Emitter		In(x)Ga(1-x)P	0.490	230	N-	Si	2.0E+17
13	Sub-Emitter		In(x)Ga(1-x)P	0.490	300	N-	Si	2.0E+17
12	Base 1	ELDL	Al(x)Ga(1-x)As	0.050	110	P	C	5.0E+19
11	Base 1	ELDL	Al(x)Ga(1-x)As	0.005 to 0.05	100	P	C	1.0E+19
10	Base 1, Buffer		GaAs	0.000	30	i	UID	1.0E+16
9		980 nm	In(x)Ga(1-x)As	0.200	120	i	UID	1.0E+16
8			Gaas		30	i	UID	1.0E+16
7		980 nm	In(x)Ga(1-x)As	0.200	120	i	UID	1.0E+16
6	Base 2, Buffer		Gaas	0.000	30	i	UID	1.0E+16
5	Base 2	ELDL	Al(x)Ga(1-x)As	0.000	100	P	C	1.0E+19
4	Base 2	ELDL	Al(x)Ga(1-x)As	0.000	720	P	C	5.0E+19
3	Collector		Al(x)Ga(1-x)As	0.000	2160	I	UID	1.0E+16
2	Ordered		In(x)Ga(1-x)P	0.490	120	N-	Si	3.0E+17
1	Sub-Collector		GaAs		5000	N	Si	5.0E+18
0	Buffer		GaAs		3000	UID	UID	UID
	Substrate		4" GaAs			SI (US)		

FIG. 2

Parameter Name	Unit	Mean
Emitter Sheet Resistance	Ω/sq	38.76
Emitter Spec. Contact Resistivity	10^{-7} Ω cm^2	13.18
Base Sheet Resistance	Ω/sq	142.43
Base Spec. Contact Resistivity	10^{-7} Ω cm^2	1.89
Collector Sheet Resistance	Ω/sq	15.89
Collector Sp. Contact Resistivity	10^{-6} Ω cm^2	0.58
Current Gain @ 1KA/cm^2 14x14		1.47
Vce Offset Voltage @ I_B=100μA	V	0.16
BVbeo @ 2A/cm^2	V	7.69
BVbeo @ 2A/cm^2	V	9.78
BVbeo @ 2A/cm^2	V	10.70

FIG. 3

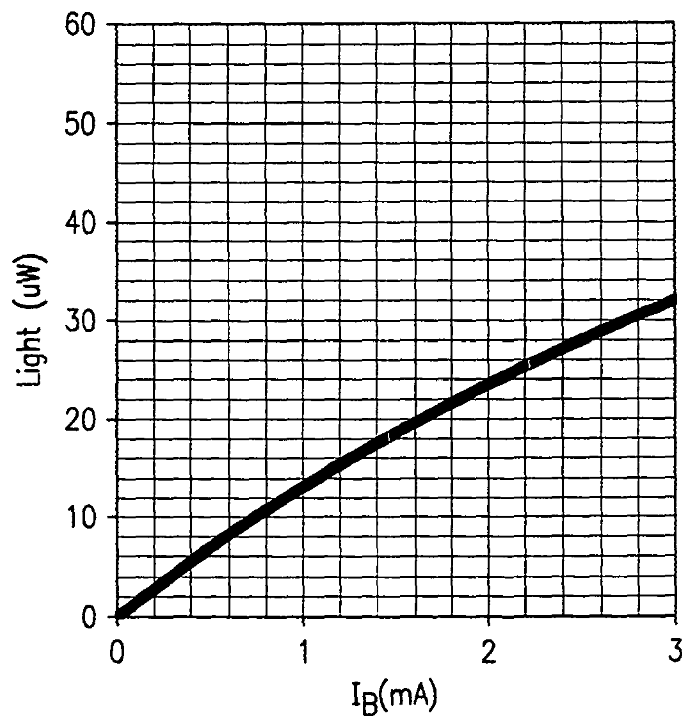


FIG. 4

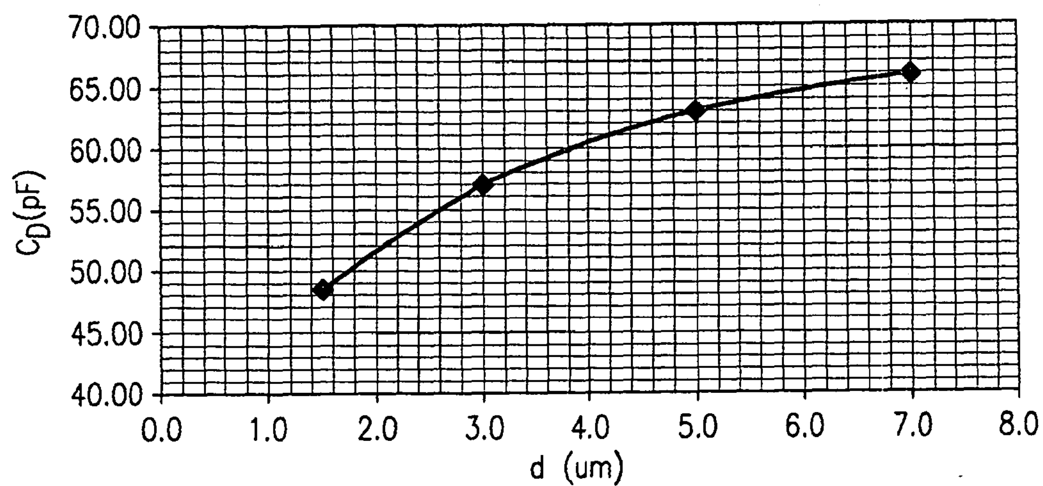


FIG. 5

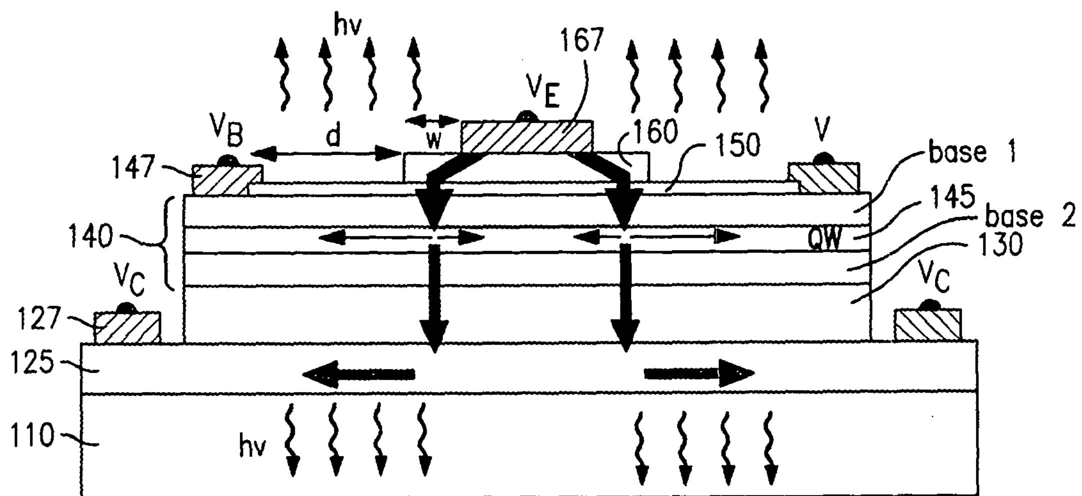


FIG. 6

Layer	Comment	Character	Material	x	Thickness (Å)	Type	Dopant	Level (/cm^3)
18	Sub-Emitter		In(x)Ga(1-x)As	0.500	500	N	Te	2.0E+19
17	Sub-Emitter		In(x)Ga(1-x)As	0.0-0.5	500	N	Te	2.0E+19
16	Sub-Emitter		Al(x)Ga(1-x)As	0.000	1200	N	Si	5.0E+18
15	Emitter		In(x)Ga(1-x)P	0.490	230	N-	Si	2.0E+17
14	Tunnel Barrier		In(x)Ga(1-x)P	0.490	300	N-	Si	2.0E+17
13	Base 1		Al(x)Ga(1-x)As	0.050	150	P	C	5.0E+19
12	Base 1	ELDL	Al(x)Ga(1-x)As	0.005 to 0.05	200	P	C	1.0E+19
11	Base 1, Buffer		GaAs	0.000	30	i	UID	1.0E+16
10	DQS	1000 nm	In(x)Ga(1-x)As		5 ML	i	UID	1.0E+16
9			GaAs	0.000	30	i	UID	1.0E+16
8	DQS	1000 nm	In(x)Ga(1-x)As		5 ML	i	UID	1.0E+16
7	Base 2, Buffer		GaAs	0.000	30	i	UID	1.0E+16
6	Base 2	ELDL	Al(x)Ga(1-x)As	0.000	150	P	C	1.0E+19
5	Base 2	ELDL	Al(x)Ga(1-x)As	0.000	120	P	C	5.0E+19
4	Base 2	ELDL	Al(x)Ga(1-x)As	0.000	650	P	C	5.0E+19
3	Collector		Al(x)Ga(1-x)As	0.000	2160	I	UID	1.0E+16
2	Ordered		In(x)Ga(1-x)P	0.490	120	N-	Si	3.0E+17
1	Sub-Collector		GaAs		5500	N	Si	5.0E+18
0	Buffer		GaAs		3000	UID	UID	UID
	Substrate		4" GaAs			SI (US)		

FIG. 7

Layer	Comment	Character	Material	x	Thickness (Å)	Type	Dopant	Level (/cm^3)
16	Sub-Emitter		In(x)Ga(1-x)As	0.500	500	N	Te	2.0E+19
15	Sub-Emitter		In(x)Ga(1-x)As	0.0-0.5	500	N	Te	2.0E+19
14	Sub-Emitter		Al(x)Ga(1-x)As	0.000	1200	N	Si	5.0E+18
13	Emitter		In(x)Ga(1-x)P	0.490	230	N-	Si	2.0E+17
12	Tunnel Barrier		In(x)Ga(1-x)P	0.490	300	N-	Si	2.0E+17
11	Base 1		Al(x)Ga(1-x)As	0.050	150	P	C	5.0E+19
10	Base 1	ELDL	Al(x)Ga(1-x)As	0.005 to 0.050	200	P	C	1.0E+19
9	Base 1, Buffer		GaAs	0.000	30	i	UID	1.0E+16
8	C-QW	1010 nm	In(x)Ga(1-x)As	0.250	100	i	UID	1.0E+16
7	Base 2, Buffer		GaAs	0.000	30	i	UID	1.0E+16
6	Base 2	ELDL	Al(x)Ga(1-x)As	0.000	100	P	C	1.0E+19
5	Base 2	ELDL	Al(x)Ga(1-x)As	0.000	180	P	C	5.0E+19
4	Base 2	ELDL	Al(x)Ga(1-x)As	0.000	640	P	C	5.0E+19
3	Collector		Al(x)Ga(1-x)As	0.000	2160	I	UID	1.0E+16
2	Ordered		In(x)Ga(1-x)P	0.490	120	N-	Si	3.0E+17
1	Sub-Collector		GaAs		5500	N	Si	5.0E+18
0	Buffer		GaAs		3000	UID	UID	UID
	Substrate		4" GaAs			SI (US)		

FIG. 8

Layer	Comment	Character	Material	x	Thickness (Å)	Type	Dopant	Level (/cm³)
18	Sub-Emitter		In(x)Ga(1-x)As	0.500	500	N	Te	2.0E+19
17	Sub-Emitter		In(x)Ga(1-x)As	0.0-0.5	500	N	Te	2.0E+19
16	Sub-Emitter		Al(x)Ga(1-x)As	0.000	1200	N	Si	5.0E+18
15	Sub-Emitter		In(x)Ga(1-x)P	0.490	230	N-	Si	2.0E+17
14	Tunnel Barrier		In(x)Ga(1-x)P	0.490	300	N-	Si	2.0E+17
13	Base 1	ELDL	Al(x)Ga(1-x)As	0.000	200	P	C	5.0E+19
12	Base 1	ELDL	Al(x)Ga(1-x)As	0.000	150	P	C	1.0E+19
11	Base 1, Buffer		GaAs	0.000	30	i	UID	1.0E+16
10	DQS	1020 nm	In(x)Ga(1-x)As		5 ML	i	UID	1.0E+16
9	Base 2, Buffer		GaAs	0.000	20	i	UID	1.0E+16
8	QW	1020 nm	In(x)Ga(1-x)As		50	i	UID	1.0E+16
7	Buffer		GaAs	0.000	30	i	UID	1.0E+16
6	Base 2	ELDL	Al(x)Ga(1-x)As	0.000	150	P	C	1.0E+19
5	Base 2	ELDL	Al(x)Ga(1-x)As	0.000	130	P	C	5.0E+19
4	Base 2	ELDL	Al(x)Ga(1-x)As	0.000	640	P	C	5.0E+19
3	Collector		Al(x)Ga(1-x)As	0.000	2160	I	UID	1.0E+16
2	Ordered		In(x)Ga(1-x)P	0.490	120	N-	Si	3.0E+17
1	Sub-Collector		GaAs		5500	N	Si	5.0E+18
0	Buffer		GaAs		3000	UID	UID	UID
	Substrate		4" GaAs			SI (US)		

FIG. 9

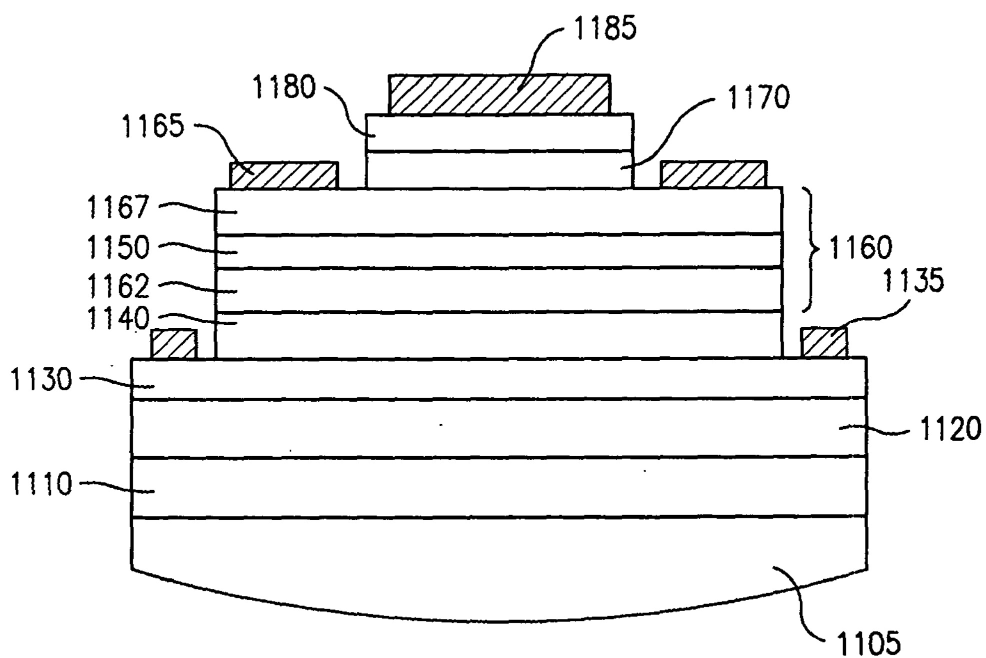


FIG. 10

Layer	Comment	Material	x	Thickness (Å)	Type	Dopant	Level (/cm^3)
16	Sub-Emitter/Contact	In(x)Ga(1-x)As	0.500	500	N	Te	2.0E+19
15	Sub-Emitter	In(x)Ga(1-x)As	0.0-0.5	500	N	Te	2.0E+19
14	Emitter	Al(x)Ga(1-x)As	0.000	1200	N	Si	5.0E+18
13	Emitter/Etch Stop	In(x)Ga(1-x)P	0.490	530	N-	Si	2.0E+17
12	Base 1/Contact	GaAs	0.000	150	P	C	5.0E+19
11	Base 1	GaAs	0.000	200	P	C	1.0E+19
10	Barrier 1	GaAs	0.000	60	i	UID	1.0E+16
9	QW	InGaAsN		120	i	UID	1.0E+16
8	Barrier 2	GaAs	0.000	60	i	UID	1.0E+16
7	Base 2	GaAs	0.000	100	P	C	1.0E+19
6	Base 2	GaAs	0.000	630	P	C	5.0E+19
5	Collector	GaAs	0.000	3000	I	UID	1.0E+16
4	Etch Stop	In(x)Ga(1-x)P	0.490	120	N-	Si	3.0E+17
3	Sub-Collector/Contract	GaAs		5500	N	Si	5.0E+18
2	Buffer	GaAs		1500	UID	UID	UID
1	Etch Stop	In(x)Ga(1-x)P	0.490	250	N-	Si	3.0E+17
0	Buffer	GaAs		1000	UID	UID	UID
	Substrate	4" GaAs			SI		

FIG. 11

Layer	Comment	Material	x	Thickness (Å)	Type	Dopant	Level (/cm^3)
18	Sub-Emitter/Contract	In(x)Ga(1-x)As	0.500	500	N	Te	2.0E+19
17	Sub-Emitter	In(x)Ga(1-x)As	0.0-0.5	500	N	Te	2.0E+19
16	Emitter	Al(x)Ga(1-x)As	0.000	1200	N	Si	5.0E+18
15	Emitter/Etch Stop	In(x)Ga(1-x)P	0.490	530	N-	Si	2.0E+17
14	Base 1/Contact	Al(x)Ga(1-x)As	0.000	150	P	C	5.0E+19
13	Base 1	Al(x)Ga(1-x)As	0.000	200	P	C	1.0E+19
12	Barrier 1	GaAs	0.000	60	i	UID	1.0E+16
11	QW 1	InGaAsN		120	i	UID	1.0E+16
10	Barrier	GaAs	0.000	60	i	UID	1.0E+16
9	QW 2	InGaAsN		120	i	UID	1.0E+16
8	Barrier 2	GaAs	0.000	60	i	UID	1.0E+16
7	Base 2	Al(x)Ga(1-x)As	0.000	100	P	C	1.0E+19
6	Base 2	Al(x)Ga(1-x)As	0.000	630	P	C	5.0E+19
5	Collector	Al(x)Ga(1-x)As	0.000	3000	I	UID	1.0E+16
4	Etch Stop	In(x)Ga(1-x)P	0.490	120	N-	Si	3.0E+17
3	Sub-Collector/Contract	GaAs		5500	N	Si	5.0E+18
2	Buffer	GaAs		1500	UID	UID	UID
1	Etch Stop	In(x)Ga(1-x)P	0.490	250	N-	Si	3.0E+17
0	Buffer	GaAs		1000	UID	UID	UID
	Substrate	4" GaAs			SI		

FIG. 12

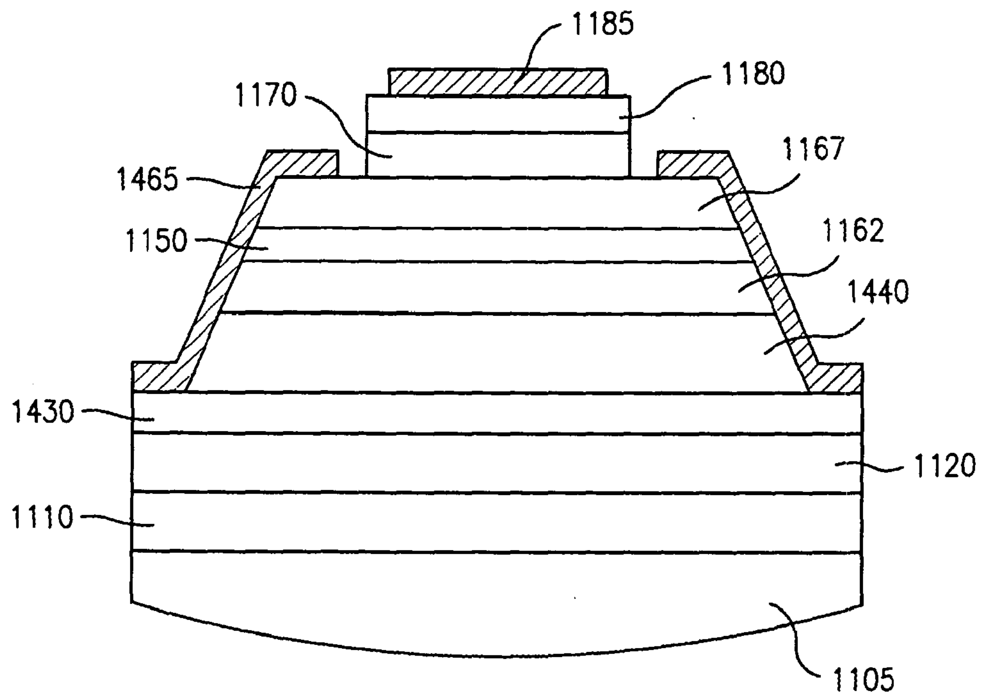


FIG. 13

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2012/064778

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/737(2006.01)i, H01L 29/778(2006.01)i, H01L 33/00(2010.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/00; H01L 33/04; H05B 37/02; H01S 5/20

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: optical tiltied charge device, collector, base, emitter, tunnel barrier, InGaP, InGaAsN

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2010-0289427 A1 (GABRIEL WALTER et al.) 18 November 2010 See abstract, paragraphs [0006]-[0017],[0046]-[0048] and figures 1,16,20	1-3,6-19,21-29
Y A	WO 2007-121524 A1 (EPITACTIX PTY LTD.) 01 November 2007 See abstract, page 5,lines 15-20 and figures 2,12A,12B	1-3,6-16 17-19,21-29
Y A	US 2003-0211647 A1 (DAVID P. BOUR et al.) 13 November 2003 See abstract, paragraphs [0025]-[0034] and figures 1A,1B	17-19,21-29 1-3,6-16
A	US 2010-0202484 A1 (NICK HOLONYAK, JR. et al.) 12 August 2010 See abstract, paragraphs [0012]-[0013],[0033]-[0042] and figures 8-11	1-3,6-19,21-29
A	US 2005-0007323 A1 (LAN ROBERT APPELBAUM et al.) 13 January 2005 See abstract, paragraphs [0031]-[0037] and figure 2A	1-3,6-19,21-29

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

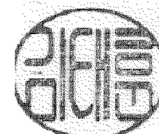
Date of the actual completion of the international search
27 FEBRUARY 2013 (27.02.2013)

Date of mailing of the international search report
04 MARCH 2013 (04.03.2013)

Name and mailing address of the ISA/KR

Facsimile No. 82-42-472-7140

Authorized officer
KIM, Tae Hoon



Telephone No. 82-42-481-8407

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2012/064778

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2010-0289427 A1	18.11.2010	NONE	
WO 2007-121524 A1	01.11.2007	NONE	
US 2003-0211647 A1	13.11.2003	EP 1361601 A2	12.11.2003
		EP 1361601 A3	27.07.2005
		JP 2003-332696 A	21.11.2003
		US 6756325 B2	29.06.2004
		US 7033938 B2	25.04.2006
		US 2004-0219703 A1	04.11.2004
US 2010-0202484 A1	12.08.2010	AU 2011-203817 A1	04.08.2011
		CA 2748597 A1	15.07.2010
		CN 102273029 A	07.12.2011
		EP 2386132 A2	16.11.2011
		JP 2012-514870 A	28.06.2012
		KR 10-2011-0112415 A	12.10.2011
		TW 201034324 A	16.09.2010
		US 2010-0202483 A1	12.08.2010
		WO 2010-080694 A2	15.07.2010
		WO 2010-080694 A3	07.10.2010
US 2005-0007323 A1	13.01.2005	US 7244997 B2	17.07.2007