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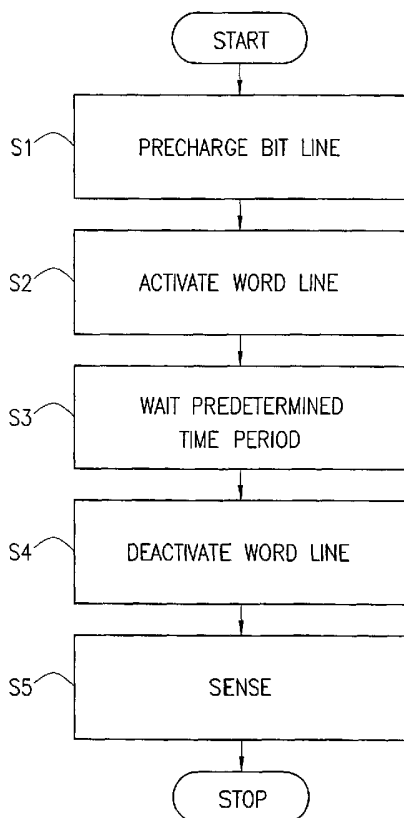
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[Continued on next page]

(54) Title: PCRAM REWRITE PREVENTION



(57) Abstract: A programmable conductor memory cell is read by a sense amplifier but without rewriting the contents of the memory cell. If the programmable contact memory cell has an access transistor, the access transistor is switched off to decouple the cell from the bit line after a predetermined amount of time. The predetermined amount of time is sufficiently long enough to permit the logical state of the cell to be transferred to the bit line and also sufficiently short to isolate the cell from the bit line before the sense amplifier operates. For programmable contact memory cells which do not utilize an access transistor, an isolation transistor may be placed in the bit line located between and serially connection the portion of the bit line from the sense amplifier to the isolation transistor and the portion of the bit line from the isolation transistor to the memory cell. The isolation transistor, normally conducting, is switched off after the predetermined time past the time the bit line begins to discharge through the programmable contact memory cell, thereby isolating the programmable contact memory cell from the sense amplifier before a sensing operation begins.

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PCRAM REWRITE PREVENTION

FIELD OF INVENTION

[0001] The present invention relates to integrated memory circuits. More specifically, it relates to a method for reading a programmable conductor random access memory (PCRAM) cell.

BACKGROUND OF THE INVENTION

[0002] Dynamic random access memory (DRAM) integrated circuit arrays have existed for more than thirty years and their dramatic increase in storage capacity has been achieved through advances in semiconductor fabrication technology and circuit design technology. The tremendous advances in these two technologies have also achieved higher levels of integration that permit dramatic reductions in memory array size and cost, as well as increased process yield.

[0003] Fig. 1 is a schematic diagram of a DRAM memory cell 100 comprising an access transistor 101 and a capacitor 102. The capacitor 102, which is coupled to a $V_{cc}/2$ potential source and the transistor 101, stores one bit of data in the form of a charge. Typically, a charge of one polarity (e.g., a charge corresponding to a potential difference across the capacitor 102 of $+V_{cc}/2$) is stored in the capacitor 102 to represent a binary "1" while a charge of the opposite polarity (e.g., a charge corresponding to a potential difference across the capacitor 102 of $-V_{cc}/2$) represents a binary "0." The gate of the transistor 101 is coupled to a word line 103, thereby permitting the word line 103 to control whether the capacitor 102 is conductively coupled via the transistor 101 to a bit

line 104. The default state of each word line 103 is at ground potential, which causes the transistor 101 to be switched off, thereby electrically isolating capacitor 102.

[0004] One of the drawbacks associated with DRAM cells 100 is that the charge on the capacitor 102 may naturally decay over time, even if the capacitor 102 remains electrically isolated. Thus, DRAM cells 100 require periodic refreshing. Additionally, as discussed below, refreshing is also required after a memory cell 100 has been accessed, for example, as part of a read operation.

[0005] Fig. 2 illustrates a memory device 200 comprising a plurality of memory arrays 150a, 150b. (Generally, in the drawings, elements having the same numerical value are of the same type. For example, sense amplifiers 300a and 300b in Fig. 2 have identical circuitry to sense amplifier 300 of Fig. 3. A lower case alphabetic suffix is generally used to discriminate between different units of the same type. However, upper case prefixes, such as “N” and “P” may denote different circuitry associated with negative or positive typed variants.) Each memory array 150a, 150b includes a plurality of memory cells 100a-100d, 100e-100h arranged by tiling a plurality of memory cells 100 together so that the memory cells 100 along any given bit line 104a, 104a', 104b, 104b' do not share a common word line 103a-103d. Conversely, the memory cells 100 along any word line 103 do not share a common bit line 104a, 104a', 104b, 104b'. Each memory array has its own set of bit lines. For example, memory array 150a includes bit lines 104a, 104b, while memory array 150b includes bit lines 104a', 104b'. The bit lines from each adjacent pair of memory arrays 150a, 150b are coupled to a common sense amplifier 300a, 300b. For example, bit lines

104a, 104a' are coupled to sense amplifier 300a, while bit lines 104b, 104b' are coupled to sense amplifier 300b. As explained below, the sense amplifiers 300a, 300b are used to conduct the sense/refresh portion when a memory cell 100a-100h is read.

[0006] Reading a DRAM memory cell comprises the operations of accessing and sensing/refreshing.

[0007] The purpose of the access operation is to transfer charge stored on the capacitor 102 to the bit line 104 associated with the memory cell 100. The access operation begins by precharging each bit line 104a, 104a', 104b, 104b' to a predetermined potential (e.g., $V_{cc}/2$) by coupling each bit line 104a, 104b to a potential source (not illustrated). Each bit line 104a, 104b is then electrically disconnected. The bit lines 104a, 104a', 104b, 104b' will float at the predetermined potential due to the inherent capacitance of the bit lines 104a, 104a', 104b, 104b'. Subsequently, the word line (e.g., 103a) associated with a memory cell being read (e.g., 100a) is activated by raising its potential to a level which causes each transistor 101a, 101e coupled to the word line 103a to gate. It should be noted that due to inherent parasitic capacitance between bit lines 104 and word lines 103, activation of a word line 103 will cause the potential at each associated bit line 104 to increase slightly. However, in typical DRAM systems, the magnitude of this potential change is insignificant in comparison to the magnitude of the potential change on the bit lines due to charge sharing. Therefore, with respect to DRAM systems only, further discussion regarding the effect of parasitic capacitance is omitted.

[0008] Activation of the word line 103a causes each capacitor 102a, 102e of each memory cell 100a, 100e coupled to that word line 103a to share its charge with its associated bit line 104a, 104b. The bit lines 104a', 104b' in the other array 150b remain at the pre-charge potential. The charge sharing causes the bit line 104a, 104b potential to either increase or decrease, depending upon the charge stored in the capacitors 102a, 102e. Since only the bit lines 104a, 104b of one memory array has its potential altered, at each sense amplifier 300a, 300b, a differential potential develops between the bit lines 104a, 104b associated with the activated word line 103a and the other bit lines 104a', 104b' associated with the same sense amplifier 300a, 300b. Thus, the access operation causes the bit lines 104a, 104b associated with the cell 100a being read to have a potential which is either greater than or less than the pre-charged voltage. However, the change in potential is small and requires amplification before it can be used.

[0009] The sense/refresh operation serves two purposes. First, the sense/refresh operation amplifies the small change in potential to the bit line coupled to the cell which was accessed. If the bit line has a potential which is lower than the pre-charge potential, the bit line will be driven to ground during sensing. Alternatively, if the bit line has a potential which is higher than the pre-charge potential, the bit line will be driven to Vcc during sensing. The second purpose of the sense/refresh operation is to restore the state of the charge in the capacitor of the accessed cell to the state it had prior to the access operation. This step is required since the access operation diluted the charge stored on the capacitor by sharing it with the bit line.

[0010] Fig. 3 is a detailed illustration of a sense amplifier 300, which comprises a N-sense amp 310N and a P-sense amp portion 310P. The N-sense amp 310N and the P-sense amp 310P include nodes NLAT* and ACT, respectively. These nodes are coupled to controllable potential sources (not illustrated). Node NLAT* is initially biased to the pre-charge potential of the bit lines 104 (e.g., $V_{cc}/2$) while node ACT is initially biased to ground. In this initial state, the transistors 301-304 of the N- and P- sense amps 310N, 310P are switched off. The sense/refresh operation is a two phased operation in which the N- sense amp 310N is triggered before the P- sense amp 310P.

[0011] The N- sense amp 310N is triggered by bringing the potential at node NLAT* from the pre-charge potential (e.g., $V_{cc}/2$) towards ground potential. As the potential difference between node NLAT* and the bit lines 104a, 104a', 104b, 104b' approach the threshold potential of NMOS transistors 301, 302, the transistor with the gate coupled to the higher voltage bit line begins to conduct. This causes the lower voltage bit line to discharge towards the voltage of the NLAT* node. Thus, when node NLAT* reaches ground potential, the lower voltage bit line will also reach ground potential. The other NMOS transistor never conducts since its gate is coupled to the low voltage digit line being discharged towards ground.

[0012] The P- sense amp 310P is triggered (after the N- sense amp 310N has been triggered) by bringing the potential at node ACT from ground towards V_{cc} . As the potential of the lower voltage bit line approaches ground (caused by the earlier triggering of the N- sense amp 310N), the PMOS transistor with its gate coupled to the lower

potential bit line will begin to conduct. This causes the initially higher potential bit line to be charged to a potential of V_{cc} . After both the N- and P- sense amps 310N, 310P have been triggered, the higher voltage bit line has its potential elevated to V_{cc} while the lower potential bit line has its potential reduced to ground. Thus, the process of triggering both sense amps 310N, 310P amplifies the potential difference created by the access operation to a level suitable for use in digital circuits. In particular, the bit line 104a associated with the memory cell 100a being read is driven from the pre-charge potential of $V_{cc}/2$ to ground if the memory cell 100a stored a charge corresponding to a binary 0, or to V_{cc} if the memory cell 100a stored a charge corresponding to a binary 1, thereby permitting a comparator (or differential amplifier) 350a coupled to bit lines 104a, 104a' to output a binary 0 or 1 consistent with the data stored in the cell 100a on signal line 351. Additionally, the charge initially stored on the capacitor 102a of the accessed cell is restored to its pre-access state.

[0013] Efforts continue to identify other forms of memory elements for use in memory cells. Recent studies have focused on resistive materials that can be programmed to exhibit either high or low stable ohmic states. A programmable resistance element of such material could be programmed (set) to a high resistive state to store, for example, a binary "1" data bit or programmed to a low resistive state to store a binary "0" data bit. The stored data bit could then be retrieved by detecting the magnitude of a readout current switched through the resistive memory element by an access device, thus indicating the stable resistance state it had previously been programmed to.

[0014] Recently chalcogenide glasses fabricated with solid electrolyte such as a metal doped chalcogenide have been investigated as data storage memory cells for use in memory devices, such as DRAM memory devices. U.S. Patents 5,761,115, 5,896,312, 5,914,893, and 6,084,796 all describe this technology and are incorporated herein by reference. The storage cells are called programmable conductor cells (alternatively, they are also known as programmable metallization cells). One characteristic of such a cell is that it typically includes solid metal electrolyte such as a metal doped chalcogenide and a cathode and anode spaced apart on a surface of the fast ion conductor. Application of a voltage across the cathode and anode causes growth of a metal dendrite which changes the resistance and capacitance of the cell which can then be used to store data.

[0015] One particularly promising programmable, bi-stable resistive material is an alloy system including Ge:Se:Ag. A memory element comprised of a chalcogenide material has a natural stable high resistive state but can be programmed to a low resistance state by passing a current pulse from a voltage of suitable polarity through the cell. This causes a programmable conductor, also known as a dendrite, to grow between the anode and cathode which lowers the cell resistance. A chalcogenide memory element is simply written over by the appropriate current pulse and voltage polarity (reverse of that which writes the cell to a low resistance state) to reprogram it, and thus does not need to be erased. Moreover, a memory element of chalcogenide material is nearly nonvolatile, in that it need only be rarely (e.g., once per week) connected to a power supply or refreshed, in order to retain its programmed low resistance state. Such memory cells, unlike DRAM cells, can be accessed without requiring a refresh.

[0016] While conventional sense amp circuitry, such as those associated with DRAM cells, are capable of sensing programmable conductor random access memory (PCRAM) cells, the natural refresh operation associated with these sense amplifiers are not required in a PCRAM context. Indeed, frequent rewriting of PCRAM cells is not desirable because it can cause the PCRAM cell to become resistant to rewriting. Accordingly, there is a need and desire for a circuit and method for reading PCRAM cells without refreshing them.

SUMMARY OF THE INVENTION

[0017] The present invention is directed to a method and apparatus for reading a PCRAM memory cell without refreshing the cell. At a predetermined time after the programmable conductor of the PCRAM cell has been coupled to its bit line, the programmable conductor is electrically decoupled from the bit line. The predetermined time is chosen to be a point in time before the N- and P- sense amplifiers have been activated. In this manner, the N- and P- sense amplifier can change the potential on the bit line without causing the altered potential to rewrite the PCRAM cell. In PCRAM arrays which use access transistors having gates coupled to word lines, the present invention may be practiced by deactivating the word line at the predetermined time after the word line has been activated. In PCRAM arrays which do not include access transistors, isolation transistors may be added on each bit line between the PCRAM cell and the sense amplifier to decouple the PCRAM cells from their associated bit lines.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] The foregoing and other advantages and features of the invention will become more apparent from the detailed description of exemplary embodiments of the invention given below with reference to the accompanying drawings in which:

[0019] FIG. 1 is a schematic diagram of a conventional DRAM cell;

[0020] FIG. 2 is a schematic diagram of a conventional DRAM array;

[0021] FIG. 3 is schematic diagram a conventional sense amplifier;

[0022] FIG. 4 is a schematic diagram of a PCRAM cell;

[0023] FIG. 5 is a schematic diagram a PCRAM array;

[0024] FIGS. 6A and 6B are timing diagrams illustrating the voltages on the word and bit lines when a PCRAM cell is read in high resistance and low resistance states, respectively.

[0025] FIG. 7 is a flow chart illustrating the method of the invention;

[0026] FIG. 8 is a block diagram of a processor based system including a PCRAM in accordance with the principles of the present invention;

[0027] FIG. 9 is a schematic diagram of a PCRAM array according to a second embodiment of the present invention; and

[0028] FIG. 10 is a schematic diagram of an alternative embodiment of a PCRAM cell for use with the PCRAM array of FIG. 9.

DETAILED DESCRIPTION OF THE INVENTION

[0029] Now referring to the drawings, where like reference numerals designate like elements, there is shown in Fig. 4 a PCRAM cell 400 and in Fig. 5 a memory device 500 a memory device comprised of a plurality of PCRAM cells 400a-400h. As illustrated in Fig. 4, a PCRAM cell 400 comprises an access transistor 401, a programmable conductor memory element 402, and a cell plate 403. The access transistor 401 has its gate coupled to a word line 405 and one terminal coupled to a bit line 406. A small portion of an array of such cells is shown in Fig. 5 as including bit lines 406a, 406a', 406b, 406b', and word lines 405a, 405b, 405c, and 405d. As shown in Fig. 5, the bit lines 406a, 406b are coupled to a respective pre-charge circuits 501a, 105b, which can switchably supply a pre-charge potential to the bit lines 406a, 406a', 406b, 406b'. The other terminal of the access transistor 401 is coupled to one end of the programmable conductor memory element 402, while the other end of the programmable conductor memory element 402 is coupled to a cell plate 403. The cell plate 403 may span and be coupled to several other

PCRAM cells. The cell plating 403 is also coupled to a potential source. In the exemplary embodiment the potential source is at 1.25 volts ($V_{dd}/2$).

[0030] The access transistor 401, as well as the other access transistors, are depicted as N-type CMOS transistors, however, it should be understood that P-type CMOS transistors may be used as long as the corresponding polarities of the other components and voltages are modified accordingly. The programmable conductor memory element 402 is preferably made of chalcogenide, however, it should be understood that any other bi-stable resistive material known to those with ordinary skill in the art may also be used. In the exemplary embodiment, the programmable conductor memory element 402 stores a binary 0 when has a resistance of approximately 10 K ohm, and a binary 1 when it has a resistance greater than 10 M ohm. The programmable conductor is ideally programmed to store a low resistance, e.g., binary 0, by a voltage of +0.25 volt and can be restored to a high resistance value, e.g., a binary 1, by a programming voltage of -0.25 volt. The programmable conductor can be nondestructively read by a reading voltage having a magnitude of less than 0.25 volt. In the exemplary embodiment, the reading voltage is 0.2 volt. However, it should be readily apparent that alternate parameters may be selected for the PCRAM cell without departing from the spirit and scope of the invention.

[0031] Fig. 5 illustrates a memory device 500 comprising a plurality of memory arrays 550a, 550b. Each memory array 550a, 550b includes a plurality of memory cells 400a-400d, 400e-400h arranged by tiling a plurality of memory cells 400 together so that the memory cells 400 along any given bit line 406a, 406a', 406b, 406b' do not share a

common word line 405a-405d. Conversely, the memory cells 400 along any word line 405a-405d do not share a common bit line 406a, 406a', 406b, 406b'. Each word line is switchably to a word line driver 512a-512d via a transistor 510a-510d. Additionally, each word line may also be switchably coupled to ground via transistors 520a-520d. The gates of the transistors 510a-510d, 520a-520d are coupled to signal lines 511a-511d used to selectively couple/decouple the word lines 405a-405d to/from the word line drivers 512a-512b /ground. Each memory array 550a, 550b has its own set of bit lines. For example, memory array 550a includes bit lines 406a, 406b, while memory array 550b includes bit lines 406a', 406b'. The bit lines from each adjacent pair of memory arrays 550a, 550b are coupled to a common sense amplifier 600a, 600b. For example, bit lines 406a, 406a' are coupled to sense amplifier 600a, while bit lines 406b, 406b' are coupled to sense amplifier 600b. For simplicity, Fig. 5 illustrates a memory device having only two arrays 550a, 550b, and eight cells 400a-400h. However, it should be understood that real world memory devices would have significantly more cells and arrays. For example, a real world memory device may include several million cells 400.

[0032] The memory device 500 also includes a plurality of pre-charge circuits 501a-501b. One pre-charge circuit (e.g., 501a) is provided for each pair of bit lines coupled to a sense amplifier (e.g., 406a, 406a'). Each pre-charge circuit (e.g., 501a) includes two transistors (e.g., 501a, 501b). One terminal of each transistor is coupled to a potential source. In the exemplary embodiment, the potential source is at 2.5 volts (V_{dd}). Another terminal of each transistor (e.g., 502a, 502b) is coupled to its corresponding bit line (e.g., 406a, 406a', respectively). The gate of the each transistor (e.g., 502a, 502b) is coupled to

a pre-charge control signal. As illustrated, the transistors (e.g., 502a, 502b) are P-MOS type transistor. Thus, when the pre-charge signal is low, the transistors (e.g., 502a, 502b) conducts, thereby pre-charging the bit lines (e.g., 406a, 406a'). When the pre-charge signal is high, the transistors (e.g., 502a, 502b) are switched off. Due to capacitance inherent in the bit lines (e.g., 406a, 406a'), the bit lines will remain at approximately the pre-charge voltage level of 2.5 volts for a predetermined period of time.

[0033] Reading a PCRAM cell, for example, cell 400a, in the PCRAM device 500 comprises the operations of accessing and sensing.

[0034] The purpose of the access operation is to create a small potential difference between the bit lines (e.g., 406a, 406a') coupled to the same sense amplifier (e.g., 300a) of the memory cell 400a being read. This small potential difference can be subsequently amplified by a sense amplifier 300 to the threshold required to subsequently drive a comparator coupled to the bit lines to output a value corresponding to the contents of the memory cell 400a. Now also referring to Fig. 7, the access operation begins with the pre-charging of the bit lines 406a, 406a', 406b, 406b' of the memory device 500 via pre-charge circuits 501a-501b (step S1). The bit lines may be pre-charged by temporarily bringing the pre-charge signal low, causing transistors 502a-502d to conduct the pre-charge voltage (V_{dd}) to the bit lines 406a, 406a', 406b, 406b'. Once the pre-charge signal returns to a high state, the transistors 502a-502d stop conducting, but the bit lines 406a, 406a', 406b, 406b' will remain at the pre-charge potential for a predetermined period due to the capacitance inherent in the bit lines.

[0035] In the exemplary embodiment, bit lines 406a, 406a', 406b, 406b' are pre-charged to 2.5 volts and the cell plate 403a, 403b is tied to 1.25 volts. The 1.25 volt potential difference between the bit line and the cell plate will cause the bit line to discharge to the cell plate through the access transistor 401 (when it is in a conductive state) and the programmable conductor memory element 402. The discharge rate is dependent upon the resistive state of the programmable conductor memory element 402. That is, a low resistive state will cause the bit line to discharge faster than a high resistive state. As the bit line discharges, its voltage will fall from the pre-charge voltage toward the cell plate voltage.

[0036] In the memory device 500, the word lines 405a-405d are normally at ground potential. Thus the access transistors 401a-401e are normally switched off. Now also referring to Figs. 6A and 6B, at time T1, the word line 405a associated with the cell 400a to be read is activated by bringing its potential from ground to a predetermined level (step S2). The predetermined level is designed to create a reading voltage at the programmable contact 402a, which as previously explained, must have a magnitude less than the magnitude of a writing voltage. In the exemplary embodiment, the word line 401a is brought to 2.25 volt. Since the threshold voltage of the transistor 401a is 0.8 volt, the potential at the interface between the transistor 401a and the programmable contact 402a is 1.45 volt. This results in a reading voltage of 0.2 volt since the voltage at the interface between the programmable contact 402a and the cell plate 403a is maintained at 1.25 volt.

[0037] Due to the inherent parasitic capacitance between the word line 401a and its associated bit lines 406a the potential in the associated bit line 406a increase as the word line 401a is activated. In the exemplary embodiment, the potential in bit line 406a increases by 0.1 volt to 2.6 volt. It should be noted that the word lines 405c, 405d coupled to complementary bit lines 406a', 406b' remain at ground potential. Thus, bit lines 406a', 406b' remain at the pre-charge potential, which is 2.5 volt in the exemplary embodiment.

[0038] The increased potential of bit line 406a is used in combination with the two bi-stable resistive states of the programmable contact 402a to cause one of the bit lines (e.g., 406a) coupled to a sense amplifier (e.g., 300a) to have either a greater or lesser voltage than the other bit line (e.g., 406a') coupled to the same sense amplifier 300a. Essentially, the parasitic capacitance between word lines and associated bit lines is used to achieve an initial state where the bit line (e.g., 406a) associated with the cell 400a being read is at a higher potential than the other bit line 406a' coupled to the same sense amplifier 300a. The memory is designed and operated so that if the programmable contact 402a has a high resistive state, bit line 406a discharges slowly, thereby causing it to maintain its relatively higher potential. However, if the programmable contact 402a has a low resistive state, bit line 406a discharges at a faster rate, so that bit line 406 transitions to a lower potential state than bit line 406a'. These two effects can be seen by comparing Fig. 6A (illustrating the effects of a programmable contact at a high resistive state) and Fig. 6B (illustrating the effects of a programmable contact at a low resistive state.)

[0039] At time T2, a predetermined time t after time T1 (step S3), the word line 405a associated with the cell 400a being read is deactivated by returning its potential to ground (step S4). Word line deactivation may be achieved by, for example, grounding terminal 511a, which will cause the transistor 510a serially coupling the word line driver 512a to the word line 405a to stop conducting. This shuts off access transistors 401a, 401 thereby preventing further discharge of the bit line through the programmable contact 402a, 402e. This also prevents the amplified potential difference developed during the subsequent sensing operation from refreshing (writing) the programmable contact 402a, 402e. In the rare instance when it would be desirable to refresh the contents of the programmable contact 402a, 402e, the word line can be held high for a longer period of time. This mode of operation is shown via the dashed trace in Figs. 6A and 6B. In the exemplary embodiment, the predetermined time t is approximately 15 nanosecond (i.e., $T2 = T1 + 15$ ns).

[0040] It should be noted that the values of t and T2 may be varied without departing from spirit of the invention. In particular, the objectives of the present invention will be realized by electrically decoupling the programmable contact from the bit line at any time before the bit line voltages are amplified by the sense amplifiers 310N, 310P to a level which result in the potential difference across the programmable contact reaching threshold required to write the programmable contact. Thus, while Figs. 6A and 6B illustrate T2 occurring prior to either sense amplifiers 310N, 310P being activated, depending upon the electrical characteristics of the memory device 500, T2 may occur, for example, between the activation of the N- sense amp 310N and the P- sense amp 310P. Regardless, the

predetermined time t must be sufficiently long to permit the logical state of the programmable conductor 402a to be reflected on the bit line 406a; i.e., the bit line 406a voltage to be sufficiently altered from the pre-charge voltage by the discharge through the programmable conductor 402a so that the two resistive states of the programmable conductor 402a can be distinguished and amplified by the sense amplifier 300a.

[0041] At time period T3, the N- sense amplifier 310N is activated (start of step S5). As previously noted with respect to DRAM systems, activating the N-sense amplifier causes the bit line (e.g., 406a') having the lower potential to be pulled with the NLAT signal toward ground. In the exemplary embodiment, T3 is approximately 30 nanosecond after T1. However, it should be noted that the value T3 may be varied without departing from spirit of the invention.

[0042] At time period T4, the P- sense amplifier 310P is activated. As previously noted with respect to DRAM systems, activating the P-sense amplifier causes the bit line (e.g., 406a) having the higher potential to be pulled towards Vcc. In the exemplary embodiment, T4 is approximately 35 nanosecond after T1 (end of step S5). However, it should be noted that the value of T4 may be varied without departing from spirit of the invention.

[0043] At time T5, the sense amplifier 300a associated with the cell 400a being read will have one of its bit lines (e.g., 406a) at Vcc potential and the other bit line (e.g., 406a') at ground potential. Since one bit line coupled to sense amplifier 300a is now at ground potential while the other bit line is now at Vcc potential, a comparator (or differential

amplifier) 350 can be used to output a value corresponding to the contents of the cell 400a on signal line 351a.

[0044] Fig. 9 is an illustration of a memory device 900 according to an alternate embodiment of the present invention. This alternate embodiment is designed for use with PCRAM cells which do not include an access transistor 401. For example, Fig. 10 illustrates one example of a PCRAM cell 400' which utilizes a pair of diodes 1001a, 1001b in lieu of an access transistor. As illustrated, the PCRAM cell 400' features a programmable conductor memory element 402 which is coupled to a bit line 104. The programmable conductor memory element 402 is also coupled to the word line via a diode circuit 1002. The diode circuit comprises two diodes 1001a, 1001b arranged as shown.

[0045] The memory device 900 is otherwise very similar to the memory device 500 of the first embodiment. However, memory device 900 includes new isolation transistors 901a-901d which serially connect the sense amplifiers 300a, 300d to the bit lines 406a, 406a', 406b, 406b'. The invention operates in memory device 900 in a manner very similar to memory device 500 except that instead of deactivating word lines 405a to electrically decouple memory cell 400a from amplified voltages on the bit line 406a' prior to sensing, the isolation transistor 901a, which is normally conducting, is turned off, thereby bifurcating the bit line 406a. The portion of the bit line between the transistor 901a and the sense amplifier 301a will then be sensed while the portion of the bit line between the transistor 901a and the pre-charge circuit 501a will be isolated from the sense amplifier.

[0046] Fig. 8 is a block diagram of a processor based system 800, such as a computer system, containing a PCRAM semiconductor memory 802 as described in connection with the other figures. The memory 802 may be constituted as one or more memory chips or memory integrated circuits mounted on a memory module, for example, a plug-in memory module such as a SIMM, DIMM, or other plug-in memory module. The processor based system 800 includes a processor 801, a memory 802, a mass storage 803, and an I/O device 804, each coupled to a bus 805. While a single processor 801 is illustrated, it should be understood that processor 801 could be any type of processor and may include multiple processor and/or processors and co-processors. Memory 802 is illustrated in Fig. 9 as having a plurality of PCRAM chips 500. However, memory 802 may only include a single PCRAM device 500, or a larger plurality of PCRAM devices 500 than illustrated, and/or may include additional forms of memories, such as non-volatile memory or cache memories. While one mass storage 803 device is illustrated, the processor based system 800 may include a plurality of mass storage devices, possibly of varying types such as, but not limited to, floppy disks, CDRoms, CD-R, CD-RW, DVD, hard disks, and disk arrays. I/O device 804 may likewise comprise a plurality of I/O devices of varying types, including, but not limited to keyboard, mouse, graphic cards, monitors, and network interfaces. Bus 805, while illustrated as a single bus may comprise a plurality of buses and/or bridges, which may be coupled to each other or bridged by other components. Some of the devices 801-804 may be coupled to only a single bus 805, others may be coupled to a plurality of buses 805.

[0047] The present invention provides a PCRAM cell 400 and a method for reading the contents of the cell 400 using sense amplifiers but without rewriting the contents of the cell. Rewrite prevention is achieved by isolating the programmable conductor 402 of the cell 400 from the bit line 406 a predetermined amount of time after the programmable conductor 402 has been electrically coupled to the bit line 406. The predetermined amount of time corresponds a time prior to the activation time of both the N- and P- sense amps 310N, 310P. In the exemplary embodiment, the PCRAM cell 400 includes an access transistor 401 for electrically coupling and decoupling the cell to the bit line. The access transistor 401 has a gate coupled to a word line. Thus, in the exemplary embodiment, the word line is deactivated the predetermined amount of time after it has been activated, thereby ensuring that the activation of the N- and P- sense amplifiers 310N, 310P do not rewrite the cell 400. In another embodiment, the PCRAM cell 400 does not include an access transistor. For example, the PCRAM cell instead utilize diodes. In any embodiment without an access transistor, isolation transistor may be inserted between the programmable contact memory element and the bit line associated with the programmable contact memory element. The isolation transistors, which are normally conducting, may be switched off at the same predetermined time as in the exemplary embodiment, after the word line has been activated, thereby achieving the same result of isolating the programmable contact memory element from the elevated voltages generated during sensing.

[0048] While the invention has been described in detail in connection with the exemplary embodiment, it should be understood that the invention is not limited to the

above disclosed embodiment. Rather, the invention can be modified to incorporate any number of variations, alternations, substitutions, or equivalent arrangements not heretofore described, but which are commensurate with the spirit and scope of the invention. Accordingly, the invention is not limited by the foregoing description or drawings, but is only limited by the scope of the appended claims.

CLAIMS

What is claimed is:

1. A memory device comprising,

an apparatus for reading data from a programmable conductor random access memory cell, said apparatus comprising:

an access circuit for coupling said memory cell between an addressed and activated word line and an addressed and activated bit line during a read operation;

a sense amplifier coupled to said addressed and activated bit line for sensing a logical state of said memory cell; and

preventing circuitry for preventing said memory cell from being refreshed in response to said read operation.

2. The memory device of claim 1, wherein said access circuit is a transistor circuit and said preventing circuitry causes said activated word line to be deactivated after a logical state of said memory cell is transferred to said activated bit line and before said sense amplifier senses a logical state of said memory cell.

3. The memory device of claim 2, wherein said preventing circuitry comprises a transistor which causes said activated word line to be deactivated.

4. The memory device of claim 3, wherein said transistor is serially connected between said word line and a driver for said word line and is turned on during said read operation and turned off to deactivate said row line.

5. The memory device of claim 3, wherein said transistor is connected between said word line and ground and is turned off during said read operation and is turned on to deactivate said word line.

6. The memory device of claim 1, wherein said preventing circuitry comprises a transistor serially connected between an activated bit line and a sense amplifier associated with the activate bit line, said serially connected transistor being turned on during a read operation and turned off before said memory cell can be refreshed.

7. The memory device of claim 1, wherein said preventing circuitry causes said activated word line to be deactivated a predetermined amount of time after said memory cell begins to transfer a logical state to said activated bit line.

8. The memory device of claim 7, wherein said sense amplifier further comprises a first sense amplifier portion and a second sense amplifier portion.

9. The memory device of claim 8, wherein said predetermined amount of time is after said first sense amplifier portion is activated and before said second sense amplifier portion is activated.

10. The memory device of claim 8, wherein said first sense amplifier portion is a N-sense amplifier, and said second sense amplifier portion is a P-sense amplifier.

11. The memory device of claim 1 further comprising:

a pre-charge circuit for pre-charging the addressed and activated bit line and an another bit line, wherein said addressed and accessed bit line and said other bit line are coupled to the sense amplifier.

12. The memory device of claim 11, wherein said pre-charge circuit pre-charges the addressed and activated bit line and the another bit line prior to the sense amplifier sensing said addressed and activated bit line.

13. An system comprising,

a processor; and

a memory, said memory further comprising,

an apparatus for reading data from a programmable conductor random access memory cell, said apparatus comprising:

an access circuit for coupling said memory cell between an addressed and activated word line and an addressed and activated bit line during a read operation;

a sense amplifier coupled to said addressed and activated bit line for sensing a logical state of said memory cell; and

preventing circuitry for preventing said memory cell from being refreshed in response to said read operation.

14. The system of claim 13, wherein said access circuit is a transistor circuit and said preventing circuitry causes said activated word line to be deactivated after a logical state of said memory cell is transferred to said activated bit line and before said sense amplifier senses a logical state of said memory cell.

15. The system of claim 14, wherein said preventing circuitry comprises a transistor which causes said activated word line to be deactivated.

16. The system of claim 15, wherein said transistor is serially connected between said word line and a driver for said word line and is turned on during said read operation and turned off to deactivate said row line.

17. The system of claim 15, wherein said transistor is connected between said word line and ground and is turned off during said read operation and is turned on to deactivate said word line.

18. The system of claim 13, wherein said preventing circuitry comprises a transistor serially connected between an activated bit line and a sense amplifier associated with the activate bit line, said serially connected transistor being turned on during a read operation and turned off before said memory cell can be refreshed.

19. The system of claim 13, wherein said preventing circuitry causes said activated word line to be deactivated a predetermined amount of time after said memory cell begins to transfer a logical state to said activated bit line.

20. The system of claim 19, wherein said sense amplifier further comprises a first sense amplifier portion and a second sense amplifier portion.

21. The system of claim 20, wherein said predetermined amount of time is after said first sense amplifier portion is activated and before said second sense amplifier portion is activated.

22. The system of claim 20, wherein said first sense amplifier portion is a N-sense amplifier and said second sense amplifier portion is a P-sense amplifier.

23. The system of claim 13 further comprising:

a pre-charge circuit for pre-charging the addressed and activated bit line and an another bit line, wherein said addressed and accessed bit line and said other bit line are coupled to the sense amplifier.

24. The system of claim 23, wherein said pre-charge circuit pre-charges the addressed and activated bit line and the another bit line prior to the sense amplifier sensing said addressed and activated bit line.

25. A method for reading data from a programmable conductor random access memory cell, said method comprising:

activating an addressed word line containing said programmable conductor random access memory cell and transferring a logical value in said cell to an associated addressed bit line;

deactivating said addressed word line; and

sensing a logical value transferred to said bit line after said word line is deactivated.

26. The method of claim 25, wherein said deactivating takes place a predetermined amount of time after said activating.

27. The method of claim 25, wherein said sensing further comprises,

activating a first sense amplifier unit; and

activating a second sense amplifier unit a second predetermined time after said activating of said first sense amplifier unit.

28. The method of claim 25, wherein said deactivating takes place a first predetermined amount of time after said activating of an addressed word line.

29. The method of claim 28, wherein said first predetermined amount of time is after said activating of said first sense amplifier unit and before said activating of said second sense amplifier unit.

30. The method of claim 28, wherein said first predetermined amount of time is before said activating of said first sense amplifier unit and before said activating of said second sense amplifier unit.

31. A method for reading data from a programmable conductor random access memory cell, said method comprising:

activating an addressed word line containing said programmable conductor random access memory cell and transferring a logical value in said cell to an associated addressed bit line;

switching off an isolation transistor located on the associated addressed bit line and serially connecting a sense amplifier and said cell;

sensing a logical value transferred to said bit line after said word line is deactivated.

32. The method of claim 31, wherein said switching off takes place a predetermined amount of time after said activating.

33. The method of claim 31, wherein said sensing further comprises,

activating a first sense amplifier unit; and

activating a second sense amplifier unit a second predetermined time after said activating of said first sense amplifier unit.

34. The method of claim 32, wherein said switching off takes place a first predetermined amount of time after said activating of an addressed word line.

35. The method of claim 34, wherein said first predetermined amount of time is after said activating of said first sense amplifier unit and before said activating of said second sense amplifier unit.

36. The method of claim 34, wherein said first predetermined amount of time is before said activating of said first sense amplifier unit and before said activating of said second sense amplifier unit.

37. A method for reading data from a programmable conductor random access memory cell, said method comprising:

pre-charging a first bit line coupled to the programmable conductor random access memory cell, said memory cell including a programmable conductor memory element;

pre-charging a second bit line;

increasing voltage on said first bit line;

switching on an access transistor of said cell to couple the programmable conductor memory element to said first bit line;

switching off the access transistor of said cell to decoupling the programmable conductor memory element from said first bit line;

sensing voltage on said first bit line and said second bit line to determine a logical state of said programmable conductor memory element;

wherein said switching off is performed before said sensing.

38. A method for reading data from a programmable conductor random access memory cell, said method comprising:

36. The method of claim 34, wherein said first predetermined amount of time is before said activating of said first sense amplifier unit and before said activating of said second sense amplifier unit.

37. A method for reading data from a programmable conductor random access memory cell, said method comprising:

pre-charging a first bit line coupled to the programmable conductor random access memory cell, said memory cell including a programmable conductor memory element;

pre-charging a second bit line;

increasing voltage on said first bit line;

switching on an access transistor of said cell to couple the programmable conductor memory element to said first bit line;

switching off the access transistor of said cell to decoupling the programmable conductor memory element from said first bit line;

sensing voltage on said first bit line and said second bit line to determine a logical state of said programmable conductor memory element;

wherein said switching off is performed before said sensing.

38. A method for reading data from a programmable conductor random access memory cell, said method comprising:

switching on an isolation transistor to couple a first bit line to a sense amplifier, said first bit line also coupled to a programmable conductor memory element of the programmable conductor random access memory cell;

pre-charging said first bit line;

pre-charging a second bit line;

increasing voltage on said first bit line;

switching off said isolation transistor to decouple said programmable conductor memory element from said sense amplifier;

sensing voltage on said first bit line and said second bit line to determine a logical state of said programmable conductor memory element;

wherein said switching off is performed before said sensing.

FIG. 1
(PRIOR ART)

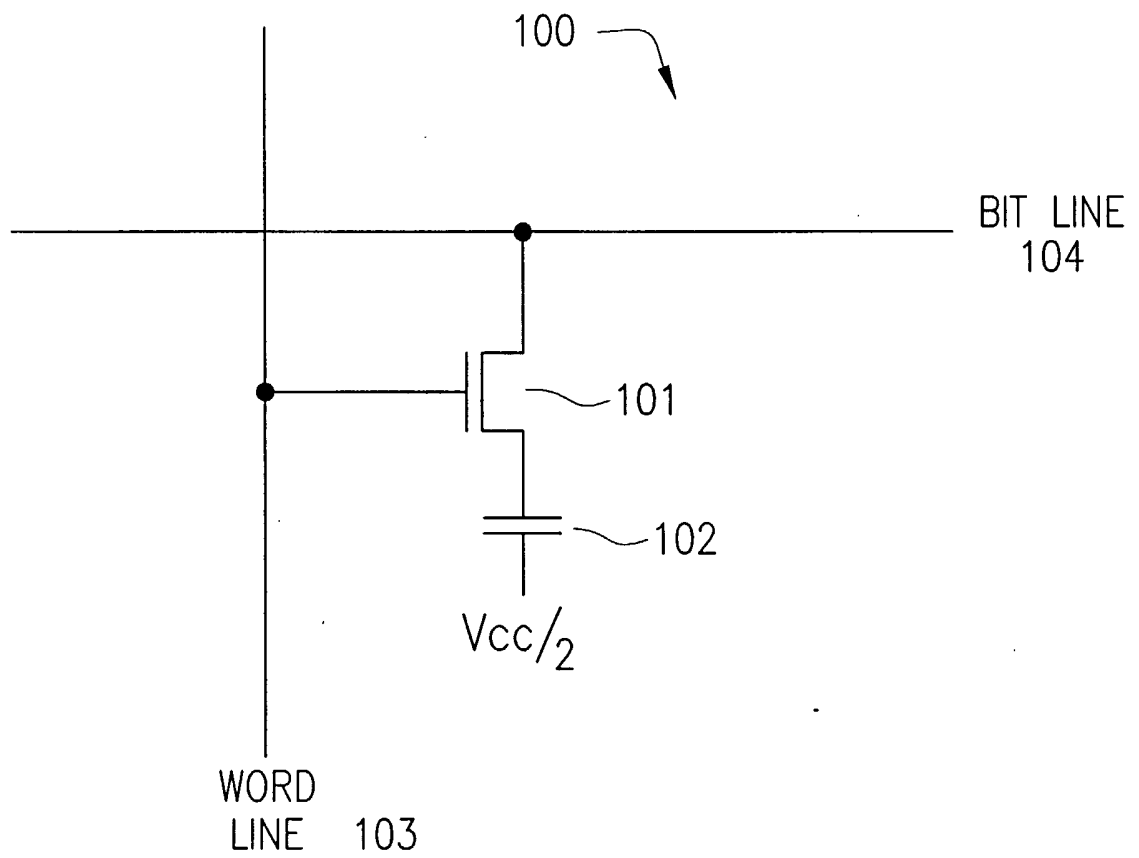


FIG. 2
(PRIOR ART)

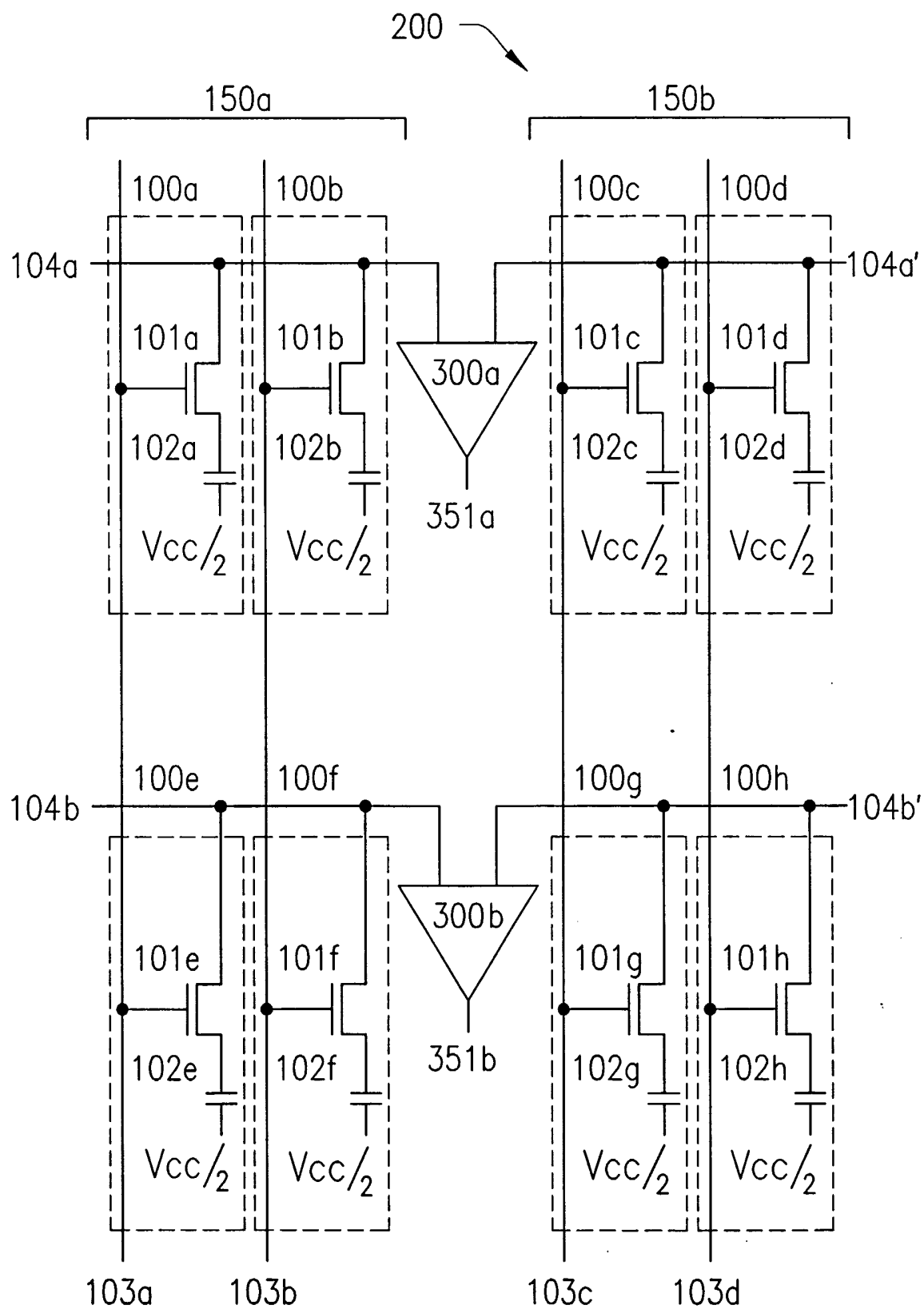


FIG. 3
(PRIOR ART)

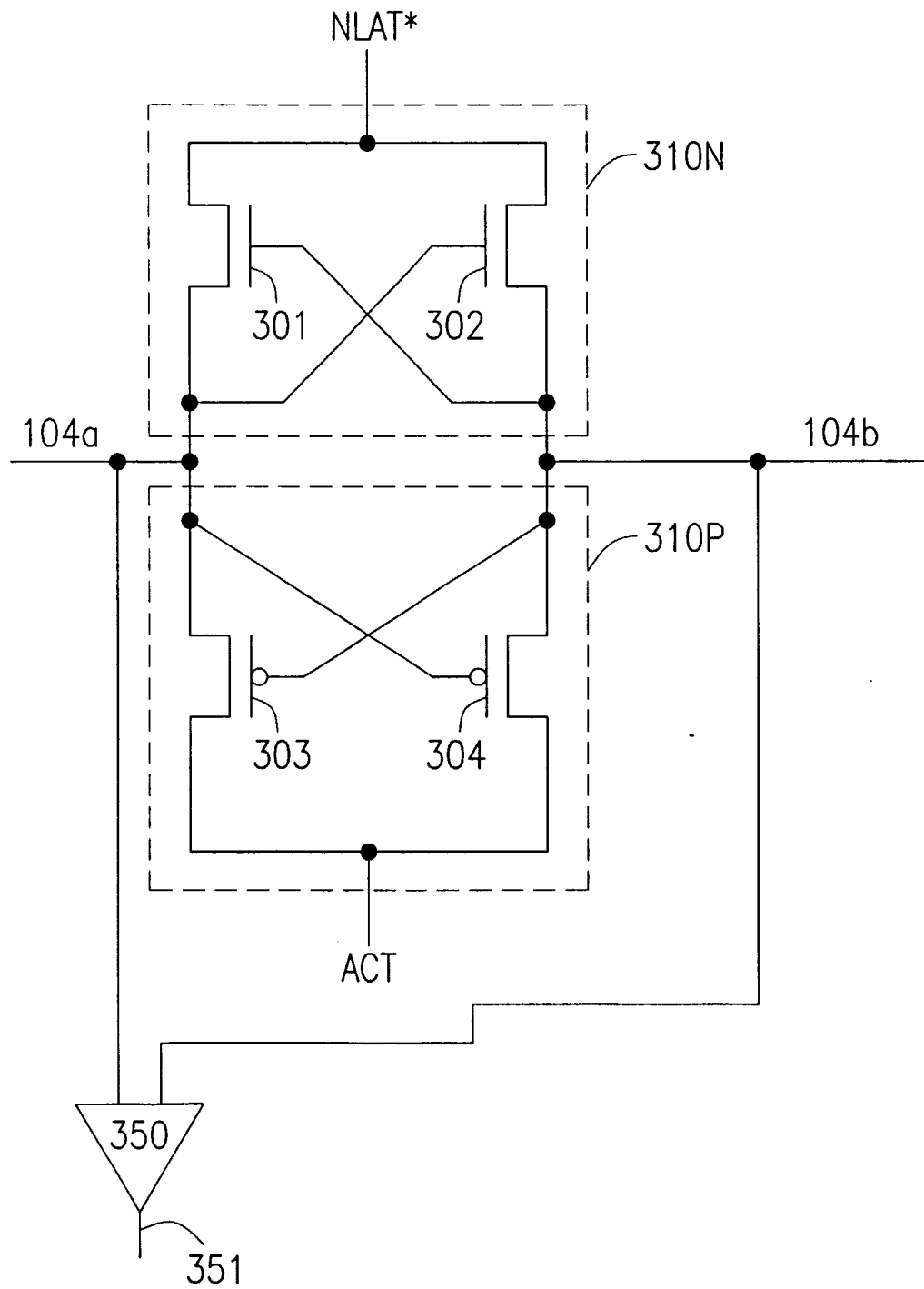


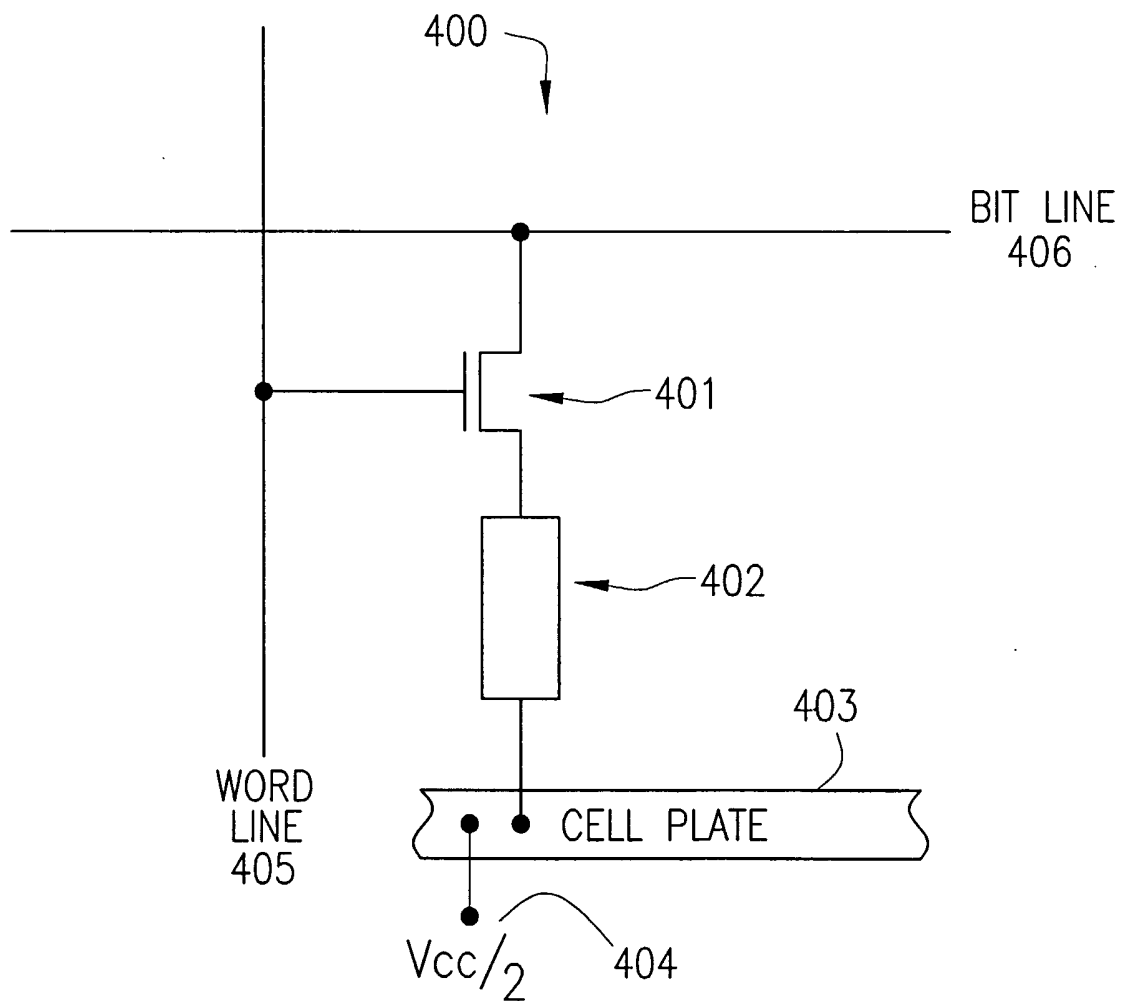
FIG. 4

FIG. 5

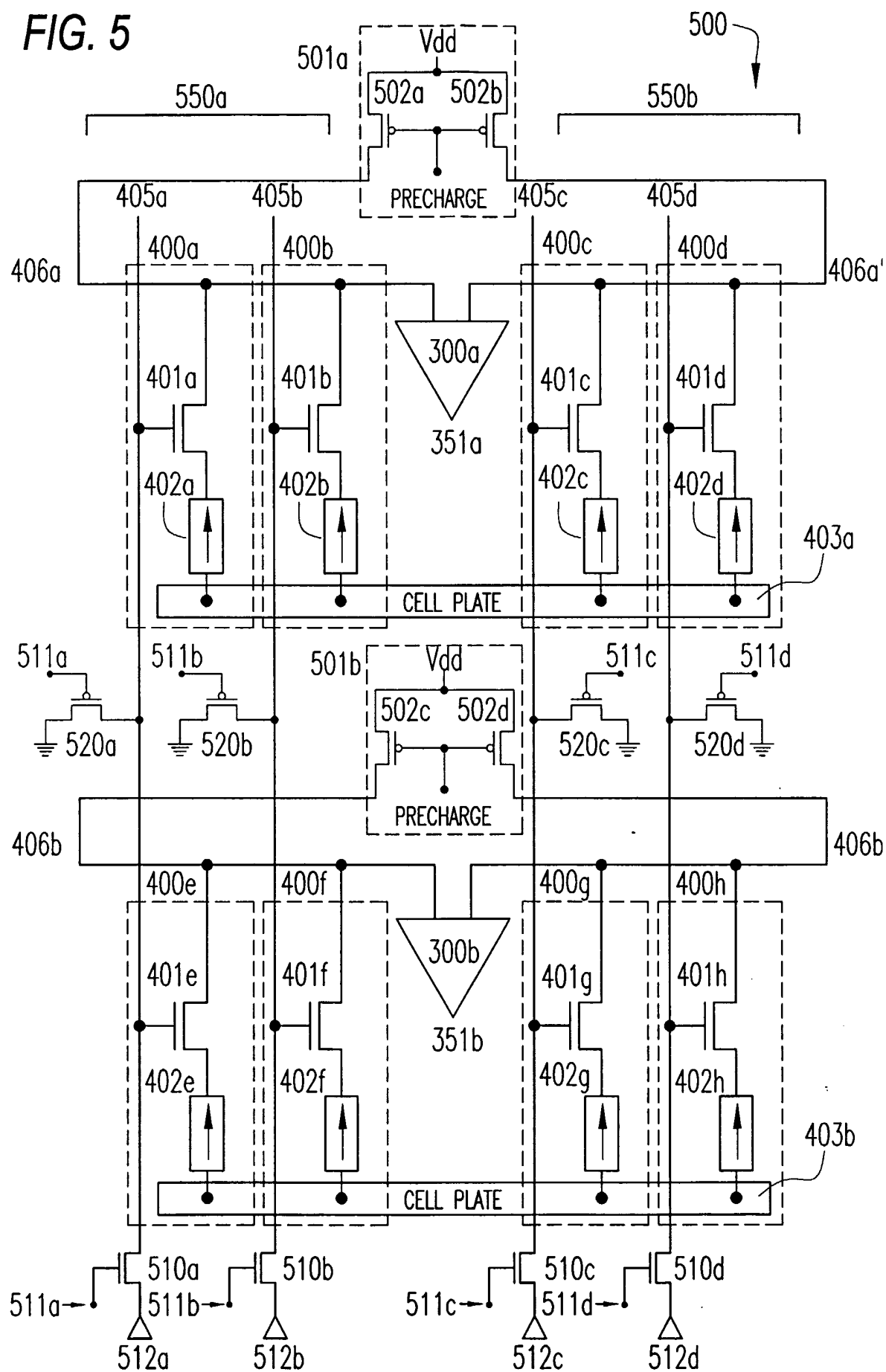


FIG. 6A

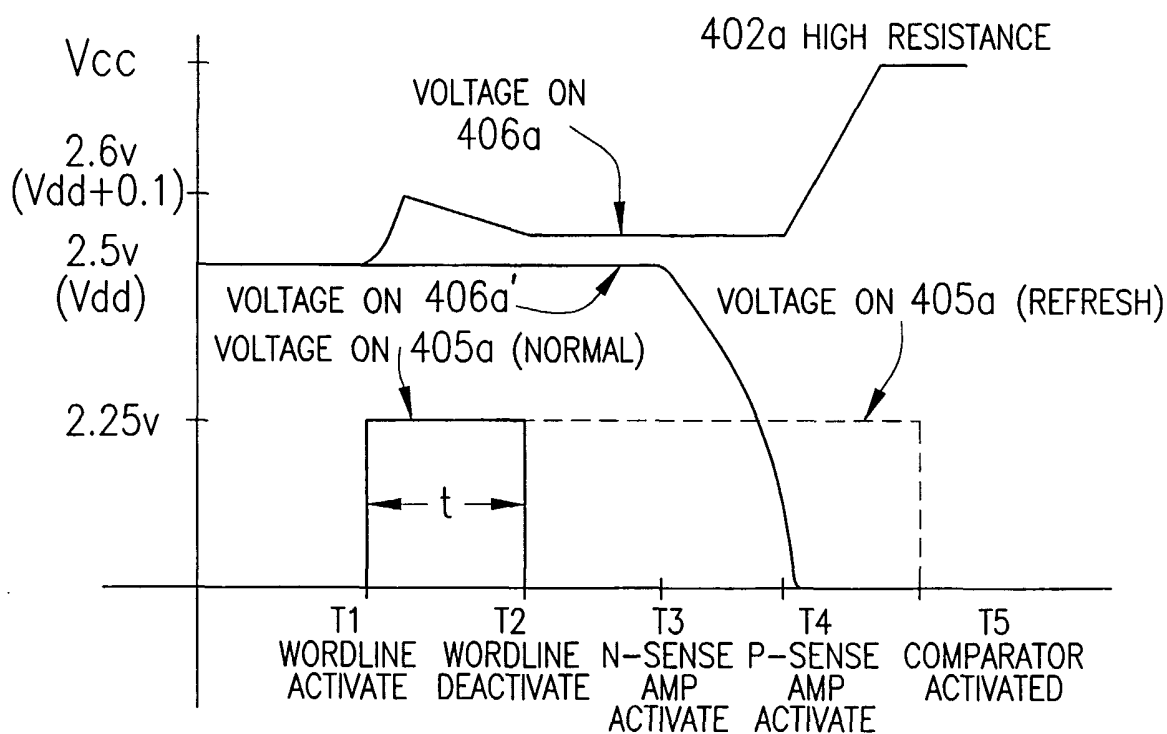


FIG. 6B

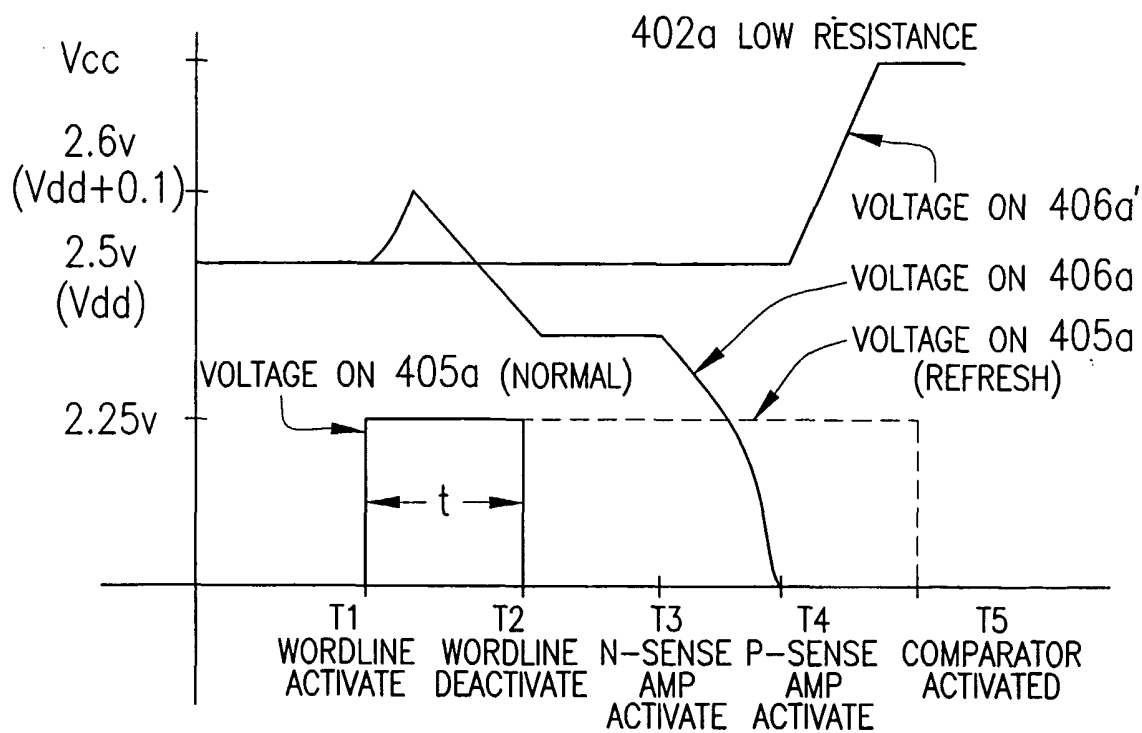


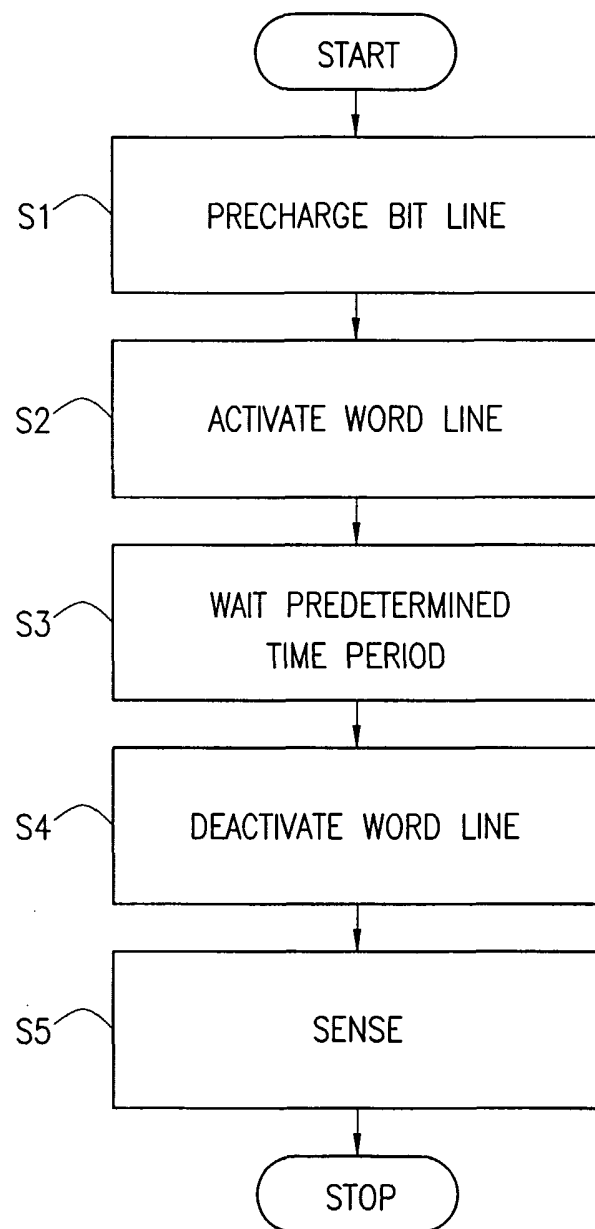
FIG. 7

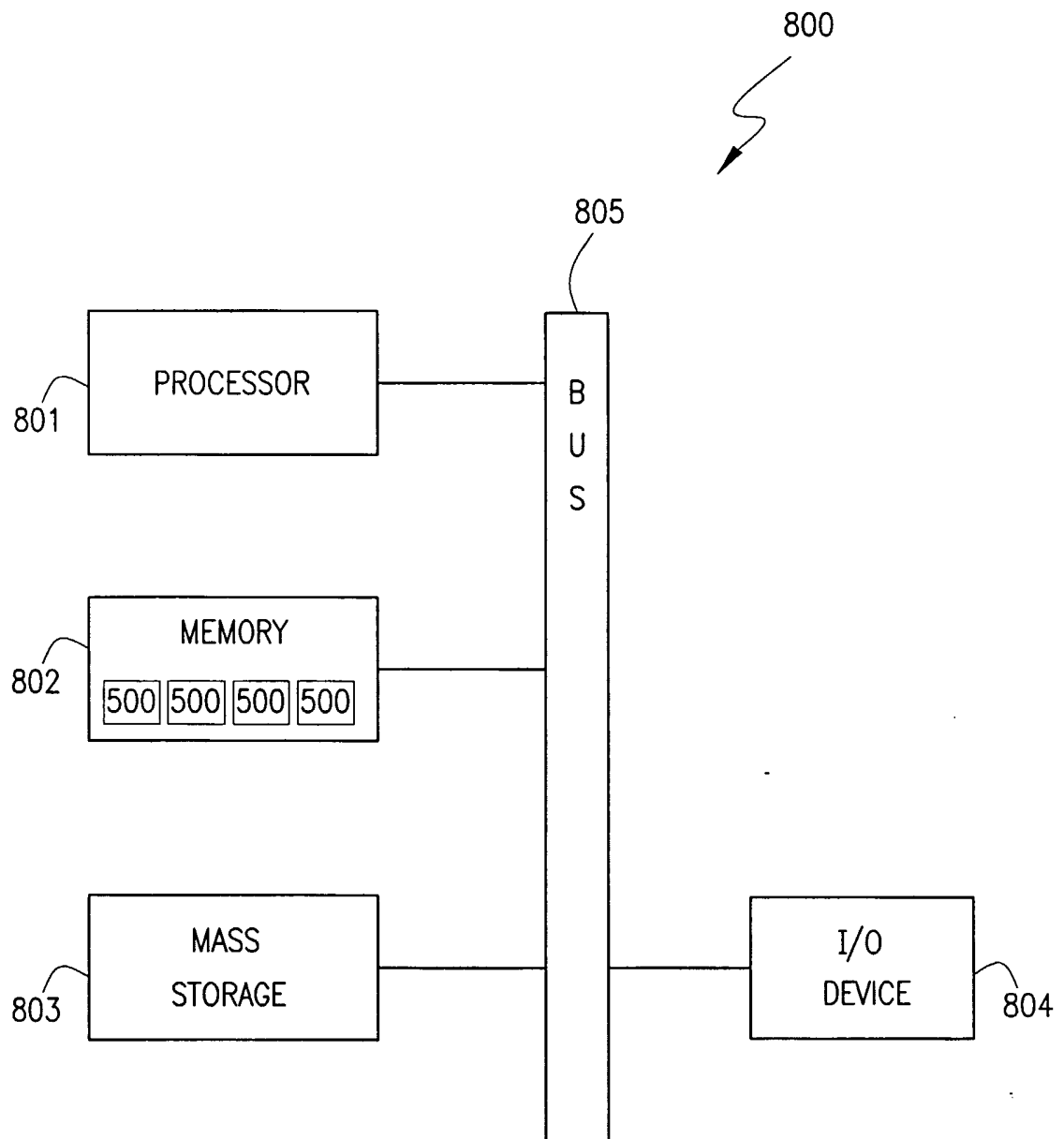
FIG. 8

FIG. 9

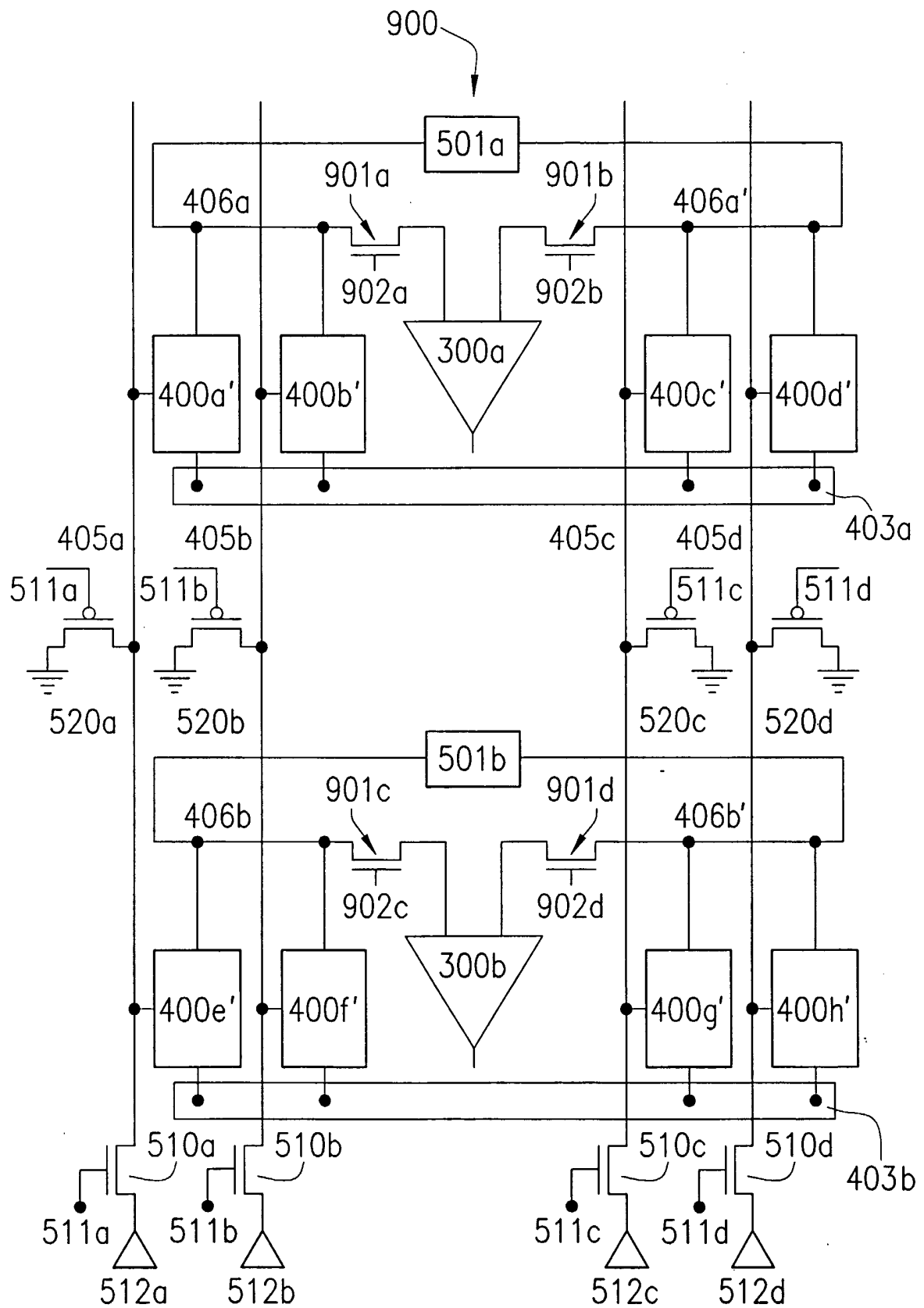
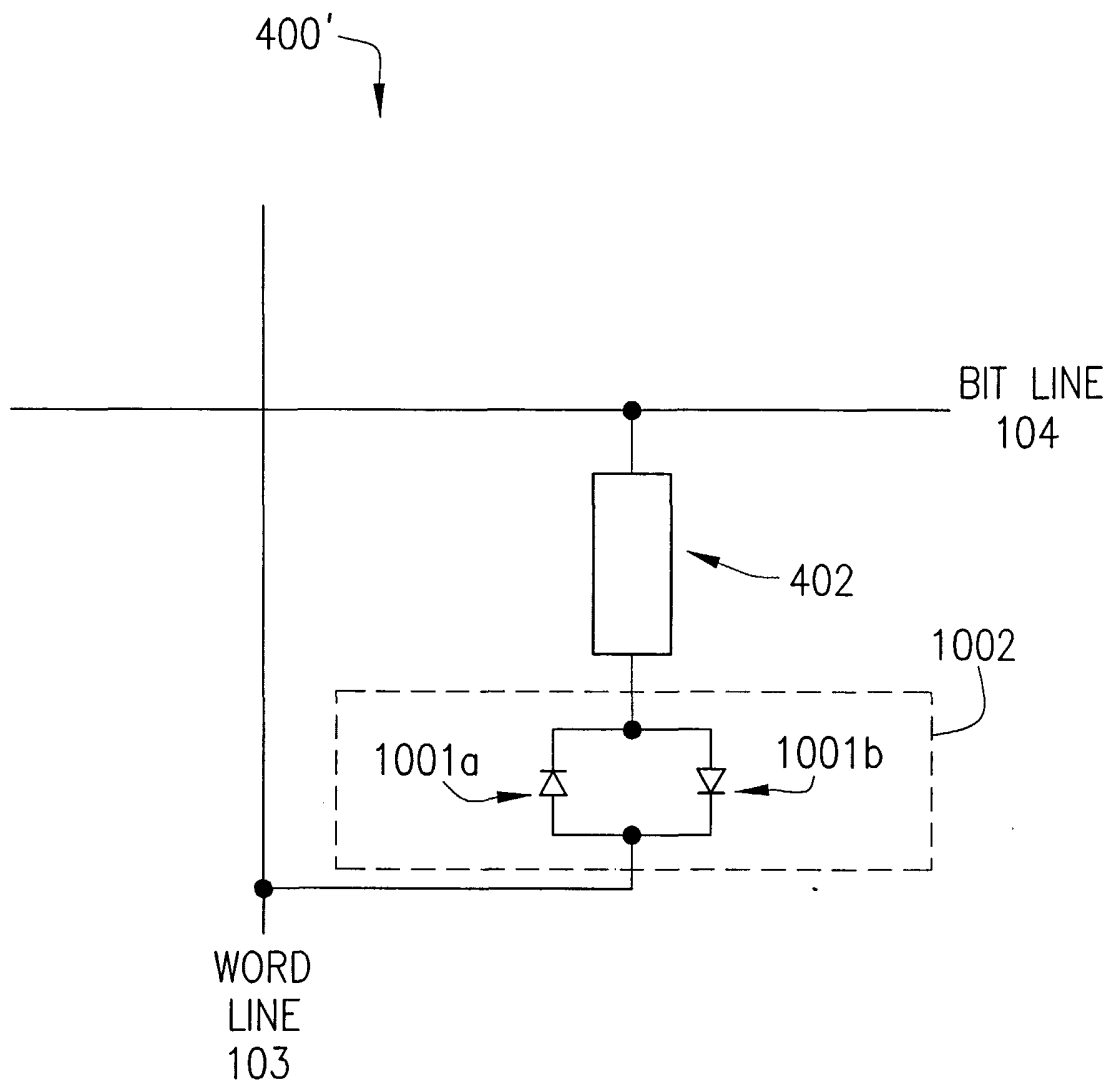


FIG. 10



INTERNATIONAL SEARCH REPORT

PCT/US 03/00239

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G11C11/34

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHEDMinimum documentation searched (classification system followed by classification symbols)
IPC 7 G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 5 883 827 A (MORGAN DONALD M) 16 March 1999 (1999-03-16) column 7, line 10 -column 8, line 19 column 5, line 35 - line 49 figures 6,7 ---	1,6-8, 10-13, 18-20, 22-24, 31-38 2-5,9, 14-17, 21,25-30
P,X	US 6 462 981 B2 (NUMATA ET AL) 8 October 2002 (2002-10-08) column 6, line 11 -column 7, line 37 column 11, line 13 - line 25 figures 1,2 --- -/--	1-38

☒ Further documents are listed in the continuation of box C.☒ Patent family members are listed in annex.

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Date of the actual completion of the international search

22 May 2003

Date of mailing of the international search report

24/06/2003

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INTERNATIONAL SEARCH REPORT

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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