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— *with international search report*

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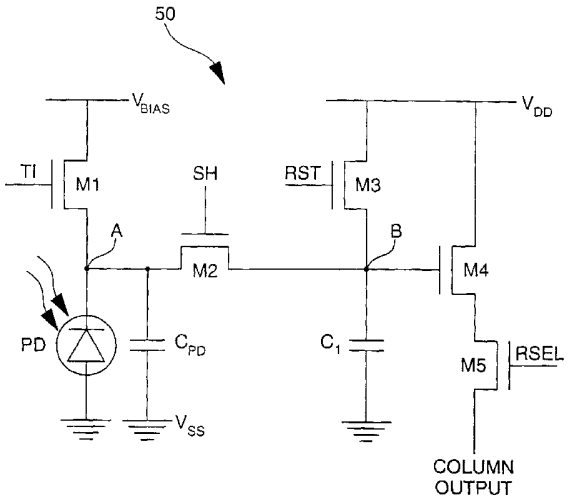
(54) Title: CMOS IMAGE SENSOR AND METHOD FOR OPERATING A CMOS IMAGE SENSOR WITH INCREASED DYNAMIC RANGE




(57) Abstract: There is disclosed a CMOS technology image sensor and a method for operating such an image sensor. This sensor includes a plurality of pixels (50) each including a photo-sensor element (PD) producing charge carriers in proportion to its illumination and storage means (C1) capable of being coupled and uncoupled from the photo-sensor element at a determined instant in order to store, on a memory node (B) of the pixel, a measuring signal representative of the charge carriers produced by said photo-sensor element during an exposure phase. Each pixel includes at least one MOS transistor (M1; M3) connected in series via its drain or source terminals to the photo-sensor element, and the transistor is configured such that it operates at least partially in weak inversion so that, during the exposure phase, the pixel has a logarithmic response for illumination levels higher than a determined illumination level. This at least partially logarithmic response enables the pixel dynamic range to be increased.

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# INTERNATIONAL SEARCH REPORT

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PCT/EP 02/05980

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L27/146 H04N3/15

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category ° | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | KAVADIAS S ET AL: "A logarithmic response CMOS image sensor with on-chip calibration" IEEE JOURNAL OF SOLID-STATE CIRCUITS, AUG. 2000, IEEE, USA, vol. 35, no. 8, pages 1146-1152, XP002187643 ISSN: 0018-9200 figures 1,2 Section II: On-pixel calibration Section III A: Pixel structure --- | 1,2,15, 16 |
| X | US 5 235 197 A (WASHKURAK WILLIAM D ET AL) 10 August 1993 (1993-08-10) figures 2,3 column 2, line 42 -column 5, line 47 --- -/-- | 1,2,15, 16 |

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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| Date of the actual completion of the international search | Date of mailing of the international search report |
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| Name and mailing address of the ISA | Authorized officer |
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| European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016 | Visscher, E |

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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Information on patent family members

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