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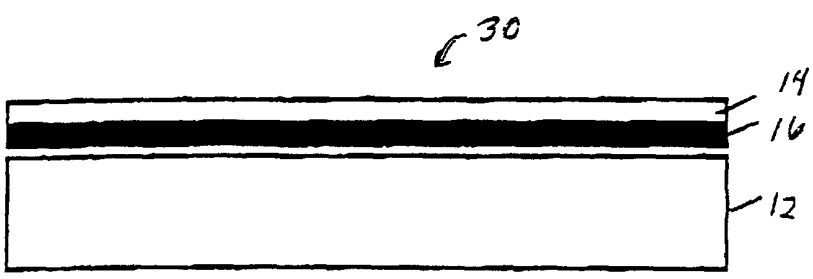
For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: WAFER BONDING TECHNIQUES TO MINIMIZE BUILT-IN STRESS OF SILICON MICROSTRUCTURES AND MICRO-MIRRORS



(57) Abstract: A bonded wafer fabrication mechanism for a micro-mirror structure provides for oxidizing a device wafer instead of a handle wafer or splitting thermal oxidation processing between the device wafer and the handle wafer prior to etching. The flatness of mirrors in micro-mirror structures fabricated according to such a mechanism is substantially improved.

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WAFER BONDING TECHNIQUES TO MINIMIZE BUILT-IN STRESS OF SILICON MICROSTRUCTURES AND MICRO-MIRRORS

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims priority from the following U.S. Provisional Patent Application, the disclosure of which is incorporated by reference in its entirety for all purposes:

U.S. Provisional Patent Application Serial No. 60/176,325, entitled "New Wafer Bonding Techniques to Minimize Built-in Stress of Silicon Microstructures and Micro Mirrors," filed January 18, 2000.

BACKGROUND OF THE INVENTION

The invention relates to the fabrication of Silicon-On-Insulator (SOI) structures.

There is great interest in making small opto-mechanical structures out of SOI material using micromachining techniques. One type of SOI wafer is a bonded SOI wafer. Often a bonded SOI wafer is manufactured as two wafers, a device wafer and a handle wafer. The handle wafer is thermally oxidized to form on its surface an oxide layer. Both wafers are chemically treated to become hydrophilic, are aligned and their polished surfaces allowed to come into contact. The wafers adhere to each other and, after a high temperature annealing process, are strongly bonded together. The bonded wafer is ground and polished to form a finished wafer consisting of a handle wafer, an intermediate buried oxide and a device silicon wafer. The device wafer can typically range from less than one micron to several tens of microns in thickness.

Prior scanners use a single crystal SOI fabricated mirror. Generally, to produce a moveable mirror in SOI material, the silicon of the handle wafer is etched away from beneath the device layer and the buried oxide layer serves as a convenient hard etch stop layer during this process. The remaining thin device layer of silicon is etched to form a one- or two-dimensional moveable mirror, as described in U.S. Patent 5,629,790, to Neukermans et al.

Although a silicon mirror should have nearly zero stress and therefore present an optically flat surface, conventional SOI wafer manufacturing processes can affect the flatness of the silicon device layer. Detailed interferometric measurements of the flatness of silicon mirrors approximately 1.5 by 2.1 mm made of bonded SOI material 10 um thick show a non-flatness of up to 0.3 waves (lambda=633um) when fabricated using the standard technology. For very large flat mirrors that are extremely thin as required in many applications, this flatness is not adequate.

SUMMARY OF THE INVENTION

In one aspect of the invention, a method of fabricating a Silicon-On-Insulator (SOI) bonded wafer structure includes oxidizing a device silicon wafer and bonding the oxidized device silicon wafer to a handle silicon wafer.

Embodiments of the invention may include one or more of the following features.

Fabricating the SOI bonded wafer structure can further include lapping the device silicon wafer down to a desired thickness and etching the device silicon wafer to define a mirror.

Fabricating the SOI bonded wafer structure can further include oxidizing the handle silicon wafer prior to bonding the oxidized device silicon wafer to the handle silicon wafer.

The oxidizing of the handler silicon wafer and the oxidizing of the device silicon wafer can each result in oxide films approximately equal to one-half of a desired thickness.

The device silicon wafer, the handle silicon wafer, or both of the silicon wafers can be made of polysilicon.

Among the advantages of the present invention are the following. If the buried oxide layer is grown on the device wafer instead of the handle wafer, the flatness of a silicon mirror fabricated with an SOI manufacturing process so modified may be substantially improved. Similar results may be obtained if an oxide film half the desired thickness is grown on both the handle and device wafers, or the oxide film is split between the two wafers in some other manner.

Other features and advantages of the invention will be apparent from the following detailed description and from the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a side view of a prior art silicon bonded wafer structure.

FIG. 2 is a side view of micro-mirror structure fabricated from a silicon bonded wafer structure.

FIG. 3 is a side view of a silicon bonded wafer structure fabricated using a thermally oxidized device wafer.

FIG. 4 is a side view of a silicon bonded wafer structure fabricated using thermally oxidized handle and device wafers.

FIG. 5 is a side view of a bonded wafer structure fabricated using polysilicon instead of single crystal silicon as the device wafer.

FIG. 6 is a schematic depiction of polysilicon resistive sensors arranged in a Wheatstone bridge arrangement for measuring torque.

DETAILED DESCRIPTION

Referring to FIG. 1, a prior art silicon bonded wafer structure 10 including a set of bonded wafers, more particularly, a handle wafer 12 and a device wafer 14, separated by an oxide layer 16, is shown. Using conventional fabrication techniques, the wafers are bonded as follows. The handle wafer 12 is thermally oxidized to form the oxide layer 16, which typically has a thickness of a few thousand Angstrom. The device wafer 14 is bonded to the oxidized handle wafer 12. Once bonded, the device wafer 14 is lapped down or otherwise thinned to a required thickness.

Referring to FIG. 2, a micro-mirror structure 20 produced from the silicon bonded wafer structure 10 (of FIG. 1) is shown. To transform the silicon bonded wafer structure 10 to the micro-mirror structure 20, etching is performed and a moveable mirror 32 is defined in the device wafer 14. This process is described in U.S. Patent Application Serial Nos. 5,629,790 and 6,044,705, both to Neukermans et al., both incorporated herein by reference. It is found that for very large thin mirrors (e.g., several mm in size and 2-10 micron thick) produced by this process, there are some residual stresses that make such mirrors marginal for use in very

demanding optical applications.

Referring to FIG. 3, an enhanced silicon bonded wafer structure 30 includes the handle wafer 12, the device wafer 14 and the oxide layer 16 disposed therebetween. In order to fabricate the enhanced silicon bonded wafer structure 30, the device wafer 14 is thermally oxidized to form the oxide layer 16. The oxidized device wafer 14 and handle wafer 12 are bonded, and the device wafer 14 is thinned. A micro-mirror structure is provided from the silicon bonded wafer structure 30 using techniques as shown and described in FIG. 2. The mirrors manufactured on the silicon bonded wafer structure 30 are much flatter than those manufactured using conventionally provided a set of bonded wafers.

Other embodiments are contemplated. For example, and with reference to FIG. 4, both the handle wafer 12 and the device wafer 14 can be oxidized to form the oxide layer 16 prior to bonding. The wafers 12, 14 may be oxidized with the same or different thickness. Preferably, the thickness of the oxide grown on the handle wafer 12 is equal to or less than the thickness of the oxide grown on the device wafer 14.

Specifically, using a buried oxide layer of 4000Å and a device wafer or device silicon layer of 10 microns, a mirror 1.5 by 2.1 mm shows an average non-flatness (lambda=633nm) of: 0.22 waves when the handle wafer is oxidized 4000Å; 0.11 waves when the device wafer is oxidized 4000Å; and 0.12 waves when the handle and device wafers are both oxidized 2000Å.

Removal of an interfacial silicon layer on the device wafer 16 by a very short chemical etch after removing the buried oxide layer further relieves built-in stresses.

Although not shown, a single crystal silicon device layer also allows for the incorporation of high sensitivity shear sensors, which allow the positioning of mirrors in micro-mirror structures like the one shown in FIG. 2 with great accuracy.

In yet another embodiment, an SOI structure that includes polysilicon is used to produce a more ductile material.

Referring to FIG. 5, a silicon bonded wafer structure 50 includes the handle wafer 12 and the oxide wafer 16, but the single crystal device wafer 14 (of FIGS. 1-4) is replaced by a polysilicon device wafer 52, of the same size. The polysilicon wafer 52 is lapped down to the desired thickness and, after etching, gives rise to the structure 50. The top layer 52 is polysilicon, and, as before, the intermediate layer 16 is oxide and the bottom layer 12 is a single crystal silicon layer. The polysilicon wafer yields a thick (5-100 micron), stress free layer of polysilicon that is suitable as a mirror plate. The resultant layer of polysilicon is then treated as the single crystal layer for purposes of mirror construction. The polysilicon layer can be used to define polysilicon hinge sensors as well, and in the same manner as single crystal silicon.

The handle wafer 12 can also be made of polysilicon. Thus, one or both of the wafers 12, 14 can be made of polysilicon and an oxide formed on the device wafer 14 (whether it be made of polysilicon or single crystal silicon) as described above.

Referring to FIG. 6, a partial view of a hinge 60 shows four polysilicon resistive sensors 62 placed in a

Wheatstone bridge type arrangement 64 so that the output corresponds to a shear measurement, that is, the diagonal axis of the Wheatstone bridge 64 is along the direction of hinge 62. Applying voltage to a-a produces an output b-b if shear is present. This arrangement is similar to that of measuring torque with classical strain gauges. It may be noted that the polysilicon hinge sensors are not as sensitive as those made from the single crystal silicon.

Other embodiments are within the scope of the following claims.

What is claimed is:

1. A method of fabricating a Silicon-On-Insulator (SOI) bonded wafer structure comprising:

oxidizing a surface portion of a device silicon wafer; and

bonding the oxidized surface portion of the device silicon wafer to a handle silicon wafer.

2. The method of claim 1, further comprising:

lapping the device silicon wafer down to a desired thickness; and

etching the device silicon wafer to define a mirror.

3. The method of claim 2, further comprising:

oxidizing the handle silicon wafer prior to bonding the oxidized device silicon wafer to the handle silicon wafer.

4. The method of claim 3, wherein the oxidizing of the handler silicon wafer and the oxidizing of the device silicon wafer each result in oxide films approximately equal to one-half of a desired thickness.

5. The method of claim 1, wherein the device silicon wafer is made of single crystal silicon.

6. The method of claim 1, wherein the handle silicon wafer is made of single crystal silicon.

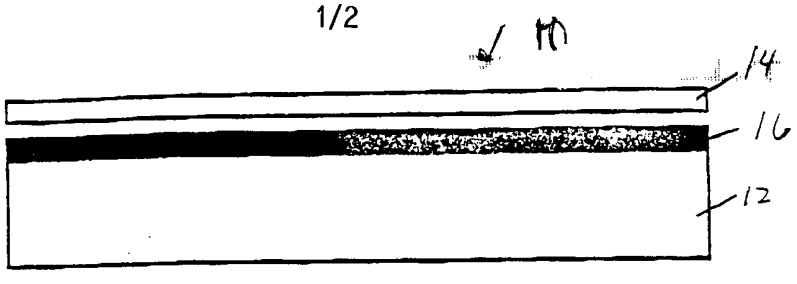

FIG. 1

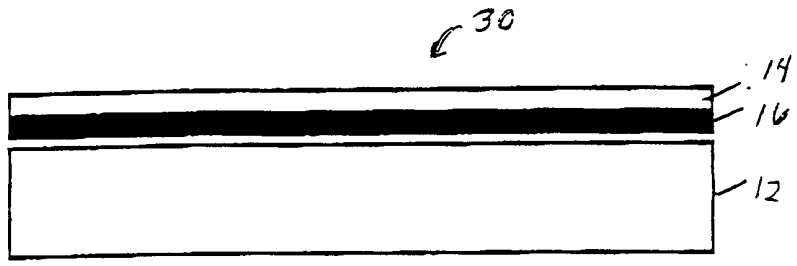

FIG. 3

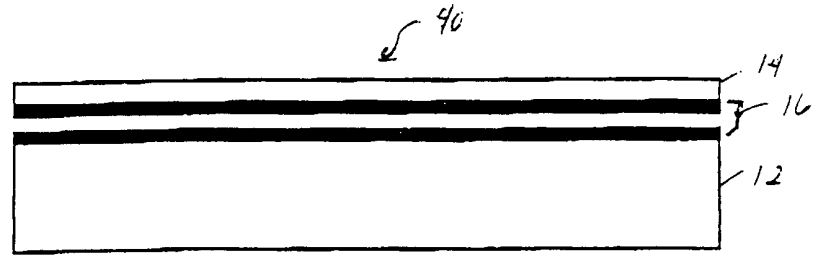

FIG. 4

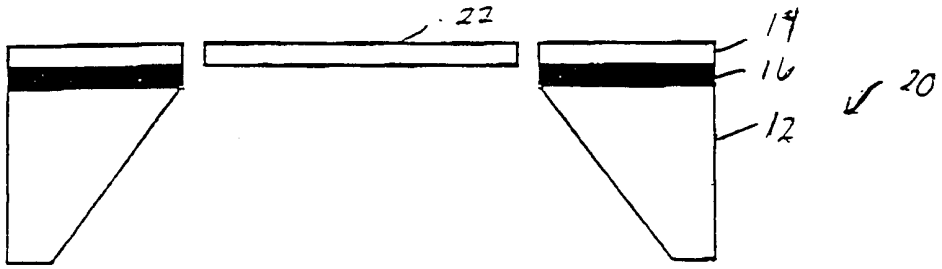

FIG. 2

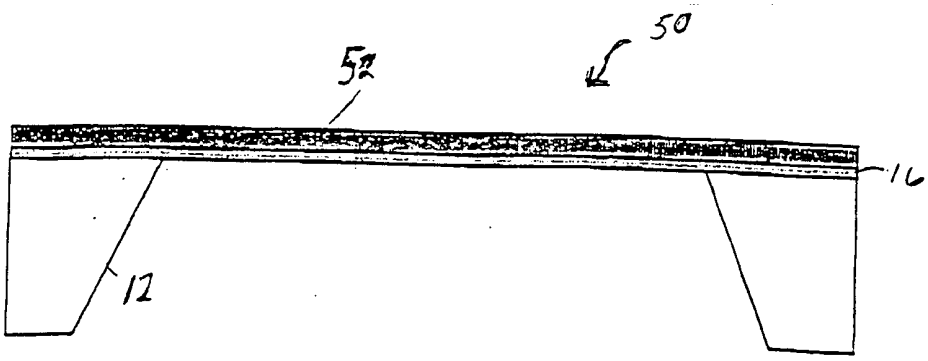

FIG. 5

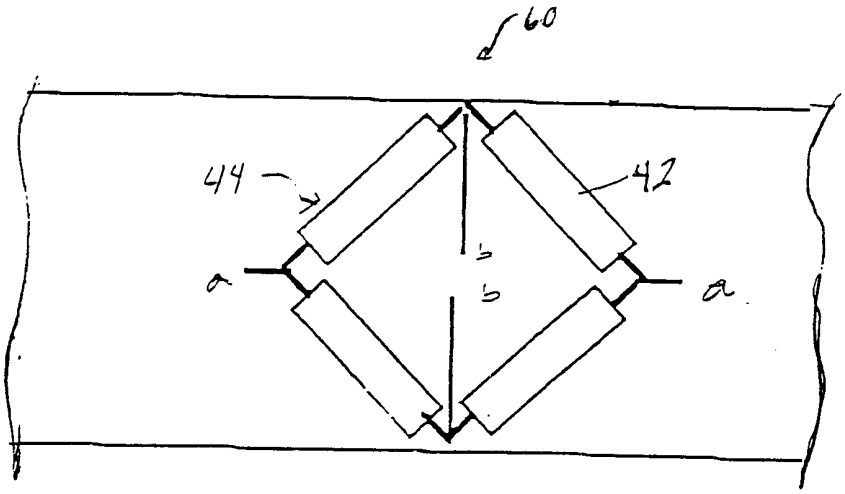

FIG. 6

INTERNATIONAL SEARCH REPORT

Internatic Application No
PCT/US 01/01758

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/20 H01L21/762

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L G02B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, IBM-TDB, INSPEC, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 209 173 A (PHILIPS NV) 21 January 1987 (1987-01-21) abstract; claims; figures 1-3 page 4, line 34 -page 6, line 4 ---	1,5,6
A	US 5 629 790 A (NEUKERMANS ARMAND P ET AL) 13 May 1997 (1997-05-13) cited in the application abstract; claims; figures --- -/--	1-6

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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Date of the actual completion of the international search	Date of mailing of the international search report
23 April 2001	02/05/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Wirner, C

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INTERNATIONAL SEARCH REPORT

Internatic Application No
PCT/US 01/01758

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	HILLER K ET AL: "Low temperature approaches for fabrication of high-frequency microscanners" MINIATURIZED SYSTEMS WITH MICRO-OPTICS AND MEMS, SANTA CLARA, CA, USA, 20-22 SEPT. 1999, vol. 3878, pages 58-66, XP000998250 Proceedings of the SPIE - The International Society for Optical Engineering, 1999, SPIE-Int. Soc. Opt. Eng, USA ISSN: 0277-786X page 62, paragraph 3; figure 6; table 1 ---	1-6
X	BAUMGART H ET AL: "Evaluation of wafer bonding and etch back for SOI technology" PHILIPS JOURNAL OF RESEARCH,NL,ELSEVIER, AMSTERDAM, vol. 49, no. 1, 1995, pages 91-124, XP004011508 ISSN: 0165-5817 page 94, line 18 - line 25 ---	1,5,6
X	PATENT ABSTRACTS OF JAPAN vol. 017, no. 514 (E-1433), 16 September 1993 (1993-09-16) -& JP 05 136014 A (SUMITOMO METAL MINING CO LTD), 1 June 1993 (1993-06-01) abstract; figures ---	1,5,6
X	PATENT ABSTRACTS OF JAPAN vol. 1995, no. 06, 31 July 1995 (1995-07-31) -& JP 07 074329 A (TOSHIBA CORP), 17 March 1995 (1995-03-17) abstract; figures ---	1,5,6
X	US 5 597 410 A (YEN YUNG C) 28 January 1997 (1997-01-28) abstract; claims; figures -----	1,5,6

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Internatic Application No
PCT/US 01/01758

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0209173 A	21-01-1987	NL 8501773 A	16-01-1987
		AU 585355 B	15-06-1989
		AU 5885486 A	24-12-1986
		CA 1245776 A	29-11-1988
		DE 3676367 D	07-02-1991
		ES 556144 D	01-07-1987
		ES 8707023 A	16-09-1987
		JP 2608548 B	07-05-1997
		JP 61294846 A	25-12-1986
		US 4983251 A	08-01-1991
US 5629790 A	13-05-1997	US 5488862 A	06-02-1996
		US 5648618 A	15-07-1997
		US 6044705 A	04-04-2000
JP 05136014 A	01-06-1993	NONE	
JP 07074329 A	17-03-1995	NONE	
US 5597410 A	28-01-1997	NONE	