



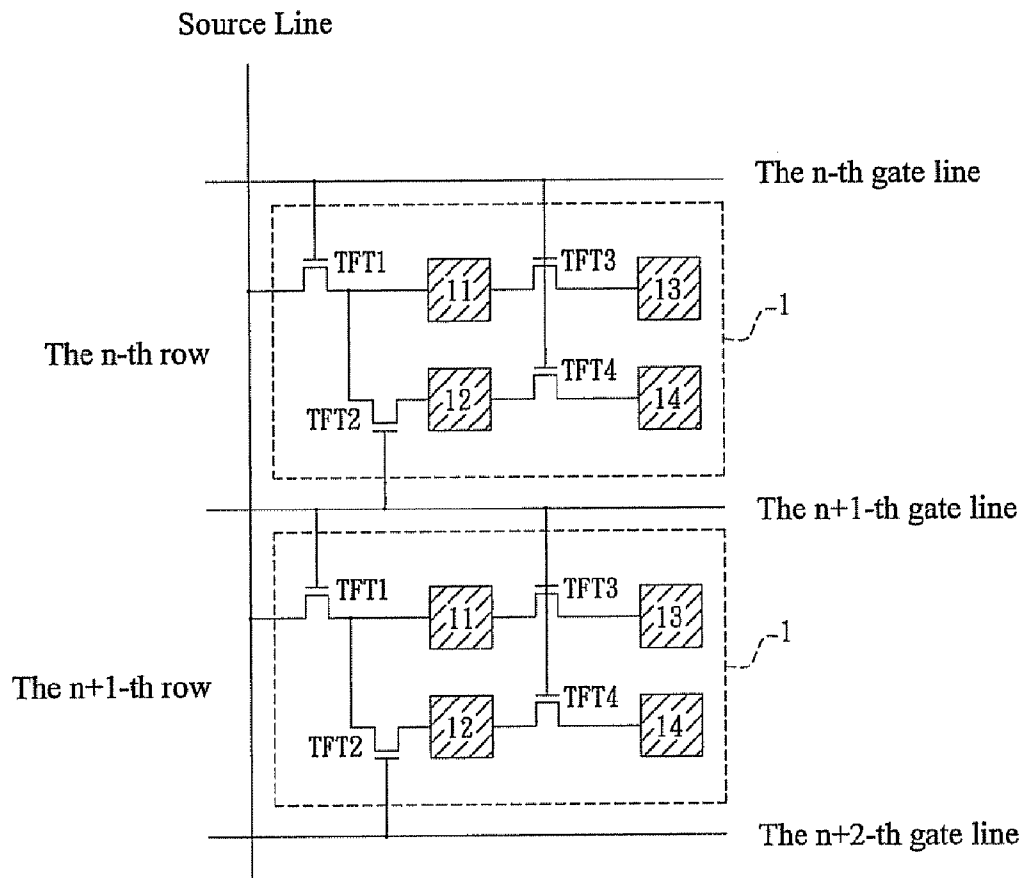
US 20120235979A1

(19) **United States**(12) **Patent Application Publication**
SHIBAZAKI et al.(10) **Pub. No.: US 2012/0235979 A1**(43) **Pub. Date: Sep. 20, 2012**(54) **LIQUID CRYSTAL DISPLAY SUB-PIXEL
WITH THREE DIFFERENT VOLTAGE
LEVELS****Publication Classification**(51) **Int. Cl.**
G09G 3/36 (2006.01)
G09G 5/00 (2006.01)(75) Inventors: **Minoru SHIBAZAKI**, Kobe (JP);
Keitaro Yamashita, Kobe (JP)(73) Assignee: **TPO Displays Corp.**(52) **U.S. Cl. 345/212; 345/87**(21) Appl. No.: **13/433,073**(22) Filed: **Mar. 28, 2012**(57) **ABSTRACT**

This present invention provides a liquid crystal display (LCD) device in which the sub-pixel is provided with three different voltage levels, so that image quality is improved without the configuration of additional gate lines. The present invention overcomes the reduction of aperture ratio in conventional LCD devices due to the configuration of additional gate lines. By the present invention, the white washout problem relating to the off-axis viewing angle can be overcome while the aperture ratio is not reduced.

Related U.S. Application Data(63) Continuation of application No. 12/381,262, filed on
Mar. 9, 2009.(30) **Foreign Application Priority Data**

Mar. 21, 2008 (JP) 2008-073756



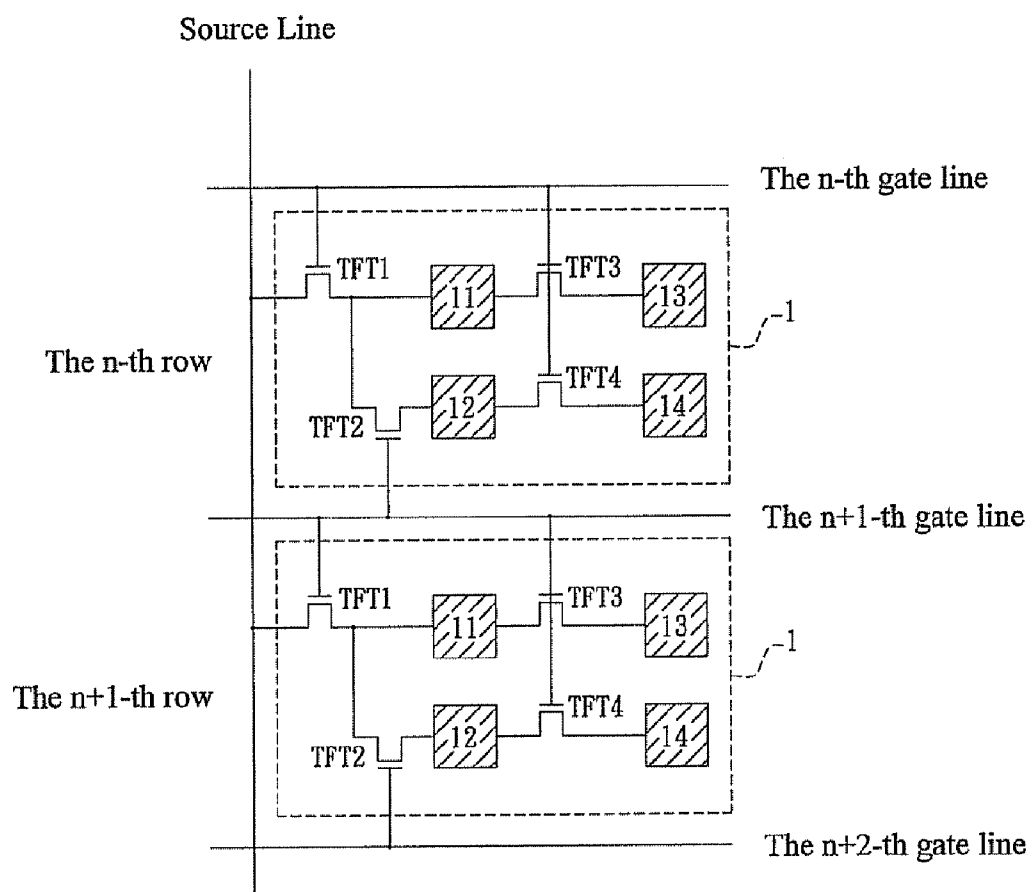


Fig. 1

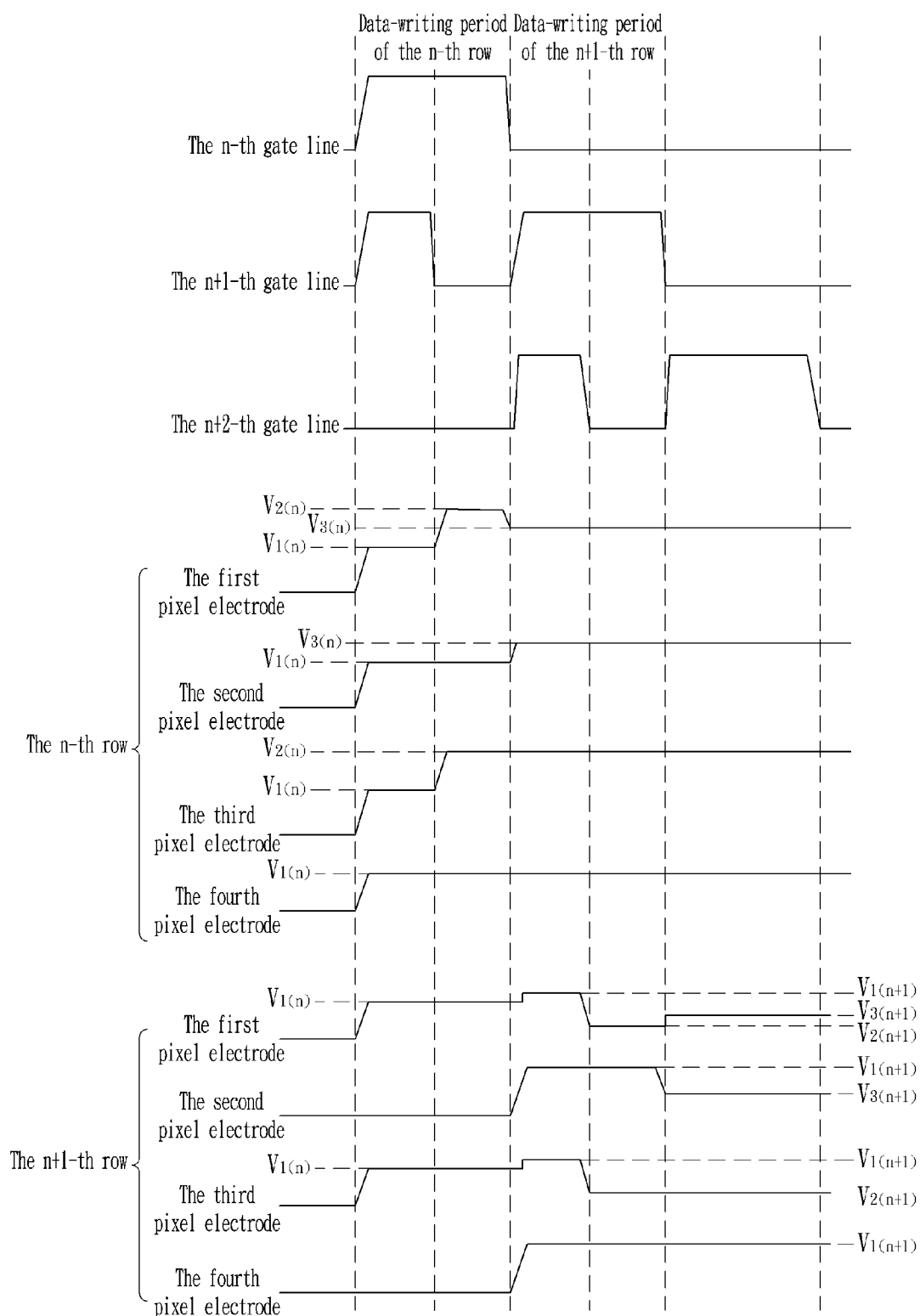


Fig. 2

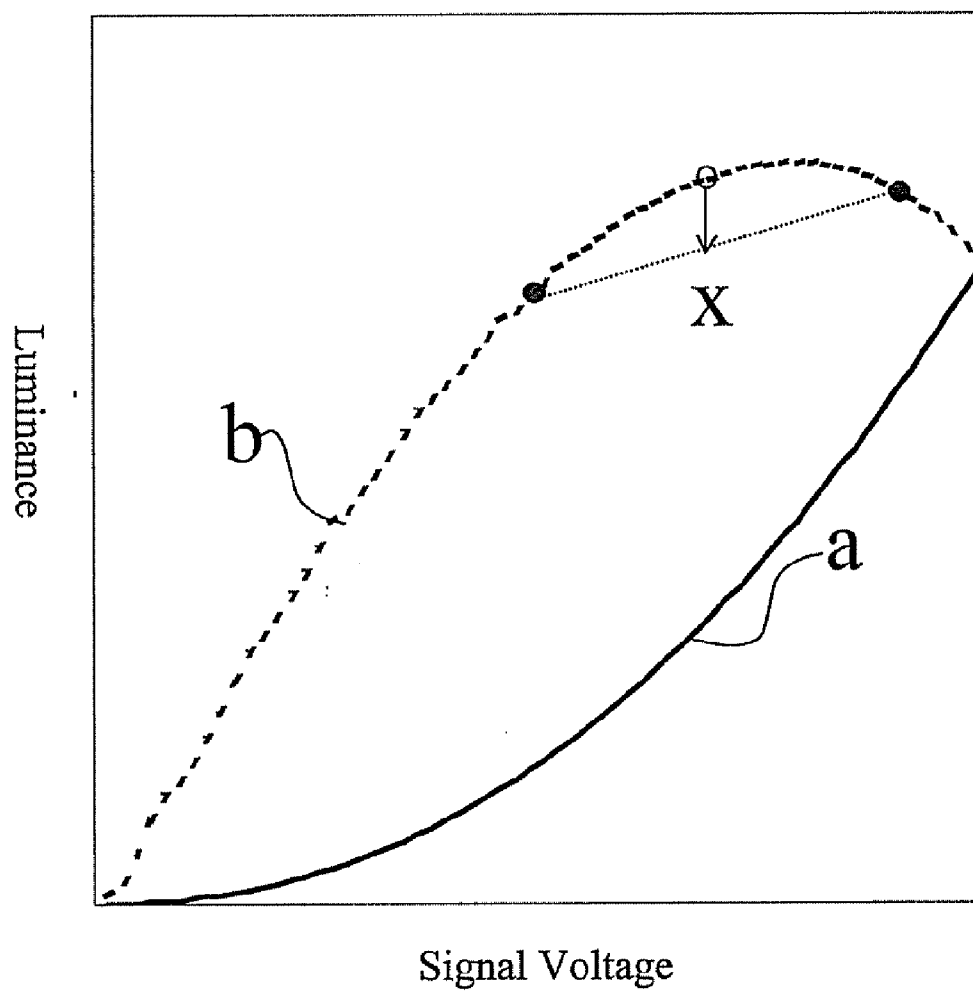


Fig. 3 (Prior Art)

LIQUID CRYSTAL DISPLAY SUB-PIXEL WITH THREE DIFFERENT VOLTAGE LEVELS

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a liquid crystal display (LCD) device, and more particularly, to an LCD device that improves the issue of white washout relating to the off-axis viewing angle.

[0003] 2. Description of the Related Art

[0004] Since LCD devices have the advantages of thin sizes and low power consumption, they are widely used as the screens of computers, portable electronic devices and televisions. Generally such an LCD device is constructed by a liquid crystal layer sandwiched between an upper substrate and a lower substrate, and then electrodes formed on the respective substrates are used to control the orientation of liquid crystal molecules for display.

[0005] Depending upon the brightness of environment, the so-called transmissive LCD may function in two modes, including a transmissive mode utilizing the backlight and a reflective mode utilizing the incident light. The transmissive LCD includes a transmissive area and a reflective area, in which the transmissive area is used in the transmissive mode, while the reflective area is used in the reflective mode. In the transmissive area, incident light coming from the backside of the display panel passes through the liquid crystal layer directly and then emits from the front side of the display panel. In the reflective area, incident light coming from the front side of the display panel passes through the liquid crystal layer and is reflected by a reflector, and then emits from the front side of the display panel.

[0006] Along with the expanding needs for small-sized LCDs used in devices like mobile phones, transmissive LCD devices are required to provide higher image quality. For a conventional transmissive LCD device, to make the respective gamma curves of the transmissive and reflective modes consistent, the liquid crystal cells in the transmissive and reflective areas are provided with varied cell gaps. However, this will make the manufacturing process more complicated. Further, because of the height difference in the boundary area, it is difficult to control the orientation of liquid crystal molecules with high accuracy. On the other hand, for applying different driving voltage levels for the reflective and transmissive modes, it requires to control the voltage by means of dividing pixels in the transmissive area, which causes the circuits to become complicated and reduces the aperture ratio as well.

[0007] FIG. 3 shows the gamma curve of a transmissive LCD device disclosed in the JP Patent publication No. 2006-313358, wherein the pixels in the transmissive area are divided for voltage control. As FIG. 3 shows, compared to the gamma curve a, with a viewing angle of 0 degree at the front side, the gamma curve b, with a viewing angle of 45 degrees at the front side, is shifted. In this case, if pixels T1 and T2 in the transmissive area are provided with different signal voltages, the average luminance values from the viewing angle of 45 degrees at the front side will approach the gamma curve a, referring to the arrow in FIG. 3. As a result, the pixels in the transmissive area can be divided and thus provided with different signal voltages, making the average luminance values of this area approach those of the reflective area. Besides, the

conventional LCD devices generally have the white washout problem relating to the off-axis viewing angle.

[0008] To overcome the white washout problem, two additional gate lines are arranged in the LCD device to control two different voltage levels to be applied to two pixel electrodes within a pixel unit. However, such construction will reduce the aperture ratio; moreover, when such construction is applied to a transmissive LCD device, the corresponding data will not be written into the pixel electrodes in the reflective mode, which results in issues of white saturation and black saturation of the image.

SUMMARY OF THE INVENTION

[0009] An object of the present invention is to provide an LCD device in which the sub-pixel is provided with three different voltage levels, so that image quality is improved without the configuration of additional gate lines, and the reduction of aperture ratio in conventional LCD devices resulting from adding gate lines is also addressed.

[0010] An embodiment of the LCD device of the present invention comprises a source line, an n-th gate line, an n+1-th gate line and a sub-pixel. The sub-pixel is arranged on the n-th row and comprises a first semiconductor switch, a second semiconductor switch, a third semiconductor switch, a fourth semiconductor switch, a first pixel electrode, a second pixel electrode, a third pixel electrode and a fourth pixel electrode. The first semiconductor switch is electrically connected to the n-th gate line, the source line and the first pixel electrode, the n-th gate line enabling the source line and the first pixel electrode by switching on the first semiconductor switch. The second semiconductor switch is electrically connected to the n+1-th gate line, the first pixel electrode and the second pixel electrode, the n+1-th gate line enabling the first pixel electrode and the second pixel electrode by switching on the second semiconductor switch. The third semiconductor switch is electrically connected to the n-th gate line, the first pixel electrode and the third pixel electrode, the n-th gate line enabling the first pixel electrode and the third pixel electrode by switching on the third semiconductor switch. The fourth semiconductor switch is electrically connected to the n-th gate line, the second pixel electrode and the fourth pixel electrode, the n-th gate line enabling the second pixel electrode and the fourth pixel electrode by switching on the fourth semiconductor switch. After a data-writing period of the n-th row, the second pixel electrode and the fourth pixel electrode have a first voltage level, while the first pixel electrode and the third pixel electrode have a second voltage level. During a data-writing period of the n+1-th row, the n+1-th gate line enables the first pixel electrode and the second pixel electrode by switching on the second semiconductor switch so as to provide the first pixel electrode and the second pixel electrode with a third voltage level respectively.

[0011] In an embodiment of the present invention, during a data-writing period of the n-th row, the source line is provided with the first voltage level and the second voltage level sequentially. During a data-writing period of the n-th row, after the n-th gate line and the n+1-th gate line control the first voltage level and provide the first voltage level to the first pixel electrode, the second pixel electrode, the third pixel electrode and the fourth pixel electrode, the n-th gate line controls the second voltage level and provides the second voltage level to the first pixel electrode and the third pixel electrode. The third voltage level is between the first voltage level and the second voltage level. The first pixel electrode

and the second pixel electrode are used in a reflective mode. The first semiconductor switch, the second semiconductor switch, the third semiconductor switch and the fourth semiconductor switch are thin film transistors. The LCD device is used in an electronic device.

[0012] A method for driving an LCD device of the present invention comprises the steps of: providing a first voltage level to a first pixel electrode, a second pixel electrode, a third pixel electrode and a fourth pixel electrode of a sub-pixel; providing a second voltage level to the first pixel electrode and the third pixel electrode of the sub-pixel; and during a data-writing period of pixels of the next row, enabling the first pixel electrode and the second pixel electrode so as to provide a third voltage level thereto.

[0013] With the LCD device of the present invention, the reduction of aperture ratio will be prevented, and the issue of white washout relating to the off-axis viewing angle is addressed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] FIG. 1 is a schematic view showing the pixel arrangement of an embodiment of an LCD device of the present invention;

[0015] FIG. 2 is a timing diagram showing the driving circuit of an embodiment of an LCD device of the present invention; and

[0016] FIG. 3 is a diagram showing the gamma curve of a conventional transfective LCD device according to the prior art.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0017] FIG. 1 is a schematic view showing the pixel arrangement of an embodiment of an LCD device of the present invention. As FIG. 1 shows, the LCD device comprises a source line, a plurality of gate lines and a sub-pixel 1. The sub-pixel 1 is arranged on the n-th row and comprises first to fourth semiconductor switches TFT1 to TFT4 and first to fourth pixel electrodes 11 to 14. The first semiconductor switch TFT1 is electrically connected to the n-th gate line, the source line and the first pixel electrode 11. The n-th gate line enables the source line and the first pixel electrode 11 by switching on the first semiconductor switch TFT1. The second semiconductor switch TFT2 is electrically connected to the n+1-th gate line, the first pixel electrode 11 and the second pixel electrode 12. The n+1-th gate line enables the first pixel electrode 11 and the second pixel electrode 12 by switching on the second semiconductor switch TFT2. The third semiconductor switch TFT3 is electrically connected to the n-th gate line, the first pixel electrode 11 and the third pixel electrode 13. The n-th gate line enables the first pixel electrode 11 and the third pixel electrode 13 by switching on the third semiconductor switch TFT3. The fourth semiconductor switch TFT4 is electrically connected to the n-th gate line, the second pixel electrode 12 and the fourth pixel electrode 14. The n-th gate line enables the second pixel electrode 12 and the fourth pixel electrode 14 by switching on the fourth semiconductor switch TFT4.

[0018] In this embodiment, the first to fourth semiconductor switches TFT1 to TFT4 are N-type TFTs. The first semiconductor switch TFT1 has a source terminal connected to the source line, a drain terminal connected to the first pixel electrode 11, and a gate terminal connected to the n-th gate line.

The second semiconductor switch TFT2 has a source terminal connected to the drain terminal of the first semiconductor switch TFT1, a drain terminal connected to the second pixel electrode 12, and a gate terminal connected to the n+1-th gate line. The third semiconductor switch TFT3 has a source terminal connected to the first pixel electrode 11, a drain terminal connected to the third pixel electrode 13, and a gate terminal connected to the n-th gate line. The fourth semiconductor switch TFT4 has a source terminal connected to the second pixel electrode 12, a drain terminal connected to the fourth pixel electrode 14, and a gate terminal connected to the n-th gate line.

[0019] Moreover, the first to fourth semiconductor switches TFT1 to TFT4 are not limited to N-type TFTs; they can be P-type TFTs as well.

[0020] FIG. 2 is a timing diagram showing a method for driving an LCD device of the present invention. First, during the data-writing period of the n-th row, the source line is provided with a first voltage level V1(n) and a second voltage level V2(n) sequentially. In detail, the n-th gate line and the n+1-th gate line of the next row control the first to fourth semiconductor switches TFT1 to TFT4 and switch all of them on; thus, the source line provides with the first voltage level V1(n) to the first to fourth pixel electrodes 11 to 14. Since the n-th gate line switches on the first semiconductor switch TFT1, the third semiconductor switch TFT3 and the fourth semiconductor switch TFT4 only, the voltage level of the pixel electrodes 12 and 14 are set at the first voltage level V1(n). The source line, then, provides with the second voltage level V2(n) to the other pixel electrodes 11 and 13.

[0021] In addition, during the data-writing period of the n-th row, the first voltage level V1(n) may be given to the first semiconductor switch TFT1 and the third semiconductor switch TFT3 of a pixel on the next row. Then, the first voltage level V1(n) is provided for the pixel electrodes 11 and 13, and the correct data of the next row will be written into them accordingly.

[0022] Next, during the data-writing period of the n+1-th row, the n+1-th gate line controls the second semiconductor switch TFT2 of the n-th row and switches it on, enabling the first pixel electrode 11, which is provided with the first voltage level V1(n), and the second pixel electrode 12, which is provided with the second voltage level V2(n). Therefore, during the data-writing period of the n+1-th row, the first pixel electrode 11 and the second pixel electrode 12 of the n-th row is provided with a third voltage level V3(n), which is between the first voltage level V1(n) and the second voltage level V2(n). As a result, a pixel structure will comprise pixel electrodes of three different voltage levels.

[0023] Similarly, since the steps with respect to the n-th gate line and the sub-pixel of the n-th row can be applied to those of the n+1-th row, the correct data will be written into the pixel electrodes 11 and 13 of the n+1-th row.

[0024] With an LCD device of the present invention, a sub-pixel can comprise pixel electrodes of three different voltage levels without the configuration of additional gate lines or source lines. As a result, aperture ratio of the LCD device is not reduced, and the image quality is enhanced. Furthermore, by using the third and fourth pixel electrodes in the transmissive mode, and the first and second pixel electrodes in the reflective mode, the issue of white washout relating to the off-axis viewing angle can be addressed. Besides, the disadvantage of issues of white saturation and black saturation of the image can be avoided.

[0025] The LCD device of the present invention may also be used in a portable electronic device such as mobile phone, digital camera, PDA, automotive display, aircraft display, digital photo frame or portable DVD player.

1-8. (canceled)

9. An electronic device, comprising:

a liquid crystal display (LCD) device, comprising:

a source line;

an n-th gate line;

an n+1-th gate line; and

a sub-pixel of the n-th row, said sub-pixel comprising a first semiconductor switch, a second semiconductor switch, a third semiconductor switch, a fourth semiconductor switch, a first pixel electrode, a second pixel electrode, a third pixel electrode and a fourth pixel electrode;

wherein said first semiconductor switch is electrically connected to said n-th gate line, said source line and said first pixel electrode, said n-th gate line enabling said source line and said first pixel electrode by switching on said first semiconductor switch; said second semiconductor switch is electrically connected to said n+1-th gate line, said first pixel electrode and said second pixel electrode, said n+1-th gate line enabling said first pixel electrode and said second pixel electrode by switching on said second semiconductor switch; said third semiconductor switch is electrically connected to said n-th gate line, said first pixel electrode and said third pixel electrode, said n-th gate line enabling said first pixel electrode and said third pixel electrode by switching on said third semiconductor switch; said fourth semiconductor switch is electrically connected to said n-th gate line, said second pixel electrode and said fourth pixel electrode, said n-th gate line enabling said second pixel electrode and said fourth pixel electrode by switching on said fourth semiconductor switch; and

wherein after a data-writing period of the n-th row, said second pixel electrode and said fourth pixel electrode have a first voltage level, while said first pixel electrode and said third pixel electrode have a second voltage level; and during a data-writing period of the n+1-th row, said n+1-th gate line enables said first pixel electrode

and said second pixel electrode by switching on said second semiconductor switch so as to provide said first pixel electrode and said second pixel electrode with a third voltage level respectively.

10. A method for driving an LCD device, comprising the steps of:

electrically connecting a first semiconductor switch with a n-th gate line, a source line and a first pixel electrode; switching on said first semiconductor switch by said n-th gate line to enable said source line and said first pixel electrode;

electrically connecting a second semiconductor switch with a n+1-th gate line, said first pixel electrode and a second pixel electrode;

switching on said second semiconductor switch by said n+1-th gate line to enable said first pixel electrode and said second pixel electrode;

electrically connecting a third semiconductor switch with said n-th gate line, said first pixel electrode and a third pixel electrode;

switching on said third semiconductor switch by said n-th gate line to enable said first pixel electrode and said third pixel electrode;

electrically connecting a fourth semiconductor switch with said n-th gate line, said second pixel electrode and a fourth pixel electrode;

switching on said fourth semiconductor switch by said n-th gate line to enable said second pixel electrode and said fourth pixel electrode;

after a data-writing period of the n-th row, providing a first voltage level to said second pixel electrode and said fourth pixel electrode, and providing a second voltage level to said first pixel electrode and said third pixel electrode; and

during a data-writing period of the n+1-th row, enabling said first pixel electrode and said second pixel electrode by said n+1-th gate line through switching on said second semiconductor switch so as to provide a third voltage level respectively to said first pixel electrode and said second pixel electrode.

* * * * *