

[54] **LADDER TERMINATION CIRCUIT**

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[22] Filed: **March 24, 1971**

[21] Appl. No.: **127,503**

[52] U.S. Cl. **330/19, 330/17, 330/22, 330/30 R, 340/347 DA**

[51] Int. Cl. **H03f 3/68**

[58] Field of Search **330/19, 22, 30 D, 30 R; 340/347 DA**

[56]

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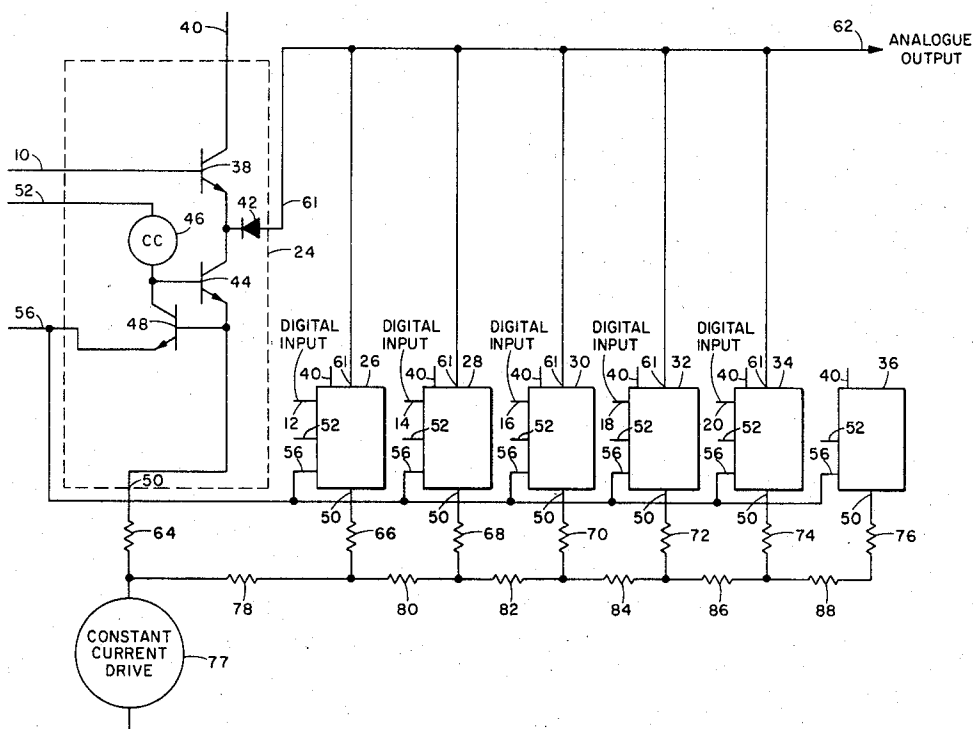
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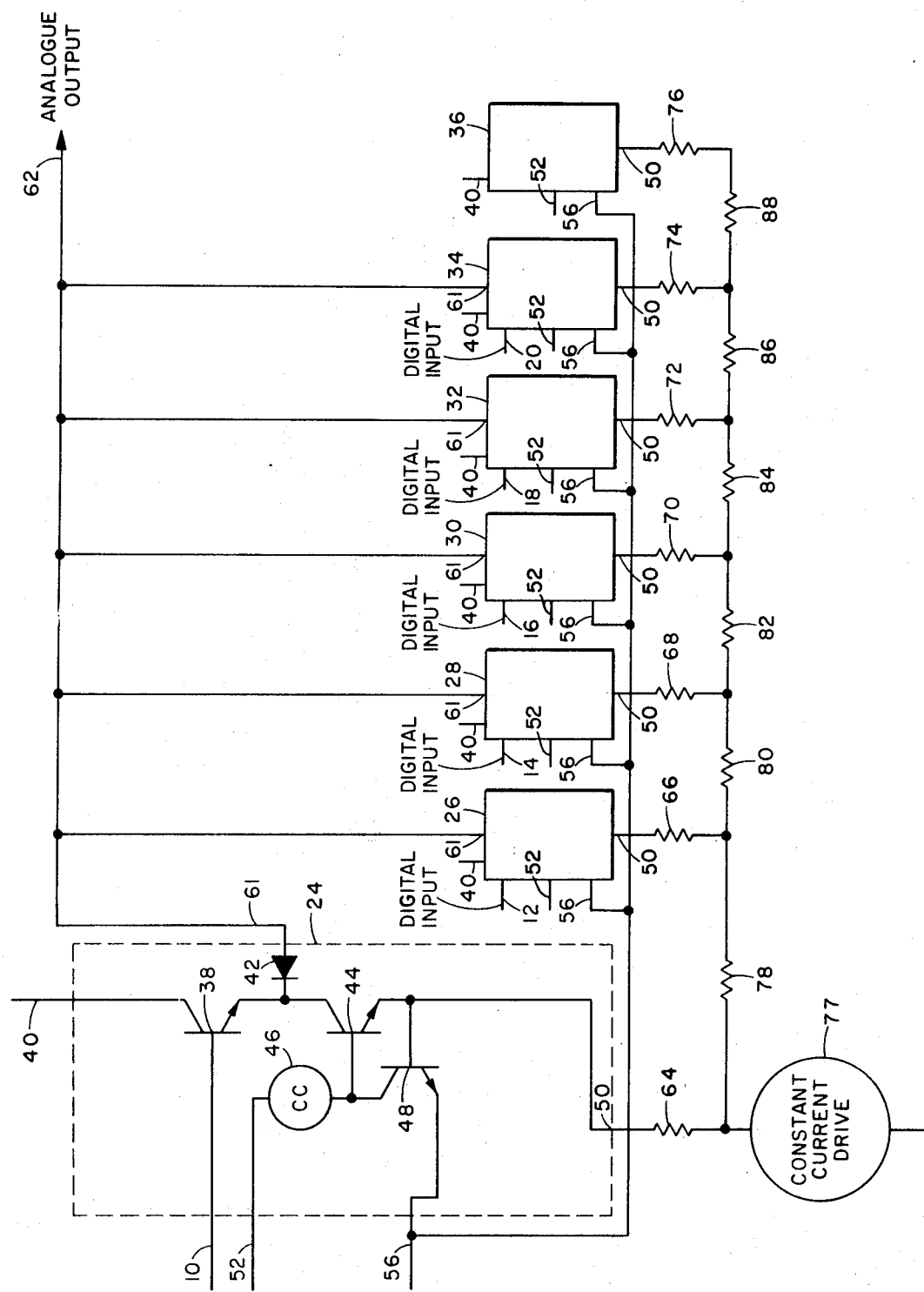
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ABSTRACT

An improved and simplified termination circuit for the ladder portion of a digital to analog converter. the termination circuit includes an amplifier having unity current factor, known ladder termination voltage, and a very low impedance looking from the ladder into the amplifier.

6 Claims, 1 Drawing Figure





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LADDER TERMINATION CIRCUIT

BACKGROUND

A digital number is converted in accordance with the prior art into an analog amount by circuits employing a known resistance network which is called a ladder. The various branches of the network or rungs of the ladder carry currents which are digitally related and a digital number input causes the current in a rung or rungs of the ladder to flow in an analog output circuit. The several rungs are terminated in the prior art by connections to respective transistors which are operated in a common base mode and whose emitter areas are related to the current flow in the respective rungs, whereby the current flow in the several rungs may be independent of each other and may be independently connected to the analog output circuit, so that the current in the analog output circuit may be controlled in a digital manner. The transistors having various areas of the emitters are difficult to deposit on a chip with high enough degree of accuracy to provide a low and uniform resistance at the several emitters and the same potential at the several emitters, and also to provide a properly scaled current flow from the several emitters.

It is an object of this invention to provide an improved terminating network for the rungs of a digital to analog ladder circuit.

It is another object of this invention to provide a termination network comprising an amplifier having a unity amplification factor for current and produces a known ladder termination voltage and a low resistance when seen from the direction of the rungs of the ladder.

SUMMARY

According to this invention, the analog output terminal is connected to the rungs of a ladder by way of separate amplifiers. Each amplifier, which is simpler, cheaper to make and more accurate than known such amplifiers, has a one to one current ratio whereby the currents going into and out of the amplifier are equal. The amplifier also produces a known ladder termination voltage whereby an input or bias terminal of the amplifier controls the output voltage at the ladder terminal of the amplifier and also the amplifier is so constructed that the ladder terminal into the amplifier sees a low impedance or resistance. The amplifier consists of two transistors, the bases of which are being connected to the collector of the other and the emitter of the one being connected to the base of the other. A constant current source supplies current for the collector emitter path of the other transistor. The current to be amplified flows in the collector to emitter path of the one transistor.

DESCRIPTION

The invention will be better understood upon reading the following description in connection with the accompanying drawing, the single FIGURE of which illustrates a digital to analog ladder including the termination amplifiers of the present invention.

In the FIGURE, a binary number, consisting of the digits, zeros and ones, is applied to the several terminals 10, 12, 14, 16, 18 and 20. The most significant digit is applied to the input terminal 10 and the other digits are applied in the order of lesser significance to

the input terminals 12, 14, 16, 18 and 20, respectively. The contents of the dotted rectangle 24 and of the rectangles 26, 28, 30, 32 and 34 are the same. The contents of the rectangle 36 differ from the contents of the rectangles 24 to 34 only in that there is no provision for a digital input terminal such as the terminals 10 to 20 of the rectangles 24 to 34 whereby an output terminal such as 61 is not required for the rectangle 36. Therefore, only the contents of the rectangle 24 are described. The input terminal 10 is connected to the base of an NPN transistor 38 which acts as a switch. Since all the transistors shown are of the NPN type, no further mention of the type of transistors will be made in this description. The collector of the transistor 38 is connected to an input terminal 40 to which the positive terminal of the power supply source (not shown) is to be connected. The emitter of the transistor 38 is connected to the cathode of a diode 42 and to the collector of a transistor 44. (In the rectangle 36, no transistor 38 or diode 42, which comprise switching means, or input terminal such as 10 need be provided and the terminal 40 is connected directly to the collector of a transistor such as the transistor 44.) The base of the transistor 44 is connected to a terminal of a constant current source 46 and to the collector of transistor 48. The emitter of the transistor 44 is connected to the base of the transistor 48 and to a ladder terminal 50 of the amplifier in the rectangle 24. A voltage supply terminal 52 is connected at the other terminal thereof to the constant current source 46. The connection 61 to the anode of the diode 42 is the output of the amplifier 24. Each of the amplifiers comprising the elements 44, 46 and 48 as well as the switch which comprises the elements 38 and 42 in the rectangles 26 to 34 are, as has been noted, identical with the amplifier 24. However, only the input terminals 12 to 20, the bias terminals 56, the ladder terminals 50, the supply terminals 40 and the output terminals 61 are shown for the rectangles 26 to 34 and, for the rectangle 36, the input terminal and the output terminal 61 are omitted. All the terminals 61 are connected to the analog terminal 62 whereby the current at the terminal 62 is the sum of the current from the several terminals 61 as controlled by the digital inputs 10 to 20.

While the ladder network having branches or rungs is well known, it is described for completeness. The ladder terminals 50 of the amplifiers 24, 26, 28, 30, 32, 34 and 36 are connected to one terminal of the respective resistors 64, 66, 68, 70, 72, 74 and 76. The other terminal of the resistor 64 is connected to one terminal of constant current device 77 whose other terminal is connected to the other terminal of the source (not shown) which is connected to the terminal 40. The said other terminal of the resistor 64 is connected to the other terminal of the resistor 66 by way of a resistor 78. The other terminals of the resistors 66 and 68 are connected by way of resistor 80. The other terminals of the resistors 68 and 70 are connected by way of resistor 82. The other terminal of the resistors 70 and 72 are connected by way of resistor 84. The other terminals of the resistors 72 and 74 are connected by way of resistor 86, and the other terminals of the resistors 74 and 76 are connected by way of a resistor 88. Then, if the resistance of the resistors 64, 66, 68, 70, 72 and 74 are each equal to twice the resistances of resistors 76, 78,

80, 82, 84, 86 and 88, then the conventional current flowing out of the terminals 50 of the rectangles 24, 26, 28, 30, 32, 34 and 36 are equal to 32I, 16I, 8I, 4I, 2I, I and I, respectively where the constant current drive 77 is equal to 64I. As noted above, there is no terminal 61 for the rectangle 36, whereby when digital zeros (using positive logic) are applied to all the digital input terminals 10, 12, 14, 16, 18 and 20, 63I current flows in the analog terminal 62 and when digital ones are applied to the terminals 10, 12, 14, 16, 18 and 20 no current flows in the digital output terminal 62 and, similarly for any binary number applied to the terminals 10, 12, 14, 16, 18 and 20, the most significant digit being applied to the terminal 10, as noted above, the current flow in the analog terminal 62 is determined by the value of the binary number.

Having explained the general operation of digital to analog converters, the operation of the amplifier included in the rectangle 24 is now described. As noted, the transistor 38 and the diode 42 comprise a switch and are not part of the amplifier. As noted above, conventional current flows from the terminal 40, through the collector to emitter paths of the transistors 38 and 44 in series to the ladder terminal 50 when a binary one is applied to the base of the transistor 38, and this current flows from the terminal 62 through the diode 42 through the collector to emitter path of the transistor 44 and through the terminal 50 when the transistor 38 is blocked by the application of a negative voltage with respect to the voltage at the terminal 62 indicating a binary zero applied to the base thereof, and the other amplifiers included in the rectangles 26 to 34 operate similarly. The ratio of the current flow at the collector of the transistor 44 to that at the terminal 50 for each of the amplifiers in the rectangles 24 to 34 must be unity at all times for the digital to analog converter to operate properly. That is, the current at the collector of the transistor 44 must always be equal to the current at the terminal 50 and to accomplish this result, the amplifiers in the rectangles 24 to 34, must have a current amplification value of unity.

Since both of the transistors 44 and 48 have high Betas, (on the order of 100), and since the current supplied by the source 46 is small, the base current for the transistor 48 is very small. Furthermore due to the high Beta of the transistor 44, the base current for this transistor is also small. Therefore, the collector current of the transistor 44 is substantially equal to the current at terminal 50. Also, it will be noted that some of the current flow out of the emitter of the transistor 44 is derived from the base thereof whereby the current at the emitter of the transistor 44 is greater than the current at the collector thereof. At least some of this additional current (which is very small) is used to supply base current for the transistor 48 and therefore does not appear at the terminal 50. Therefore, due to the two cooperating effects, the current amplification of the amplifier in the rectangles 24-34 are all equal to unity.

As is required for proper operation of the ladder, the voltage at all the ladder terminals 50 is maintained at the same voltage, the voltage being related to the voltage of the bias terminal 56. This is accomplished as follows.

It will be noted that the collector to emitter current for the transistor 48 is supplied by a constant current source 46. Due to the high beta of transistor 44, a small amount of the current provided by the constant current source 46 is used as base current for the transistor 44. Since this base current is very low, the current flowing out of the emitter of the transistor 48 is constant and is very nearly equal to the current supplied by the constant current source 46. A constant desired bias voltage is connected to the bias terminal 56, whereby the voltage at the base of the transistor 48, and therefore at the terminal 50 of the amplifier 24, differs from the voltage at the terminal 58 by the emitter to base drop of the transistor 48. Since each of the amplifiers 26, 28, 30, 32 and 34 and 36 contain similar circuits and since corresponding elements in the several amplifiers are as nearly identical as the state of the art will permit, and since the terminals 56 are all connected together, the voltage at the terminal 50 of all the amplifiers 24, 26, 28, 33, 34 and 36 are the same.

Furthermore, the resistance of the amplifiers 24 to 36 is low looking into the amplifiers from the ladder terminals 50. This is due to the fact that the terminal 50 is connected to a base of a transistor 48 and to the emitter of another transistor 44. Due to the negative feedback produced by the connection of the transistors 44 and 48, as is well known, the resistance of the amplifiers in the rectangles 24 to 36 is low. Since this resistance is low with respect to the resistance of the ladder elements 64 to 88 the ladder can be accurately constructed without the necessity of taking into account large amplifier resistances.

While a 6 bit ladder is shown, the number of bits can be made as great or as small as desired by adding or subtracting amplifiers and ladder sections. While NPN transistors are shown, PNP transistors may be substituted therefore in a known manner. While this invention is best suited to be put on a chip, discrete elements may be used if desired.

What is claimed is:

1. An amplifier having unity current amplification between a first current supply terminal and a network terminal and which provides low resistance at said network terminal to circuits connected to said network terminal comprising

first and second transistors each having a collector, an emitter and a base,

constant current source means for feeding a constant current to the collector of said first transistor,

means for connecting the collector of said first transistor to the base of said second transistor,

means for connecting the base of said first transistor to the emitter of said second transistor,

means for connecting the emitter of said first transistor to a bias terminal,

switch means coupled between said first current supply terminal and the collector of said second transistor,

a second current supply terminal,

diode means coupled between said second current supply terminal and the collector of said second transistor, and

means for connecting the base of said first transistor and the emitter of said second transistor to said network terminal.

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2. The invention of claim 1 wherein said switch means comprises a third transistor, the emitter of which is connected to the collector of said second transistor, the collector of which is connected to the first current supply terminal and the base of which is adapted to receive switching signals, and said diode means is connected to conduct current from said second current supply terminal to the collector of said second transistor.

3. The invention of claim 1 in which said first and second transistors are NPN transistors.

4. The invention of claim 1 further including second constant current source means coupled to said network terminal.

5. The invention of claim 2 wherein said first, second

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and third transistors are NPN transistors and further including second constant current source means coupled to said network terminal to draw current therefrom, and said diode means comprises a diode with the anode thereof connected to said second current supply terminal and with the cathode thereof connected to the collector of said second transistor and the emitter of said third transistor.

6. The invention of claim 5 wherein the Beta of said first and second transistors is of the order of 100 and the current of said first constant current source means is small relative to the current of said second constant current source means.

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