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(54) Title of the invention : DIRECT METALLIZATION PROCESS FOR REALIZATION OF HIGH POWER MICROWAVE INTEGRATED CIRCUITS CONTAINING HIGH CURRENT CARRYING THICK COPPER TRACES ON ALUMINA SUBSTRATE FOR GROUND AND SPACE APPLICATIONS

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(57) Abstract :
The present invention relates to a direct method for realization of High Power Microwave Integrated Circuits, containing high current carrying thick copper traces, using photosensitive thick dry film, on seed layer metallized alumina Al2 O3 substrate. The process includes electro plating of copper on exposed pattern area; followed by electro-less nickel plating and gold electroplating. This method is also be used to realize high power MIC circuits on other hard substrates like AlN, BeO, SiC etc. with seed layer metallization. By this method minimum line feature of 100/100 micron line/gap having 50 micron thickness is achieved with very good edge finish and verticality. Fig. 1

No. of Pages : 14 No. of Claims : 12

WE CLAIM:

1. A method of fabricating microwave integrated circuits with high current carrying thick copper traces, comprising the steps of

- preparing a bare hard substrate (1) as Base material;
- forming at least two seed layers (2,3) on the Bare hard substrate (1) such that the layers are deposited on opposite sides of the substrate by sputtering;
- preparing a dry film mould (4) on the seed layer coated hard substrate by exposure and development process;
- plating a layer of copper(Cu) on the exposed parts of dry film mould (4) by electroplating to form a thick copper tracks(6);
- forming nickel phosphate(NiP) layer (7) on the upper surface of thick copper tracks(6) by Electroless Nickel phosphorus plating;
- forming a gold(Au) layer (8) by electroplating;
- removing thick dry film for Cr-Cu seed layer; and
- etching of Cr-Cu seed layer by chemical etchant.

2. The method as claimed in claim 1, wherein the bare hard substrate is alumina (Al_2O_3).

3. The method as claimed in claim 1, wherein the bare hard substrate is selected from substrates such as Silicon Carbide (SiC), Aluminum Nitride(AlN), Beryllium Oxide(BeO), etc.,

4. The method as claimed in claim 1, wherein the two seed layers comprises chromium as first adhesion layer and copper as second conducting layer.

5. The method as claimed in claim 1, wherein forming of a dry film mould comprising preparation of a photosensitive thick dry film (4) on the surface of sputtered seed layer substrate (3) by lamination.

6. The method as claimed in claim 1 and 5, wherein the formed thick dry film(4) is followed by preparing a photo mask(5), exposing the photo mask(5) on dry film(4).

7. The method as claimed in claim 4, wherein the first adhesion layer having thickness about 200-300 angstrom and second conducting layer having thickness about 2-3 micron.

8. The method as claimed in claim 1, wherein the copper traces (6) formed on metallized hard substrate have thickness range up to 50 microns

9. The method as claimed in claim 1, wherein the copper traces (6) formed on metallized hard substrate have adhesion strength of 370 Kg/Cm^2 or better

10. The method as claimed in claim 1, wherein the copper traces (6) formed on metallized hard substrate have current carrying capacity of 100 ampere per mm width.

11. The method as claimed in claim 1, wherein the copper traces (6) formed on metallized hard substrate have line/space tolerance 100 ±2 micron.

12. The method as claimed in claim 1, wherein the formed nickel phosphorus NiP film is about 1-3 micron and the formed gold film is about 2-3 micron.

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FORM 2

THE PATENTS ACT, 1970
(39 of 1970)
AND
THE PATENTS RULES, 2003

COMPLETE SPECIFICATION

(See section 10; rule 13)

TITLE OF THE INVENTION

"DIRECT METALLIZATION PROCESS FOR REALIZATION OF HIGH POWER MICROWAVE INTEGRATED CIRCUITS CONTAINING HIGH CURRENT CARRYING THICK COPPER TRACES ON ALUMINA SUBSTRATE FOR GROUND AND SPACE APPLICATIONS"

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The following specification particularly describes
the invention and the manner
in which it is to be performed

Title : Direct metallization process for realization of High Power Microwave Integrated Circuits containing high current carrying thick Copper traces on Alumina substrate for ground and Space applications

Filed of Invention:

The present invention relates to the field of High power Microwave Integrated Circuits in satellite communication and related applications. The present invention specially relates to the direct method for realization of thick high power bias lines in devices like high power Solid State Power Amplifies (SSPA).

Background of Invention:

High power and high current devices realized by thin copper conductive tracks require wide conductive tracks with increase lengths for thermal management. It increases the circuit area which hinders the miniaturization of circuit size. It can be avoided by using thick copper conductive tracks.

Direct Bonded Copper (DBC) is one of the methods to achieve the thick copper conductive tracks (1). But, it requires precise control of oxygen partial pressure and temperature in the firing process in order to form proper CuO_2 phase at the interface of Copper foil and the ceramic interface and also limited line resolution for miniaturization (2). Pattern plating method for fabrication of thick copper tracks using screen printed seed layer had poor adhesion strength due to weak bonding between seed layer and substrate (3, 4). Pattern plating method used in fabrication of thick copper tracks on hard substrate, were electroplated nickel was used as diffusion barrier layer had poor barrier properties. This is due to crystalline nature of barrier layer which provided the diffusion paths for copper to reach surface through gold (5).

Object of the present invention:

The objective of the present invention is to develop a direct method to fabricate microwave integrated circuit useful for high power and high current

applications having thick copper conductive traces on alumina substrate with good adhesion strength and diffusion barrier layer.

Summary of the invention:

In accordance with the present invention, the method of fabricating high power Microwave Integrated Circuits comprises solvent cleaning of alumina substrate, sputtering Chromium / Copper seed layer on alumina substrate, laminating photosensitive thick dry film on sputter layered alumina substrate, forming the required dry film mould on the substrate which consists of exposure and development, Micro etching in the copper exposed areas, electroplating of copper followed by electro-less plating of nickel phosphate (NiP) and electroplating of gold in the dry film mould, removing dry film mould, etching of the Chromium/Copper seed layer. The comparison of the present developed method is compared with DBC is shown in table 1.

Table 1

Comparison of this process with other available process

Sr. No.	Attribute	Our process DPC (Direct Plated Copper)	DBC (Direct Bonded Copper)
1	Conductor	Pure Copper	Pure Copper
2	Copper Thickness Range	Up to 50 micron	100-400 micron
3	Line/Space Tolerance	100 micron	250 micron
4	CTE stress at room temperature	Minimal	High (zero stress state near 1100°C)
5	Current Handling	Commensurate with Cu thickness	Commensurate with Cu thickness

6	Bonding Layer	Thin film adhesion layer	Brittle ternary metal oxide
7	Adhesion strength	370 Kg/ Cm^2 or better	340 Kg/ Cm^2 or better
8	Via Formation	Via filled and surface conductor deposited at same time	Separate operation for via filling
9	Green (environment pollution)	Better due to much less Cu waste	Ordinary

As per the invention, a process for fabrication of thick copper traces on alumina substrates along with suitable RF traces for High Power Microwave Integrated Circuit applications is developed and effectively utilized for realization of circuits demanding high current/high power capacity. This high reliable process is suitable for space, air borne and ground based hardware. It comprises the step of forming a mould using photosensitive thick dry film onto sputter coated hard substrate ensures utilization of full substrate area by eliminating edge build-up. The process as per the invention yields thick copper metallization upto 50 micron on hard substrate for high current carrying capacity traces. The process can be utilized to grow higher thickness upto 75 micron using same recipe and specifications. Further, the process can be utilized irrespective of shape and size of the substrate.

Also in accordance with the present invention, this process can be performed on all other seed layer metallized hard substrates including SiC, AlN, BeO using same process recipe and specifications. Apart from Cr-Cu seed layer, other seed layers like TiW-Cu, NiCr-Cu etc. can be used for circuit realization; using the same process recipe and specifications.

Brief description of the drawing:

Fig.1 is the flow chart of the method in accordance with the present invention. Figs. 2-9 are cross sectional views of the substrate in the different steps of fabrication process.

Fig 2: shows alumina substrate.

Fig 3: shows Cr/Cu Seed layer sputter deposited alumina substrate.

Fig 4: shows Cr/Cu Seed layer sputter deposited alumina substrate with laminated dry film.

Fig 5: shows Cr/Cu Seed layer sputter deposited alumina substrate with laminated dry film exposure to UV radiation.

Fig 6: shows Cr/Cu Seed layer sputter deposited alumina substrate with laminated dry film after exposure and development of pattern.

Fig 7: shows Cr/Cu Seed layer sputter deposited alumina substrate with patterned dry film after deposition of Cu/NIP/Au pattern.

Fig 8: shows Cr/Cu Seed layer sputter deposited alumina substrate with Cu/NIP/Au pattern after dry film removal.

Fig 9: shows Cr/Cu Seed layer sputter deposited alumina substrate with electroplated Cu/NIP/Au pattern after seed layer etching.

Detailed description of the preferred embodiment:

With reference to Fig.1, the method in accordance with the present invention for alumina substrate comprises the steps of preparing the alumina substrate for seed layer sputtering by solvent cleaning; sputtering the Chromium and Copper separately on the opposite sides of the substrate so that it is covered with copper layer and chromium layer. Laminating of the photosensitive dry film on to the substrate; forming the required dry film mould on the substrate which consists of exposure and development; Micro etching in the copper exposed areas such that it provides active surface for plating; Electroplating of the copper in the exposed areas of the dry film followed by electro-less plating of nickel phosphate (NiP) and electroplating of gold; Removing the dry film mould; etching

of the Chromium/Copper seed layer under the unexposed area of the dry film before plating.

With reference to Fig.2 to 9 and Fig. 1 as the reference, alumina substrate (1) is cleaned by solvent cleaning. In the chrome/copper sputtering step as shown in the fig.3, a chromium adhesion layer (2) and copper seed layer (3) are respectively and orderly deposited on the surface of the alumina substrate (1) by sputtering technology. Thickness of the chromium adhesion layer (2) is 200-300 angstroms and the copper seed layer (3) thickness is 2 to 3 microns. The Chromium (2) and Copper (3) seed layers are useful to electroplating of copper on alumina substrate (1).

In the photosensitive thick dry film (4) lamination step as shown in the fig.4, dry film is laminated on the seed layer copper surface (3). The dry film (4) is a polymeric resin, which will react with itself when exposed to ultra violet radiation (9) in order to protect the seed layer copper (3) under the dry film (4).

Dry film mould formation step consists of exposure and development processes. Fig. 5 shows the exposure process. According to circuit, a photo mask (5) is made. The photo mask (5) is flatly positioned and adhered to the dry film (4) of the alumina substrate (1). Then the alumina substrate (1) with photo mask (5) is sent into the exposure chamber. After creating a vacuum in the exposure chamber ultra violet radiation (9) irradiate the dry film (4) through photo mask (5). The dry film (4), which is irradiated by the ultra violet radiation (9) through photo mask (5), is polymerized by the ultraviolet radiation (9) and the dry film (4) which is not irradiated by the ultraviolet radiation (9), does not react and keep its chemical composition.

The development process etches the polymerized part of the dry film (4) by chemical cleaning. In this way, some parts of the seed layer copper (3) are exposed from the dry film (4), and those parts of the seed layer copper (3) forms the required circuit in order to form the thick copper tracks (6) of the circuit on the

alumina substrate. In this way dry film (4) mould can be formed on the alumina substrate (1) as shown in the Fig.6.

Fig. 7 shows the plating process of copper (6), Nickel phosphate (NiP) (7) and gold (8). Copper is applied to fill the exposed parts of the dry film (4) mould on the alumina substrate (1) with suitable width and thickness by electroplating technology to form the thick copper tracks (6). Electro-less NiP (7) and electroplated gold (8) are deposited on the upper surface of the thick copper tracks (6) to form the amorphous Nickel Phosphate (NiP) (7) film and gold film (8). The NiP film (7) prevents the atoms of the thick copper tracks (6) diffusing into the gold (8) and vice versa. The gold film (8) improves the performance of the circuit under high frequency environment. Gold film (8) also protects the thick copper tracks (6) from the aggressive corrosive environment. By the above process, the thick copper (6) tracks with NiP (7) and gold (8) films are near vertical, flat and smooth characteristics. Then the remaining dry film (4) on the alumina substrate (1) is removed.

Fig.8 shows the copper (6) tracks with NiP (7) and gold (8) films after removing the dry film (4). The etching process of Chromium/Copper seed layer etches the Chromium (2) and copper (3) seed layers. Fig.9 shows Cr/Cu seed layer sputter deposited alumina substrate with electroplated Cu/NiP/Au pattern after seed layer etching.

The invention has following advantages:

1) Saving of precious metal content in rest of the pattern area.
2) Can be integrated with low thickness RF traces.
3) Reduce production cost by eliminating blanket metallization.
4) 100% area of alumina substrate can be printed without sparing any peripheral area due to edge build-up problems.
5) High conductivity of micro strip traces (SR Value: 0.0003 Ω/□).
6) More accurate line dimensions (Inaccuracy less than 5% of line width).

7) Excellent Edge finish (Better than 1 micron).
8) No overhang or undercut problems due to 87 ° conductor verticality with reference to substrate surface.

Major process specifications

1) Bare alumina substrate: 99.6% pure, 25 or 10 mil thick, as fired 1" X 1"or 2" X 2" size
2) Seed layer metallization: Cr:200-300 angstrom, Cu: 2-3 micron by RF/Magnetron sputtering technique
3) Photosensitive thick Dry film: Thickness as required
4) Developing: alkaline developer
5) Copper electro plating: Acid copper bath with two power supplies to get uniformity on pattern as well as on ground surface
6) Electroless nickel plating: Electro less nickel plating solution
7) Gold electro plating: Compatible solution
8) Tolerance on over all metallization thickness: ± 4 micron
9) Seed layer etching: Two different etchants for Cu and Cr

Product Specifications

1) Grain size : 200-300 nm
2) Conductor edge verticality : 87 ° or better
3) Surface roughness : 200 nm or better
4) Current carrying capacity : 100 Amp. per mm width
5) Thickness: Cr : 200-300 angstrom
   Copper : 45-46 micron
   Electroless nickel : 1-3 micron
   Gold : 2-3 micron

Test report

Sr. No	Name of test	Test requirement as per ISRO-PAX-305	Achieved Specifications
1	Adhesion test	73 Kg/ cm^2	395.28 Kg/ cm^2
2	Bake in air test	300° C 30 minutes	No discolouration and blistering or peeling observed
3	Current carrying capacity	0.00066 A/ sq. micron	0.00133 A/sq. micron
4	Line dimension measurement	100 micron ± 10% (line & gap)	100 ±2 micron (line & gap)
5	Thickness test	50 micron	50 ±2 micron

The invention described so far is a specific embodiment of the present invention in connection with reference to the drawings which is a practical achievement, but it is to be understood that the intention is not limited to the invention with the particular embodiments described herein. But on the other hand, the intention is to cover various modifications, equivalents, and alternative arrangement falling within the scope of the invention as defined by the appended claims.

WE CLAIM:

1. A method of fabricating microwave integrated circuits with high current carrying thick copper traces, comprising the steps of

- preparing a bare hard substrate (1) as Base material;
- forming at least two seed layers (2,3) on the Bare hard substrate (1) such that the layers are deposited on opposite sides of the substrate by sputtering;
- preparing a dry film mould (4) on the seed layer coated hard substrate by exposure and development process;
- plating a layer of copper(Cu) on the exposed parts of dry film mould (4) by electroplating to form a thick copper tracks(6);
- forming nickel phosphate(NiP) layer (7) on the upper surface of thick copper tracks(6) by Electroless Nickel phosphorus plating;
- forming a gold(Au) layer (8) by electroplating;
- removing thick dry film for Cr-Cu seed layer; and
- etching of Cr-Cu seed layer by chemical etchant.

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3. The method as claimed in claim 1, wherein the bare hard substrate is selected from substrates such as Silicon Carbide (SiC), Aluminum Nitride(AlN), Beryllium Oxide(BeO), etc.,

4. The method as claimed in claim 1, wherein the two seed layers comprises chromium as first adhesion layer and copper as second conducting layer.

5. The method as claimed in claim 1, wherein forming of a dry film mould comprising preparation of a photosensitive thick dry film (4) on the surface of sputtered seed layer substrate (3) by lamination.

6. The method as claimed in claim 1 and 5, wherein the formed thick dry film(4) is followed by preparing a photo mask(5), exposing the photo mask(5) on dry film(4).

7. The method as claimed in claim 4, wherein the first adhesion layer having thickness about 200-300 angstrom and second conducting layer having thickness about 2-3 micron.

8. The method as claimed in claim 1, wherein the copper traces (6) formed on metallized hard substrate have thickness range up to 50 microns

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10. The method as claimed in claim 1, wherein the copper traces (6) formed on metallized hard substrate have current carrying capacity of 100 ampere per mm width.

11. The method as claimed in claim 1, wherein the copper traces (6) formed on metallized hard substrate have line/space tolerance 100 ±2 micron.

12. The method as claimed in claim 1, wherein the formed nickel phosphorus NiP film is about 1-3 micron and the formed gold film is about 2-3 micron.

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Abstract:

The present invention relates to a direct method for realization of High Power Microwave Integrated Circuits, containing high current carrying thick copper traces, using photosensitive thick dry film, on seed layer metallized alumina Al_2O_3 substrate. The process includes electro plating of copper on exposed pattern area; followed by electro-less nickel plating and gold electroplating. This method is also be used to realize high power MIC circuits on other hard substrates like AlN, BeO, SiC etc. with seed layer metallization. By this method minimum line feature of 100/100 micron line/gap having 50 micron thickness is achieved with very good edge finish and verticality.

Fig. 1

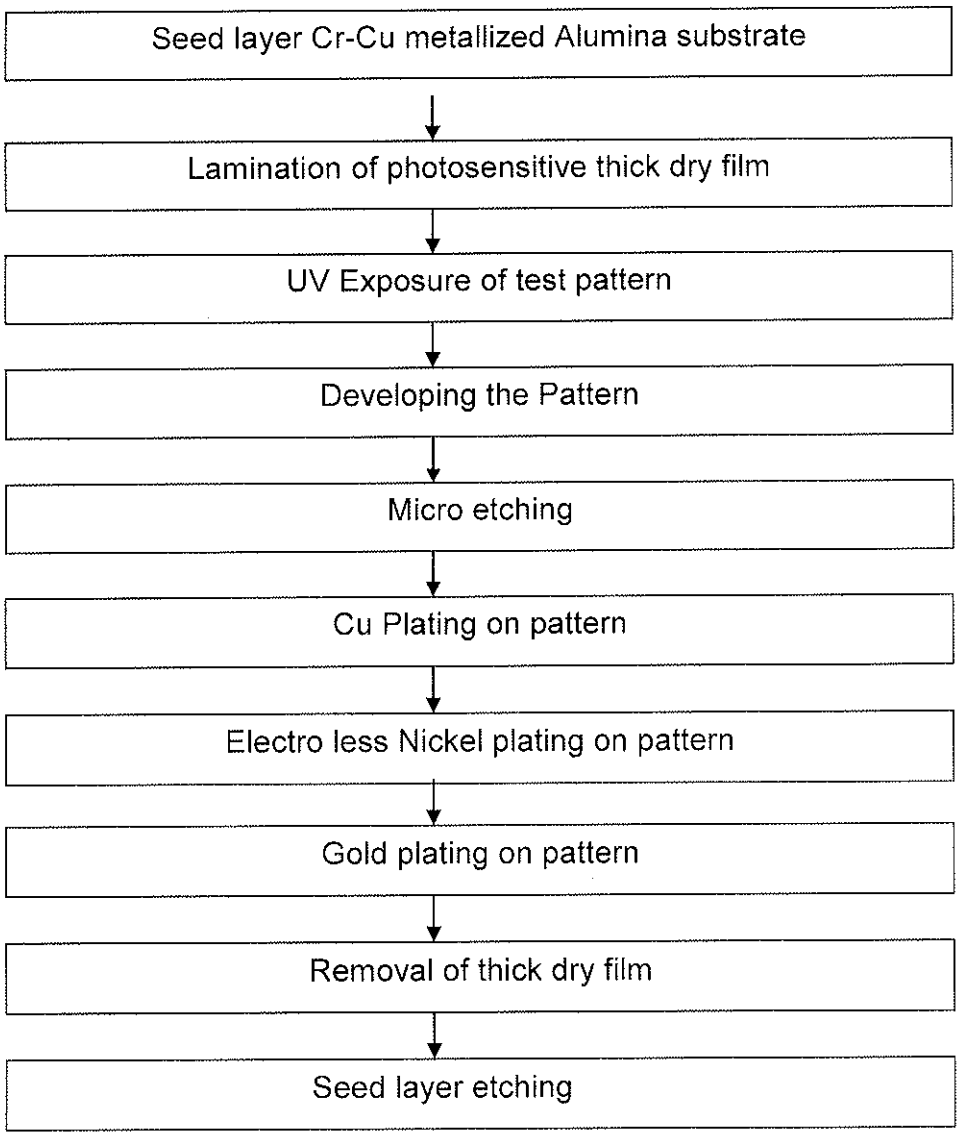

Seed layer Cr-Cu metallized Alumina substrate
Lamination of photosensitive thick dry film
UV Exposure of test pattern
Developing the Pattern
Micro etching
Cu Plating on pattern
Electro less Nickel plating on pattern
Gold plating on pattern
Removal of thick dry film
Seed layer etching

Fig.1

Fig 2

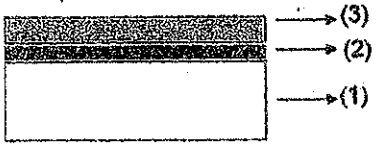


Fig : 3

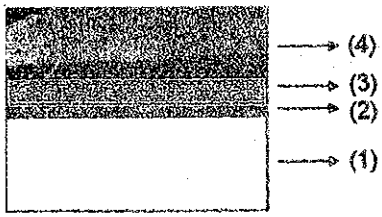


Fig 4

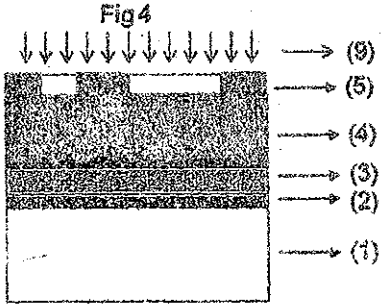


Fig 5

Fig 6

(1) Alumina substrate
(2) Cr seed layer
(3) Cu Seed layer
(4) Dry film
(5) Photo mask
(6) Electroplated Cu layer
(7) Electro-less NiP layer
(8) Electroplated gold layer
(9) U V radiation

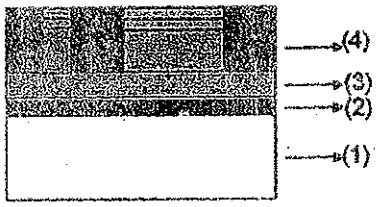
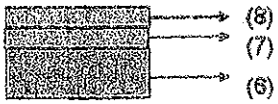


Fig 7



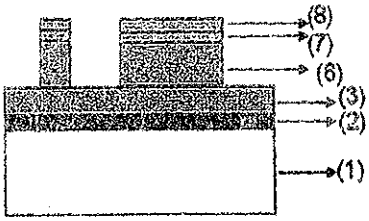


Fig 8

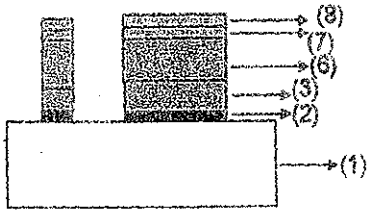


Fig 9