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ning of each regular issue of the PCT Gazette.

(54) Title: TRANSISTOR WITH INDEPENDANT GATE STRUCTURES

(57) Abstract: A method of making a transistor with independent gate structures (701, 703). The gate structures are each adjacent to sidewalls of a semiconductor structure (105). The method includes depositing at least one conformal layer that includes a layer of gate material (203) over a semiconductor structure that includes the channel region. A planar layer (403) is formed over the wafer. The planar layer has a top surface below the top surface of the at least one conformal layer at a location over the substrate. The at least one conformal layers are etched to remove the gate material over the semiconductor structure.



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INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H01L 21/302, 21/304

US CL : 438/396, 397, 706, 710, 714, 720

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 438/396, 397, 706, 710, 714, 720

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6,531,350 B2 (SATO et al) 11 March 2003, see col. 7, lines 25-30, col. 8, lines 9-50, col. 9, lines 16-17.	1-5, 7-11, 13-14, 16-19, 20-25, 27-31
Y	US 6,768,158 B2 (LEE et al) 27 July 2004, see col. 3, lines 30-31, col. 4, lines 15-20, col. 6, lines 28-36.	33
Y	US 6,689,650 B2 (GAMBINO et al) 20 February 2004, see col. 4, lines 47-52.	15
Y	US 6,846, 734 B2 (AMOS et al) 25 January 2005, see col. 6, lines 16-21.	6, 26



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