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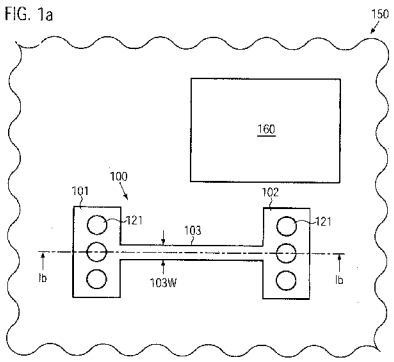
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(54) **Title**: SEMICONDUCTOR DEVICE COMPRISING EFUSES OF ENHANCED PROGRAMMING EFFICIENCY

FIG. 1a



(57) **Abstract**: In sophisticated integrated circuits, an electronic fuse (200) may be formed such that an increased sensitivity to electromigration may be accomplished by including at least one region of increased current density. This may be accomplished by forming a corresponding fuse region (203) as a non-linear configuration, wherein at corresponding connection portions of linear segments, the desired enhanced current crowding may occur during the application of the programming voltage. Hence, increased reliability and more space- efficient layout of the electronic fuses may be accomplished.

WO 2010/062360 A1

SEMICONDUCTOR DEVICE COMPRISING eFUSES OF ENHANCED PROGRAMMING EFFICIENCY

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present disclosure generally relates to the field of fabricating integrated circuits, and, more particularly, to forming electronic fuses for providing device-internal programming capabilities in complex integrated circuits.

2. DESCRIPTION OF THE RELATED ART

In modern integrated circuits, a very high number of individual circuit elements, such as field effect transistors in the form of CMOS, NMOS, PMOS elements, resistors, capacitors and the like are formed on a single chip area. Typically, feature sizes of these circuit elements are steadily decreasing with the introduction of every new circuit generation to provide currently available integrated circuits with an improved degree of performance in terms of speed and/or power consumption. A reduction in size of transistors is an important aspect in steadily improving device performance of complex integrated circuits, such as CPUs. The reduction in size is commonly associated with an increased switching speed, thereby enhancing signal processing performance. In addition to the large number of transistor elements, a plurality of passive circuit elements, such as capacitors, resistors and the like, are typically formed in integrated circuits that are used for a plurality of purposes, such as for decoupling.

Due to the decreased dimensions of circuit elements, not only the performance of the individual transistor elements may be increased, but also their packing density may be improved, thereby providing the potential for incorporating increased functionality into a given chip area. For this reason, highly complex circuits have been developed, which may include different types of circuits, such as analog circuits, digital circuits and the like, thereby providing entire systems on a single chip (SoC). Furthermore, in sophisticated microcontroller devices, an increasing amount of storage capacity may be provided on chip with the CPU core, thereby also significantly enhancing the overall performance of modern computer devices.

In modern integrated circuits, minimal features sizes have now reached approximately 50 nm and less, thereby providing the possibility of incorporating various functional circuit portions at a given chip area, wherein, however, the various circuit portions may have a significantly different performance, for instance with respect to lifetime, reliability and the like. For example, the operating speed of a digital circuit portion, such as a CPU core and the like, may depend on the configuration of the individual transistor elements and also on the characteristics of the metallization system, which may include a plurality of stacked metallization layers so as to comply with a required complex circuit layout. Thus, highly sophisticated manufacturing techniques may be required in order to provide the minimum critical feature sizes of the speed-critical circuit components. For example, sophisticated digital circuitry may be used on the basis of field effect transistors which represent circuit components in which conductivity of a channel region is controlled on the basis of a gate electrode that is separated from the channel region by a thin dielectric material. Performance of the individual field effect transistors is determined, among other things, by the capability of the transistor to switch from a high impedance state into a low impedance state at high speeds, wherein, also, a sufficiently high current may be driven in the low impedance state. This drive current capability is determined, among other things, by the length of the conductive channel that forms in the channel region upon application of an appropriate control voltage to the gate electrode. For this reason, and in view of ever increasing the overall packing density of sophisticated semiconductor devices, the channel length and thus the length of the gate electrode is continuously being reduced, which in turn may require an appropriate adaptation of the capacitive coupling of the gate electrode to the channel region. Consequently, the thickness of the gate dielectric material may also have to be reduced in order to maintain controllability of the conductive channel at a desired high level. However, the shrinkage of the gate dielectric thickness may be associated with an exponential increase of the leakage currents, which may directly channel through the thin gate dielectric material, thereby contributing to enhanced power consumption and thus waste heat, which may contribute to sophisticated conditions during operation of the semiconductor device. Moreover, charge carriers may be injected into the gate dielectric material and may also contribute to a significant degradation of transistor characteristics, such as threshold voltage of the transistors, thereby also contributing to variability of the transistor characteristics over the lifetime of the product. Consequently, reliability and performance of certain sophisticated circuit portions may be determined by material characteristics and process techniques for forming highly sophisticated circuit elements, while other circuit portions may include less

critical devices which may thus provide a different behavior over the lifetime compared to critical circuit portions. Consequently, the combination of the various circuit portions in a single semiconductor device may result in a significant different behavior with respect to performance and reliability, wherein the variations of the overall manufacturing process flow may also contribute to a further discrepancy between the various circuit portions. For these reasons, for complex integrated circuits, frequently additional mechanisms may be implemented to allow the circuit itself to adapt performance of certain circuit portions to comply with performance of other circuit portions, for instance after completing the manufacturing process and/or during use of the semiconductor device, for instance when certain critical circuit portions may no longer comply with corresponding performance criteria, thereby requiring an adaptation of certain circuit portions, such as re-adjusting an internal voltage supply, resetting overall circuit speed and the like.

For this purpose, so-called electronic fuses or e-fuses may be provided in the semiconductor devices, which may represent electronic switches that may be activated once in order to provide a desired circuit adaptation. Hence the electronic fuses may be considered as having a high impedance state, which may typically also represent a "programmed" state, and may have a low impedance state, typically representing a non-programmed state of the electronic fuse. Since these electronic fuses may have a significant influence on the overall behavior of the entire integrated circuit, a reliable detection of the non-programmed and the programmed state may have to be guaranteed, which may have to be accomplished on the basis of appropriately designed logic circuitry. Furthermore, since typically these electronic fuses may be actuated once over the lifetime of the semiconductor device under consideration, a corresponding programming activity may have to ensure that a desired programmed state of the electronic fuse is reliably generated in order to provide well-defined conditions for the further operational lifetime of the device. However, with the continuous shrinkage of critical device dimensions in sophisticated semiconductor devices, the reliability of programming corresponding electronic fuses may require tightly set margins for the corresponding voltages used to program the electronic fuses, which may not be compatible with the overall specifications of the semiconductor devices or may at least have a severe influence on the flexibility of operating the device.

With reference to Figures 1a-1b, a typical electronic fuse in a sophisticated semiconductor device will now be described in order to more clearly set forth the difficulties in providing electronic fuses in advanced semiconductor devices.

Figure 1a schematically illustrates a top view of a portion of a semiconductor device 150 which may represent any semiconductor device including sophisticated digital circuitry, such as a CPU core, a controller for graphic applications, memory areas and the like. The semiconductor device 150 may thus comprise a circuit portion 160, which may represent a sophisticated transistor element, such as a field effect transistor having a gate length of 50 nm and less, as previously discussed. Furthermore, the device 150 comprises an electronic fuse 100 that may represent a one-time programmable electronic switch, which may be converted from a low impedance state into a high impedance state upon a current pulse generated by applying an appropriate programming voltage to the electronic fuse 100. As illustrated, the fuse 100 comprises a first contact area 101 and a second contact area 102 and an intermediate region 103, provided in the form of a conductive line, which represents the actual fuse element which may alter its impedance state upon connecting the contact areas 101 and 102 with an appropriate voltage source. Typically, the contact areas 101, 102 and the conductive line 103 are formed of an appropriate electrode material, which may also be used for forming corresponding gate electrode structures of field effect transistors, such as is provided in the portion 160. For example, polysilicon in combination with a metal silicide are frequently used materials for forming the electronic fuse 100. Moreover, as illustrated, each of the contact areas 101, 102 may be connected to corresponding contact elements that are formed in a contact level of the device 150, as will be described in more detail with reference to Figure 1b.

Figure 1b schematically illustrates a cross-sectional view of the device 150 along the line Ib of Figure 1a. As illustrated, the device 150 comprises a substrate 151, such as a silicon substrate and the like, above which is formed a layer 152, which may represent a semiconductor layer or an insulating material, depending on the position of the electronic fuse 100 within the semiconductor device 150. Furthermore, when the material 152 represents a semiconductor region, an insulating material 153 may be provided, for instance on the basis of a material as may also be used as a gate dielectric material for forming field effect transistors. Moreover, a contact level 120 is formed above the layer 152 so as to enclose the electronic fuse 100 and other circuit elements, such as transistors and the like. Typically, the

contact level comprises a dielectric material 122 in combination with an etch stop material 123, such as silicon dioxide and silicon nitride, respectively, in which are formed the contact elements 121 that usually comprise a conductive material such as tungsten, possibly in combination with a conductive barrier material (not shown), such as titanium nitride and the like.

The semiconductor device 150 may be formed on the basis of well-established process techniques in which sophisticated circuit elements such as gate electrodes of field effect transistors and the like may be formed on the basis of critical dimensions of 50 nm and less. For this purpose, an appropriate gate electrode material in combination with a gate dielectric material may be provided and may be patterned on the basis of sophisticated lithography and etch techniques, wherein the contact areas 101, 102 and the region 103 may also be patterned. For example, the conductive line 103 may have a similar geometric configuration compared to gate electrode structures. That is, a width 103W (Figure 1a) may correspond to the gate length of critical transistor elements, while a length 103L may be several hundred nanometers, depending on the overall configuration. It should be appreciated that, similarly as is the case for transistor elements, the electronic fuse 100 is also to be designed in view of not unduly consuming valuable die area in the device 150. Furthermore, in view of programmability of the fuse 100, that is, of the region 103, it is preferable to provide a minimum cross-sectional area so as to allow a significant modification of the electrical behavior of the region 103 upon applying a sufficiently high current flowing through the region 103. Consequently, the region 103 may be designed in accordance with the corresponding design rules for the device under consideration.

In a further advanced manufacturing stage, that is, patterning the gate electrode structures and thus the contact areas 101, 102 and the region 103, and after forming appropriate drain and source areas for transistor elements, typically the conductivity of semiconductor regions may be increased, for instance by forming a metal silicide in corresponding drain and source areas and gate electrodes, thereby also forming a metal silicide 104 in the contact areas 101, 102 and the region 103. This may be accomplished on the basis of well-established process techniques. It should be appreciated that, during the corresponding manufacturing process, respective sidewalls spacers 105 may also have been formed, which may typically be used for defining corresponding dopant profiles in transistor areas and act as a mask during the silicidation process. Thereafter, the contact level 120 may be formed on

the basis of well-established process techniques including the deposition of the materials 123 and 122 and patterning the same in order to obtain appropriate contact openings, which are subsequently filled with conductive material, such as tungsten and the like. Next, a plurality of metallization layers (not shown) are formed, which may provide the wiring fabric for the circuit elements and also for the electronic fuse 100 in accordance with the overall circuit layout.

When operating the device 150 and programming the electronic fuse 100, a sufficiently high voltage is to be applied between the contact areas 101 and 102 in order to generate a sufficient high current density, which may result in a permanent modification in order to blow the fuse 100. For example, in this case, the per se negative effect of electromigration may be efficiently used to induce a current-driven material diffusion in the line 103, which may result in a significant modification of the electrical performance, *i.e.*, a corresponding high impedance state may be achieved due to the "degradation" of the line 103. Electromigration is a well-known effect which may occur in conductive lines, typically metal-containing lines, when current density is very high so that the flow of electrons may cause a directed "diffusion" of ion cores, thereby increasingly transporting material along the electron flow direction. Thus, the corresponding line may increasingly suffer from a depletion of material in the vicinity of the cathode, while material may be deposited at or next to the line in the vicinity of the anode of the fuse 100. As previously discussed, a reliable distinction between a non-programmed state and a programmed state may require a corresponding significant modification of line 103, which may require significant voltages and may also require appropriately designed contact areas 101, 102 and an appropriate number of contact elements 121 connecting thereto in order to provide the required current drive capability for effecting a "blowing" of line 103. Thus, an appropriate tightly set "programming voltage window" may be required for sophisticated devices in order to obtain a high difference between the low impedance state and the high impedance state. Moreover, the corresponding margins for the programming voltage may also have to take account of any process-related fluctuations during the formation of the fuse 100, thereby requiring more tightly set programming voltages. As previously discussed, a corresponding required degree of reliability in detecting the programmed state may require sufficiently high programming voltages, which may not be compatible with the supply voltages used for sophisticated devices.

The present disclosure is directed to various methods and devices that may avoid, or at least reduce, the effects of one or more of the problems identified above.

SUMMARY OF THE INVENTION

The following presents a simplified summary of the invention in order to provide a basic understanding of some aspects of the invention. This summary is not an exhaustive overview of the invention. It is not intended to identify key or critical elements of the invention or to delineate the scope of the invention. Its sole purpose is to present some concepts in a simplified form as a prelude to the more detailed description that is discussed later.

Generally, the present disclosure relates to semiconductor devices and methods for forming the same in which electronic fuses for advanced semiconductor devices may be provided so as to exhibit an increased tolerance with respect to programming voltages, while nevertheless providing a reliable programmed state. For this purpose, the electronic fuses may receive at least one portion that is designed to generate an increased current density when programming the electronic fuse so that an increased electromigration effect may be obtained in the corresponding portion. Consequently, a significant modification of the electric conductivity may be achieved at a reduced current density, thereby enabling the usage of lower voltages and also providing the possibility of generally reducing the size of corresponding contact areas and thus the size and/or the number of corresponding contact elements connected thereto, which in turn results in an overall reduced size of the electronic fuses.

One illustrative method disclosed herein relates to the forming of an electronic fuse of an integrated circuit. The method comprises forming an electrode material above an insulating material formed above a substrate of the integrated circuit. Furthermore, the method comprises forming a first contact area, a second contact area and a fuse region of the electronic fuse from the electrode material, wherein the fuse region connects to the first and second contact areas and comprises at least one non-linear portion for generating a zone of increased current density. Furthermore, the method comprises forming contact elements in a contact level of the integrated circuit, wherein the contact elements connect to the first and second contact areas of the electronic fuse.

A still further illustrative method disclosed herein relates to the designing of an electronic fuse of a semiconductor device. The method comprises providing a first contact area and a second contact area of the electronic fuse and use a plurality of linear portions of a fuse region. The method further comprises combining the plurality of linear portions to form at least one connection region having a non-linear configuration to define a zone of increased current density.

One illustrative semiconductor device disclosed herein comprises a plurality of circuit elements formed in and above a semiconductor layer. Moreover, the semiconductor device comprises an electronic fuse formed on an insulating material, wherein the electronic fuse comprises a first contact area, a second contact area and a fuse region including at least one non-linear portion that defines a zone of increased current density. Moreover, the semiconductor device comprises a contact level formed above the semiconductor layer and comprising a plurality of contact elements connecting to the plurality of circuit elements and to the first and second contact areas of the electronic fuse. Additionally, the device comprises a metallization system formed above the contact level.

BRIEF DESCRIPTION OF THE DRAWINGS

The disclosure may be understood by reference to the following description taken in conjunction with the accompanying drawings, in which like reference numerals identify like elements, and in which:

Figure 1a schematically illustrates a top view of a conventional semiconductor device including an electronic fuse;

Figure 1b schematically illustrates a cross-sectional view of the electronic fuse of the conventional device as shown in Figure 1a;

Figures 2a-2b schematically illustrate top views of a portion of a semiconductor device including a circuit portion and an electronic fuse having a zone of increased current density, according to illustrative embodiments;

Figures 2c-2f schematically illustrate top views of respective layouts or actual electronic fuses including a chain configuration, in which a plurality of linear fuse regions are connected in series so as to obtain two or more zones of increased current density, according to further illustrative embodiments;

Figure 2g schematically illustrates a layout or an actual electronic fuse including three zones of increased current density obtained on the basis of a chain-like configuration;

Figures 2i-2l schematically illustrate top views of a layout or an actual implementation of an electronic fuse including a fuse region comprised of a "u-like" configuration according to still further illustrative embodiments;

Figure 2m schematically illustrates a top view of a layout or an actual implementation of an electronic fuse in which the fuse region may comprise a plurality of "u-turns," according to still further illustrative embodiments; and

Figure 2n schematically illustrates a cross-sectional view of a semiconductor device including an electronic fuse, according to illustrative embodiments.

While the subject matter disclosed herein is susceptible to various modifications and alternative forms, specific embodiments thereof have been shown by way of example in the drawings and are herein described in detail. It should be understood, however, that the description herein of specific embodiments is not intended to limit the invention to the particular forms disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

DETAILED DESCRIPTION

Various illustrative embodiments of the invention are described below. In the interest of clarity, not all features of an actual implementation are described in this specification. It will of course be appreciated that in the development of any such actual embodiment, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which will vary from one implementation to another. Moreover, it will be appreciated that

such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking for those of ordinary skill in the art having the benefit of this disclosure.

The present subject matter will now be described with reference to the attached figures. Various structures, systems and devices are schematically depicted in the drawings for purposes of explanation only and so as to not obscure the present disclosure with details that are well known to those skilled in the art. Nevertheless, the attached drawings are included to describe and explain illustrative examples of the present disclosure. The words and phrases used herein should be understood and interpreted to have a meaning consistent with the understanding of those words and phrases by those skilled in the relevant art. No special definition of a term or phrase, *i.e.*, a definition that is different from the ordinary and customary meaning as understood by those skilled in the art, is intended to be implied by consistent usage of the term or phrase herein. To the extent that a term or phrase is intended to have a special meaning, *i.e.*, a meaning other than that understood by skilled artisans, such a special definition will be expressly set forth in the specification in a definitional manner that directly and unequivocally provides the special definition for the term or phrase.

Generally, the present disclosure provides semiconductor devices, layouts and manufacturing techniques in which an electronic fuse may be provided with enhanced reliability even for highly critical dimensions, such as a width of the fuse region of approximately 50 nm and less, while at the same time providing the possibility of reducing the overall size of the electronic fuse. For this purpose, one or more zones of increased current density may be provided in the actual fuse region, thereby locally increasing the electromigration effect in these zones, possibly in combination with a depletion of dopant species when doped semiconductor material in combination with metal species is used for forming the electronic fuse. In some illustrative embodiments, the zones of increased current density may be obtained by combining linear segments or portions having a specific critical width such that at least one connection region is provided that contributes to an increased current density during a programming event. For example, respective linear segments or portions may be connected so as to form an angle of approximately 90 degrees so that locally a certain degree of current crowding may be generated upon applying a programming pulse to the electronic fuse. Consequently, the current crowding and thus increased current density may result in an

increase of the local current density, which in turn may result in a more pronounced modification of the overall conductivity of the electronic fuse.

With reference to Figures 2a-2n, further illustrative embodiments will now be described in more detail, wherein reference may also be made to Figures 1a-1b, if appropriate.

Figure 2a schematically illustrates a top view of a semiconductor device 250, which may comprise a circuit portion 260 formed on the basis of a plurality of circuit elements, such as transistors 261, 262 and the like. It should be appreciated that the circuit portion 260 may represent any portion of a complex circuit, such as a digital circuit portion and the like, which may or may not be functionally connected to an electronic fuse 200. That is, as previously explained, for detecting a state of the electronic fuse 200 and also for programming the same at any appropriate point in time, corresponding circuitry may be required, for instance in the form of logic gates and the like, which may represent a part of the circuit portion 260. The electronic fuse 200 may comprise a first contact area 201 and a second contact area 202 and a fuse region 203, which may represent the region in which a change of conductivity may be generated on the basis of electromigration, dopant depletion and the like, as is also previously explained. The region 203 may comprise one or more portions or zones of increased current density when the electronic fuse 200 is activated on the basis of an appropriate programming voltage. In some illustrative embodiments, the fuse region 203 may comprise one or more non-linear portions, for instance represented by the corners 203C, which may be obtained by using a plurality of linear portions 203K, 203L, 203M, 203N that may be connected so as to define a "fork-like" configuration connecting to the contact area 202.

Figure 2b schematically illustrates a top view of the electronic fuse 200 according to further illustrative embodiments in which a single portion 203C may be provided on the basis of two linear portions 203K, 203L which may be connected to define the region 203C resulting in zone 203A of increased current density upon applying a programming voltage. Thus, the electrical performance of the electronic fuse 200 may be significantly different compared to the conventional electronic fuse 100 (Figures 1a and 1b) due to the provision of a non-linear configuration of the fuse region 203, which may thus include at least one portion 203C

resulting in a zone of increased current density 203A upon programming the electronic fuse 200.

The semiconductor device 250 may be formed on the basis of well-established process techniques, as are also described with reference to the semiconductor device 150, wherein, however, during the design phase of the device 250, the non-linear configuration of the fuse region 203 is taken into consideration. Thus, during the design of the electronic fuse 200, the enhanced efficiency of applying a programming pulse may also be taken into consideration by, for instance, reducing the lateral size of the first and second contact areas 201, 202 and by reducing the number and/or the size of corresponding contact elements connecting thereto, since a magnitude of the programming current required may be reduced, thereby offering the possibility of reducing the drive current capabilities of any conductive lines connecting to the electronic fuse 200. Hence, upon designing the semiconductor device 250, the electronic fuse 200 may be defined on the basis of corresponding critical dimensions for the technology under consideration, while each fuse 200 may consume less die area, thereby providing significant space-saving of the device 250 compared to the conventional device 150 for otherwise identical technology standards. Hence, during the manufacturing sequence for forming the device 250, the appropriate process techniques may be applied, as previously described, while the additional die area may be used for additional circuitry, test structures and the like.

Figures 2c-2f schematically illustrate top views of further designs or actual implementations of the electronic fuse 200 according to further illustrative embodiments.

Figure 2c schematically illustrates the electronic fuse 200 in which a "chain configuration," comprised of three linear portions 203K, 203L and 203M, is provided and is connected such that two portions 203C of increased current density are defined. That is, the linear portions 203K and 203L are connected so as to form an angle of approximately 90 degrees and also the portions 203L and 203M are combined so as to define an angle of approximately 90 degrees, however of opposite "direction" compared to the linear portions 203K, 203L. Furthermore, in the embodiment shown, the length of the linear portions 203K, 203M may be significantly greater compared to the length of the portion 203L, so that the corresponding portions 203C may be provided in close proximity to each other, thereby even further enhancing the overall current crowd effect, as indicated by arrow 206.

Figures 2d, 2e and 2f schematically illustrate various variations of the configuration as shown in Figure 2c, wherein, for instance, the length of the corresponding portions 203L is increased. For example, if a specific total length of the region 203 may be desired, while not unduly increasing the distance between the contact areas 201, 202, the individual length of the portions 203K, 203L, 203M may be appropriately selected in accordance with the design requirements while nevertheless providing two portions 203C providing the desired current crowding upon programming the electronic fuse 200.

Figure 2g schematically illustrates a top view of a layout or an actual implementation of the electronic fuse 200 in which three portions 203C of increased current density may be provided on the basis of a "chain configuration" for linear portions 203K, 203L, 203M, 203N. Also in this case, two connected linear portions are connected such that the corresponding connection region 203C defines an angle of approximately 90 degrees.

Figure 2h schematically illustrates a top view of the electronic fuse 200, in which three connection portions 203C may be provided at a laterally restricted area by using a "u-turn" configuration in the form of the linear portions 203L, 203M, 203N in combination with an additional angled configuration by connecting the linear portion 203K with the portion 203L according to a 90 degree angle. Thus, a high degree of flexibility in creating more than one connection portion 203C may be provided, wherein the position of the corresponding contact areas 201, 202 may also be selected with a high design flexibility, thereby also providing the possibility of appropriately taking advantage of the area saving obtained by the efficient non-linear configuration of the fuse region 203.

Figures 2j-2l schematically illustrate top views of layouts or actual implementations of the electronic fuse 200 according to further illustrative embodiments in which a basic configuration with respect to the contact areas 201, 202 and the fuse region 203 is provided, wherein, however, an additional "u-turn" is provided in the fuse region 203 in order to provide connection portions 203C to define corresponding zones of increased current density.

Figure 2j schematically illustrates the fuse region 203 with linear portions 203K, 203L that connect to a "u-turn" portion 203U, the "width" of which may be substantially determined by the length of a portion 203N. Consequently, due to the reduced length of the portion 203N in the u-turn 203U, the respective portions 203C of increased current density

formed in combination with the portions 203K, 203L may be positioned in close proximity to each other, thereby providing a high efficiency in obtaining an electromigration effect upon programming the fuse 200.

Figures 2k and 2l schematically illustrate the electronic fuse 200 according to illustrative embodiments in which the corresponding length of the portion 203N in the u-turn 203U may be increased, depending on the overall design criteria.

Figure 2m schematically illustrates a top view of the electronic fuse 200 according to a further illustrative embodiment in which a plurality of u-turns 203U may be connected in series in order to increase the number of connection portions 203C while also increasing the total length of the fuse region 203 in a space-efficient manner. Hence, in addition to increasing the overall electromigration effect, thereby enhancing the "sensitivity" of the fuse 200, also the difference between the non-programmed state and the programmed state may be increased since a significantly higher degradation of conductivity may be obtained along the entire length of the fuse region 203 compared to a reduced total length. Furthermore, the relation between contact resistance in the contact areas 201, 202 relative to the "bridge resistance" of the fuse region 203 may be increased without unduly contributing to overall space consumption of the fuse 200.

Figure 2n schematically illustrates a cross-sectional view of an actual implementation of the electronic fuse 200 in the semiconductor device 250, for instance corresponding to the configuration as shown in Figure 2j. As illustrated, the semiconductor 250 may comprise a substrate 251, such as a semiconductor substrate, a silicon-on-insulator (SOI) substrate and the like. Furthermore, a device layer 252 may be provided, for instance on the basis of an appropriate semiconductor layer which may comprise isolation regions, depending on the overall circuit configuration. For example, the electronic fuse 200 may be positioned above a corresponding isolation region, which may be formed in a corresponding semiconductor layer, while, in other cases, a portion of the fuse 200 or the entire fuse 200 may be formed above a semiconductor material. Moreover, the device 250 may comprise the electronic fuse 200, the contact areas 201, 202, which may be connected to a metallization system 230 by a contact level 220. The contact level 220 may comprise a dielectric material 222, for instance in combination with an etch stop material 223, in which are provided contact elements 221 connecting to the areas 201, 202, respectively.

The semiconductor device 250 may be formed on the basis of well-established manufacturing techniques, wherein, however, the basic design of the electronic fuse 200 may be accomplished on the principles as described above. Thus, the various components of the electronic fuse 200 may be formed together with other circuit elements, such as transistors and the like, on the basis of the corresponding design rules of the device level and the technology under consideration. For instance, the electronic fuse 200 may be formed together with gate electrodes of sophisticated transistor elements, such as the transistors 261, 262 (Figure 2a), wherein the gate electrodes may be formed on the basis of a polysilicon material in combination with a metal silicide, thereby forming a metal silicide 204 on a corresponding polysilicon material 207 in the electronic fuse 200. However, due to the increased sensitivity to electromigration effects and possibly to dopant depletion of the region 203 compared to conventional configurations, as previously described with reference to the device 100, the region 203 is less sensitive to any process-related fluctuations for a given range of programming voltages compared to conventional devices. That is, for a given programming voltage and for any process-related variations, a reliably detectable high impedance state may be obtained on the basis of the fuse region 203 including one or more areas of increased current density.

In other illustrative embodiments, gate electrodes of sophisticated transistors may be formed on the basis of sophisticated materials, such as a high-k dielectric material for the gate insulation layer in combination with metal-containing gate electrode materials. Also in this case, a corresponding manufacturing sequence may be used for providing the electronic fuse 200 since increased electromigration sensitivity may be accomplished on the basis of the fuse region 203 as described above. For example, a gate dielectric material with increased permittivity, for instance having a dielectric constant of 10.0 and significantly higher, may be deposited, followed by the deposition of an appropriate sophisticated gate electrode material. Thus, a corresponding insulating material 253 may also be provided in the region 203, followed by the metal-containing gate electrode material. For instance, the material 204 representing a metal-containing material may extend completely down to the insulating layer 253. Thus, the electronic fuse 200 may be formed on the basis of a sophisticated manufacturing technique without adding additional process complexity, while a high degree of sensitivity with respect to an intended electromigration effect during the programming of the fuse 200 may still be accomplished.

Figure 2i schematically illustrates the electronic fuse 200 such that a "u-like" configuration is obtained. That is, the three linear portions 203K, 203L and 203M are connected in series so as to define two angles of approximately 90 degrees oriented in the same direction so that a corresponding current flow may be anti-parallel in the portions 203M, 203K upon programming the electronic fuse 200.

As a result, the present disclosure provides techniques, layouts and methods for forming electronic fuses that may exhibit increased sensitivity to electromigration effects, thereby allowing the usage of a wider window of programming voltages while also reducing the sensitivity to process-related variations. Furthermore, the overall space consumption of the electronic fuses may be reduced, since corresponding contact elements may be reduced in size and/or in number.

The particular embodiments disclosed above are illustrative only, as the invention may be modified and practiced in different but equivalent manners apparent to those skilled in the art having the benefit of the teachings herein. For example, the process steps set forth above may be performed in a different order. Furthermore, no limitations are intended to the details of construction or design herein shown, other than as described in the claims below. It is therefore evident that the particular embodiments disclosed above may be altered or modified and all such variations are considered within the scope and spirit of the invention. Accordingly, the protection sought herein is as set forth in the claims below.

CLAIMS

WHAT IS CLAIMED:

1. A method of forming an electronic fuse (200) of an integrated circuit, the method comprising:

forming an electrode material above an insulating material formed above a substrate (251) of said integrated circuit;

forming a first contact area (201), a second contact area (202) and a fuse region (203) of said electronic fuse from said electrode material, said fuse region (203) connecting to said first and second contact areas, said fuse region (203) comprising at least one non-linear portion for generating a zone of increased current density; and

forming contact elements (221) in a contact level (220) of said integrated circuit, said contact elements connecting to said first and second contact areas (201, 202) of said electronic fuse (200).

2. The method of claim 1, wherein forming said first and second contact areas (201, 202) and said fuse region (203) comprises forming a metal silicide in said electrode material.

3. The method of claim 1, wherein forming said first and second contact areas and said fuse region comprises providing said electrode material at least partially as a metal-containing material prior to patterning said electrode material.

4. The method of claim 1, wherein said at least one non-linear portion of said fuse region comprises two connected linear portions.

5. The method of claim 4, wherein said two connected linear portions are formed so as to connect to each other on the basis of a target angle of approximately 90 degrees.

6. The method of claim 1, wherein said fuse region (203) is formed so as to include two or more non-linear portions, each of which generates a respective zone of increased current density.

7. The method of claim 6, wherein two or more non-linear portions are formed by a sequence of connected linear portions of said fuse region.

8. A method of designing an electronic fuse (200) of a semiconductor device, the method comprising:

providing a first contact area (201) and a second contact area (202) of said electronic fuse;

using a plurality of linear portions of a fuse region (203); and

combining said plurality of linear portions so as to form at least one connection region having a non-linear configuration to define a zone of increased current density.

9. The method of claim 8, wherein at least some of said plurality of linear portions are combined to form a fork-like structure.

10. The method of claim 8, wherein said plurality of linear portions are combined so as to form a single connection region having said non-linear configuration.

11. The method of claim 10, wherein said connection region is formed by a target angle of approximately 90 degrees.

12. The method of claim 11, wherein two or more connection regions are formed on the basis of a target angle of approximately 90 degrees.

13. A semiconductor device, comprising:

a plurality of circuit elements formed in and above a semiconductor layer;

an electronic fuse (200) formed on an insulating material, said electronic fuse (200) comprising a first contact area (201), a second contact area (202) and a fuse region (203) including at least one non-linear portion defining a zone of increased current density;

a contact level (220) formed above said semiconductor layer, said contact level (220) comprising a plurality of contact elements (221) connecting to said plurality of circuit elements and to said first and second contact areas (201, 202) of said electronic fuse; and

a metallization system (230) formed above said contact level (220).

14. The semiconductor device of claim 13, wherein said fuse region is comprised of polysilicon and a metal silicide.

15. The semiconductor device of claim 13, wherein said fuse region comprises a fork-like structure.

16. The semiconductor device of claim 13, wherein said fuse region comprises a plurality of linear portions connected in series, wherein at least two of said connected linear portions are connected in a non-linear manner so as to form said non-linear portion.

17. The semiconductor device of claim 16, wherein said at least two linear portions are connected so as to form an angle of approximately 90 degrees.

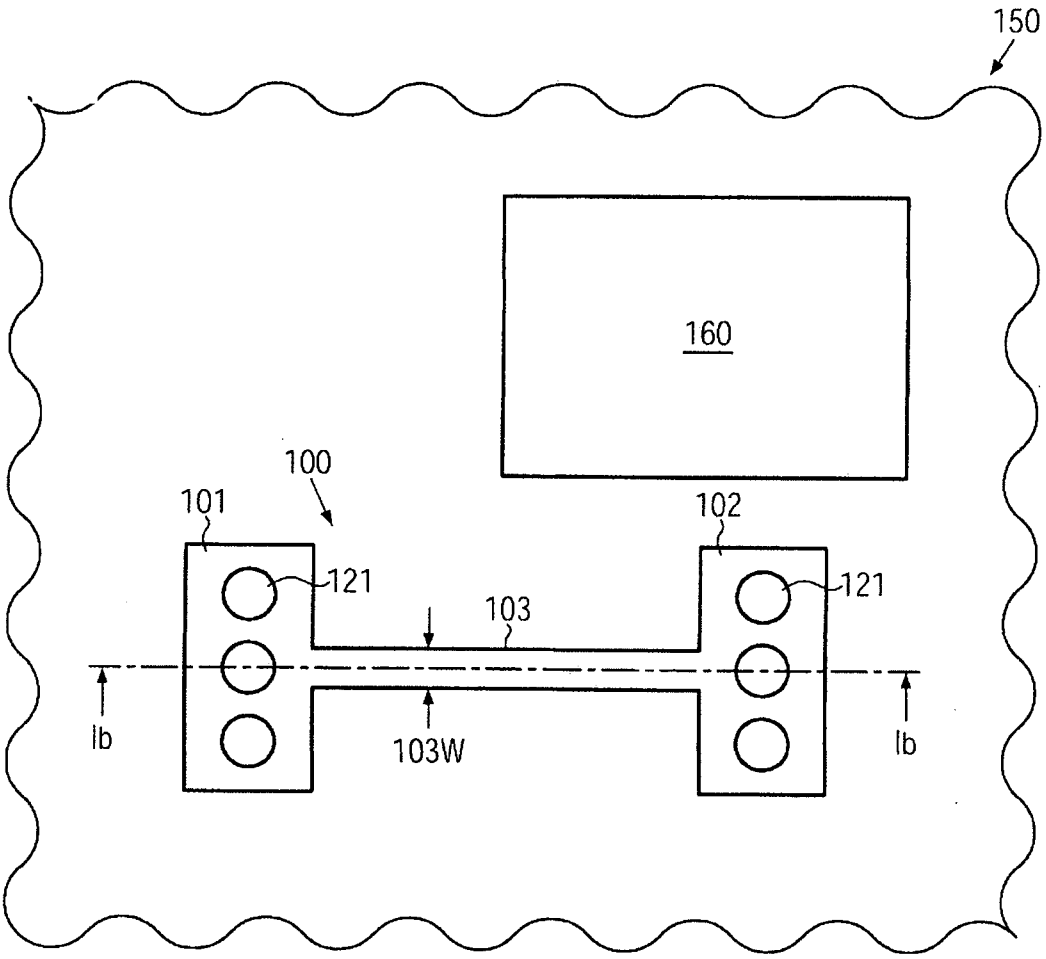


FIG. 1a
(prior art)

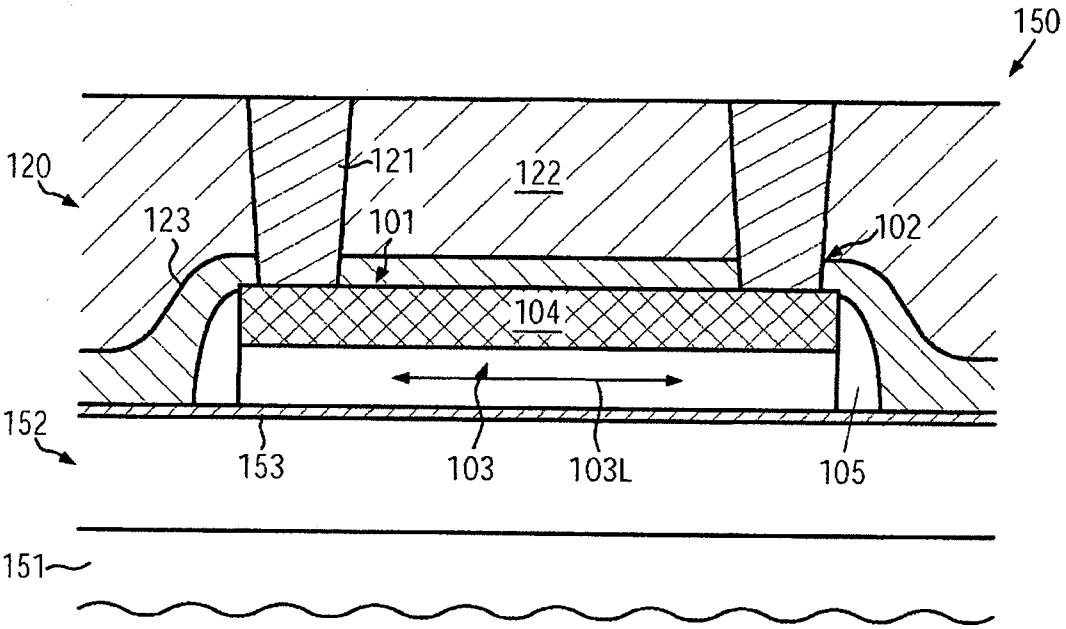


FIG. 1b
(prior art)

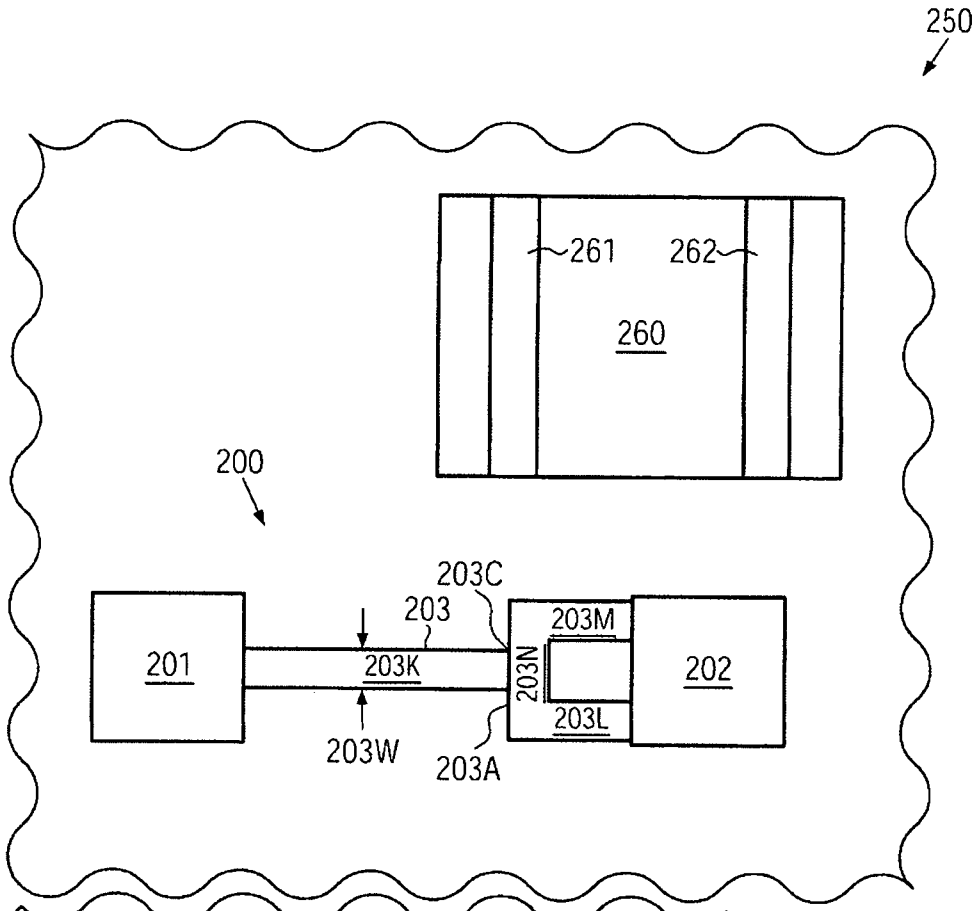

250
261
262
260
200
203C
203
203M
201
203K
203N
202
203L
203W
203A

FIG. 2a

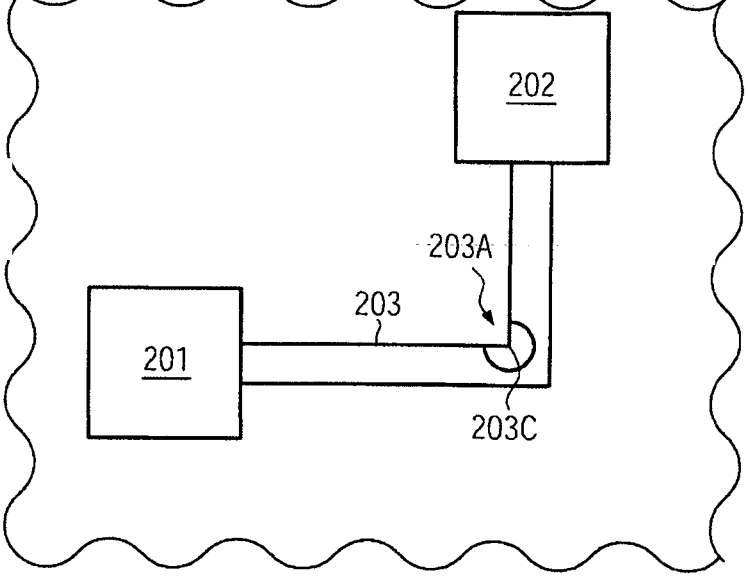

202
203A
203
201
203C

FIG. 2b

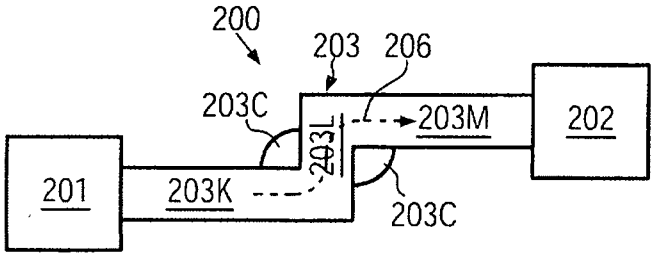


FIG. 2c

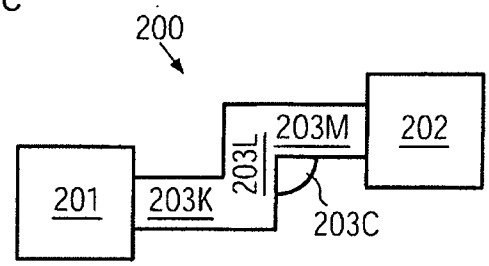


FIG. 2d

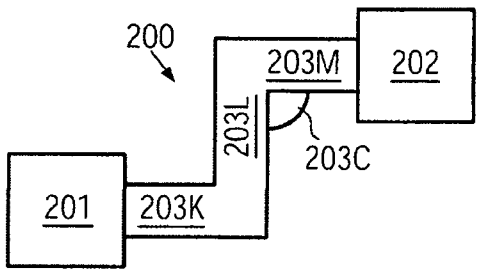


FIG. 2e

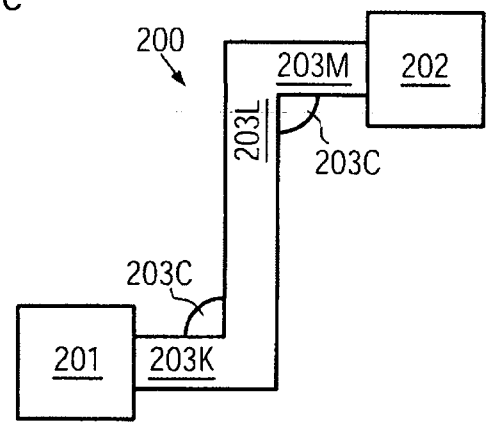


FIG. 2f

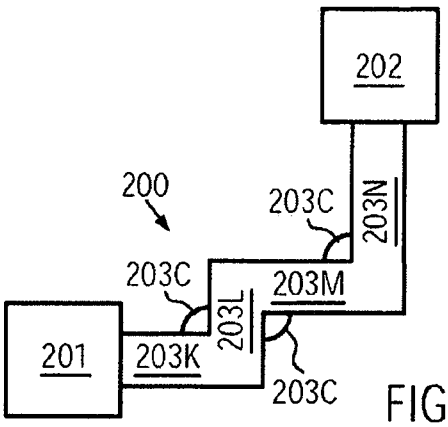


FIG. 2g

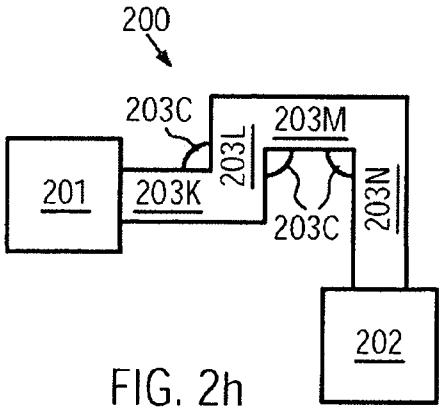


FIG. 2h

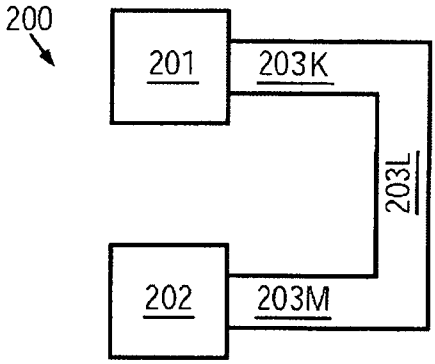


FIG. 2i

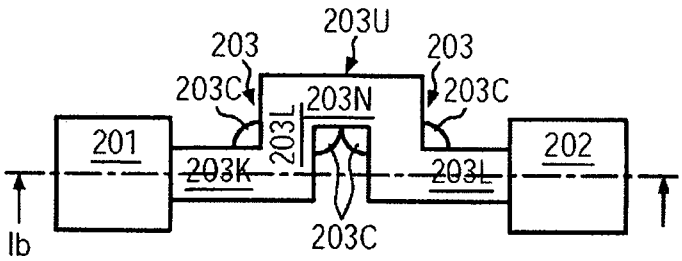


FIG. 2j

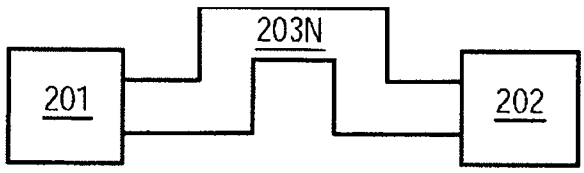


FIG. 2k

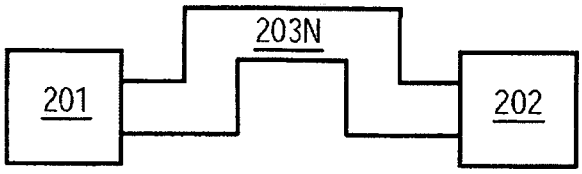


FIG. 2l

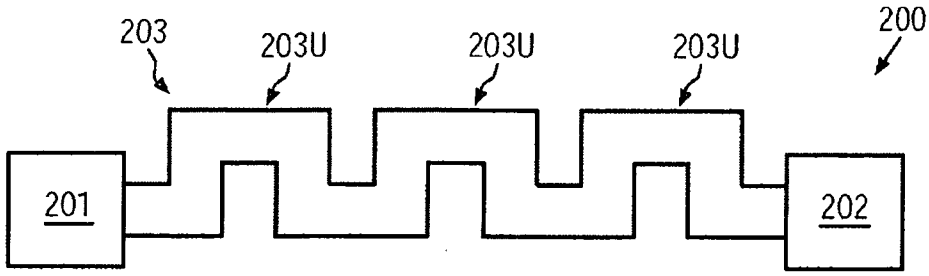

203
203U
203U
203U
200
201
202

FIG. 2m

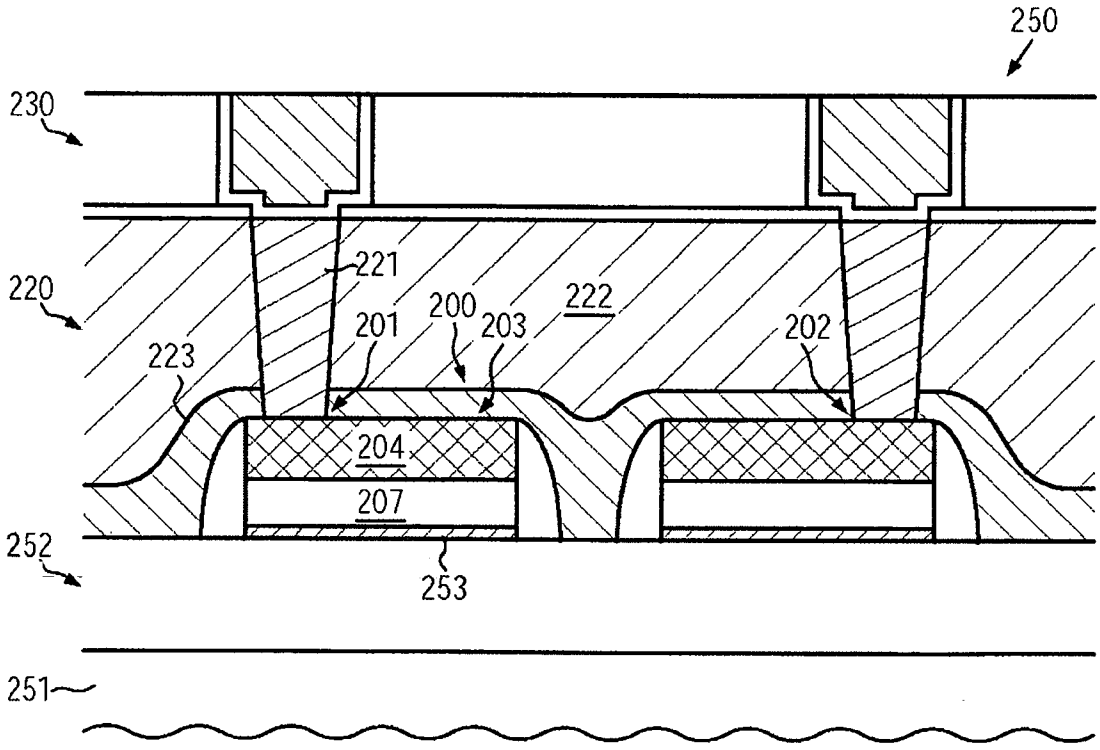

250
230
220
221
222
201
200
203
202
223
204
207
252
253
251

FIG. 2n

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2009/005901

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L23/525

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 933 591 B1 (SIDHU LAKHBEER S [US] ET AL) 23 August 2005 (2005-08-23) column 5, line 47 - line 67; figures 2,9,10 column 10, line 46 - column 11, line 21	1-6,8, 10-14, 16-17
X	CN 101 170 099 A (SHANGHAI GRACE SEMICONDUCTOR [CN]) 30 April 2008 (2008-04-30)	1-8, 10-14, 16-17
Y	the whole document	9,15
X,P	-& US 2009/140382 A1 (GAO WEN-YU [CN] ET AL) 4 June 2009 (2009-06-04)	1-8, 10-14, 16-17
Y,P	paragraphs [0035] - [0037], [0046] - [0049]; figures 5,6,11,12	9,15

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
4 February 2010	15/02/2010

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Zeisler, Peter

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2009/005901

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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X	EP 0 563 852 A1 (SIEMENS AG [DE]; IBM [US]) 6 October 1993 (1993-10-06) column 4, line 46 - column 5, line 54; figures 1-8	1,4-5,8, 10-11, 13,16-17
X	JP 04 051563 A (SEIKO EPSON CORP) 20 February 1992 (1992-02-20) the whole document	1,4,8, 10,13,16

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2009/005901

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