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(54) **Title**: COMPARATOR TESTING IN A FLASH A/D CONVERTER

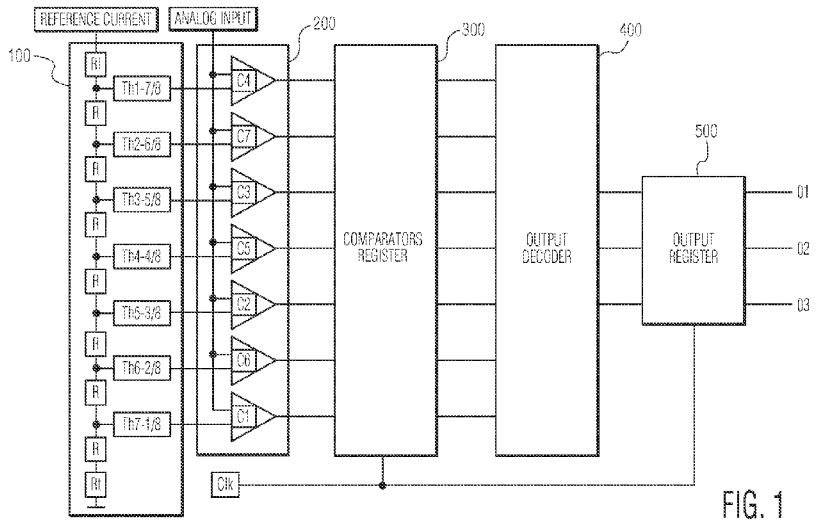


FIG. 1

(57) **Abstract**: The present disclosure relates to a testing circuit and a testing method of the comparators incorporated in a flash A/D converter. The testing circuit uses reconfigurable A/D converters to easily test and identify the defective comparators.

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COMPARATOR TESTING IN A FLASH A/D CONVERTER

BACKGROUND

[001] It has been shown that a flash A/D converter may be reconfigured either as a propagation type A/D converter or as a successive approximation A/D converter. It has also been shown that a propagation type A/D converter can be reconfigured as a D/A converter. The main reason for reconfigurability has been considered the possibility that at least one of the comparators of the flash A/D converter is defective. Therefore, there is a need determine if and which of the comparators is defective.

[002] US-A-5583502 describes a method of testing 2 bit A/D converters in a system comprising a plurality of such converters. Nothing is said about comparators testing.

[003] US-A-5124704 describes a method of testing flash A/D converters with the possibility of testing the comparators included in the converter. The converter is supposed to have differential input A/D comparators and comprises first and second logical circuits for indicating if the comparators are defective or not. The detection is based on monitoring the output current of the logical circuits. Furthermore, the logic circuits comprise NOR gates, each having 2^N input terminals, wherein N is the resolution of the converter.

[004] Drawbacks to this testing method include:

the method does not identify a specific comparator;

the method implies that a variable analog input generator is presented; and

once a defect is found, the circuit is discarded.

[005] It is therefore an object of the present invention to provide a method of testing the comparators of a flash A/D converter that provides the ability to:

i - identify the defective comparator or comparators;

ii – provide for reconfigurability of the converter;

iii – provide the test without using an external analogue signal source; and/or

iv – provide a simpler test logic.

BRIEF DESCRIPTION OF THE DRAWINGS

[006] Fig. 1 depicts a flash A/D converter.

[007] Fig. 2 depicts a reconfigurable comparator block.

[008] Fig. 3 depicts a propagation type A/D converter.

[009] Fig. 4 depicts a circuit for generating the analogue signal corresponding to a digital output.

[0010] Fig. 5 depicts a first testing circuit.

[0011] Fig. 6 depicts a system for software controlled testing.

[0012] Fig. 7 depicts a system for testing the comparator register.

[0013] Fig. 8 depicts a system for testing the output register.

[0014] Fig. 9 depicts an embodiment of a system for testing a flash analog to digital converter.

[0015] Fig. 10 is a process flow diagram of a testing process.

[0016] Fig. 11 depicts a circuit for an analog BIST test.

[0017] Fig. 12 depicts an embodiment of a reconfigurable BIST Flash A/D converter test scheme.

[0018] Fig. 13 depicts a content addressable memory.

DETAILED DESCRIPTION

[0019] Fig. 1 depicts a flash A/D converter comprising an array of comparators (e.g., block of comparators 200), each comparator having a threshold $i/2^N$, i = 1,…, N-1, wherein N is the resolution of the converter. For simplicity, let us consider a converter having a 3 bit resolution as shown in Fig. 1.

[0020] When an analog signal is applied to the comparator's inputs, the comparators generate what is commonly named a "thermometer code". The outputs of the comparators are connected to a decoder for generating a binary code corresponding to the amplitude of the analog input signal. Additionally, the A/D converter may comprise an error correction logic block for correcting the errors, which may occur in the process of conversion.

[0021] The main blocks are easily identifiable as the resistors ladder for generating the threshold voltages for the block of comparators 200. Another block is the comparators register block 300, which is used for storing the output signals of the comparators under control of the clock, Ck. The comparators register block 300 may be a simple array of D flip-flops or D latches. Another block is the output decoder block 400, which is used for transforming the "thermometer code" generated by the comparators into a binary code. And

finally, an additional block, the output register block 500, is used for storing the output signals of the decoder.

[0022] In the following paragraphs we shall focus on the compators' block 200.

[0023] Either during use or from the manufacturing process, one or more comparators could be defective, for example, it will provide erroneous information. When the manufacturing process generates the defect we may dispense with the circuit, but when the defect is generated during the working process the converter should be replaced. However, in certain situations this is not possible, because the working conditions do not allow human intervention as e.g. in dangerous working conditions, or in remote areas. Hence, the A/D converter should "take care" of itself, and therefore it should detect if defective comparators are present.

[0024] In order to make the A/D reconfigurable, switch matrices are provided between all the above-mentioned blocks. For the comparator block the circuit looks like the circuit depicted in Fig. 2.

[0025] The Switch Matrix 2 block can connect any of the comparator inputs to any threshold level Thi, i=1,…, 7. The signals P1,…, P7 are the respective output signals of the comparators and are essentially binary signals. In a normal operation, the comparator having the index i is connected to the respective Thi threshold level. The signals Pi are further connected to a respective flip-flop.

[0026] When the flash A/D converter is reconfigured as a propagation-type A/D converter only 3 out of the 7 comparators are connected to the threshold levels, the thresholds being selected via the Switch Matrix 2 under the control of the used comparators as it is shown in Fig. 3. In Fig. 3, C, C' and C" are 3 of the comparators C1,…, C7. At the output of the comparators one can find the converted digital signal as the vector **O=O1O2O3** wherein O1 is the Most Significant Bit (MSB).

[0027] The threshold of the comparator C is ½ and the threshold for the comparator C' is found in Equation 1 and the threshold for the comparator C'' is found in Equation 2.

$$V_{C'} = \mathbf{O1Th2} + \overline{\mathbf{O1}}\mathbf{Th6} \quad (1)$$

$$V_{C''} = \mathbf{O1O2Th1} + \mathbf{O1}\overline{\mathbf{O2}}\mathbf{Th3} + \overline{\mathbf{O1}}\mathbf{O2Th5} + \overline{\mathbf{O1O2}}\mathbf{Th7} \quad (2)$$

[0028] It has been shown that the threshold level defined by equation 2 can be used to determine the D/A converted signal defined by the output vector **O**, for example, an analogue signal having the expression given by the equation 3.

$$\mathbf{OUT} = \frac{\mathbf{O1}}{2} + \frac{\mathbf{O2}}{4} + \frac{\mathbf{O3}}{8} = V_{C''} + \frac{\overline{\mathbf{O3}}}{8} \qquad (3)$$

[0029] It has also been shown that the equation (3) can be used for building a simplified pipelined A/D converter.

[0030] We shall further show that equation (3) can also be used to generate the necessary input signal for testing the comparators.

[0031] Recall that a comparator changes its state whenever the input signal is larger that its threshold and therefore the output signal **OUT** from the equation 3 should be increased. A very simple way is to add to the signal **OUT** the signal 1/16, which will determine that the input signal will be situated in the middle of any quantification steps. Recall that it has been considered that the input signal is normalized and therefore all the signal levels are numbers in the interval 0,…, 1. The quantification levels are i/8, i=1,…, 7. Hence adding 1/16 to a quantization level will determine a level, which is half way between two consecutive quantization levels. This level can be obtained, for example, by taking the voltage across resistor Rt and choosing Rt=R.

[0032] As a direct consequence, the corresponding analogue signal to a digital one can be obtained as shown in Fig. 4, which is an embodiment of the invention. During the test of the comparators no external signal generator is necessary because the circuit shown in Fig. 4 generates the necessary analogue input.

[0033] An embodiment of a testing circuit is shown in Fig.5. In the testing circuit of Fig. 5 the Switch Matrix 3 is adapted to select, under the control of the configuration vector C_Vector, the correct output Pi, i= 1,…, 7 to the XOR gates. The correct output is the output selected by the the vector O1O2O3. The outputs of the XOR gates generate a first Match vector. The components of the Match vector will indicate, when they are in logical state 1, that a specific comparator is defective. It should be observed that instead of the XOR gates, any coincidence circuit can be used as e.g. XNOR, half adders, digital comparators. Even further, the whole operation can be done in software, as it is shown in Fig. 6.

[0034] In Fig. 6 the Control Unit 202 generates the vectors O1O2O3 and C_Vector and reads either the output of the selected comparators or the output of the XOR gates or both. In a first step, the Control Unit may compare the outputs of the Switch Matrix 3 with the input code O1O2O3 and determine if any of the comparators are defective. Then the results may be further compared with the match vector M1M2M3 for determining if the XOR gates are not defective. Hence, using this procedure the XOR gates may also be tested.

[0035] Let us go further with the test. As it can be observed from Fig. 1, the comparators outputs are connected to an output register of the comparator register block 300, which should be seen as an array of D-flip-flops or D-Latches. Of course, these digital circuits may be tested using, for example, a Boundary Scan test but this will increase significantly the size of the circuit. Instead of this, the outputs of the Switch Matrix 3 are connected to the inputs of the register and an additional Switch Matrix, similar to the Switch Matrix 3 is added to the outputs of the register.

[0036] After testing the first 3 comparators, a similar array of XOR gates is added to the output of the register.

[0037] An embodiment of a full testing apparatus is shown in Fig. 7. There have been shown only 3 out of the 7 D flip-flops whose clock input has not been shown for simplicity. The Switch Matrix, which is connected at the output of the flip-flops, is configured by the same C_Vector as the Switch Matrix connected at the input of the flip-flops.

[0038] It is also shown the possibility to test the flip-flops in a similar manner as the comparators. The result are indicated by the matching vector M'1M'2M'3 obtained at the output of the Switch Matrix 3'. Software implementation of the test is also similar as in the case of the comparators. For increasing clarity, the XOR gates from the output of the Switch Matrix 3 are not shown, but it should be understood that they may be present in the circuit.

[0039] Finally, the output register can also be tested as it is shown in Fig. 8, wherein all of the features shown in Fig. 7 have been maintained and the output register comprising the flip-flops/latches D'1, D'2 and D'3 has been added. The clock (Ck) line has also been added. The output register is tested on the falling edge/0state of the clock, while the comparator register is tested on the rising edge/1state of the clock. This reduces the time needed for the test to one clock period. Alternatively, the test can be carried out in two consecutive clock periods either on the rising edge or on the falling edge of the clock.

[0040] The result of the test is the output vector **M"1M"2M"3,** which is obtained at the output of the XOR gates. The software-based test can be used mutatis mutandis and it is not further shown here.

[0041] To this end, we have shown that the comparators and the registers can be tested using the possibility of a reconfigurable flash A/D converter to be configured as a propagation type A/D converter.

[0042] So far, we have not yet shown how to test the output decoder 400 shown in Fig. 1. The output decoder should not be tested if either at least one of the comparators or at least one of the registers is found to be defective. If after a test they are found OK then testing is

straightforward: **O1O2O3** determines the analogue input level; the converter is configured as a flash one i.e. as it is shown in Fig. 1; and the output vector **M"1M"2M"3** shows if the decoder is defective or not.

[0043] The final arrangement is shown in Fig. 9. In Fig. 9 there have been indicated all possible options for testing the AD converter, both in hardware and in software. Advantages of this testing method are:

no boundary scan needed;

the possibility to test N comparators at a time, wherein N is the resolution of the converter;

no need for external generators;

the test results can be stored in a separate memory such that a further or a periodical test will avoid any defective device and therefore reduce the test time;

the method could be extended to test the Switch Matrices, too and therefore a full test of the converter is possible; and

the method could be particularly useful for testing converters working in hard accessible places or remote areas.

[0044] Fig. 10 depicts a process flow diagram of an embodiment of a method for testing a flash A/D converter. When the test process is started, the analog input signal is decoupled from the input of the converter and the necessary input signal is determined by the digital code O1O2O3 as it was described earlier. Hence, in a first step, the converter is reconfigured as a propagation type A/D converter. After a rising edge of the clock signal a first group of comparators are tested and if one of the comparators is found defective the finding is stored in a table or in an equivalent storage device. This will allow that during a further test of the device, the defective device is not tested again. The same applies after a test of the comparators flip-flops.

[0045] After a falling edge of the clock signal, the output flip-flops/latches are tested and the result is managed as the testing results of the previous steps.

[0046] After the full testing of the A/D, the testing sequence is ended and the normal working sequence of the A/D is resumed.

[0047] Depending on the results of a first test, during subsequent tests the devices found defective are not tested anymore.

[0048] Besides the advantage of testing flash A/D converters, the method allows for improving the analog BIST testing. An analog BIST testing circuit looks as it is shown in Fig. 11. Fig. 11 depicts an embodiment of a BIST implementation. Incorporating BIST into

a device requires the addition of three functional blocks: a pattern generator, a signature (or response) analyzer, and a test controller. The pattern generator stimulates the circuitry under test (CUT). The signature analyzer gathers the CUT's response to the test pattern and compresses it to a single value, referred to as a signature. The test controller coordinates the actions of the test circuitry and provides a simple external interface.

[0049] Under the above considerations, the Analog BIST test reduces to the circuit shown in Fig. 12. The proposed BIST schematic comprises the BIST controller i.e. our control unit in previous figures and the signature analyzer, which comprises the XOR gates in our implementations. A feature of the current disclosure is that the signatures, for example, the vector **O1O2O3** determines both the analog input for testing, determines the reconfiguration of the A/D converter and makes the whole test without having any external interface. This results in a significant reduction in the complexity of the test structure.

[0050] We should further observe that the comparison between the output of any device under test and the vector O1O2O3 can be made using Content Addressable Memory (CAM) elements as is shown in Fig. 13. A CAM element includes the same connections as a Read/Write memory and in the embodiment of Fig. 13 includes:

a Read/Write (R/W) connection for determining the operation which is performed by the memory, e.g., read from the memory or write into the memory;

an Address connection for secting the CAM element;

Data_In connection for inputting an input bit into the CAM element;

Data_Out connection for reading the content of the CAM element; and

a clock (Ck) connection for synchronizing the operations of the CAM element with the circuit including it.

[0051] The CAM element further comprises a Data_Scan input for inputting data and for determining whether the inputted data matches the content stored in the memory. The result of the comparison is delivered at a Scan_Match output terminal. Depending on the implementation of the CAM a Scan_Match equal to 0 indicates that the content of the CAM element equals the Data_Scan input and a Scan_Match equal to 1 indicates that the content of the CAM element does not equal the Data_Scan input, or the other way around. The CAM elements can be grouped in arrays like any other memory elements for forming registers.

[0052] In an embodiment, such a register is included in the Control Unit and it is used for both storing the control vector C_Vector and for comparison of the outputs of the circuits under test. In this case, the outputs of the circuits under test are connected to the respective Data_Scan inputs of the CAM cell and the result of the test will be read from the respective

Scan_Match outputs. In this way, the necessary hardware for test will be reduced as it is not necessary to add the XOR gates for comparison or to make software operations for testing the circuit. It is further observed that in general the Control Unit may include built in CAM registers and therefore no additional hardware would be necessary for testing the A/D converter.

[0053] In another embodiment of the register, the Comparator register is implemented as a plurality of CAM elements, each element being connectable to a respective comparator. The Data_In terminal of each CAM element is coupled to the respective outputs of the comparators, the Data_Scan input is connected to a respective test bit included in the control vector C_Vector and the Scan_Match output will indicate whether or not the respective comparator is defective. Analogously, the output register may be implemented as a CAM register and the above considerations apply mutatis mutandis. Using this approach, the hardware needed for test is reduced.

[0054] Embodiments of the invention can take the form of an entirely hardware embodiment, an entirely software embodiment, or an embodiment containing both hardware and software elements. In one embodiment, the invention is implemented in software, which includes but is not limited to firmware, resident software, microcode, etc.

[0055] Furthermore, embodiments of the invention can take the form of a computer program product accessible from a computer-usable or computer-readable storage medium providing program code for use by or in connection with a computer or any instruction execution system. For the purposes of this description, a computer-usable or computer readable storage medium can be any apparatus that can store the program for use by or in connection with the instruction execution system, apparatus, or device.

[0056] The computer-useable or computer-readable storage medium can be an electronic, magnetic, optical, electromagnetic, infrared, or semiconductor system (or apparatus or device), or a propagation medium. Examples of a computer-readable storage medium include a semiconductor or solid state memory, magnetic tape, a removable computer diskette, a random access memory (RAM), a read-only memory (ROM), a rigid magnetic disk, and an optical disk. Current examples of optical disks include a compact disk with read only memory (CD-ROM), a compact disk with read/write (CD-R/W), a digital video disk (DVD), and high-definition (HD) disks such as Blu-Ray and HD-DVD.

[0057] An embodiment of a data processing system suitable for storing and/or executing program code includes at least one processor coupled directly or indirectly to memory elements through a system bus such as a data, address, and/or control bus. The memory

elements can include local memory employed during actual execution of the program code, bulk storage, and cache memories which provide temporary storage of at least some program code in order to reduce the number of times code must be retrieved from bulk storage during execution.

[0058] Although the operations of the method(s) herein are shown and described in a particular order, the order of the operations of each method may be altered so that certain operations may be performed in an inverse order or so that certain operations may be performed, at least in part, concurrently with other operations. In another embodiment, instructions or sub-operations of distinct operations may be implemented in an intermittent and/or alternating manner.

[0059] Although specific embodiments of the invention have been described and illustrated, the invention is not to be limited to the specific forms or arrangements of parts so described and illustrated. The scope of the invention is to be defined by the claims appended hereto and their equivalents.

WHAT IS CLAIMED IS:

1. A method of testing a flash analog to digital converter, the flash analog to digital converter including a threshold generator (100) coupled to a comparator block (200) comprising a set of comparators, the set of comparators being further coupled to a comparator register (300), the comparator register (300) being coupled to an output decoder (400), the output decoder being coupled to an output register (500); the method comprising the step of reconfiguring the flash analog to digital converter into a propagation-type analog to digital converter.

2. A method of testing a flash analog to digital converter as claimed in claim 1 further comprising the step of generating an analog signal determined by the threshold generator, the value of said analog signal being determined by a test vector used for testing the flash analog to digital converter, the analog signal being inputted into the set of comparators.

3. A method of testing a flash analog to digital converter as claimed in claims 1 or 2 further comprising the steps of:
- selecting from the set of comparators a subset which are used in the propagation type of analog to digital converter, the selection being determined by the test vector; and
- comparing the test vector with a set of outputs of the selected comparators, for determining if and which comparator is defective.

4. A method of testing a flash analog to digital converter as claimed in claims 1, 2, 3 further comprising the step of testing the comparator register, wherein a comparator register set is selectively coupled to a set of comparator outputs corresponding to the set of comparators, the method comprising the steps of:
- selecting the comparators register set using the test vector; and
- comparing output signals generated by the comparators register set with the test vector for determining if and which register is defective.

5. A method of testing a flash analog to digital converter as claimed in any of the previous claims further comprising the step of testing the output register by

comparing the test vector with another signal generated by the output register for determining if and which part of the register is defective.

6. A method of testing a flash analog to digital converter as claimed in any of the previous claims wherein the comparing step comprises XORing the test vector with the respective outputs of the devices under test.

7. A method of testing a flash analog to digital converter as claimed in claims 1 to 5, wherein the step of comparing is achieved by subtracting the test vector from the respective outputs of the devices under test.

8. A method of testing a flash analog to digital converter as claimed in claims 1 to 5, wherein the step of comparing on is achieved in a content addressable memory, said content addressable memory storing the test vector.

9. A method of auto testing a flash analog to digital converter wherein a test vector determines an analog input in the converter, the test vector being further used as a signature vector, and the test vector is used to reconfigure the flash analog to digital converter into a propagation type analog to digital converter.

10. A self BIST comprising the steps claimed in any of the claims 1 to 9.

11. An analog to digital conversion system adapted to be tested comprising:

- a flash analog to digital converter comprising:
  - a reference threshold generator (100);
  - a comparator block (200) comprising a set of comparators, the comparator block being coupled to the reference threshold generator;
  - a comparator register (300) coupled to the comparator block;
  - an output decoder (400) coupled to the comparator register;
  - an output register (500) coupled to the output decoder;
- a Control Unit for generating a control vector (O1O2O3); and
- a first switch matrix (Switch Matrix 2) coupled between the reference threshold generator (100) and the comparator block (200);

wherein the control vector reconfigures the flash analog to digital converter into a propagation type analog to digital converter, the control vector being further used for testing the comparator block (200).

12. An analog to digital conversion system as claimed in claim 11, wherein an analog signal, which is inputted into the analog to digital converter, is obtained by adding signals obtained at selected outputs of the first switch matrix by the control vector.

13. An analog to digital conversion system as claimed in claims 11 - 12, further comprising a first plurality of comparing devices coupled to a selected set of comparators from the comparator block and further receiving the control vector for determining if and which comparator may be defective.

14. An analog to digital conversion system as claimed in claim 13, wherein the first plurality of comparing devices comprises XOR gates.

15. An analog to digital conversion system as claimed in claim 13, wherein the first plurality of comparing devices comprises a first plurality of Content Addressable memory cells.

16. An analog to digital conversion system as claimed in claims 11 - 15, wherein the comparator register comprises a first plurality of memory cells which are selectively connected to the first plurality of comparators, the first plurality of memory cells being coupled to a second plurality of comparing devices, the comparing devices further receiving the control vector for determining if and which comparator may be defective.

17. An analog to digital conversion system as claimed in claim 16, wherein the second plurality of comparing devices comprises XOR gates.

18. An analog to digital conversion system as claimed in claim 16, wherein the second plurality of comparing devices comprises a second plurality of Content Addressable memory cells.

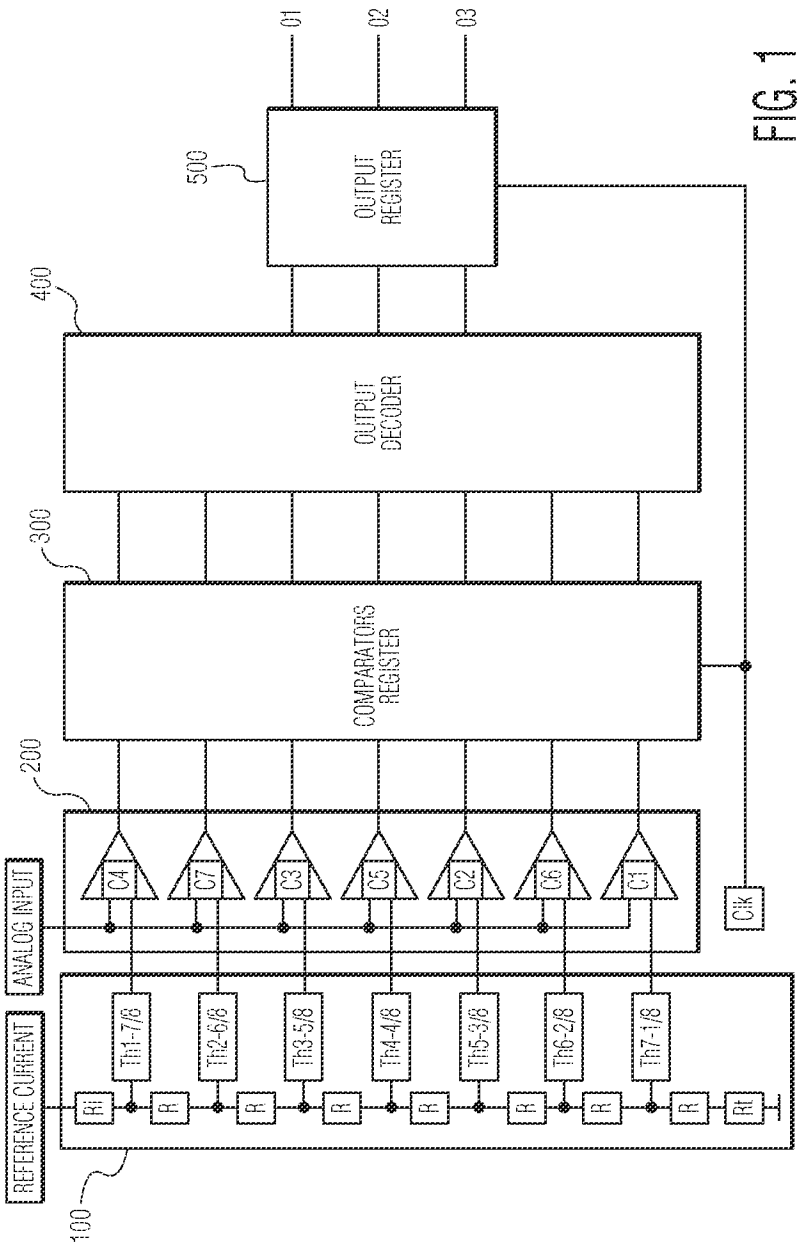

01
02
03
500
OUTPUT REGISTER
400
OUTPUT DECODER
300
COMPARATORS REGISTER
200
C4
C7
C3
C5
C2
C6
C1
Clk
ANALOG INPUT
REFERENCE CURRENT
Th1-7/8
Th2-6/8
Th3-5/8
Th4-4/8
Th5-3/8
Th6-2/8
Th7-1/8
Ri
R
Rt
100

FIG. 1

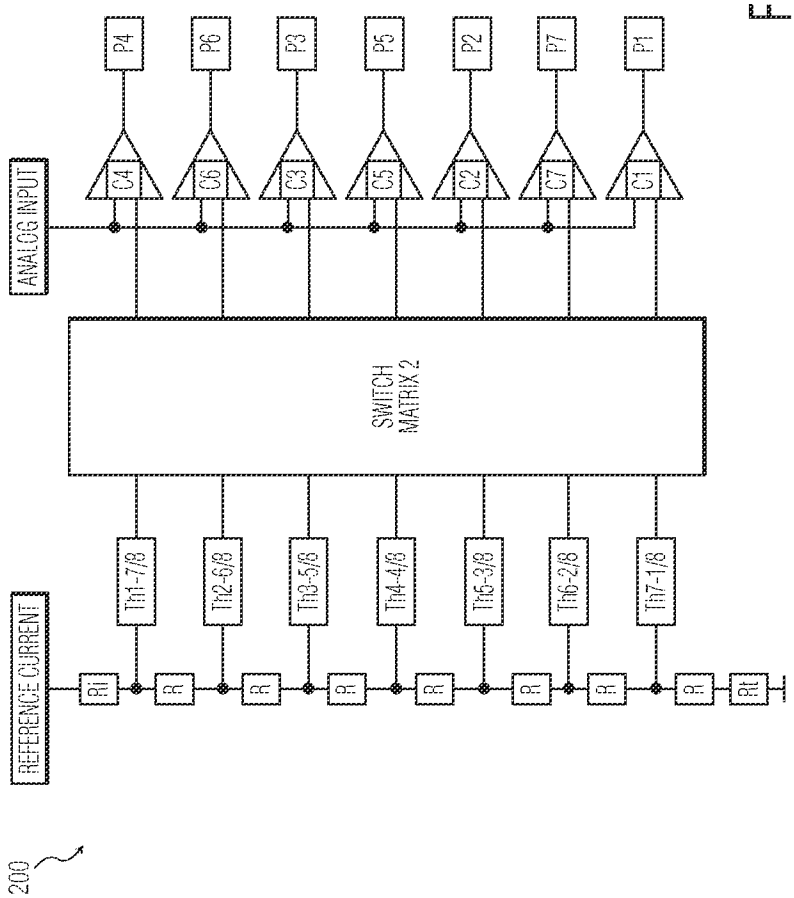

P4
P6
P3
P5
P2
P7
P1
C4
C6
C3
C5
C2
C7
C1
ANALOG INPUT
SWITCH MATRIX 2
REFERENCE CURRENT
Th1-7/8
Th2-6/8
Th3-5/8
Th4-4/8
Th5-3/8
Th6-2/8
Th7-1/8
Rl
R
Rt
200

FIG. 2

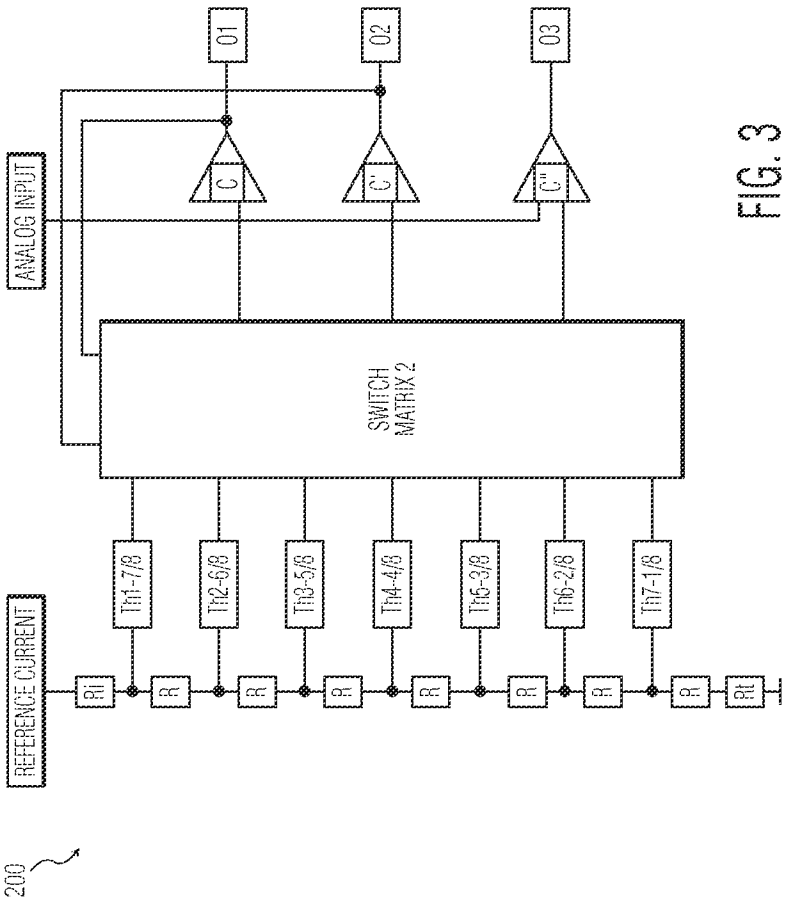

200
REFERENCE CURRENT
ANALOG INPUT
SWITCH MATRIX 2
01
02
03
C
C'
C''
Th1-7/8
Th2-6/8
Th3-5/8
Th4-4/8
Th5-3/8
Th6-2/8
Th7-1/8
R
R1

FIG. 3

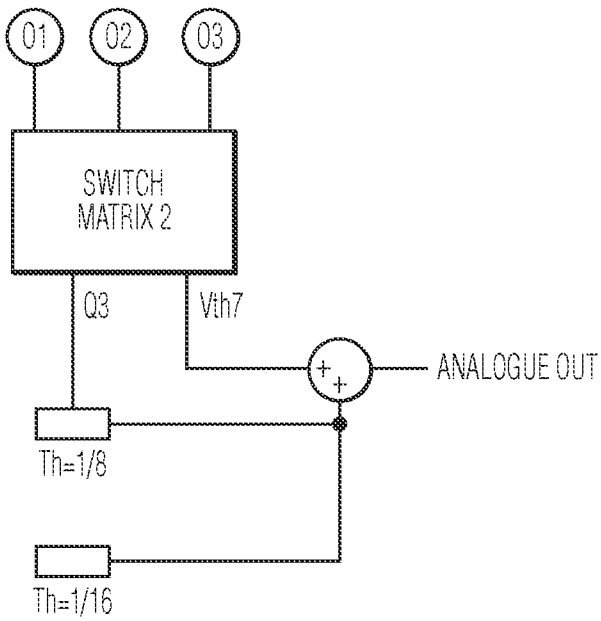


FIG. 4

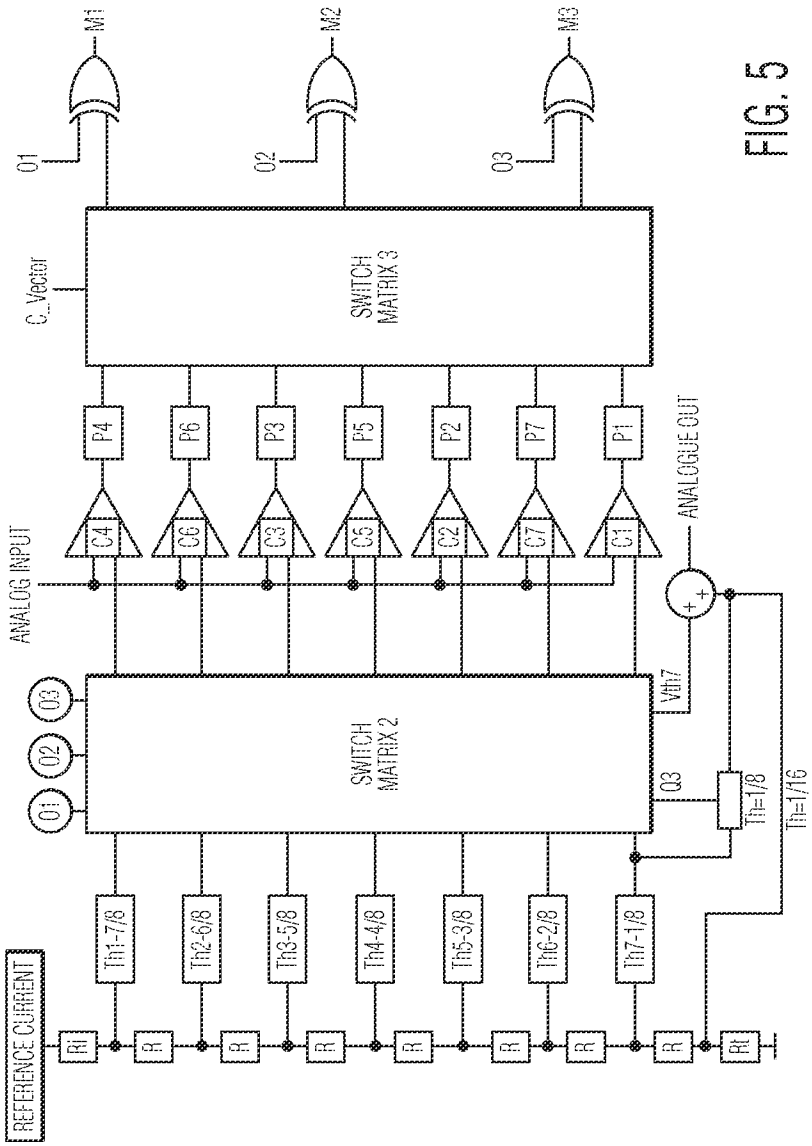

M1
M2
M3
O1
O2
O3
C_Vector
SWITCH MATRIX 3
P4
P6
P3
P5
P2
P7
P1
ANALOG INPUT
C4
C6
C3
C5
C2
C7
C1
ANALOGUE OUT
SWITCH MATRIX 2
Vth7
Q3
Th=1/8
Th=1/16
Th1-7/8
Th2-6/8
Th3-5/8
Th4-4/8
Th5-3/8
Th6-2/8
Th7-1/8
REFERENCE CURRENT
R
R
R
R
R
R
R
R

FIG. 5

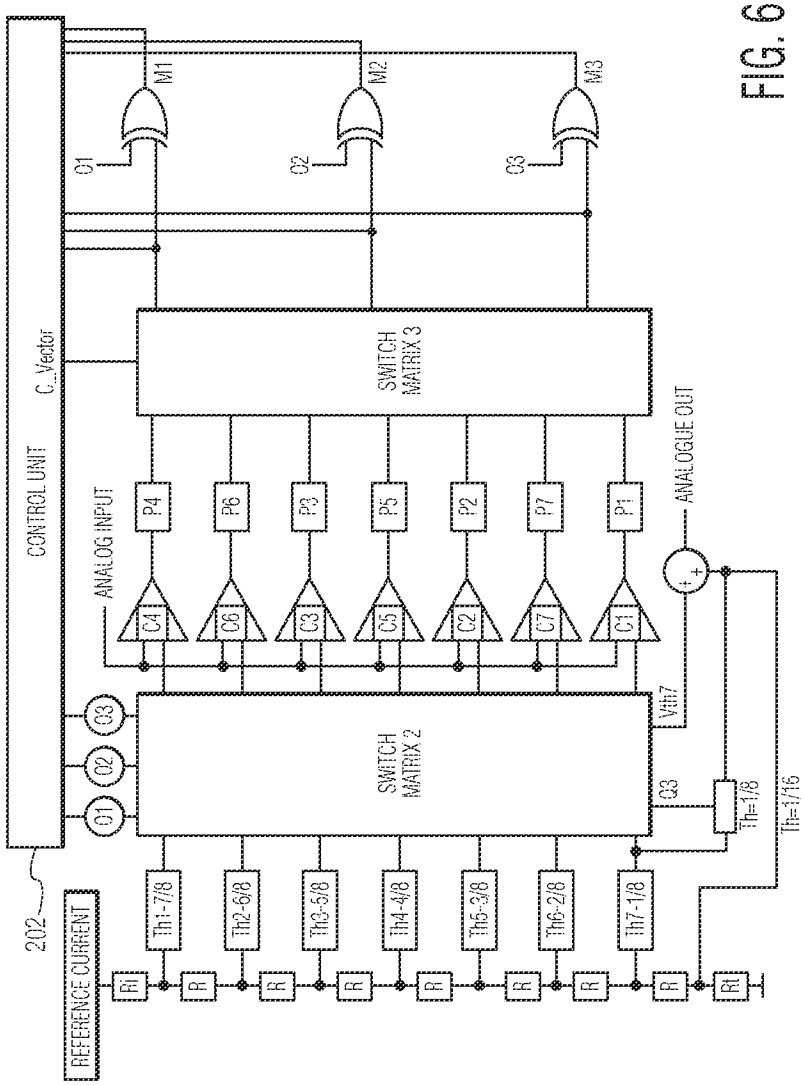

CONTROL UNIT
C_Vector
202
REFERENCE CURRENT
M1
M2
M3
Q1
Q2
Q3
SWITCH MATRIX 3
SWITCH MATRIX 2
ANALOG INPUT
ANALOGUE OUT
P4
P6
P3
P5
P2
P7
P1
C4
C6
C3
C5
C2
C7
C1
Vth7
Th=1/8
Th=1/16
Th1-7/8
Th2-6/8
Th3-5/8
Th4-4/8
Th5-3/8
Th6-2/8
Th7-1/8
R
R1

FIG. 6

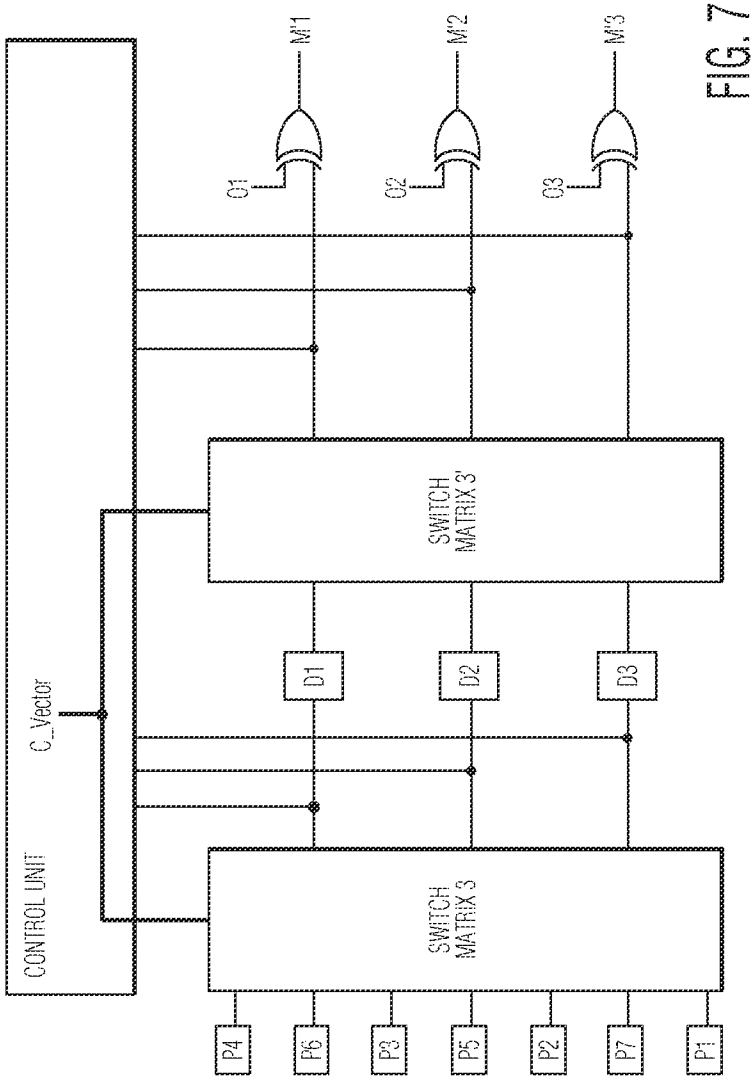

M'1
M'2
M'3
O1
O2
O3
SWITCH MATRIX 3'
D1
D2
D3
C_Vector
CONTROL UNIT
SWITCH MATRIX 3
P4
P6
P3
P5
P2
P7
P1

FIG. 7

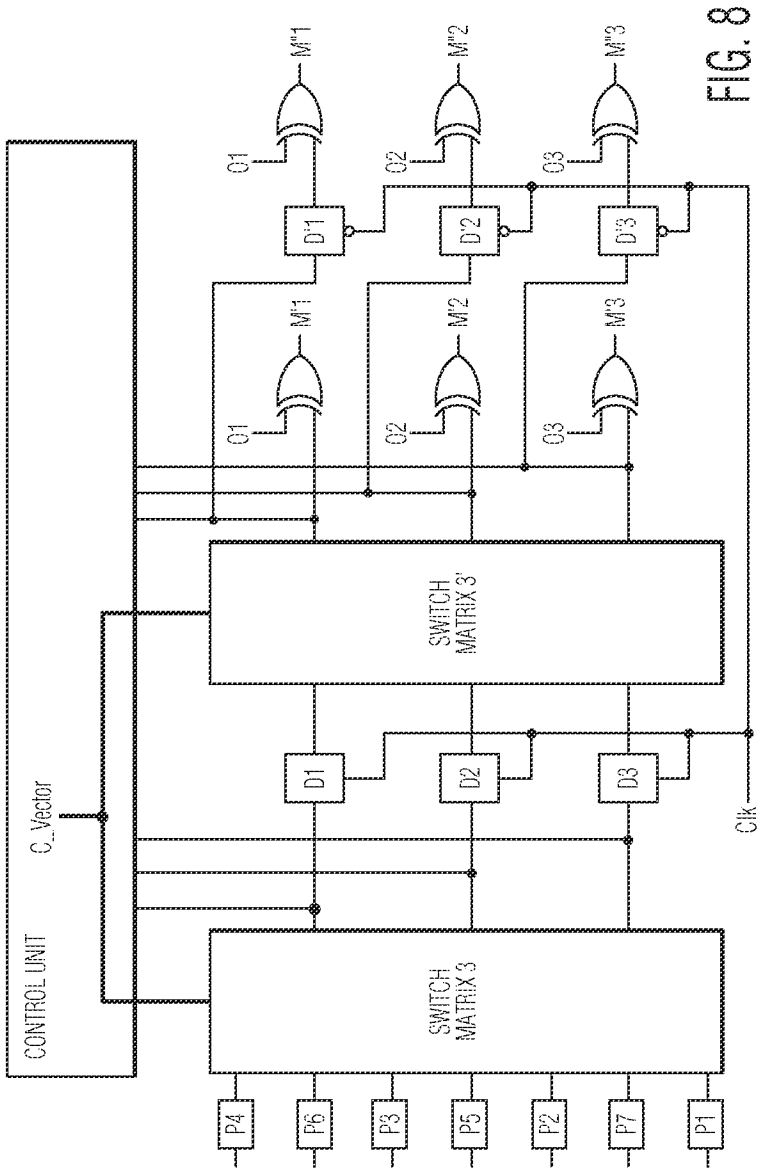

CONTROL UNIT
C_Vector
SWITCH MATRIX 3
SWITCH MATRIX 3'
D1
D2
D3
D'1
D'2
D'3
M1
M2
M3
M'1
M'2
M'3
O1
O2
O3
Clk
P4
P6
P3
P5
P2
P7
P1

FIG. 8

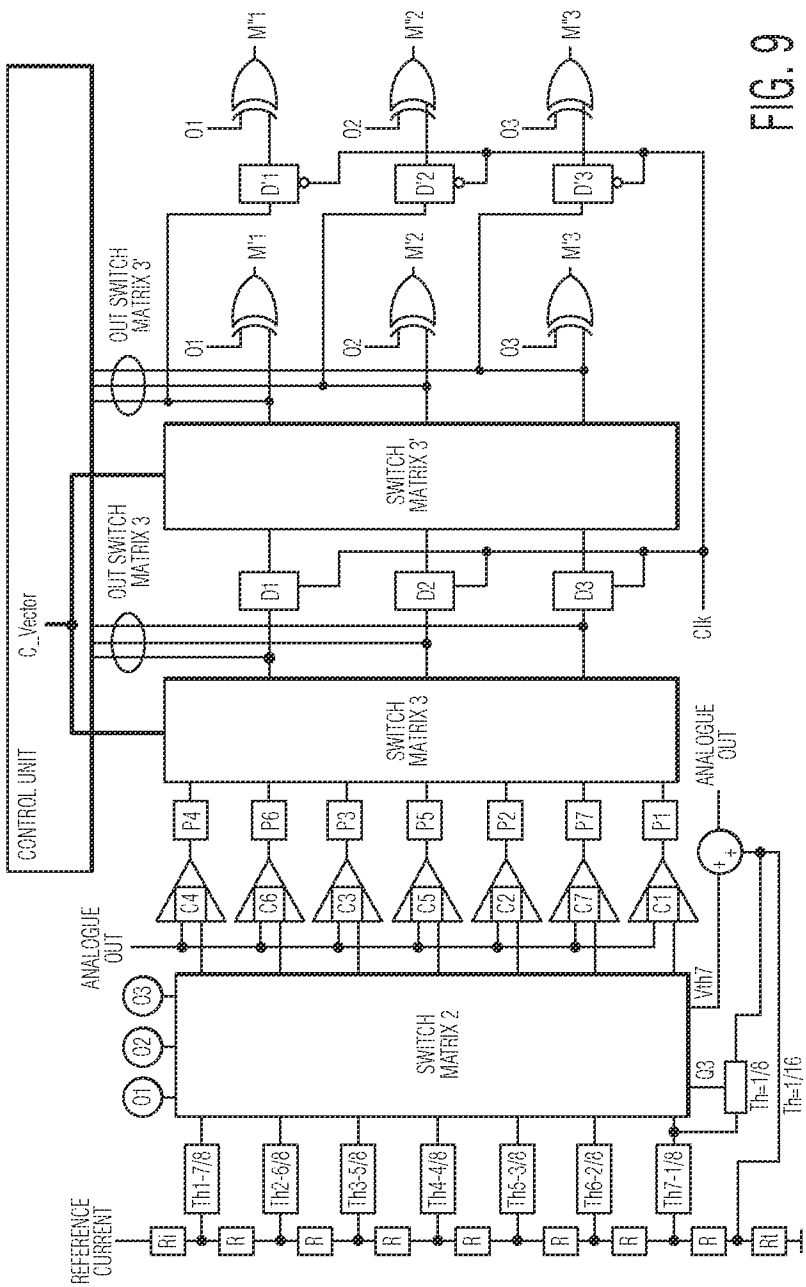

CONTROL UNIT
C_Vector
OUT SWITCH MATRIX 3
OUT SWITCH MATRIX 3'
SWITCH MATRIX 3
SWITCH MATRIX 3'
SWITCH MATRIX 2
D1
D2
D3
D'1
D'2
D'3
M1
M2
M3
M'1
M'2
M'3
O1
O2
O3
Clk
P4
P6
P3
P5
P2
P7
P1
C4
C6
C3
C5
C2
C7
C1
ANALOGUE OUT
ANALOGUE OUT
Vth7
G3
Th=1/8
Th=1/16
Th1-7/8
Th2-6/8
Th3-5/8
Th4-4/8
Th5-3/8
Th6-2/8
Th7-1/8
R
REFERENCE CURRENT

FIG. 9

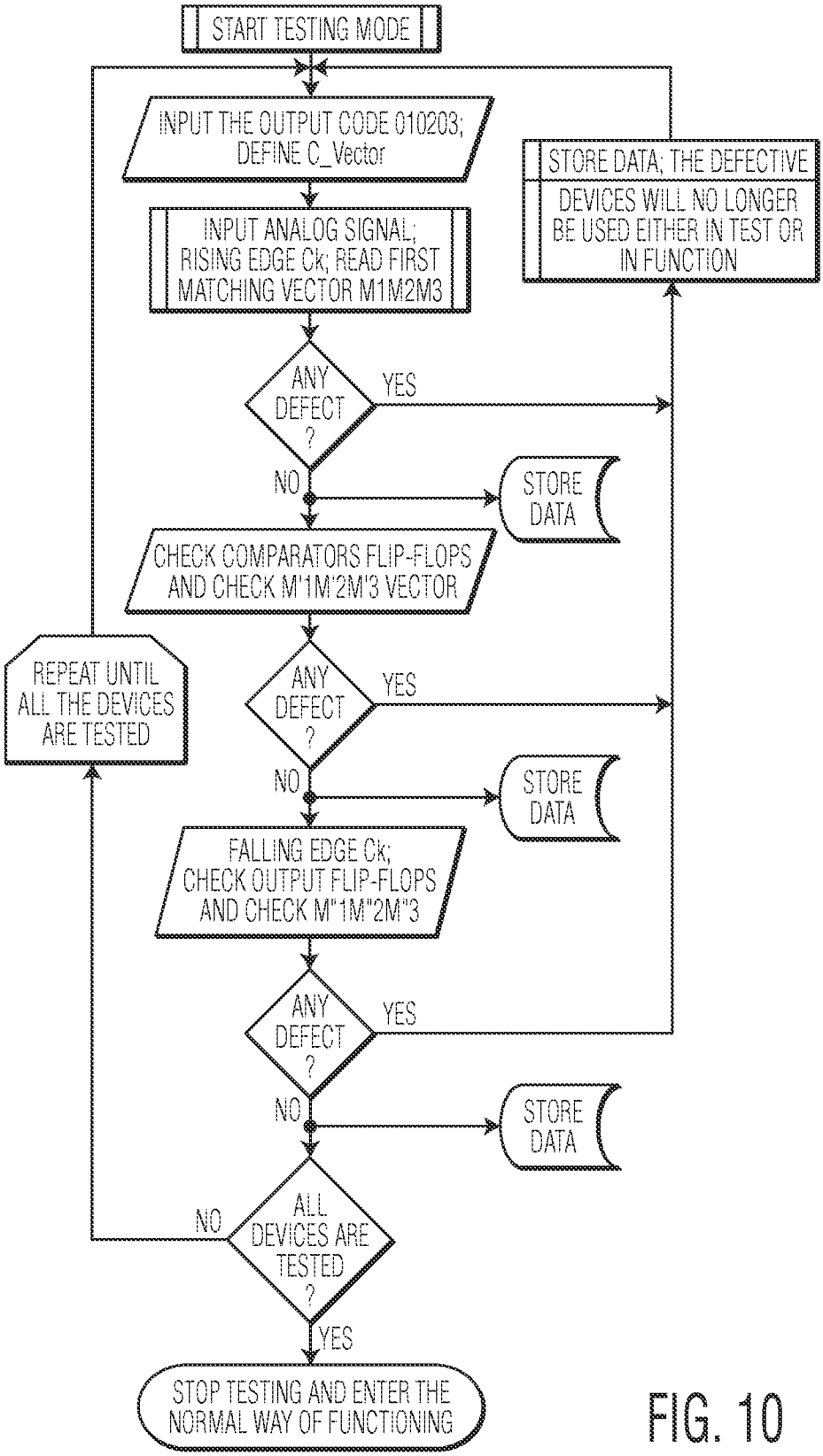

START TESTING MODE
INPUT THE OUTPUT CODE 010203; DEFINE C_Vector
INPUT ANALOG SIGNAL; RISING EDGE Ck; READ FIRST MATCHING VECTOR M1M2M3
ANY DEFECT ?
YES
NO
STORE DATA
CHECK COMPARATORS FLIP-FLOPS AND CHECK M'1M'2M'3 VECTOR
ANY DEFECT ?
YES
NO
STORE DATA
FALLING EDGE Ck; CHECK OUTPUT FLIP-FLOPS AND CHECK M"1M"2M"3
ANY DEFECT ?
YES
NO
STORE DATA
ALL DEVICES ARE TESTED ?
NO
YES
REPEAT UNTIL ALL THE DEVICES ARE TESTED
STORE DATA; THE DEFECTIVE DEVICES WILL NO LONGER BE USED EITHER IN TEST OR IN FUNCTION
STOP TESTING AND ENTER THE NORMAL WAY OF FUNCTIONING

FIG. 10

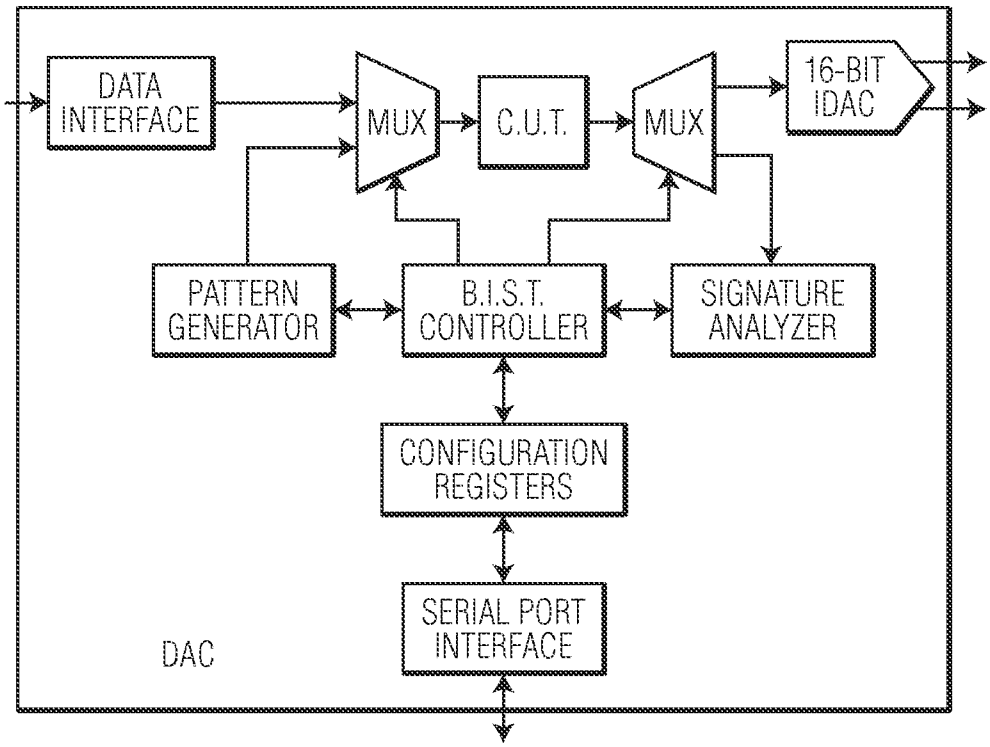

DATA INTERFACE
MUX
C.U.T.
MUX
16-BIT IDAC
PATTERN GENERATOR
B.I.S.T. CONTROLLER
SIGNATURE ANALYZER
CONFIGURATION REGISTERS
SERIAL PORT INTERFACE
DAC

FIG. 11

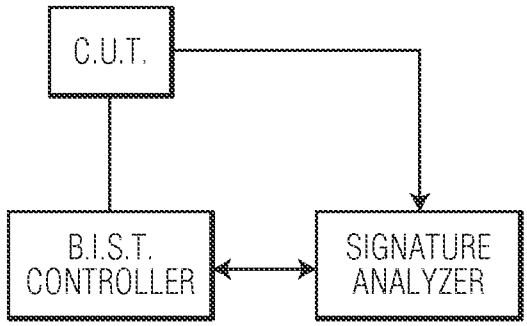

C.U.T.
B.I.S.T.
CONTROLLER
SIGNATURE
ANALYZER

FIG. 12

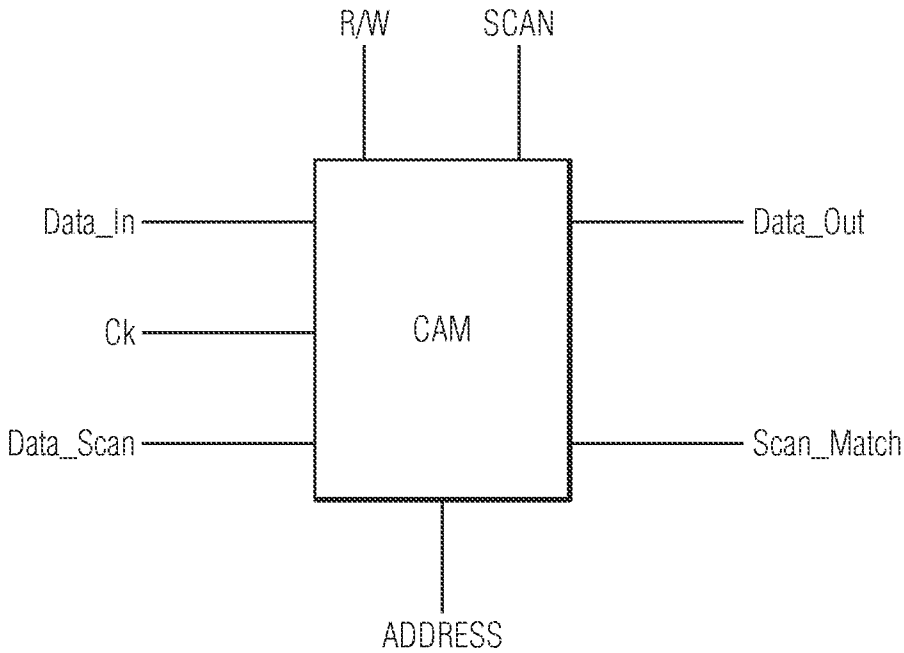

R/W
SCAN
Data_In
Ck
Data_Scan
CAM
Data_Out
Scan_Match
ADDRESS

FIG. 13

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2009/054084

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03M1/10 G01R31/28

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03M G01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CRISTIAN E ONETE: "Reconfigurable flash A/D converters" SOC CONFERENCE, 2008 IEEE INTERNATIONAL, IEEE, PISCATAWAY, NJ, USA, 17 September 2008 (2008-09-17), pages 323-326, XP031345871 ISBN: 978-1-4244-2596-9	1-2,9-12
Y	the whole document	3-8, 13-18

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
4 November 2009	11/11/2009

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Brosa, Anna-Maria

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2009/054084

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CRISTIAN E ONETE: "Reconfigurable A/D - D/A converter and its use in pipelined A/D converters" ELECTRONICS, CIRCUITS AND SYSTEMS, 2008. ICECS 2008. 15TH IEEE INTERNATIONAL CONFERENCE ON, IEEE, PISCATAWAY, NJ, USA, 31 August 2008 (2008-08-31), pages 288-291, XP031362481 ISBN: 978-1-4244-2181-7 the whole document	1,9-11
Y	JP 11 133117 A (ANDO ELECTRIC) 21 May 1999 (1999-05-21) abstract; figure 1	3-8, 13-18
Y	JP 07 262161 A (ROHM CO LTD) 13 October 1995 (1995-10-13) abstract; figure 1	3-8, 13-18
A	US 5 583 502 A (TAKEUCHI SUMITAKA [JP] ET AL) 10 December 1996 (1996-12-10) cited in the application abstract	1-18
A	US 5 124 704 A (KASE KIYOSHI [JP] ET AL) 23 June 1992 (1992-06-23) cited in the application column 1, lines 6-9, 12; figure 1 column 2, lines 6-25; claim 1	1-18

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2009/054084

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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JP 7262161 A	13-10-1995	NONE	
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US 5124704 A	23-06-1992	DE 69128116 D1	11-12-1997
		DE 69128116 T2	02-04-1998
		EP 0476331 A2	25-03-1992