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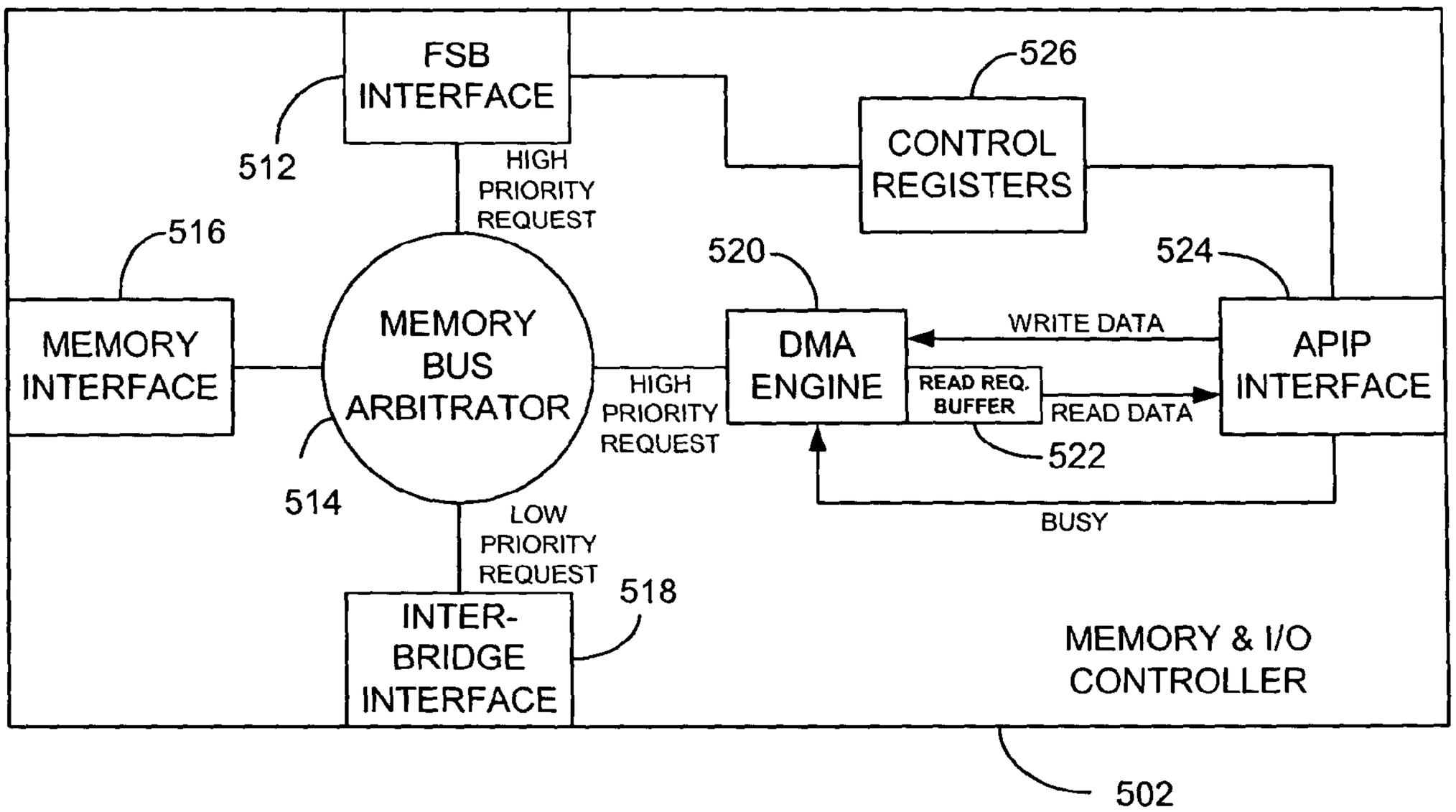
(54) Titre : ARCHITECTURE ET CONTROLEUR DE MEMOIRE D'ORDINATEUR PERMETTANT UN COUPLAGE ETROIT DANS UN SYSTEME HYBRIDE DE TRAITEMENT UTILISANT UN PORT DE PROCESSEUR D'INTERFACE ADAPTATIF

(54) Title: MEMORY CONTROLLER WITH ADAPTIVE PROCESSOR INTERFACE PORT



(57) Abrégé/Abstract:
A computer system architecture and memory controller (502) for close-coupling within a hybrid computing system using an adaptive processor interface port ("APIP") (524) added to, or in conjunction with, the memory and I/O controller chip of the core logic. Memory accesses to and from this port, as well as the main microprocessor bus, are then arbitrated by the memory control circuitry (514) forming a portion of the controller chip. In this fashion, both the microprocessors and the adaptive processors of the hybrid computing system exhibit equal memory bandwidth and latency. In addition, because it is a separate electrical port from the microprocessor bus, the APIP is not required to comply with, and participate in, all FSB protocol (512). This results in reduced protocol overhead which results higher yielded payload on the interface.

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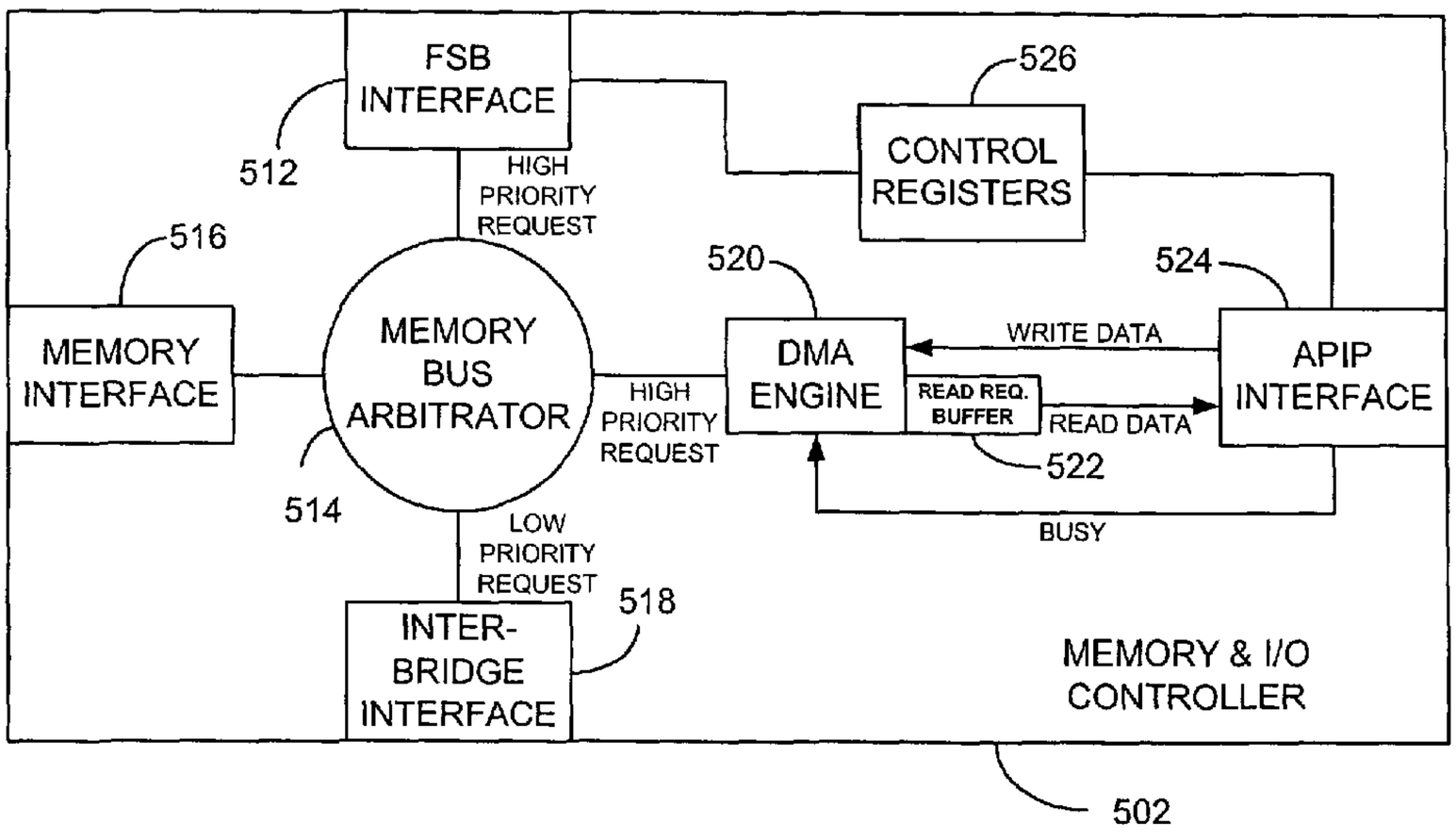
(54) Title: MEMORY CONTROLLER WITH ADAPTIVE PROCESSOR INTERFACE PORT



(57) Abstract: A computer system architecture and memory controller (502) for close-coupling within a hybrid computing system using an adaptive processor interface port ("APIP") (524) added to, or in conjunction with, the memory and I/O controller chip of the core logic. Memory accesses to and from this port, as well as the main microprocessor bus, are then arbitrated by the memory control circuitry (514) forming a portion of the controller chip. In this fashion, both the microprocessors and the adaptive processors of the hybrid computing system exhibit equal memory bandwidth and latency. In addition, because it is a separate electrical port from the microprocessor bus, the APIP is not required to comply with, and participate in, all FSB protocol (512). This results in reduced protocol overhead which results higher yielded payload on the interface.

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COMPUTER SYSTEM ARCHITECTURE AND MEMORY CONTROLLER FOR CLOSE-COUPLING WITHIN A HYBRID PROCESSING SYSTEM UTILIZING AN ADAPTIVE PROCESSOR INTERFACE PORT

CROSS REFERENCE TO RELATED PATENT APPLICATIONS

The present invention claims priority from, and is a continuation-in-part application of, U.S. Patent Application Ser. No. 09/755,744 filed January 5, 2001 for: "Multiprocessor Computer Architecture Incorporating a Plurality of Memory Algorithm Processors in the Memory Subsystem" which is a divisional application of U.S. Patent Application Ser. No. 09/481,902 filed January 12, 2000 (now U.S. Patent No. 6,247,110) which is a continuation application of U.S. Patent Application Ser. No. 08/992,763 filed December 17, 1997 (now U.S. Patent No. 6,076,152). The present invention is related to the subject matter of U.S. Patent No. 6,339,819 issued January 15, 1992 for: "Multiprocessor with Each Processor Element Accessing Operands in Loaded Input Buffer and Forwarding Results to FIFO Output Buffer". The foregoing patent application and issued patents are assigned to SRC Computers, Inc., assignee of the present invention, the disclosures of which are herein specifically incorporated in their entirety by this reference.

BACKGROUND OF THE INVENTION

The present invention relates, in general, to the field of computer systems and techniques for interconnecting various processing or computing elements. More particularly, the present invention relates to a hybrid computer system architecture and memory controller for close-coupling within a hybrid computing system using an adaptive processor interface port.

Hybrid computer systems are those that incorporate both standard microprocessors and adaptive processors. These are typically large multiprocessor server-type systems that reside on a shared network and are not directly operated with a user interface console. The overall performance and flexibility of such systems is directly proportional to the level of coupling between the microprocessors and the adaptive processors. That is to say, if

the two processor types are treated as peers and have equal bandwidths and latencies to a shared memory, the system performance will be maximized.

To date, there have been several accepted methodologies for coupling the two forms of processors. The most basic of which was to connect the adaptive processor via the standard input/output ("I/O") ports to the microprocessor. This is relatively simple in practice but provides only a very loose coupling with low bandwidths and high latencies relative to the bandwidths and latencies of the processor bus. Since both types of processors must share the same memory, this leads to significantly reduced performance in the adaptive processors. This technique also limits the amount of processor interaction that can realistically occur.

The second typical method of interconnection is to place the adaptive processor in the memory space of the microprocessor such as disclosed in certain specific embodiments disclosed in the aforementioned patents and patent applications. This connection yields a much tighter coupling as well as bandwidths and latencies typically equal to the microprocessor bus. However, particularly for small transfers, there may be more overhead associated with this connection than is desired. This is due to the "slaved" nature of the standard memory subsystem in a personal computer environment.

The third known method is to place the adaptive processor directly on the microprocessor bus or primary microprocessor interconnect (e.g. the Front Side Bus "FSB"). This method would seem to insure that the adaptive processor will have the same bandwidth and latency to the rest of the system as the microprocessors. However, in reality, this may not be true. In the case of Intel® microprocessors, a foreign device such as the adaptive processor, may be subject to special treatment and is classified as a third party agent. As such, it may not be able to use many features of the bus such as those associated with movement of cached data or data movement to I/O devices. It may also be the case that the adaptive processor is itself a whole circuit board and connection of it to the microprocessor may violate the bus layout ground rules. In addition, the adaptive processor would also have to participate in all of the microprocessor bus protocol, such as correctly

responding to cache coherency related transactions, even though it may not be a coherent bus agent.

SUMMARY OF THE INVENTION

There is however a way to accomplish the desired coupling while eliminating issues associated with residing on the microprocessor bus. This is through the use of a dedicated adaptive processor interface port ("APIP") added to, or in conjunction with, the memory and I/O controller chip of the core logic, typically called the "North Bridge", on Intel® based processor boards today. Memory accesses to and from this port as well as the main microprocessor bus, are then arbitrated by the circuitry inside the memory controller. In this fashion, both the microprocessors and the adaptive processors exhibit equal memory bandwidth and latency. In addition, because it is a separate electrical port from the microprocessor bus, the APIP is not required to comply with, and participate in, all FSB protocol. This results in reduced protocol overhead which results higher yielded payload on the interface.

To accelerate data movement to the adaptive processor, it is also possible to include a Direct Memory Access ("DMA") engine inside the North Bridge. This would allow the adaptive processor to issue a single "read" request over the APIP that would result in the DMA engine actually retrieving and transmitting a large data block to the adaptive processor. This DMA engine can handle both a "read" and "write" request simultaneously to allow streaming operations to occur as efficiently as possible within the adaptive processor.

To allow very large systems to be constructed, this port can be provided with enough drive capability to allow it to be connected to an external interconnect such as a large crossbar switch. In this fashion, many of the adaptive processors and microprocessors can work in a randomly interconnected way to solve problems. Due to the potential for any given port of the switch to be busy at any point in time, it may be desirable for the outbound path of the APIP to be equipped with a small buffer to allow the

completion of "read" memory accesses that may be underway when the path goes busy without the loss of data. As soon as the path is free, the buffer can be drained and transmitted and the current DMA resumed. One way to indicate a busy path could be communicated through the use of a "busy" signal sent from the busy receiver port to the transmitter to which it is connected. Consequently, the APIP will stop transmission when it receives a "busy" signal and will generate a separate "busy" signal when it can no longer receive data for whatever reason.

To aid in control of the adaptive processor as well as in direct communication between the adaptive processor and the microprocessor, a series of preferably 64 bit registers should be included in the memory controller. These registers could then be made accessible from either the microprocessor or the adaptive processor.

Typically there is a need for processors to interrupt each other in a large system. The same is true when dealing with a hybrid system. Therefore, the APIP can be provided with the ability to accept inter-processor interrupts from the microprocessor and send them to other processors in the system as well as performing the reverse function and receive inter-processor interrupts. This port could be similar in physical appearance to an AGP graphics port. In fact, since the accelerated graphics port ("AGP") is typically not used on servers due to the absence of monitors, it would actually be possible to use the same device pins on the memory controller and use a register to allow the port to be configured as either AGP or APIP.

Particularly disclosed herein is a computer system which comprises at least one microprocessor presenting a first bus, a memory controller coupled to the first bus and also coupled to a memory bus and an adaptive processor port, a memory block coupled to the memory bus and an adaptive processor coupled to the adaptive processor port.

Further disclosed herein is a hybrid computing system comprising at least one microprocessor, a memory block, a memory controller coupled to the microprocessor and the memory block for controlling accesses to the memory

block by the at least one microprocessor and at least one adaptive processor coupled to the memory controller with the memory controller further controlling accesses to the memory block by the at least one adaptive processor.

Still further disclosed herein is a computing system comprising first and second processing elements, a memory block and a memory controller coupled to the first processing element through a first bus and the second processing element through a second bus with the memory controller controlling accesses to the memory block by the first and second processing elements.

Also disclosed herein is a memory controller for a computing system comprising a memory bus arbitrator coupled between first and second processing elements and a memory block with the memory bus arbitrator controlling access to the memory block by the first and second processing elements.

BRIEF DESCRIPTION OF THE DRAWINGS

The aforementioned and other features and objects of the present invention and the manner of attaining them will become more apparent and the invention itself will be best understood by reference to the following description of a preferred embodiment taken in conjunction with the accompanying drawings, wherein:

Fig. 1 is a high-level functional block diagram of a typical computing system, for example, a personal computer ("PC") implemented in conjunction with a memory and input/output ("I/O") controller ("North Bridge") and a peripheral component interconnect ("PCI") bus I/O controller ("South Bridge");

Fig. 2 is a functional block diagram of a typical I/O connected hybrid computing system comprising a number of microprocessors and adaptive processors, with the latter being coupled to an I/O bridge;

Fig. 3 is a functional block diagram of a typical memory connected hybrid computing system comprising a number of microprocessors and adaptive processors, with the latter being coupled to the system memory;

Fig. 4 is a functional block diagram of a typical Front Side Bus ("FSB") connected hybrid computing system comprising a number of microprocessors and adaptive processors, with the latter being coupled directly to the FSB;

Fig. 5 is a corresponding functional block diagram of an adaptive processor interface port ("APIP") connected hybrid computing system in accordance with the present invention comprising a number of microprocessors and adaptive processors, with the latter being coupled directly to a memory and I/O controller;

Fig. 6 is a functional block diagram of a memory and I/O controller implementing an APIP interface for use with an adaptive processor;

Fig. 7 is a functional block diagram of a multi-adaptive processor (MAP™, a trademark of SRC Computers, Inc.) for possible use as an adaptive processor in a hybrid computing system in accordance with the present invention; and

Fig. 8 is a functional block diagram of a portion of an adaptive processor interface port connected hybrid computing system in accordance with another embodiment of the present invention wherein the functions of the memory and I/O controller have been incorporated into the microprocessor itself.

DESCRIPTION OF A REPRESENTATIVE EMBODIMENT

With reference now to Fig. 1, a high-level functional block diagram of a typical computing system 100 is shown. The computing system 100 may be, for example, a personal computer ("PC") which incorporates a commercially available integrated circuit ("IC") memory controller ("North Bridge") 102 such as the P4X333/P4X400 devices available from VIA Technologies, Inc.; the M1647 device available from Acer Labs, Inc. and the 824430X device available from Intel Corporation. The North Bridge IC 102 is coupled by means of a Front Side Bus ("FSB") to a processor 104 such as one of the Pentium® series of processors also available from Intel Corporation.

The North Bridge IC 102 is coupled via a separate memory bus to system memory 106 which may comprise, for example, a number of

synchronous dynamic random access ("SDRAM") memory modules. A dedicated accelerated graphics port ("AGP") is provided for interfacing the system 100 to a graphics accelerator while an inter-bridge bus couples the North Bridge IC 102 to an additional input/output I/O controller IC ("South Bridge") 108. The South Bridge IC may be, for example, an SLC90E66 device available form Standard Microsystems, Corporation or the VT8235 device available from VIA Technologies.

The South Bridge IC 108 couples the system 100 to a peripheral component interconnect ("PCI") bus for interfacing to a number of dedicated PCI slots 110. Interconnections with a universal serial bus ("USB"), system management ("SM") bus and general purpose ("GP") I/O bus are also provided as well as to an industry standard architecture/extended I/O ("ISA/EIO") bus to a basic input/output system ("BIOS") block 112 and a system controller 114 which controls a number of the various components of the system 100.

With reference additionally now to Fig. 2, a functional block diagram of a typical I/O connected hybrid computing system 200 is shown. The hybrid computing system 200 comprises one or more North Bridge ICs 202_0 through 202_N, each of which is coupled to four microprocessors 204_{00} through 204_{03} through and including 204_{N0} through 204_{N3} by means of a Front Side Bus. The North Bridge ICs 202_0 through 202_N are coupled to respective blocks of memory 206_0 through 206_N as well as to a corresponding I/O bridge element 208_0 through 208_N. A network interface card ("NIC") 212_0 through 212_N couples the I/O bus of the respective I/O bridge 208_0 through 208_N to a cluster bus coupled to a common clustering hub (or Ethernet Switch) 214.

As shown, an adaptive processor element 210_0 through 210_N is coupled to, and associated with, each of the I/O bridges 208_0 through 208_N. This is the most basic of the existing approaches for connecting an adaptive processor 210 in a hybrid computing system 200 and is implemented, essentially via the standard I/O ports to the microprocessor(s) 204. While relatively simple to implement, it results in a very "loose" coupling between the adaptive processor 210 and the microprocessor(s) 204 with resultant low bandwidths and high latencies relative to the bandwidths and latencies of the

processor bus. Moreover, since both types of processors 204, 210 must share the same memory 206, this leads to significantly reduced performance in the adaptive processors 210. Functionally, this architecture effectively limits the amount of interaction between the microprocessor(s) 204 and the adaptive processor 210 that can realistically occur.

With reference additionally now to Fig. 3, a functional block diagram of a typical memory connected hybrid computing system 300 is shown. The hybrid computing system 300 also comprises a number of North Bridge ICs 202_0 through 202_N, each of which is coupled to four microprocessors 204_{00} through 204_{03} through and including 204_{N0} through 204_{N3} by means of a Front Side Bus. The North Bridge ICs 202_0 through 202_N are coupled to respective blocks of memory 206_0 through 206_N as well as to a corresponding I/O bridge element 208_0 through 208_N. A network interface card ("NIC") 212_0 through 212_N couples the I/O bus of the respective I/O bridge 208_0 through 208_N to a cluster bus coupled to a common clustering hub (or Ethernet Switch) 214.

As shown, an adaptive processor element 310_0 through 310_N is coupled to, and associated with, each of the blocks of memory 206_0 through 206_N. In this particular computing system 300 architecture, the adaptive processor 310 is effectively placed in the memory 206 space of the microprocessor(s) 204 in a manner as disclosed in certain of the afore-mentioned patents. The architecture of the computing system 200 shown yields a much tighter coupling between the microprocessor(s) 204 and the adaptive processor 310 than that of the computing system 200 of the preceding figure as well as providing bandwidths and latencies typically equal to the microprocessor bus itself. Nevertheless, particularly for small transfers, there may be more overhead associated with this type of interconnection than is desired due to the effectively "slaved" nature of the standard memory subsystem in a personal computing environment.

With reference additionally now to Fig. 4, a functional block diagram of a typical Front Side Bus ("FSB") connected hybrid computing system 400 is shown. The hybrid computing system 400 again comprises a number of North Bridge ICs 202_0 through 202_N, each of which is coupled to four

microprocessors 204_{00} through 204_{03} through and including 204_{N0} through 204_{N3} by means of a Front Side Bus. The North Bridge ICs 202_0 through 202_N are coupled to respective blocks of memory 206_0 through 206_N as well as to a corresponding I/O bridge element 208_0 through 208_N. A network interface card ("NIC") 212_0 through 212_N couples the I/O bus of the respective I/O bridge 208_0 through 208_N to a cluster bus coupled to a common clustering hub (or Ethernet Switch) 214.

As shown, an adaptive processor element 210_0 through 210_N is coupled to, and associated with, each of the Front Side Buses coupled to the microprocessors 204_{00} through 204_{03} through and including 204_{N0} through 204_{N3}. In this particular architecture, the adaptive processor 410 is placed directly on the microprocessor 204 bus or Front Side Bus. This interconnection scheme would seem to insure that the adaptive processor 410 will have the same bandwidth and latency to the rest of the computing system 400 as the microprocessor(s) 204. However, in reality this may not be true. In the case of Intel® microprocessors, a "foreign" device such as the adaptive processor 410, may be subject to special treatment and is classified as a "third party agent". As such, it may not be able to use many features of the Front Side Bus such as those associated with the movement of cached data or data movement to I/O devices. It may also be the case that the adaptive processor 410 is itself an entire circuit board and connection of it to the microprocessor may violate the bus layout ground rules. In addition, the adaptive processor 410 would also have to participate in all of the microprocessor 204bus protocol, such as correctly responding to cache coherency related transactions, even though it may not itself be a coherent bus agent.

With reference additionally now to Fig. 5, a corresponding functional block diagram of an adaptive processor interface port ("APIP") connected hybrid computing system 500 in accordance with the present invention. The computing system 500 comprises a number of memory and I/O controllers 502_0 through 502_N, each of which is coupled to four microprocessors 204_{00} through 204_{03} through and including 204_{N0} through 204_{N3} by means of a Front Side Bus. The memory and I/O controllers 502_0 through 502_N are coupled to

respective blocks of memory 206_0 through 206_N as well as to a corresponding I/O bridge element 208_0 through 208_N. A network interface card ("NIC") 212_0 through 212_N couples the I/O bus of the respective I/O bridge 208_0 through 208_N to a cluster bus coupled to a common clustering hub (or Ethernet Switch) 214.

As shown, an adaptive processor element 510_0 through 510_N is coupled to, and associated with, each of the memory and I/O controllers 502_0 through 502_N through an adaptive processor interface port ("APIP") thereby improving the computing system 500 performance and eliminating the disadvantages of the foregoing conventional techniques. In other implementations of the present invention, one or more of the adaptive processor(s) 510 may be replaced with a conventional microprocessor coupled to the APIP interface.

In a preferred embodiment as disclosed herein, this may be effectuated through the use of a dedicated adaptive processor interface port added to, or associated with, the memory and I/O controller 502 (such as a North Bridge chip). Memory accesses to and from this APIP port, as well as those to and from the main microprocessor 204 bus (e.g. the Front Side Bus), are then arbitrated by the memory control circuitry inside the memory and I/O controller 502. In this fashion, both the microprocessor(s) 204 and the adaptive processor(s) 510 would have equal memory bandwidth and latency. In addition, because it is a separate electrical port from that of the microprocessor bus, the APIP is not required to comply with, and participate in, all FSB protocols. This results in reduced protocol overhead which, in turn, results in a higher yielded payload on the interface.

With reference additionally now to Fig. 6, a functional block diagram of the memory and I/O controller 502 implementing an APIP interface of the preceding figure is shown. The memory and I/O controller 502 includes an FSB interface 512 controlled by a memory bus arbitrator 514 for responding to high priority requests to/from the microprocessors 204_{00} through 204_{03} through and including 204_{N0} through 204_{N3}. The memory bus arbitrator 514 also controls a memory interface 516 for providing access to the blocks of

memory 206_0 through 206_N. Low priority requests through the I/O bridge elements 208_0 through 208_N are made through an inter-bridge interface 518 as controlled by the memory bus arbitrator 514.

In lieu of, or in addition to, the conventional AGP bus interface, the memory and I/O controller 502 includes an APIP interface 524 as shown for interfacing and communication with an adaptive processor element 510_0 through 510_N. A direct memory access ("DMA") engine 520, in conjunction with a read request buffer 522 for "reads" handles high priority requests to and from the memory bus arbitrator 514 and the APIP interface 524 over, for example, separate "write data" and "read data" buses. The APIP interface 524 may, in an exemplary embodiment, include the provision of a "busy" signal from the APIP interface to the DMA engine 520. Further, a number of control registers 526 may also be provided coupling the FSB interface 512 to the APIP interface 524.

In operation, the DMA engine 520 can serve to accelerate data movement to the adaptive processor 510 through the memory and I/O controller 502. This functionality allows the adaptive processor(s) 510 to issue a single "read" request over the APIP interface 524 that would result in the DMA engine 520 actually retrieving and transmitting a large data block to the adaptive processor 510. The DMA engine 520 can handle both a "read" and "write" request simultaneously in order to allow streaming operations to occur as efficiently as possible within the adaptive processor 510.

To allow very large computing systems 500 to constructed, the APIP interface 524 can be provided with sufficient drive capability to allow it to be connected to an external interconnect, for example, a large crossbar switch. In this fashion, many of the adaptive processor(s) 510 and microprocessor(s) 204 can work in a randomly interconnected way to solve problems. Due to the potential for any given port of the switch to be busy at any point in time, it may be desirable for the outbound path of the APIP interface 524 to be equipped with a small buffer (e.g. read request buffer 522) to allow the completion of "read" memory accesses that may be underway when the path goes "busy" without the loss of data. As soon as the path is free, the buffer

522 can be drained and transmitted and the current DMA operation resumed. One way to indicate a busy path could be communicated through the use of a "busy" signal sent from the busy receiver port to the transmitter to which it is connected. Consequently, the APIP interface 524 will stop transmission when it receives a "busy" signal and will generate a separate "busy" signal when it can no longer receive data for whatever reason.

To aid in control of the adaptive processor 510 as well as in direct communication between the adaptive processor(s) 510 and the microprocessor(s) 204, a series of, for example, 64 bit control registers 526 may be included as a portion of the memory and I/O controller 502. These registers 526 would be ideally accessible from either the microprocessor(s) 204 or the adaptive processor(s) 510. Typically there is a need for processors 204 to interrupt each other in a relatively large computing system 500. The same is true when dealing with a hybrid computing system. Therefore, the APIP interface 524 can be provided with the ability to accept inter-processor 204 interrupts from the microprocessor 204 and send them to other processors 204 in the system as well as performing the reverse function and receive inter-processor 204 interrupts.

In a particular implementation, the APIP interface 524 may be similar in physical appearance to an AGP graphics port. In fact, since the accelerated graphics port ("AGP") is typically not used on servers due to the absence of monitors, it is possible to use the same pins otherwise available on a typical North Bridge device and use a register in order to enable the port to be configured as either AGP or APIP.

With reference additionally now to Fig. 7, a functional block diagram of a multi-adaptive processor element (MAP™, a trademark of SRC Computers, Inc.) for possible use as an adaptive processor element 510 is shown. The adaptive processor element 510 includes a user array 539 which may comprise one or more field programmable gate arrays ("FPGAs") as disclosed in the foregoing issued patents and pending patent application. A chain port may be provided for directly coupling two or more adaptive processor elements 510 as shown.

A control chip 532 couples the adaptive processor element 510 to the APIP interface 524 of the associated memory and I/O controller 502 and provides control functionality to the corresponding user array 530. On-board memory 534 is coupled to the control chip 532 and user array 530, for example, though six ports. Briefly, the write data and read data lines of the memory and I/O controller 502 are coupled to the control chip (or block) 532 which provides addresses to the on-board memory 534 and receives addresses from the user array 530 on a number of address lines. Data supplied on the write data line is provided by the control chip 532 to the on-board memory 534 on a number of data lines and data read out of the on-board memory 534 is provided on these same lines both to the user array 530 as well as the control chip 532 for subsequent presentation to the APIP interface 524. As indicated, a chain port may be coupled to the user array 530 for communication of read and write data directly with one or more other adaptive processors 510.

With reference additionally now to Fig. 8, a functional block diagram of a portion of an adaptive processor interface port connected hybrid computing system 800 in accordance with another embodiment of the present invention is shown. In the computing system 800, the functions of the memory and I/O controller 802 have been incorporated into the microprocessor 804 as shown. In this manner, a memory interface 516 of the memory and I/O controller 802 may be coupled to a memory block 806, an inter-bridge interface 518 may be coupled to an I/O bridge 808 and an APIP interface 524 may be coupled to an adaptive processor 810. In the computing system 800, the functionality of the memory and I/O controller 502 (Fig. 6) is maintained but, by integrating its functionality into the microprocessor 804 by the inclusion of an integral memory and I/O controller 802, the need for a separate chip or integrated circuit device is eliminated.

While there have been described above the principles of the present invention in conjunction with specific computing system architectures and components, it is to be clearly understood that the foregoing description is made only by way of example and not as a limitation to the scope of the

invention. Particularly, it is recognized that the teachings of the foregoing disclosure will suggest other modifications to those persons skilled in the relevant art. Such modifications may involve other features which are already known per se and which may be used instead of or in addition to features already described herein. Although claims have been formulated in this application to particular combinations of features, it should be understood that the scope of the disclosure herein also includes any novel feature or any novel combination of features disclosed either explicitly or implicitly or any generalization or modification thereof which would be apparent to persons skilled in the relevant art, whether or not such relates to the same invention as presently claimed in any claim and whether or not it mitigates any or all of the same technical problems as confronted by the present invention. The applicants hereby reserve the right to formulate new claims to such features and/or combinations of such features during the prosecution of the present application or of any further application derived therefrom.

What is claimed is:

CLAIMS

WE CLAIM:

1. A computer system comprising:

at least one microprocessor presenting a first bus;

a memory controller coupled to said first bus; said memory controller coupled to a memory bus and an adaptive processor port;

a memory block coupled to said memory bus; and

an adaptive processor coupled to said adaptive processor port.

2. The computer system of claim 1 wherein said computer system further comprises a plurality of microprocessors coupled to said first bus.

3. The computer system of claim 1 wherein said memory controller further comprises:

a second bus coupled to a computer system clustering hub.

4. The computer system of claim 3 further comprising:

at least one additional memory controller coupled to said clustering hub through another second bus and further coupled to at least one other microprocessor through another first bus.

5. The computer system of claim 4 further comprising

another memory block coupled to said at least one additional memory controller through another memory bus.

6. The computer system of claim 4 further comprising:

at least one additional adaptive processor coupled to another adaptive processor port of said at least one additional memory controller.

7. The computer system of claim 1 wherein said adaptive processor port is alternatively configurable as a graphics port.

8. The computer system of claim 1 wherein said first bus comprises a Front Side Bus.

9. The computer system of claim 1 wherein said adaptive processor comprises:

a control element coupled to said adaptive processor port;

a user array coupled to said control element; and

a memory element coupled to said control element and said user array.

10. The computer system of claim 9 wherein said user array further comprises:

a chain port for coupling said adaptive processor element to a second adaptive processor element.

11. The computer system of claim 9 wherein said user array comprises a field programmable gate array.

12. The computer system of claim 1 wherein said memory controller comprises:

a memory bus arbitrator;

a first bus interface associated with said memory bus arbitrator for controlling memory access requests received on said first bus;

a memory bus interface associated with said memory bus arbitrator for controlling access to said memory block; and

an adaptive processor port interface associated with said memory bus arbitrator for controlling memory access requests received on said adaptive processor port.

13. The computer system of claim 12 further comprising:

a direct memory access engine coupling said memory bus arbitrator and said adaptive processor port interface.

14. The computer system of claim 13 wherein said direct memory access engine is coupled to said adaptive processor port interface by means of respective read and write data lines.

15. The computer system of claim 13 further comprising:

a read request buffer associated with said direct memory access engine.

16. The computer system of claim 13 further comprising a busy signal line coupling said adaptive processor port interface and said direct memory access engine.

17. The computer system of claim 12 further comprising:

at least one control register in communication between said first bus interface and said adaptive processor port interface.

18. The computer system of claim 12 further comprising:

a second bus interface associated with said memory bus arbitrator.

19. The computer system of claim 1 wherein said memory controller comprises an integrated circuit device.

20. The computer system of claim 1 wherein said at least one microprocessor comprises said memory controller.

21. A hybrid computing system comprising:

at least one microprocessor;

a memory block;

a memory controller coupled to said microprocessor and said memory block for controlling accesses to said memory block by said at least one microprocessor; and

at least one adaptive processor coupled to said memory controller, said memory controller further controlling accesses to said memory block by said at least one adaptive processor.

22. The hybrid computing system of claim 21 wherein said memory controller comprises:

a memory bus arbitrator;

a first bus interface associated with said memory bus arbitrator for controlling memory access requests received from said at least one microprocessor;

a memory bus interface associated with said memory bus arbitrator for controlling access to said memory block; and

an adaptive processor port interface associated with said memory bus arbitrator for controlling memory access requests received from said at least one adaptive processor.

23. The hybrid computing system of claim 22 further comprising:

a direct memory access engine coupling said memory bus arbitrator and said adaptive processor port interface.

24. The hybrid computing system of claim 23 wherein said direct memory access engine is coupled to said adaptive processor port interface by means of respective read and write data lines.

25. The hybrid computing system of claim 23 further comprising:

a read request buffer associated with said direct memory access engine.

26. The hybrid computing system of claim 23 further comprising a busy signal line coupling said adaptive processor port interface and said direct memory access engine.

27. The hybrid computing system of claim 22 further comprising:

at least one control register in communication between said first bus interface and said adaptive processor port interface.

28. The hybrid computing system of claim 22 further comprising:

a second bus interface associated with said memory bus arbitrator.

29. The hybrid computing system of claim 21 wherein said memory controller comprises an integrated circuit device.

30. The hybrid computing system of claim 21 wherein said at least one microprocessor comprises said memory controller.

31. A computing system comprising:

first and second processing elements;

a memory block; and

a memory controller coupled to said first processing element through a first bus and said second processing element through a second bus, said memory controller for controlling accesses to said memory block by said first and second processing elements.

32. The computing system of claim 31 wherein said first processing element comprises a microprocessor.

33. The computing system of claim 32 wherein said second processing element comprises a microprocessor.

34. The computing system of claim 32 wherein said second processing element comprises an adaptive processor.

35. The computing system of claim 31 comprising:

a memory bus arbitrator;

a first bus interface associated with said memory bus arbitrator for controlling memory access requests received from said first processing element;

a memory bus interface associated with said memory bus arbitrator for controlling access to said memory block; and

a second bus interface associated with said memory bus arbitrator for controlling memory access requests received from said second processing element.

36. The computing system of claim 35 further comprising:

a direct memory access engine coupling said memory bus arbitrator and said second bus interface.

37. The computing system of claim 35 wherein said direct memory access engine is coupled to said second bus interface by means of respective read and write data lines.

38. The computing system of claim 35 further comprising:

a read request buffer associated with said direct memory access engine.

39. The computing system of claim 35 further comprising a busy signal line coupling said second bus interface and said direct memory access engine.

40. The computing system of claim 31 further comprising:

at least one control register in communication between said first bus interface and said second bus interface.

41. The computing system of claim 30 further comprising:

a third bus interface associated with said memory bus arbitrator.

42. The computing system of claim 31 wherein said memory controller comprises an integrated circuit device.

43. The computing system of claim 31 wherein said memory controller is integrated into said first processing element.

44. A memory controller for a computing system comprising:

a memory bus arbitrator coupled between first and second processing elements and a memory block, said memory bus arbitrator controlling access to said memory block by said first and second processing elements.

45. The memory controller of claim 44 wherein said first processing element comprises a microprocessor.

46. The memory controller of claim 44 wherein said first processing element comprises an adaptive processor.

47. The memory controller of claim 45 wherein said second processing element comprises a microprocessor.

48. The memory controller of claim 45 wherein said second processing element comprises an adaptive processor.

49. The memory controller of claim 44 wherein said memory controller allows interrupts to be exchanged between said first and second processing elements.

50. The memory controller of claim 44 further comprising:

at least one register accessible by both said first and second processing elements.

51. The memory controller of claim 44 further comprising a first port interface coupling said memory bus arbitrator to said first processing element and a second port interface coupling said memory bus arbitrator to said second processing element.

52. The memory controller of claim 51 wherein said second port interface is alternatively adaptable as a graphics port interface.

53. The memory controller of claim 51 further comprising:

a direct memory access engine associated with said second port interface.

54. The memory controller of claim 53 wherein said second port interface is capable of asserting a busy signal to said direct memory access engine.

55. The memory controller of claim 44 wherein said memory bus arbitrator forms a portion of a microprocessor.

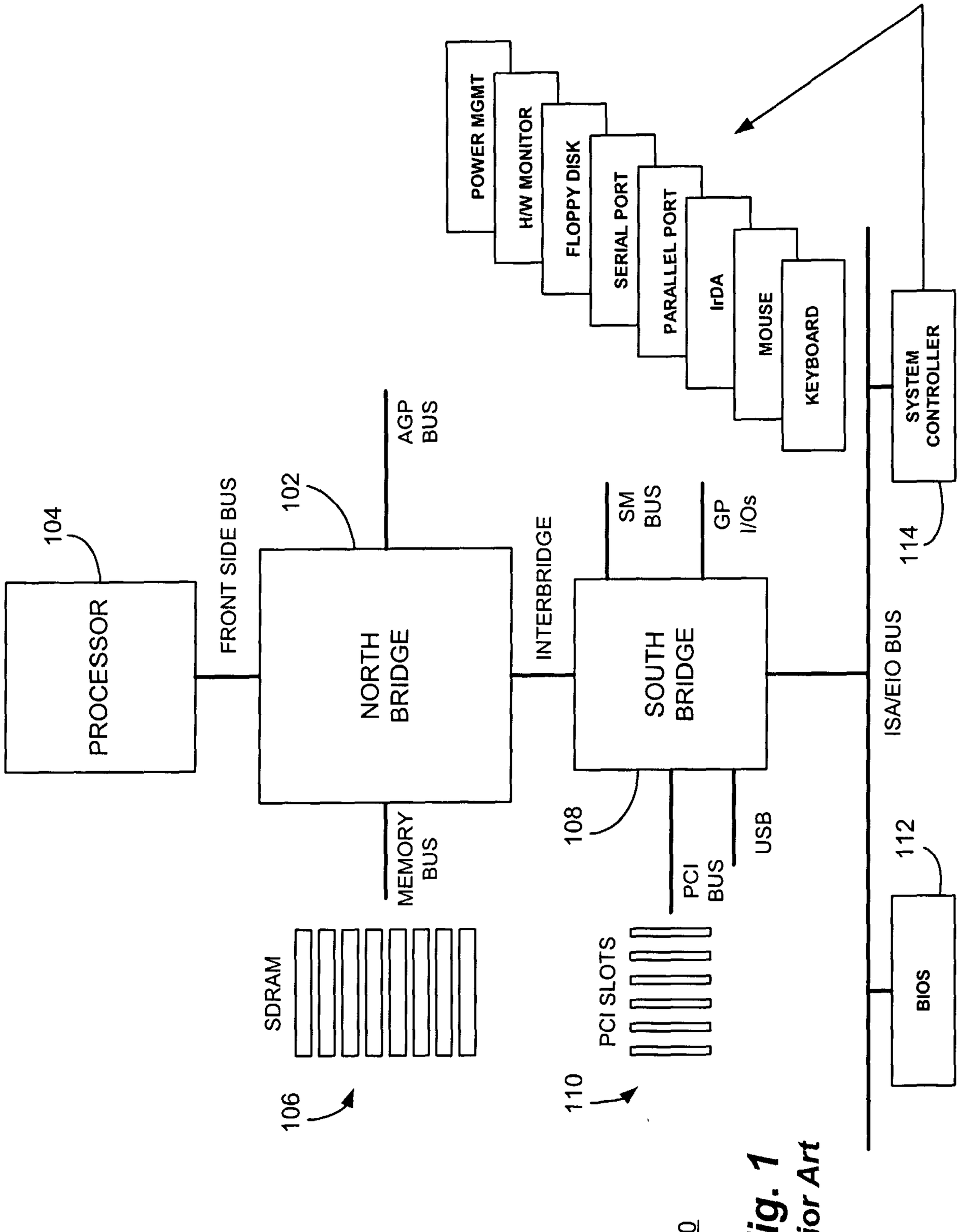


Fig. 1
Prior Art

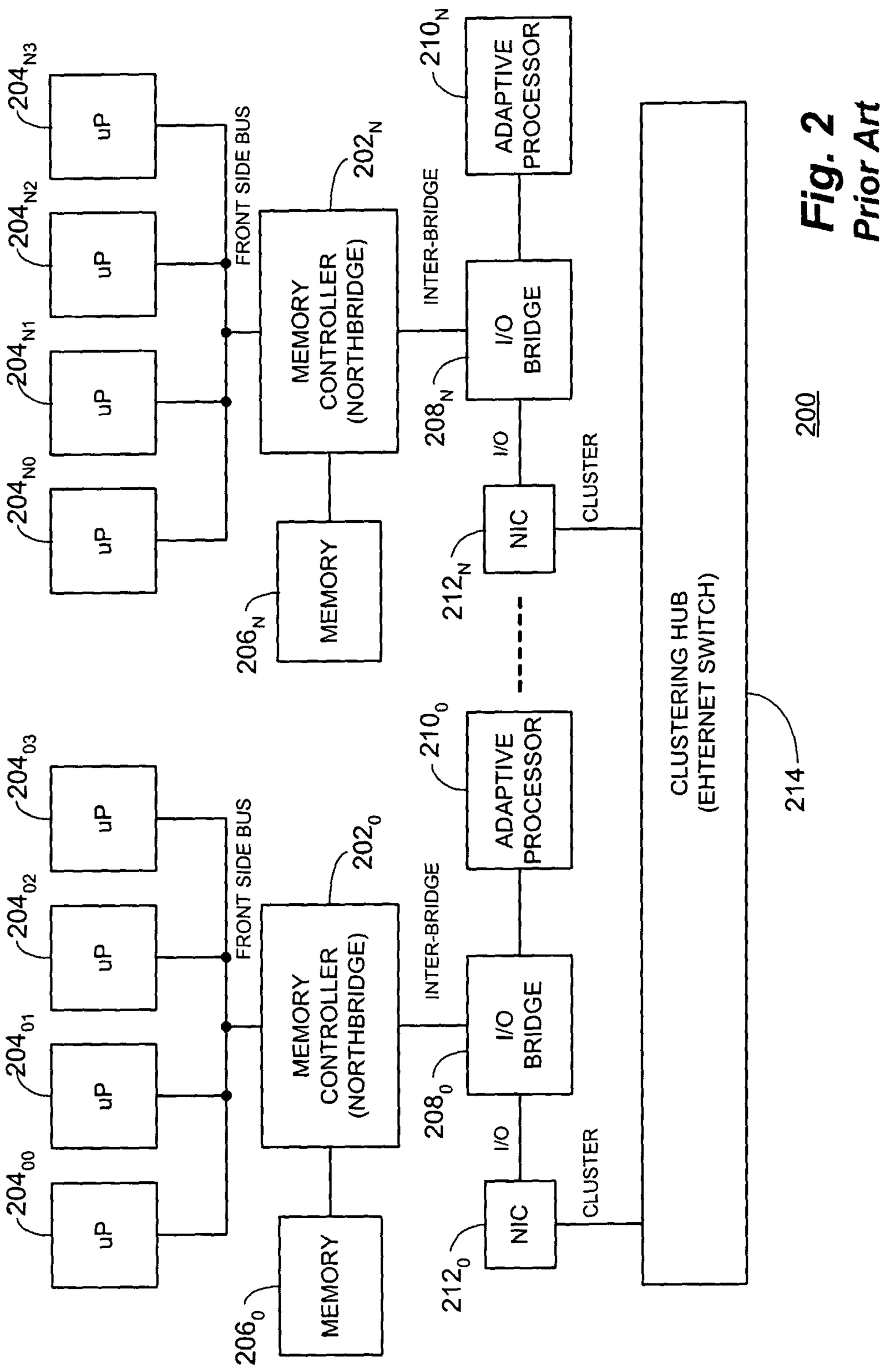
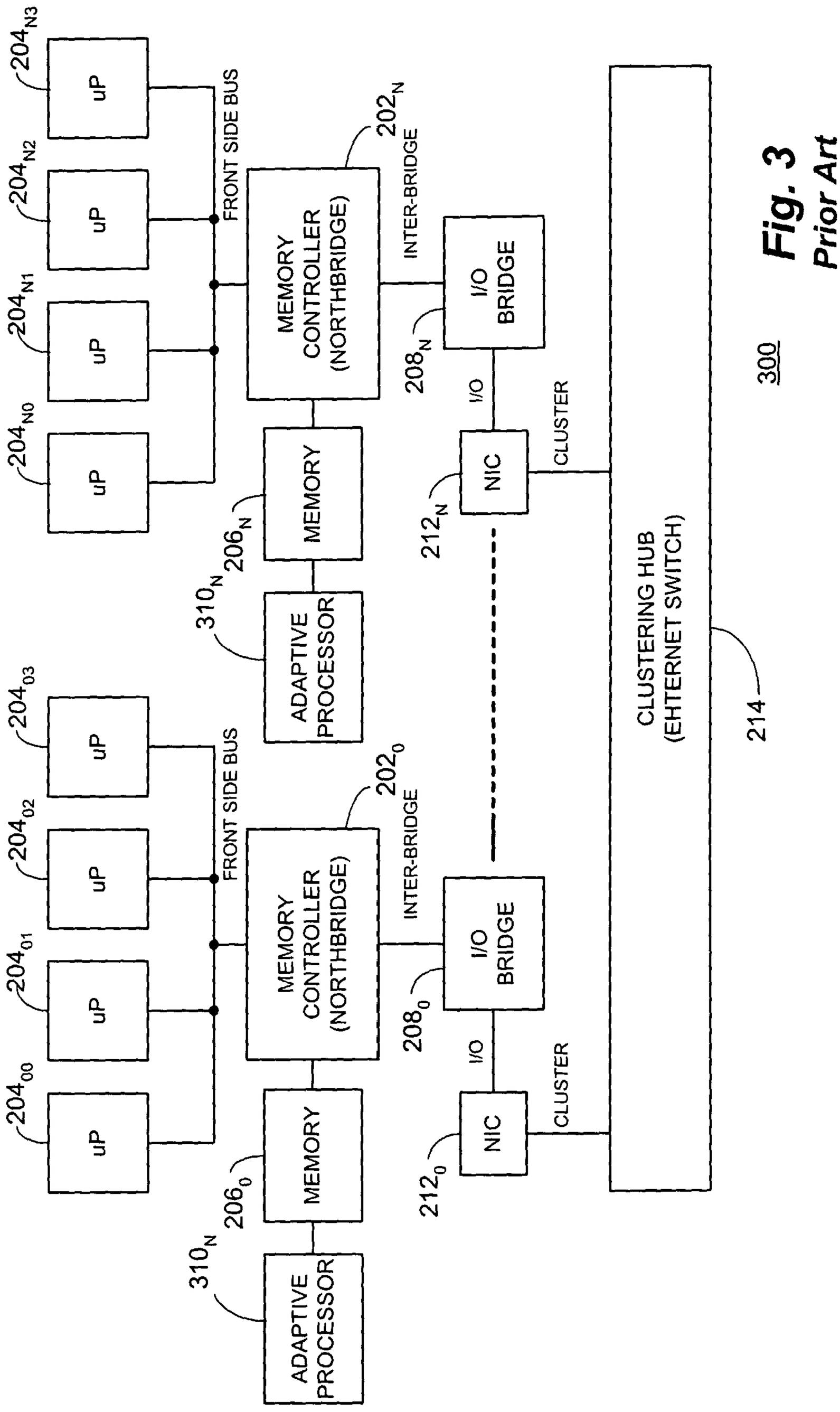


Fig. 2
Prior Art



300

Fig. 3
Prior Art

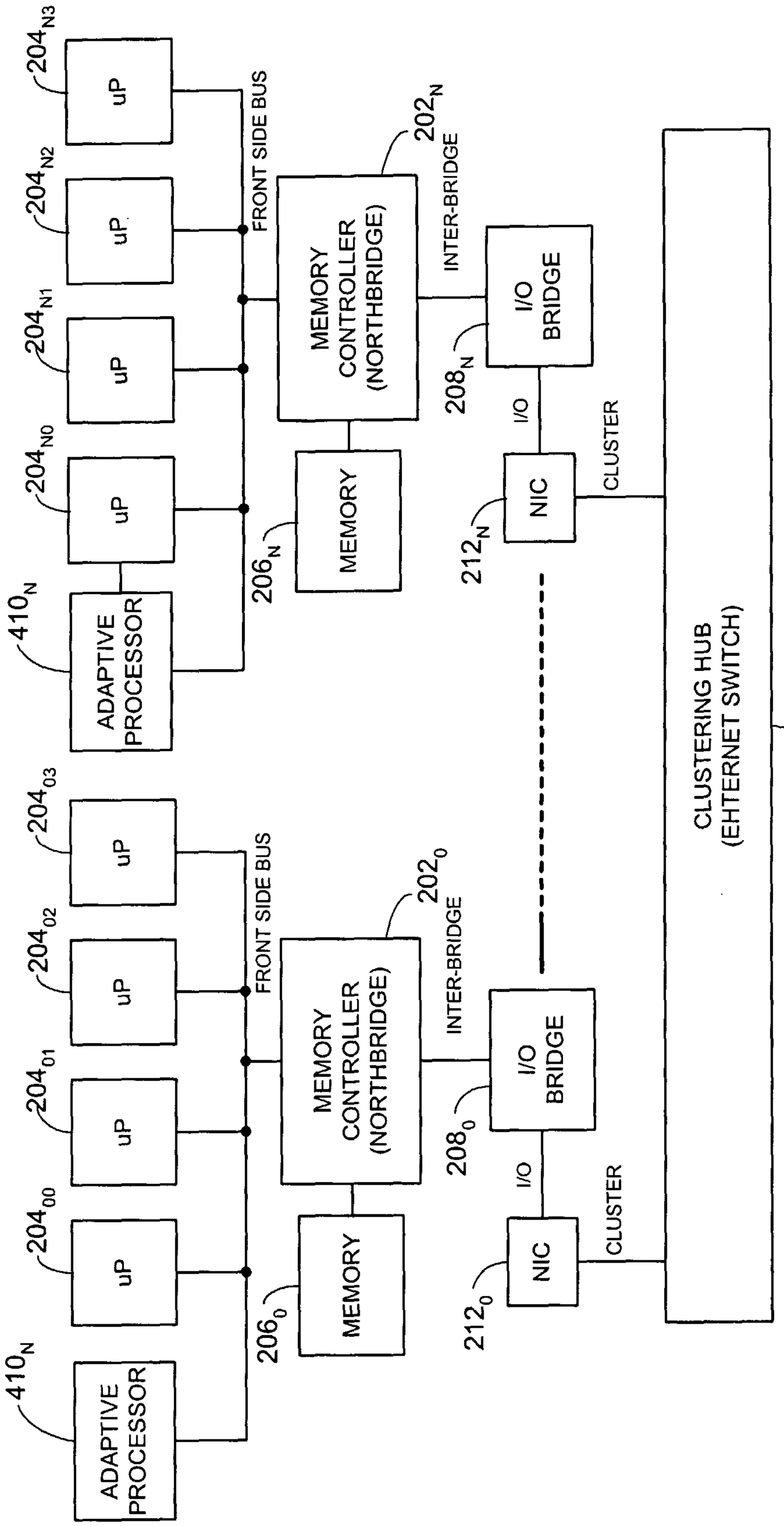
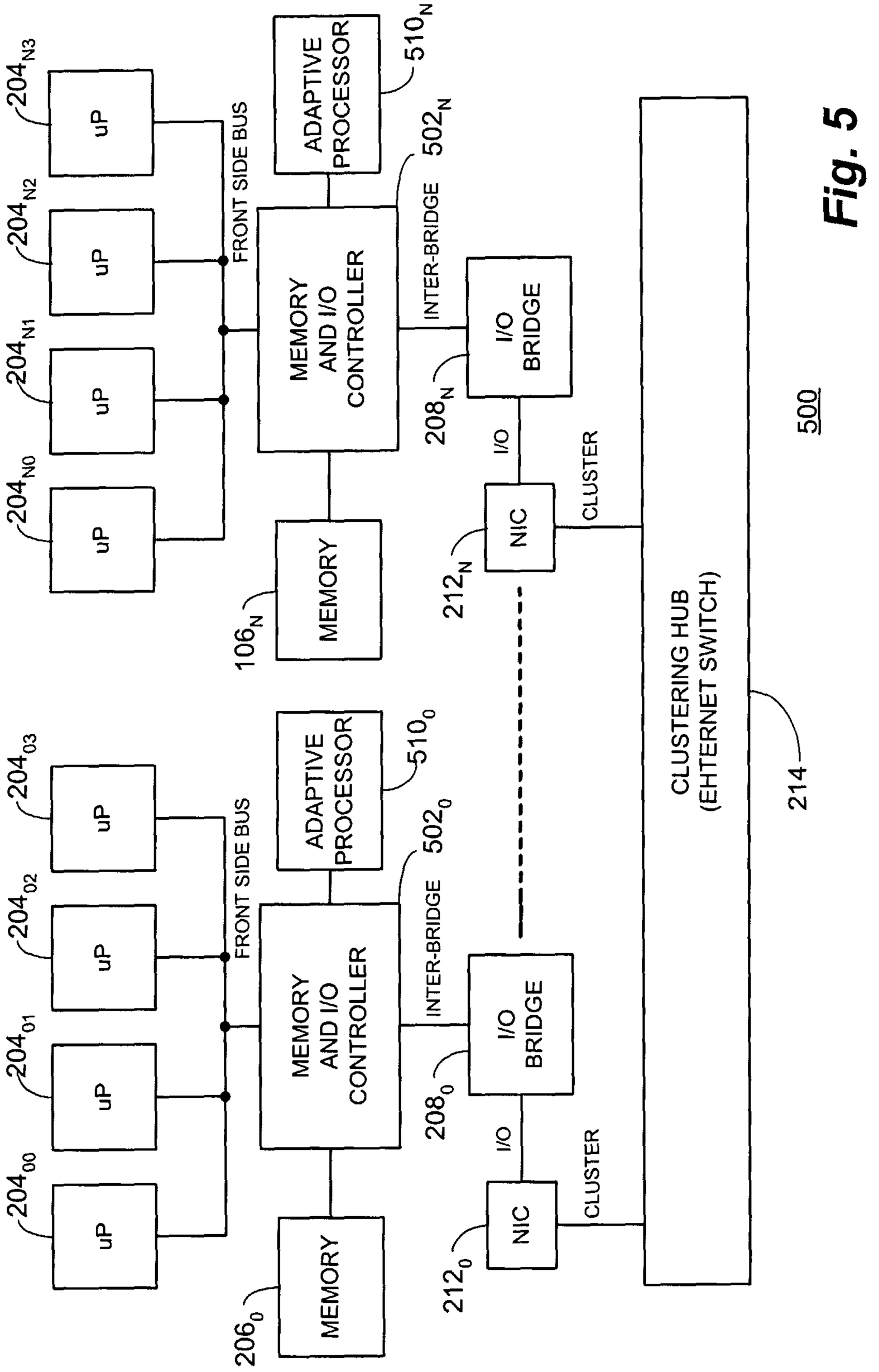


Fig. 4
Prior Art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204N2
204N1
204N0
uP
FRONT SIDE BUS
MEMORY AND I/O CONTROLLER
106N
MEMORY
ADAPTIVE PROCESSOR
510N
502N
INTER-BRIDGE
I/O BRIDGE
208N
I/O
NIC
212N
CLUSTER
CLUSTERING HUB
(EHTERNET SWITCH)
214
500
204 03
204 02
204 01
204 00
206 0
510 0
502 0
208 0
212 0

Fig. 5

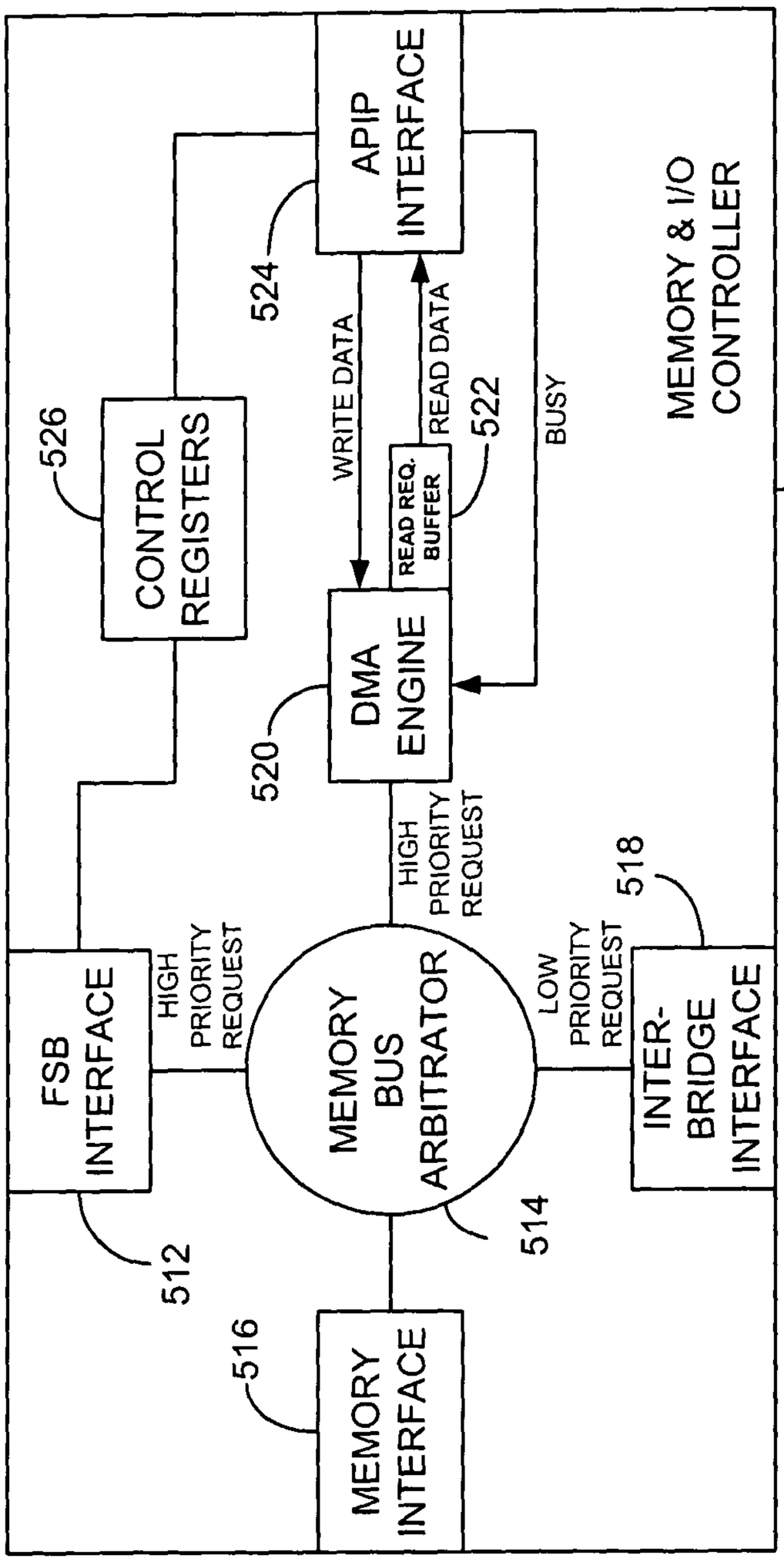

MEMORY & I/O CONTROLLER
502
APIP INTERFACE
524
WRITE DATA
READ DATA
READ REQ. BUFFER
522
BUSY
CONTROL REGISTERS
526
DMA ENGINE
520
HIGH PRIORITY REQUEST
FSB INTERFACE
HIGH PRIORITY REQUEST
MEMORY BUS ARBITRATOR
LOW PRIORITY REQUEST
INTER-BRIDGE INTERFACE
518
512
514
516
MEMORY INTERFACE

Fig. 6

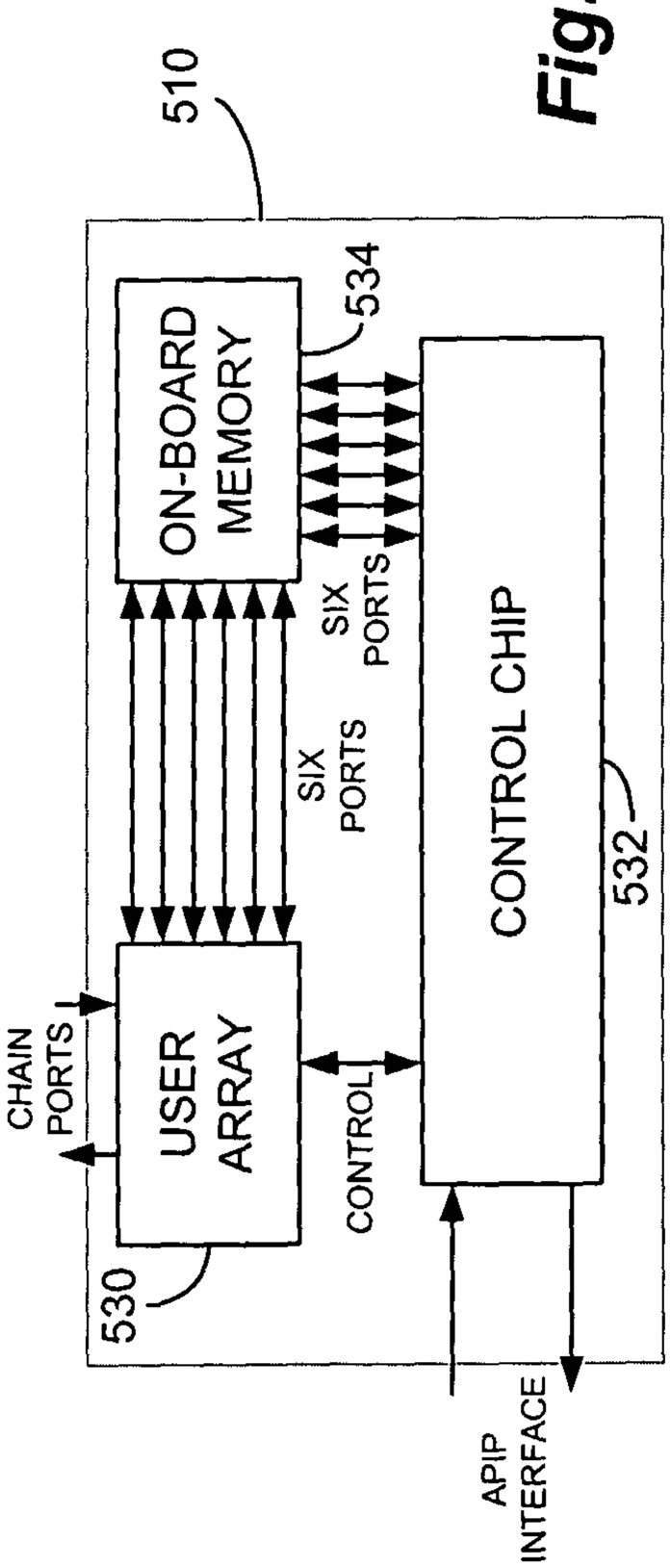
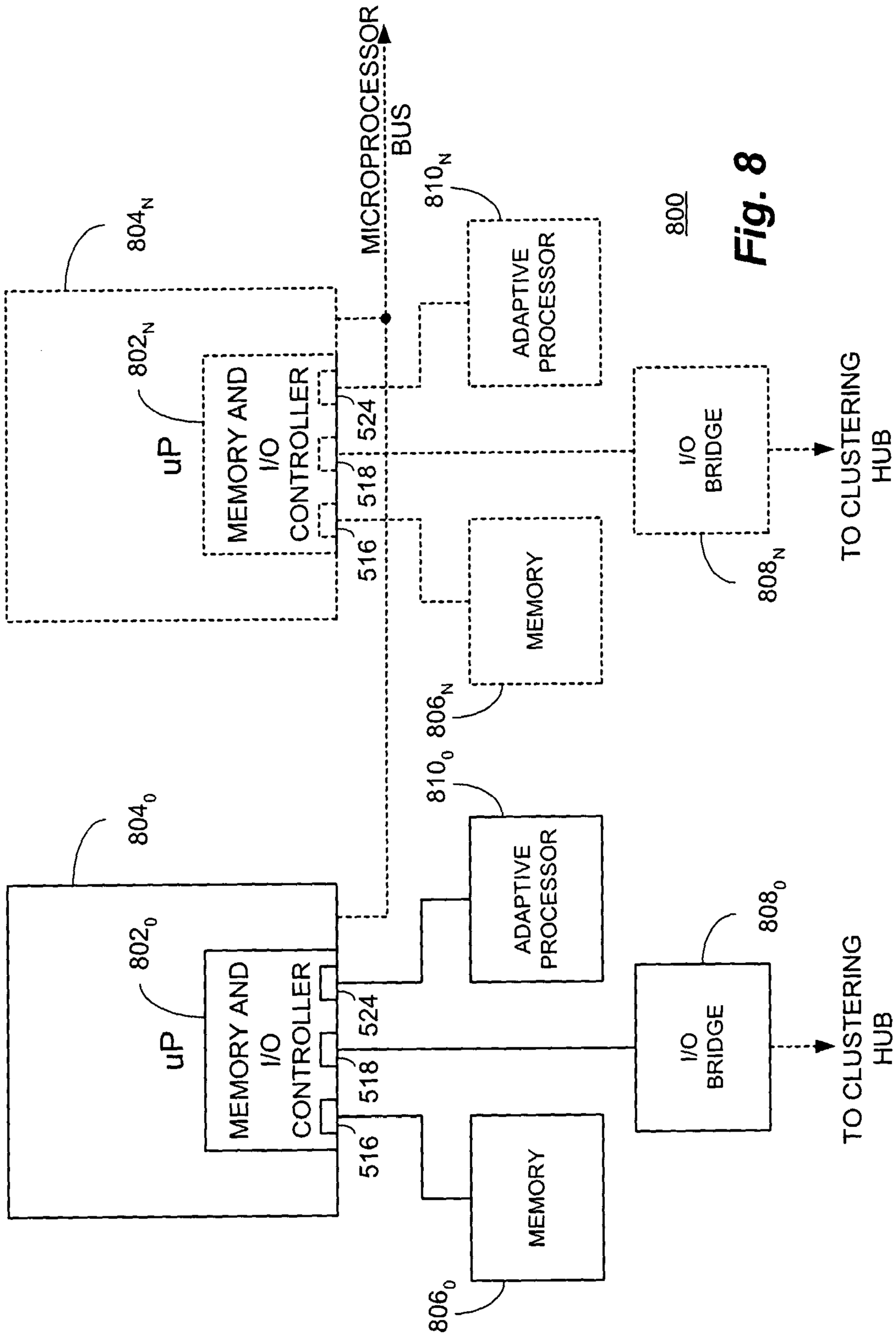
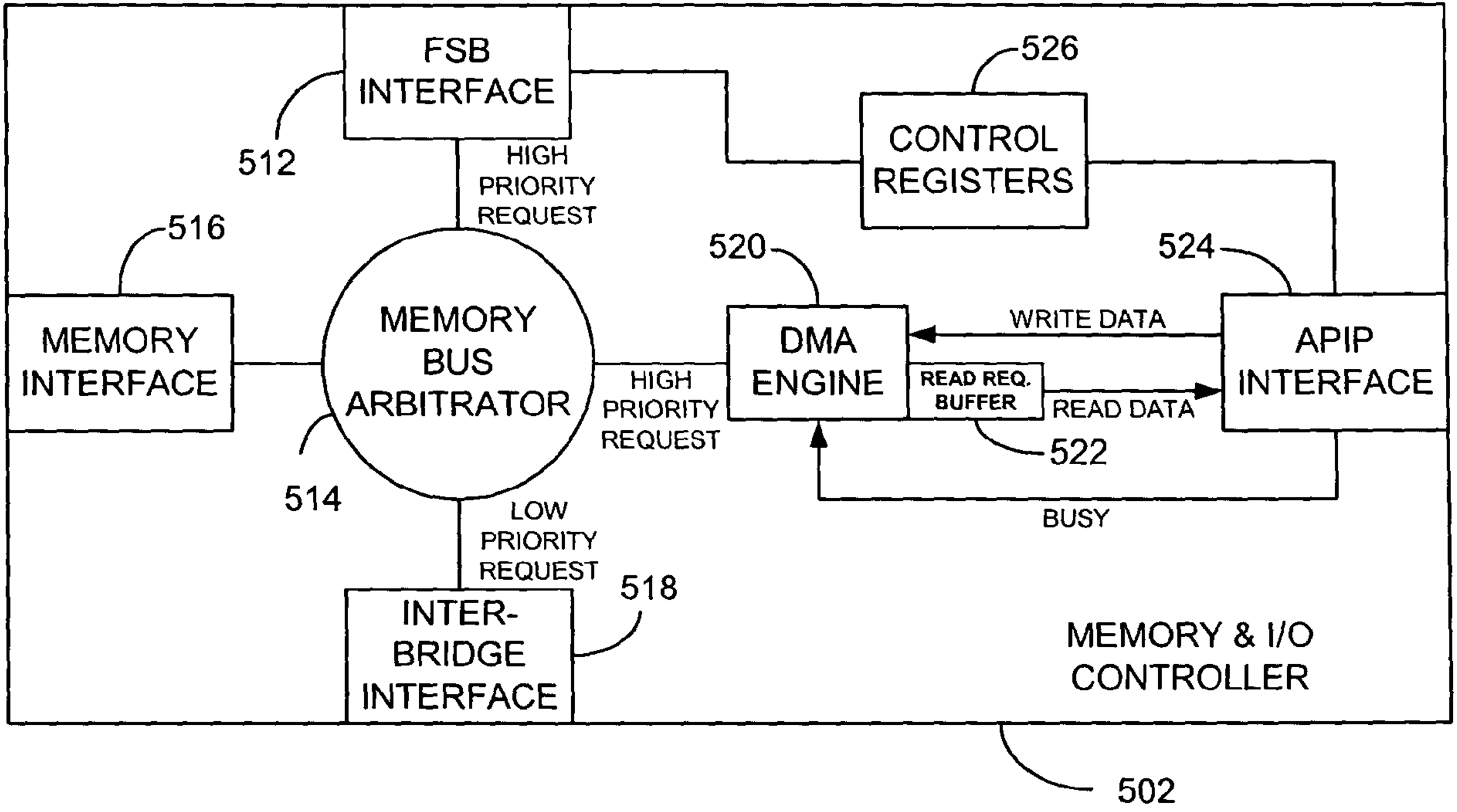

510
ON-BOARD MEMORY
534
SIX PORTS
SIX PORTS
CONTROL CHIP
532
CHAIN PORTS
USER ARRAY
CONTROL
530
APIP INTERFACE

Fig. 7


800
Fig. 8
804_N
802_N
uP
MEMORY AND I/O CONTROLLER
516
518
524
MICROPROCESSOR BUS
810_N
ADAPTIVE PROCESSOR
806_N
MEMORY
I/O BRIDGE
808_N
TO CLUSTERING HUB
804_0
802_0
uP
MEMORY AND I/O CONTROLLER
516
518
524
810_0
ADAPTIVE PROCESSOR
806_0
MEMORY
I/O BRIDGE
808_0
TO CLUSTERING HUB


FSB INTERFACE
512
HIGH PRIORITY REQUEST
526
CONTROL REGISTERS
516
MEMORY INTERFACE
MEMORY BUS ARBITRATOR
514
520
DMA ENGINE
524
APIP INTERFACE
WRITE DATA
READ REQ. BUFFER
READ DATA
522
HIGH PRIORITY REQUEST
BUSY
LOW PRIORITY REQUEST
518
INTER-BRIDGE INTERFACE
MEMORY & I/O CONTROLLER
502