MEMORY INTEGRATED CIRCUIT

A memory integrated circuit contains a sensing circuit (12) that receives signals from addressed memory cells. The sensing circuit determines in which of a number of ranges the signals fall, the number of ranges being greater than the number values to which the cells can be programmed. An output circuit is provided that is arranged to supply either only data words that have been inferred from the detection, or also further information that provides more information about the ranges that have been detected than the data words only. Depending on a control signal from external terminals of the memory integrated circuit the output circuit supplies the data words only to the external terminals or also the further information about the detected ranges in addition to the data words.
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Memory integrated circuit

The invention relates to a memory integrated circuit, and more in particular to the correction of errors in words read from such a memory.

US patent application No. 2003/0217323 discloses a memory system wherein the analog output signals from memory cells are digitized with higher resolution than minimally necessary to distinguish between different stored digital values. The excess resolution is used to make reconstructions of the digital values and to generate reliability information about the quality of the reconstruction. In general, the scope of possible analog output signal values from memory cells is subdivided into ranges. A set of nominal ranges corresponds to reliable digital values and intermediate ranges between these nominal ranges correspond to uncertain digital values. Dependent on the range within which the output signal from a memory cell lies, one digital value or another is selected and a reliability of the digital value is determined.

The system of US patent application No. 2003/0217323 contains a controller that has on one side a line connected to a host and on the other side lines coupled to row and column address decoders and sense amplifiers that are coupled to a memory matrix. The controller uses an Error Correcting Code to perform error correction on the reconstructed digital data from the sense amplifiers, optionally using the reliability information to increase the error correction capacity. US patent application No. 2003/0217323 concerns a system with an EEPROM, which typically returns a page of data from a row of the memory matrix in response to an address.

It is well known to implement host computers and its mass memory in different integrated circuits (ICs). Typically the host computer IC and the memory IC are connected via an address/data bus over which the host supplies addresses and the memory returns data stored at the specified addresses. The conventional approach is that such an address/data bus makes the internal operations of the memory IC, which are specific to the analog aspects of the representation of data in the memory, transparent at the data address bus: the conversion of analog signals to digital data is done in the memory IC.
This situation has the disadvantage that it prevents that optimal use can be made of the same type of memory ICs in circuits with different demands, or for accessing data that has to meet different quality standards. In some circuits maximum reliability is desirable only for selected data words. For this purpose, it would be desirable to have information about the reliability of the digital data based on the analog signal level available in a computer IC only for the selected data words. Information about all data words would merely constitute useless overhead in this case, whereas output of only corrected data words would not enable maximum reliability. Moreover implementation of strong error correction circuitry in the memory IC (which typically is made with a manufacturing that is not optimized to realize logic circuits efficiently) would constitute unnecessary overhead.

In some other circuits no reliability data is needed at all. In circuits that compute video output signals for example a certain amount of unreliability is acceptable, so that uncorrected data may be used, irrespective of its reliability. In this type of circuit supply of reliability information would be useless overhead. In other circuits however, all possible reliability is needed during processing. In this way, for example, the reliability of different computed data, which is computed from the digital data, can be differentiated according to the reliability of different parts of the original digital data. A memory IC that implements a fixed technique to use information about the range wherein the output signal from a memory cell lies cannot optimally meet the needs of all these circuits.

US patent application No. 2003/0217323 does not address this problem. This patent application is silent about the kind of information that is passed along the line between the controller and the host. The patent application shows a controller that is architecturally internal to the memory, because control of row and column decoders and sense amplifiers diverges from the controller. This controller is described to handle error correction. No indication is given that the host is able to affect error correction, let alone that reliability information is supplied to the host.

Among others, it is an object of the invention to provide for a memory integrated circuit which allows for a more flexible use of information about the reliability of data that has been determined from output signals from memory cells.

The invention provides for a memory integrated circuit according to Claim 1. According to the invention the memory IC has an output circuit, which functions as a control interface that allows external processor circuitry to control whether or not the memory IC will output further information that has been derived from the range in which output signals from the memory matrix have been found to lie and provides more information than
necessary for only identifying the stored data word. The further information is preferably output via the same external terminals as the data words.

Various embodiments of the control interface for the selective output of reliability information may be used. In one embodiment different read commands are provided for reading data with and without the further information about the range respectively. Thus, a minimum number of overhead commands is needed. Different commands can be identified for example by using special read control terminals of the memory IC or by applying different control signals to data terminals of the memory IC when applying the read address.

In another embodiment a special separate read command may be provided to read only the further information for data words, after a normal read command has been given to read the data words. In this way, for example, a decision whether it is necessary to read the additional information can be postponed until after reading the data words. In a further embodiment, the special read command for the further data words may have a higher address resolution than the normal read command. In this way, the bandwidth overhead for reading of further information can be limited to data words or sub-groups of data words for which special attention is needed.

In one embodiment for example, the memory integrated circuit is designed to shift out the data words for a series of memory locations serially in response to a normal read command and the special read command allows for addressed reading of further information for selected locations within the series.

Further information may be interleaved between data words for example, or appended to a series of data words, or the data words may even be split when further information is output, at least one of the split parts being augmented with further information.

When the further information is interleaved with data words, preferably blocks of data words and blocks of further information for groups of memory locations may be interleaved. Preferably a standard block size is used for different memories with different row sizes, so that in at least in some memories the block size may be smaller than the row size. This reduces the need to adapt the data processing circuit to a particular type of memory. In this way a family of integrated circuits may be realized, wherein different integrated circuit types in the family each have a memory matrix with a respective width, the width of different integrated circuit types in the family being mutually different, the size of the blocks between which the the further information is interleaved being the same for all types, e.g. 512 words, or another plurality of words.
The output circuit may, for example, contain a shift register with parallel inputs to capture detected information for a row of memory cells in parallel and an output for shifting the captured data serially to the external outputs of the memory integrated circuit. In this case, a further shift register in parallel with the shift register for the data words may be provided to capture and shift out the further information for a row of memory cells. This further information may be shifted out to the terminals of the memory IC for example after the data words have been shifted out, if the memory IC has been commanded to do so. Alternatively, further information for a row may be shifted out of the further shift register and stored in an internal RAM of memory IC while the data words are shifted out to the external pins. In this case, further information may be retrieved later by selective addressing of the RAM.

These and other objects and advantageous aspects of the invention will be described by means of a number of examples shown in the following figures.

Figure 1 shows an electronic circuit with a non-volatile memory
Figure 2 shows a sensing circuit
Figures 3a-d show output circuits

Figure 1 shows an electronic circuit with a memory IC 1 and a data processor 18 in one or more separate IC's. An address/control output 108, 110 of data processor 18 is coupled to memory integrated circuit 1 and a data output 19 is coupled from memory integrated circuit 1 to data processor 18. Although data output 19 and address/control output 108, 110 are shown separately for the sake of exposition, it should be realized that in practice time-division multiplexing may be used to implement the functions of these connection with a single, shared set of IC terminals.

Memory IC 1 contains a non-volatile memory matrix 100 and a control circuit 102. A word line address decoder 104, a bit line driver 106 and sensing circuits 12 in memory IC 1 are coupled to memory matrix 100. An output circuit 14 in memory IC is coupled between sensing circuits 12 and data output 19. Control circuit 102 receives the control output 110 from data processor 18 and controls address decoder 104 and output circuit 14. Address decoder 104 receives the address output 108 from data processor 18 and supplies word line selection signals to memory matrix 100. Memory matrix 100 has bitline
outputs 16 coupled to sensing circuits 12. Sensing circuits 12 each have a plurality of outputs coupled to the output circuit 14.

Although non-volatile memory matrix 100 is shown as a single block addressed by a single address, it should be appreciated that memory matrix 100 may in practice be replaced by any number of memory matrixes. In this case, different bit-line outputs may be used for different matrices. A typical example of a non-volatile memory matrix 100 contains cells with floating gate transistors, wherein information is programmed by injecting charge into a normally electrically isolated transistor gate electrode.

Figure 2 shows an embodiment of a sensing circuit 12. Sensing circuit 12 contains a first sense amplifier 20 and second sense amplifier 22 and a reference circuit 24. Bit-line 16 is coupled to first inputs of first and second sense amplifier 20, 22. Reference circuit has respective outputs coupled to second inputs of first and second sense amplifier 20, 22 respectively. The outputs of sense amplifiers 20, 22 are coupled to the outputs 17a,b of the sensing circuit 12. Instead of a plurality of parallel sense amplifiers 20, 22, one can also use a single sense amplifier, which sequentially compares sensing signals with successively selected reference levels to produce the output signals corresponding to those of the parallel sense amplifiers 20, 22.

In operation, data processing circuits 18 addresses data in non-volatile memory matrix 100. In response to the address non-volatile memory 10 outputs sensing signals on bit-lines 16. The sensing signals are analog signals, which depend on the data programmed in memory cells of memory 10 that contain the bits of addressed storage words. The signal level of the sensing signal is relatively high when the addressed cell stores a logic one and relatively low when the addressed cell stores a logic zero.

Sensing circuit 12 determines whether the sensing signal is above or below a first reference level and whether the sensing signal is above or below a second reference level. Reference circuit 24 outputs the reference levels. Sense amplifiers 20, 22 compare the sensing signal to the respective reference levels and output digital signals that indicate whether the sensing signal is above or below the respective reference levels. Effectively, sensing circuit 12 determines in which of three ranges the sensing signal lies: a highest range above the highest reference level, a lowest range below the lowest reference level or an intermediate range between the two reference levels. When the sensing signal is in the highest or lowest range the programmed signal is likely to be logical one and zero respectively. When the sensing signal is in the intermediate range the information about the programmed signal is ambiguous. Three combinations of digital output signals are possible:
"11" (here called a "likely one" signal) if the sensing signal is higher than both reference levels, "00" (here called a "likely zero" signal) if the sensing signal is lower than both reference levels and "01" (here called an "ambiguous" signal) if the sensing signal is below the highest reference level and above the lowest reference level. In an embodiment an exclusive OR circuit is used with inputs from the sense amplifiers 20, 22 to produce a signal indicating whether the result is ambiguous or not.

Output circuit 14 passes data derived from the data signals to data processor 18 via output 19. Data processor 18 supplies commands to memory IC 1 to control whether or not output circuit 14 passes further information as well derived from the signals that indicate whether the signal is ambiguous or not.

These commands from data processor may take any form. In one embodiment dedicated control terminals of memory integrated circuit 1 are used. In this embodiment data processor 18 asserts a control signal on an "ADD FURTHER INFORMATION" control line. In another embodiment memory IC 1 has inputs (coupled e.g. to the data outputs 19) for receiving combinations of bits that represent commands. Such commands may include "READ" commands and "PROGRAM" commands, according to the invention different READ commands may be provided, a first one to cause reading with further information and a second one to cause reading without further information.

In a NAND Flash memory for example the interface comprises N (N=8 for example) datalines, a Read-signal (RD), a Write-signal (WR), a Command-Latch-Enable signal (CLE) and an Address Latch Enable signal (ALE) and Busy signal. If the data processor 18 wants to read data, it puts the read command (0x00) on the data bus and pulls CLE high and pulses WR. Then it puts the LSB of the address on the data bus, pulls ALE high and pulses WR, and in the same way the other address bits are sent. The memory chip sets Busy to high, and then the host waits until busy is low again. Then the hosts pulses RD while ALE and CLE are both low to read the first data byte, followed by a next pulse on RD for the second data byte etc. If the data processor 18 wants to write data, it puts the write command (0x80) on the data bus, pulls CLE high and pulses WR. Then it puts the LSB of the address on the data bus, pulls ALE high and pulses WR, and in the same way the other address bits are send. Then the host pulls both CLE as well as ALE low and puts the first byte of data on the data bus and pulses WR, followed by the next data byte etc. After 512 bytes have been transferred the memory chip pulls Busy high and the hosts waits until busy is low again.
In such a NAND Flash memory one or more special command values may be defined for reading further information. When data processor 18 wants to read further information, it puts a special command value on the data bus and provides further signals such as for reading. The implementation of reception and decoding of such special commands in the memory can be realized substantially in the same way as for read and write commands.

In another embodiment a separate command may be provided for reading further information that is associated with a previous read command. In a further embodiment the command for reading further information may be accompanied with an address for selecting memory cells for which further information must be read from a row of memory matrix 100. In yet another embodiment control circuit 102 is arranged to monitor the address values supplied by data processor 18. In response to normal address values, control circuit 102 controls the memory IC to read and output data values from memory cells. However, an address detector (not shown) in control circuit 102 controls output circuit 14 to output the further information for the data of a previous read command when it detects a special address value. Control circuit 102 receives and interprets the commands and applies control signals to output circuit 14 to cause the corresponding output of data and/or further information. Output circuit 14 receives the data signals and the signal that indicates whether the signal is ambiguous or not from sense circuits 12. When a control signal from control circuit 102 has a first value output circuit 14 supplies only data derived from the data signals to data processor 18, and no further information derived from the signals that indicate whether the signal is ambiguous or not. When a control signal from control circuit 102 has a second value output circuit 14 supplies data words derived from the data signals to data processor 18 as well as further information derived from the signals that indicate whether the signal is ambiguous or not.

Figure 3a-d show a number of possible embodiments of output circuit 14. Figure 3a shows an embodiment that comprises a first shift register 140 and second shift register 142, each comprising shift register cells 141, 143 (only one referenced for the sake of clarity). The shift register cells 141 of first shift registers 140 are coupled to outputs of sense amplifiers 12 that indicate a data value sensed by the sense amplifiers 12. The shift register cells 143 of second shift registers 140 are coupled to outputs of sense amplifiers 12 that output signals that indicate whether the data signal is ambiguous or not. The shift register cells 141, 143 in each shift register 140, 142 are coupled in series and serial shift outputs of the shift registers 140, 142 are coupled to an input of a multiplexer 144. An output of the
multiplexer 144 is coupled to the data output 19 (not shown). In operation, in reply to a read command control circuit 102 causes the shift register cells 141, 143 of the shift registers to capture data and further information from the sense amplifiers 12. When control circuit 102 has received a command that indicates that only data must be output, control circuit 102 controls a control input 146 of multiplexer 144 to pass data from the first shift register 140 and control circuit 102 applies clock signals to a clock input 147 of the first shift register to cause serial shifting. Next memory 1 is ready to output data for a new address from data processor 18.

When control circuit 102 has received a read command indicating that data and further information must be output, control circuit first controls control input 146 of multiplexer 144 to pass data from the first shift register 140 and control circuit 102 applies clock signals to a clock input 147 of the first shift register to shift out all data serially from first shift register 140. Next control circuit 102 controls control input 146 of multiplexer 144 to pass data from the second shift register 140 and control circuit 102 applies clock signals to a clock input 147 of the second shift register 142 to shift out all further information from second shift register 142 serially. After that memory 1 is ready to output data for a new address from data processor 18.

In another embodiment, when control circuit 102 has received a read command indicating that data and further information must be output, control circuit 102 alternately controls control input 146 of multiplexer 144 to pass data and further information from the first and second shift register 140, 142 respectively and the control circuit send clock signals to the clock inputs 147 of these shift registers 140, 142 alternately.

In yet another embodiment, when control circuit 102 has received a read command indicating that data and further information must be output, control circuit 102 alternately controls control input 146 of multiplexer 144 to pass a series of data for N bit lines (N=512 for example) and a series of further information for B bit lines from the first and second shift register 140, 142 respectively and the control circuit send series of N clock signals to the clock inputs 147 of these shift registers 140, 142 alternately.

Although an embodiment has been shown wherein the shift registers shift one-bit wide data and further information, it should be understood that in practice M bit wide data and further information (M=8 or 16 for example) may be shifted. In this embodiment each first and second shift register effectively comprises M one bit shift registers in parallel and data from groups of M respective sense amplifiers 12 is captured to shift register cells from
respective ones of these one bit shift registers in response to a read command. In this embodiment groups of M bits of the data are shifted out through multiplexer 144.

Figure 3b shows an embodiment wherein a random access memory 148 has been added between second shift register 142 and multiplexer 144. In operation, first and second shift register 140, 142 are clocked at the same time, but while data that is shifted out from first shift register 140 is passed by multiplexer 144, further information that is shifted out from second shift register 142 is stored in random access memory 148. Typically, the memory capacity of random access memory 148 is much smaller than that of memory matrix 100, e.g. a capacity sufficient to store further information for data read from one or a few rows of memory matrix 100. When a row of cells in memory matrix 100 is accessed the resulting further information overwrites further information for a preceding row in random access memory 148. Subsequently, the further information may be read from selected locations in random access memory 148 and passed by multiplexer 144. That is, further information for a part of a row may be selectively addressed. For this purpose control circuit 102 has an address output coupled to random access memory 148. Preferably, control circuit 102 derives the addresses from address information received from data processor when a command to read the further information is received.

Figure 3c shows an embodiment wherein a single shift register 140 is used to shift out both data words and further information. In this embodiment a filter circuit 149 is provided between shift register 140 and data output 19. Filter circuit 149 has a control input coupled to control circuit 102 (not shown). In operation filter the 149 selectively passes both data words and further information from shift register 140 or passes only data words, filtering out further information. Shifting through shift register 140 may be clocked differently from data that is passed to data processor 18, so as to reduce time lost to empty cycles when further information is filtered out. E.g. the clock for shifting may run at twice the speed as the clock for transferring data to data processor 18. Dependent on the type of command received from data processor 18 control circuit 102 controls filter 149 to filter out the further information or not.

Figure 3d shows an embodiment wherein filter 149 writes the further information that is filtered out to a random access memory 148. In this embodiment control circuit 102 is arranged to apply addresses to random access memory 148 for selectively reading further information and to multiplexer 144 to pass the further information to the data output.
Although the invention has been described for a specific embodiment, it
should be understood that the invention is not limited to this embodiment. For example, in a
further embodiment an ECC (Error Correction Code) decoder may be added to output circuit
14, so as to correct errors in the data in memory IC 1 before passing the data to data output
19 of memory IC 1. The further information may be used during this correction, to identify
data that is less reliable. A simple, word oriented error correction scheme may be used for
example, or a more complicated error correction scheme that used data from an entire row of
memory matrix 100 to determine the corrected data. In this embodiment with error correction
in memory integrated circuit 1, according to the invention, data processor 18 is still able to
select whether integrated circuit 1 will output only the corrected data or both the corrected
data (or uncorrected data) and the further information. Thus, data processor 18 is enabled to
perform further correction, or to examine whether selected critical data is reliable.

As another example, although the invention has been described for memory
cells that each store a single bit of data, it should be understood that the invention also applies
to memory cells that each store more than one bit of data because more than two different
levels may be programmed into a memory cell (e.g. by selecting between storing Q>2
different possible quantities of charge in a memory cell). In this case sensing circuit 12
should be modified to determine in which of a number P>Q of ranges an output signal from
memory matrix 100 lies.

For example, Q nominal levels may be used in combination with Q-1 ranges
between respective pairs of nominal ranges. In a further embodiment Q+1 ranges may be
used to check also whether the signal from the memory cell is significantly above the highest
or significantly below the lowest signal levels than are expected. Detection of the range in
which the output signal from the memory matrix 100 lies may be realized using a comparison
with a correspondingly greater number of reference levels for example. But any suitable
ADC (Analog to Digital Conversion) technique may be used.

In this embodiment with Q levels and Q+1 ranges, the information from a
memory cell may be marked as unreliable if the output signal from the cell is in one of the
intermediate ranges. In a further embodiment the further information may express the pair of
nominal output signals between which there is confusion. For example, while the output data
encodes that a data value "i" of the Q nominal values has been detected, the further
information may represent whether the data is reliable, or whether it may be confused with a
higher nominal value (assuming that in the case detection that the output signal of the matrix
is in an intermediate range the data value corresponding to the next lower range is output; of
course the next higher range may be used instead, the further information indicating
confusion with the next lower range in this case).

In a further embodiment a gray code representation may be used. In this case,
the information about the range in which the output signal lies is converted into a digital data
code so that data codes for successive nominal ranges differ by one bit only (e.g. in the case
of Q=4 nominal levels successive nominal ranges of output signal values may correspond to
00, 01, 11, 10). In this embodiment the further information preferably indicates which of the
bits is unreliable. For example, the further information may contain one bit that indicates
whether the data is unreliable and another bit (or group of bits) to indicate the position of the
unreliable bit. In the example with Q=4 the three respective intermediate ranges would result
in indication of the second position, the first position and the second position respectively for
example.

Although an application of the invention to a non-volatile memory has been
described, it will be appreciated that the invention may be applied to volatile types of
memory as well. However, non-volatile memories typically suffer more from level shift of
stored data. In a DRAM, for example, it is often easier to refresh data than to detect the range
of values in which the output signal of a memory cells lies. Therefore it is especially
advantageous to apply the invention to non-volatile memory. Typically, the output signals
from the cells of such a memory are voltage signals, but instead current signals may be used,
or charge transfers etc.

Summarizing, a memory integrated circuit according to the invention contains
a sensing circuit that receives signals from addressed memory cells. The sensing circuit
determines in which of a number of ranges the signals fall, the number of ranges being
greater than the number values to which the cells can be programmed. An output circuit is
provided that is arranged to supply either only data words that have been inferred from the
detection, or also further information that provides more information about the ranges that
have been detected than the data words only. Dependent on a control signal from external
terminals of the memory integrated circuit the output circuit supplies the data words only to
the external terminals or also the further information about the detected ranges in addition to
the data words.

This allows for a more flexible use of information about the reliability of data
that has been determined from output signals from memory cells.

It should be noted that the above-mentioned embodiments illustrate rather than
limit the invention, and that those skilled in the art will be able to design many alternative
embodiments without departing from the scope of the appended claims. In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. Use of the verb "comprise" and its conjugations does not exclude the presence of elements or steps other than those stated in a claim. The article "a" or "an" preceding an element does not exclude the presence of a plurality of such elements. The invention may be implemented by means of hardware comprising several distinct elements, and by means of a suitably programmed computer. In the device claim enumerating several means, several of these means may be embodied by one and the same item of hardware. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.
CLAIMS:

1. A memory integrated circuit (1), comprising
   - a matrix of memory cells (100), each cell for storing information that
   represents one of a number of programmable values;
   - a sensing circuit (12) coupled to the matrix to receive signals affected by
   address-selected cells, and arranged to detect for each signal in which of a number of ranges
   the signal falls, the number of ranges being greater than the number of programmable values,
   - a set of at least one external terminals (19, 108, 110);
   - an output circuit (14), coupled between the set of external terminals (19, 108, 110) and the sensing circuit (12), and arranged to determine data words of inferred
   programmed values from the detected ranges, for supply to the set of external terminals (19, 108, 110) in response to a read command, the output circuit (12) having a control input
   controlled from the set of external terminals (19, 108, 110), arranged so that a control signal
   from the set of external terminals (19, 108, 110) controls whether the output circuit (14)
   supplies further information about the detected ranges in addition to the data words to the set
   of external terminals (19, 108, 110), or the data words only to the set of external terminals

2. A memory integrated circuit according to Claim 1, wherein the output circuit
   is arranged to output the further information over the external terminal or terminals of the set
   (19, 108, 110) that are used for supplying the data words.

3. A memory integrated circuit according to Claim 1, wherein the output circuit
   (14) is arranged to distinguish read commands of a first and second type from the set of
   external terminals, the output circuit (14) being arranged to return only the data words to the
   set of the external terminals (19, 108, 110) in response to read commands of the first type and
   to return both the data words and the further information in response to read commands of the
   second type.
4. A memory integrated circuit according to Claim 3, wherein the output circuit (14) is arranged to output data values and further information serially in response to a read command of the second type, serially interleaving the further information for groups of memory cells with data values for said groups of memory cells.

5. A memory integrated circuit according to Claim 4, wherein a number of cells in the group is greater than one and smaller than a number of cells in a row of the memory matrix (100).

6. A memory integrated circuit according to Claim 1, wherein the output circuit (14) is arranged to identify whether a command from the set of external terminals is of a read further information command type, the output circuit being arranged to return the further information for memory cells that have been addressed by a previous read command to a command of the read further information command type.

7. A memory integrated circuit according to Claim 6, wherein the output circuit (14) is arranged to distinguish read commands and supply data commands from the set of external terminals (19, 108, 110), the output circuit (14) being arranged to capture information about sense signals from memory cells addressed with the read commands in response to read commands, and to return only data words that have been derived from the locations addressed by read commands to the set of the external terminals (19, 108, 110) in response to the supply data commands and to return further information that has been derived from the addressed locations in response to commands of the read further information command type.

8. A memory integrated circuit according to Claim 6, wherein the output circuit (14) is arranged to receive, in association with a command of the read further information command type, an address of memory cells within a set of memory cells that have been addressed by the previous read command, the output circuit (14) being arranged to output the further information for the addressed memory cells selectively in response to the command of the read further information command type.

9. A memory integrated circuit according to Claim 1, wherein the output circuit (14) is arranged to return only the data words to the set of the external terminals (19, 108,
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10) in response to read commands from the set of external terminals with address values from a set of addresses values and to return at least the further information in response to an address value that is outside the set of address values.

10. A memory integrated circuit according to Claim 1, comprising a first shift register (140) with first parallel inputs coupled to the sensing circuit (12) for capturing the data words for a series locations in the memory matrix (100) in response to a read signal from the set of external terminals (19, 108, 110), and a second shift register (142) with second parallel inputs coupled to the sensing circuit (12) for capturing the further information for said series locations in response to said read signal, the first shift register (140) having an output for outputting the data words that are serially shifted out of the first shift register (140) in series to the set of external terminals (19, 108, 110), the output circuit (14) enabling and disabling, under control of the control signal, supply from an output of the second shift register (142) to the external terminals (19) of the set that are used for outputting the data words.

11. A memory integrated circuit according to Claim 10, wherein the second shift register (142) has an output for outputting, when enabled by the control signal, the further information as it is serially shifted out of the second shift register (142) in series via the external terminals (19) of the set that are used for outputting the data words.

12. A memory integrated circuit according to Claim 10, comprising - a randomly accessible memory circuit (148) coupled to a serial output of the second shift register (142) and arranged to store the further information when it is serially shifted out of the second serial shift register (142);
- an addressable access circuit (102) coupled between the set of external terminals (19, 108, 110) and the randomly accessible memory circuit (148), for providing random access to the further information stored in the random access memory (148) for respective ones of the locations.

13. A memory integrated circuit according to Claim 1, comprising - a shift register (140) with parallel inputs coupled to the sensing circuit (12) for receiving information about the detected ranges that defines both the data words and the further information for a series locations in the memory matrix (100) in response to a read
signal,
a filter circuit (149) coupled between a serial output of the shift register (140) and the set of external terminals (19, 108, 110) and arranged to filter out the further information when passing data from the shift register (140) to the set of external terminals (19, 108, 110).

14. A memory integrated circuit according to Claim 13, wherein the filter circuit (149) has an enable/disable input for controlling enabling and disabling of said filtering with the control signal from the control input.

15. A memory integrated circuit according to Claim 13, comprising
- a randomly accessible memory (148) circuit coupled to the filter circuit (149), for storing further information that has been filtered out by the filter circuit (149);
- an addressable access circuit (102) coupled between the set of external terminals (19, 108, 110) and the randomly accessible memory circuit (148), for providing random access to the further information in the random access memory (148) stored for respective ones of the locations.

16. An electronic circuit, comprising a memory integrated circuit according to Claim 1 and a data processing circuit (18) that is arranged to apply read commands to the memory integrated circuit (1) and to apply commands for reading the further information in association with selected ones of the commands.

17. A method of reading data from a memory integrated circuit (1) that contains a matrix of memory cells (100) that are capable of storing nominal programmable values, the method comprising
- addressing memory cells in the memory matrix (100);
- causing the addressed memory cells to feed output signals to a sensing circuit (12);
- detecting, in the sensing circuit (12), for each signal in which of a number of ranges the signal falls, the number of ranges being greater than the number of nominal programmable values;
- determining data words of inferred nominal programmed values from the detected ranges;
- supplying the data words from the memory integrated circuit (1);
- applying a control signal to the memory integrated circuit (1) to select whether or not to supply further information that, together with the data words, is more informative about the detected ranges than the data words only, in addition to the data words from the memory integrated circuit (1);
- supplying the further information from the memory integrated circuit (1) only if the control signal commands the memory integrated circuit (1) to do so.
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

INV. G11C7/10

According to International Patent Classification (IPC) or to both national classification and IPC.

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched.

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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<th>Relevant to claim No.</th>
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<td>EP 0 634 750 A (KABUSHIKI KAISHA TOSHIBA) 18 January 1995 (1995-01-18)</td>
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Date of the actual completion of the international search

15 March 2006

Date of mailing of the international search report

31/03/2006

Names and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
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Fax: (+31-70) 340-3016

Authorized officer

Arnault, S
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