Aug. 26, 1969 P. C. BROCKETT 3,464,059

TRAFFIC-ACTUATED CONTROL SYSTEM

Filed Jan. 6, 1967 2 Sheets-Sheet 1

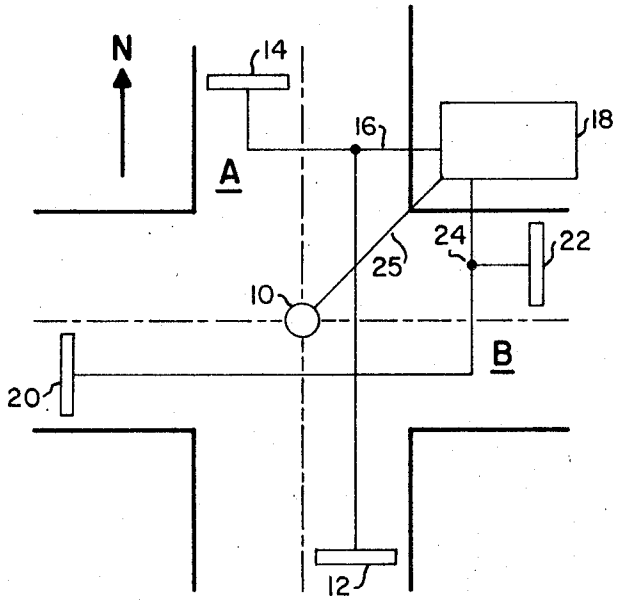
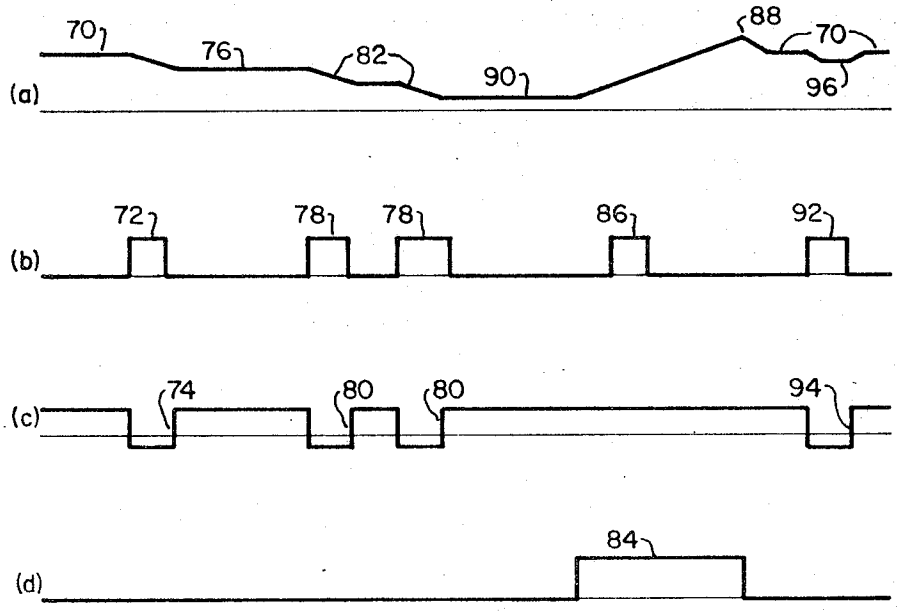


FIG. 1

FIG. 3

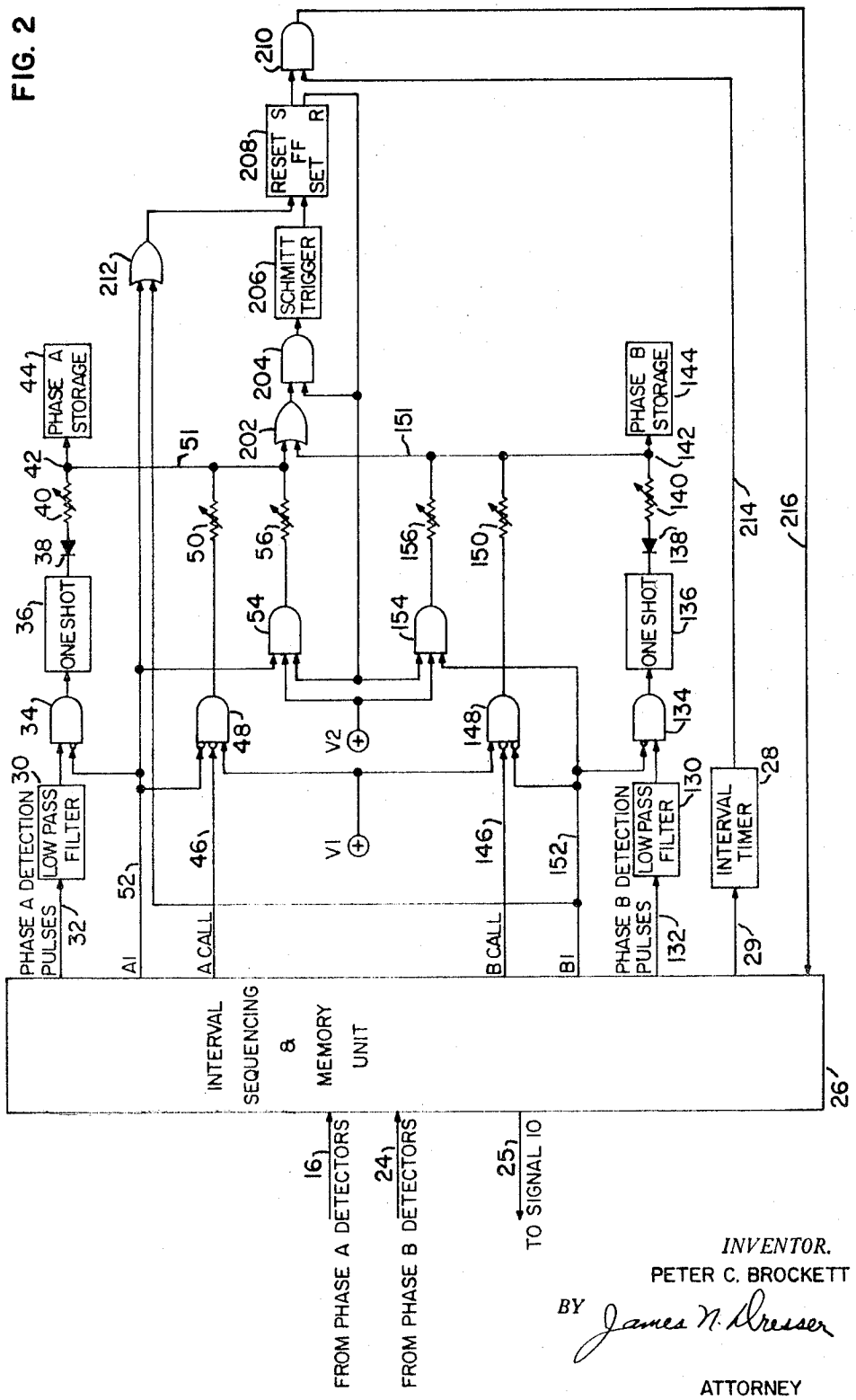


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TRAFFIC-ACTUATED CONTROL SYSTEM

Filed Jan. 6, 1967 2 Sheets-Sheet 2

FIG. 2



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TRAFFIC-ACTUATED CONTROL SYSTEM

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U.S. Cl. 340—37 9 Claims

ABSTRACT OF THE DISCLOSURE

A traffic-actuated intersection right-of-way control system in which the minimum initial interval of the right-of-way period is timed concurrently with a variable initial interval having a duration determined by the number of vehicles awaiting the right-of-way. Each vehicle waiting for the right-of-way alters a stored voltage. When the right-of-way is transferred, a fixed interval timer times the minimum initial interval, and concurrently the stored voltage is driven to a value slightly beyond its quiescent value. When both of these have finished, an output to the remainder of the control system steps the right-of-way period to its next interval.

BACKGROUND OF THE INVENTION

This invention pertains to a traffic-actuated intersection right-of-way control system. More particularly, this invention pertains to a traffic-actuated intersection control system which provides a fixed duration minimum initial interval concurrently with an initial interval having a duration dependent upon the number of vehicles waiting at the intersection for the right-of-way, so that, once right-of-way is transferred to the waiting vehicles, the initial interval of the right-of-way period does not end until both the minimum initial interval and the variable initial interval have ended.

The right-of-way at numerous traffic intersections is controlled by traffic signal lights which respond to signals generated by traffic-actuated controllers. These traffic-actuated controllers include vehicle detectors for determining when and how many vehicles have approached an intersection on the street or traffic phase which does not have right-of-way. Once the vehicle detector has detected such a vehicle, the controller is initiated so that ultimately it gives the right-of-way to the street or highway on which one or more vehicles are waiting.

The right-of-way period for a traffic phase is frequently divided into two or more intervals. The first of these is termed the initial interval of the right-of-way period. When right-of-way is transferred to a traffic phase in response to a signal from a traffic-actuated control system, one or more vehicles will have already passed the vehicle detector and will be waiting between the detector and the intersection. The initial interval of the right-of-way period is provided to allow these waiting vehicles to cross the intersection once right-of-way is transferred to their phase. Cars passing the detector after right-of-way has been transferred to their phase do not cross the intersection during the initial interval; instead they cross during a subsequent time, frequently termed a vehicle or passage interval.

At the time right-of-way is transferred, only one car may be waiting at the intersection. Alternatively, several cars may be waiting between the detector and the intersection at the time right-of-way is transferred. Accordingly, the traffic control system must provide an initial interval which is long enough to allow intersection-clearance time for the maximum number of vehicles which may be waiting between the detector and the intersection.

However, most efficient allocation of right-of-way requires that when only one vehicle is waiting at the intersection, the traffic control system must provide an initial interval of a short duration.

The length of time required for the waiting vehicles to cross the intersection is not directly proportional to the number of waiting vehicles. The first vehicle must start from rest after right-of-way is transferred to its phase and must then move through the intersection. The second vehicle starts from its rest position while the first vehicle is still in the intersection, and so it moves more rapidly through the intersection. Similarly, the remaining vehicles do not require as much additional time as do the first one or two vehicles. Thus, for maximum efficiency and minimum traffic congestion, the traffic control system must provide an initial interval which is variable between a minimum duration, sufficient to allow one or two cars to pass the intersection, and a maximum duration, sufficient to allow the maximum number of cars to pass. The traffic control system should vary the duration of the initial interval in accordance with the number of vehicles which have passed the detector prior to the transfer of right-of-way, but it should not cause it to be directly proportional to the number of waiting vehicles.

There are available traffic control systems having circuits for providing a variable initial interval of the right-of-way perod. These existing control systems utilize initial interval circuits having a first timer which provides the minimum initial interval and a second timer which provides additional periods of time of a duration dependent upon the number of vehicles which have passed the detector prior to the transfer of right-of-way. This sequential timing requires that the second timer be capable of timing a very brief period to be added to the minimum initial interval of the first timer. Since this added period is so short, it is difficult to adjust the second timer accurately, and components within the second timer must be selected with close tolerances. Such control systems are therefore expensive. Many of these control systems which utilize two sequential timers activate the second timer for a period of time dependent upon the total duration of the vehicle detection signals which have been received prior to transfer of right-of-way. However, in addition to being dependent upon the number of vehicles passing the detector, this total time duration may vary due to such factors as the speed at which the vehicles pass the detector, the length of the vehicles, the size wheels on the vehicles, etc. In addition, in such a control system the minimum initial interval of the first timer is long enough to permit, for example, two or three vehicles to cross the intersection, as selected by the highway engineer. But as these first vehicles pass the detector, they activate the second timer, and so the initial interval is unnecessarily lengthened by the second timer. This problem can be overcome by providing within the initial interval circuit counters and switches to count a minimum number of vehicles and then to switch the second timer into the circuit. However, such counting and switching circuitry is complex and expensive, and so it increases the possibility of a malfunction within the traffic control system, as well as adding to its cost.

SUMMARY OF THE INVENTION

The present invention is a traffic-actuated intersection right-of-way control system having an initial interval circuit in which a small controlled alteration is made in a stored voltage each time a vehicle is detected approaching the intersection on a traffic phase which does not have right-of-way. During the initial interval after right-of-way is transferred to that street or phase, an interval timer circuit within the control system times the minimum initial interval, and a variable timer circuit times an in-

terval with a duration dependent upon the amount by which the stored voltage has been altered. Since this voltage alteration is controlled, it is not subject to inaccuracies due to such things as the speed, length, and wheel size of the waiting vehicles. This variable timer circuit operates concurrently with the minimum initial interval timer circuit. Therefore, if only one or two vehicles are waiting for the right-of-way, the variable timer will complete its timing before the minimum timer; but if a large number of vehicles is waiting for the right-of-way, then the minimum timer completes its timing first. When both the minimum timer and the variable timer have completed their timing, the control system steps the right-of-way period to the next interval in its sequence.

It is accordingly an object of the present invention to provide an improved traffic-actuated intersection right-of-way controller.

It is another object of the present invention to provide a traffic-actuated intersection controller having an initial interval timing circuit which permits the timing of an initial interval adjusted according to the number of cars waiting for the right-of-way beyond a pre-set minimum number, without the requirement of complex counting and switching circuitry.

It is a further object of the present invention to provide a traffic actuated intersection controller having an initial interval timing circuit in which a minimum time period and a variable time period determined by the number of vehicles awaiting right-of-way are concurrently timed and jointly determine the duration of the initial interval.

It is still another object of the present invention to provide a traffic-actuated intersection right-of-way control system having an initial interval circuit which provides an initial interval that is adjusted in accordance with the number of vehicles waiting for the right-of-way, beyond a pre-set minimum number, and which is free from inaccuracies due to variations in vehicle characteristics, such as speed, length, and wheel size.

These and other objects and advantages of the present invention will be apparent from the following detailed description and claims when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGURE 1 is a plan view of a street intersection at which the right-of-way is controlled by a traffic-actuated control system.

FIGURE 2 is a block diagram of a traffic-actuated control system including both a minimum initial interval timer and a variable initial interval timer which operate concurrently.

FIGURE 3 depicts waveforms at various points in the circuit of FIGURE 2 and is useful in explaining the operation of the control system.

DESCRIPTION OF A PREFERRED EMBODIMENT

FIGURE 1 depicts a street intersection which may be controlled by means of a traffic-actuated control system including a variable initial interval circuit and incorporating the present invention. In FIGURE 1 the north-south street will be referred to as phase A and the east-west street as phase B. Signal **10** controls the right-of-way between phases A and B. Vehicle detectors **12** and **14** detect the northbound and southbound traffic, respectively, in phase A, and each vehicle passing either detector **12** or detector **14** causes a pulse to be transmitted via line **16** to the traffic-actuated control system **18** mounted with a terminal box at the side of one of the streets. Similarly, detectors **20** and **22** monitor the eastbound and westbound phase B traffic, respectively, and they are connected via line **24** to the control system **18**. The control system **18** is connected by line **25** to signal **10** to control the right-of-way between phases A and B. Detectors **12**, **14**, **20**, and **22** may be any of a number of types. For example, each may be an overhead detector of a radar or sonic type. Alternatively, they may be embedded in the roadway, in which case they may be inductive loop, magnetic, or treadle detectors, for example. It is only necessary that each detector generate an electrical signal upon the passage of a vehicle which signal can be converted to a pulse.

FIGURE 2 depicts in block diagram form the circuitry of traffic-actuated control system **18** which is made up of interval sequencing and memory unit **26**, interval timer **28**, and the variable initial interval timer. Lines **16** and **24** from the phase A and phase B detectors and line **25** to the signal **10** connect to unit **26**. Unit **26** and timer **28** are connected together by a plurality of lines, represented in FIGURE 2 by line **29**. The interval sequencing and memory unit **26** and the interval timer **28** can be of any standard design, and together they may form a traffic-actuated control system having a fixed initial interval.

Unit **26** steps the control system **18** output on line **25** in accordance with its programmed memory. Timer **28** includes circuitry to time the various intervals which make up the interval sequence. There is a line **29** corresponding to each interval of the right-of-way sequence, as well as a line **29** for other necessary control signals to timer **28**. At each interval of the sequence unit **26** applies a signal via a corresponding line **29** to timer **28** to initiate the timing of that interval. At the end of the appropriate time, timer **28** generates a control signal which is utilized to cause unit **26** to step to the next interval in the sequence. A manual control (not shown) for each interval of the sequence is supplied on either unit **26** or timer **28** to set the duration of each interval which is not varied in accordance with signals from the phase A and phase B vehicle detectors. Thus, both the phase A and the phase B minimum initial interval are set by means of these manual controls. United States Patent No. 3,267,424, issued Aug. 16, 1966, to P. C. Brockett et al., and assigned to the same assignee as the present invention, discloses and claims a traffic-actuated control system with a fixed initial interval which is suitable for use as interval sequencing and memory unit **26** and interval timer **28**. For example, in FIGURE 1 of Patent No. 3,267,424, normal interval time circuit **125** corresponds to interval timer **28** of the present invention as shown in FIGURE 2. The remainder of FIGURE 1 of Patent No. 3,267,424 corresponds to interval sequencing and memory unit **26** of the present invention. AND gate **210** of the present invention is inserted into line **141** in FIGURE 1 of Patent No. 3,267,424, so that lines **214** and **216** of the present invention correspond to line **141** of that patent. The variable initial interval circuitry forming a part of the present invention (components **32–210** of FIGURE 2) is then added to the circuitry of FIGURE 1 of Patent 3,267,424.

Each vehicle passing over detector **12** or **14** in the phase A lanes causes a phase A detection pulse which is applied from interval sequencing and memory circuit **26** to low-pass filter **30** via line **32**. The output from low-pass filter **30** is connected to the signal input of INHIBITED-AND gate **34** which has its output tied to the input of mono-stable multivibrator or one-shot **36**. The output of one-shot **36** is connected to the cathode of diode **38**, which has its anode connected through rheostat **40** to junction **42**. Junction **42** is tied to the input of phase A storage unit or storage means **44**, which, for example, may be a storage capacitor.

When phase A does not have the right-of-way, the first vehicle passing either phase A detector **12** or **14** initiates a continuing signal A CALL, in addition to causing a detection pulse on line **32**. The A CALL signal signifies that a vehicle has passed a phase A detector to call the right-of-way to phase A. This A CALL signal is applied by line **46** from interval sequencing and memory unit **26** to the first inhibit input of INHIBITED-AND gate **48**, the output of which connects through rheostat **50** to line **51** which ties it to junction **42**. During the phase A initial interval, immediately after right-of-way is transferred to

phase A, the signal AI is applied by line **52** from unit **26** to the inhibit input of INHIBITED-AND gate **34** and to the second inhibit input of INHIBITED-AND gate **48**. The signal input of INHIBITED-AND gate **48** is tied to a suitable source of potential such as first voltage source V1. Line **52** also applies the AI signal to the first input of AND gate **54**, which has its output connected through rheostat **56** to line **51** which ties it to junction **42**.

Circuitry identical to that just described for phase A is also provided for phase B. Thus, each vehicle passing detector **20** or detector **22** generates a signal over line **24** to cause a phase B detection pulse to be applied from interval sequencing and memory unit **26** to low-pass filter **130** via line **132**. The output of low-pass filter **130** is connected to the signal input of INHIBITED-AND gate **134**. The output of INHIBITED-AND gate **134** is connected to the input of one-shot multivibrator **136**, which has its output connected to the cathode of diode **138**. The anode of diode **138** connects through rheostat **140** to junction **142**. Junction **142** is connected to the input of the phase B storage unit or storage means **144**, which again may be a storage capacitor, for example.

The first vehicle to pass either phase B detector **20** or **22** during the time that phase B does not have right-of-way initiates a continuing B CALL signal which is applied by line **146** from interval sequencing and memory unit **26** to the first inhibit input of INHIBITED-AND gate **148**. INHIBITED-AND gate **148** has its output connected through rheostat **150** to line **151** which ties to junction **142**.

During the phase B initial interval, immediately after right-of-way is transferred to phase B, the signal BI is applied by line **152** from unit **26** to the inhibit input of INHIBITED-AND gate **134** and to the second inhibit input of INHIBITED-AND gate **148**. The signal input of INHIBITED-AND gate **148** is tied to first voltage source V1. Line **152** also applies the BI signal to the first input of AND gate **154**, which has its output coupled through rheostat **156** to line **151** which ties it to junction **142**.

Junctions **42** and **142** are connected to the two inputs of OR gate **202**. The output of OR gate **202** is connected to the first input of AND gate **204** which has its output tied to the input of Schmitt trigger **206**. The output of Schmitt trigger **206** is connected to the set input of flip-flop **208**, which has its set output connected to the first input of AND gate **210** and its reset output tied to the second input of AND gate **204**. The reset output of flip-flop **208** is also connected to the second inputs of AND gates **54** and **154**, both of which have their third inputs tied to a suitable source of potential such as second voltage source V2.

The AI and BI signals are applied by lines **52** and **152** respectively to the two inputs of OR gate **212**. The output of OR gate **212** is connected to the reset input of flip-flop **208**. The second input of AND gate **210** is connected via line **214** to the output of interval timer **28**. AND gate **210** has its output connected via line **216** to circuitry within interval sequencing and memory unit **26** which steps the right-of-way sequence to its next interval when an electrical signal is applied via line **216**.

OPERATION OF THIS PREFERRED EMBODIMENT

When the right-of-way is on the phase B street and no vehicle has passed either detector **12** or detector **14** to call the right-of-way to the phase A street, the phase A circuitry (components **30** through **56** in FIGURE 2) is in its quiescent condition, and no signal is applied to the phase A circuitry by lines **32**, **46** and **52** from interval sequencing and memory unit **26**. If right-of-way has been on phase B for enough time that it is no longer in its initial interval, then flip-flop **208** is in its set condition. INHIBITED-AND gates **34** and **48** are enabled, since no inhibiting inputs are applied to them on lines **46** and **52**. AND gate **54** is blocked since there are no signals applied to its first or second inputs. In addition, one-shot **36** is in its stable state, which means that its output, applied to diode **38**, is at a high voltage level in the embodiment depicted in FIGURE 2 in which V1 and V2 are both sources of positive potential. This high voltage from one-shot **36** is blocked from voltage storage unit **44** by diode **38**. The voltage on voltage storage unit **44** is at the level of the voltage from first source VI, which is adjusted to be just below the firing level of Schmitt trigger **206**. FIGURE 3(*a*) depicts the voltage on the phase A voltage storage means **44**, and in the quiescent condition this voltage is shown at level **70**.

When a vehicle passes detector **12** or detector **14**, a phase A detection pulse is applied by line **32** from unit **26** to low-pass filter **30**. FIGURE 3(*b*) depicts the phase A detection pulses on line **32**, and this phase A detection pulse from the first vehicle is shown as pulse **72**. In addition to causing detection pulse **72**, the first vehicle to pass a phase A detector during the time that phase A does not have right-of-way results in interval sequencing and memory unit **26** generating a continuing signal A CALL which is applied by line **46** to the first inhibit input of INHIBITED-AND gate **48**. INHIBITED-AND gate **48** then open circuits rheostat **50**, and so the phase A storage unit **44** is isolated from the first voltage source V1.

The phase A detection pulse **72** passes through INHIBITED-AND gate **34** to trigger one-shot multivibrator **36**. As a consequence, the one-shot assumes its unstable state in which its output drops to a low value, as shown by a pulse **74** of FIGURE 3(*c*). The duration of pulse **74** is dependent solely upon the characteristics of one-shot **36**, and so each pulse from one-shot **36** is of the same duration, as shown in FIGURE 3(*c*), even if the duration of the detection pulses varies, as shown in FIGURE 3(*b*), due to variation in vehicle speed, length, the tire size, etc. When one-shot **36** is in its unstable state, a measured amount of voltage is passed from the phase A storage unit **44** through rheostat **40** and diode **38** to the one-shot **36**, and so the voltage on storage unit **44** drops to level **76**, shown in FIGURE 3(*a*). Each subsequent vehicle passing either phase A detector **12** or **14** causes a phase A detection pulse on line **32**, such as pulses **78**. Each of these pulses **78** triggers one-shot **36** to its unstable state, as shown by pulses **80** in FIGURE 3(*b*), and so a controlled amount of voltage is removed from storage unit **44**, dropping its voltage a fixed amount, as indicated at points **82** in FIGURE 3(*a*). The amount of voltage removed from a storage unit **44** at each phase A detection pulse is controlled by the length of time which one-shot **36** remains in its unstable state and by the setting of rheostat **40**.

When right-of-way is transferred to the phase A street, the A CALL signal is terminated, and the AI signal, depicted as pulse **84** in FIGURE 3(*d*), is applied on line **52** to inhibit INHIBITED-AND gate **34** from passing any additional phase A detection pulses. Consequently, detection pulses, such as pulse **86**, initiated by vehicles passing a phase A detector after right-of-way has been transferred to phase A, have no effect on the duration of the initial interval. The AI signal on line **52** inhibits INHIBITED-AND gate **48**, and so phase A storage unit **44** remains isolated from first voltage source V1, even though the A CALL signal on line **46** has been terminated. The A CALL signal is not initiated again by vehicles passing phase A detector **12** or **14**, so long as phase A has right-of-way.

The AI signal passes through OR gate **212** to reset flip-flop **208**. The reset output of flip-flop **208** is applied to the input of AND gates **54** and **204**. The AI signal is also applied to AND gate **54**, and so the gate **54** is enabled to apply voltage from second voltage source V2 through rheostat **56** to the phase A storage unit **44**. As a consequence, the voltage on the phase A storage unit **44** increases, and this increasing voltage is passed through OR gate **202** and AND gate **204** to the input of Schmitt trigger **206**. When the voltage on storage unit **44** reaches the

firing level of Schmitt trigger **206**, depicted as level **88** in FIGURE 3(*a*), the Schmitt trigger applies a pulse to the set input of flip-flop **208**. This removes the enabling inputs applied by the reset output of flip-flop **208** to AND gates **54** and **204**. The set output of flip-flop **208** is applied to the first input of AND gate **210**.

The length of time required for the voltage on the phase A voltage storage unit **44** to reach the firing level **88** of Schmitt trigger **206** is dependent upon the level **90** of the voltage on storage unit **44** just prior to the transfer of right-of-way to the phase A street to generate the phase A initial interval. The level **90**, in turn is dependent upon the number of vehicles which have passed the phase A detectors **12** and **14** to trigger one-shot **36** so that a controlled amount of voltage is removed from storage unit **44**. The period of time is, of course, also dependent upon the setting of rheostats **40** and **56** and the magnitude of the voltage from voltage source V2. For a given value of voltage from source V2 and given settings of rheostats **40** and **56**, the length of time which elapses between the start of the phase A initial interval and the generation of the output pulse from Schmitt trigger **206** is dependent upon the number of phase A detection pulses which have been applied to line **32**.

When flip-flop **208** assumes its set condition, it applies voltage to the first input of AND gate **210**. When interval timer **28** has completed timing the minimum initial interval, it applies voltage via line **214** to the second input of AND gate **210**. Thus, if the number of cars which have passed the phase A detectors **12** and **14** prior to the transfer of right-of-way is so small that they all can cross the intersection during the minimum initial interval, the variable initial interval timer applies voltage to the first input of AND gate **210** before interval timer **28** applies voltage to the second input of the gate. Consequently, as soon as interval timer **28** indicates the end of the minimum initial interval, the coincidence of inputs to AND gate **210** causes gate **210** to apply a control signal via line **216** to interval sequencing and memory unit **26** to cause the end of the initial interval and the commencement of the next interval, which may be the vehicle or passage interval, for example. However, if several vehicles are waiting for the phase A right-of-way, it takes longer for the voltage on the phase A storage unit **44** to build up to the firing level of Schmitt trigger **206**. In such a case, interval timer **28** applies voltage via line **214** to the second input of AND gate **210**, marking the end of the minimum initial interval, before Schmitt trigger **206** fires, setting flip-flop **208** to apply voltage to the first input of AND gate **210**. Consequently, there is no output on line **216** from AND gate **210** until this longer variable time has passed, and the initial interval lasts longer to allow all the waiting vehicles to cross the intersection. When the phase A initial interval ends, the AI signal on line **52** terminates.

When flip-flop **208** turns to its set condition, the enabling input is removed from AND gates **54** and **204**. Consequently, Schmitt trigger **206** shuts off, and phase A voltage storage unit **44** is isolated from the second voltage source V2. Termination of the AI signal removes the inhibiting input from INHIBITED-AND gates **34** and **48**. Therefore, voltage from first voltage source V1 is applied to the phase A voltage storage unit **44** to return it to its initial level **70** as shown in FIGURE 3(*a*). Since the A CALL signal is not initiated during the time right-of-way is on phase A, INHIBITED-AND gate **48** does not isolate phase A storage unit **44** from first voltage source V1 during this time.

In order to fire Schmitt trigger **206**, the voltage on storage unit **44** must be at a value **88**, slightly greater than the quiescent value **70**. Consequently, the voltage from second voltage source V2 must be slightly greater than the voltage from first voltage source V1. After Schmitt trigger **206** fires to end the initial interval, INHIBITED-AND gate **48** again applies voltage source V1 to the phase A voltage storage unit **44**. Since the voltage level **88** on storage unit **44** is slightly greater than the voltage level **70** from source V1, voltage is then drained from the storage unit **44**. Voltage source V1 clamps the storage unit **44** at voltage level **70** so that no voltage can leak from the storage unit to drop this voltage to a lower level during the quiescent condition. Phase A detection pulses occurring after the end of the phase A initial interval but during the time that right-of-way is on phase A are passed by INHIBITED-AND gate **34** and trigger one-shot **36**. Thus, detection pulse **92**, shown in FIGURE 3(*b*), causes negative pulse **94** of FIGURE 3(*c*) from one-shot **36**. The drop in voltage at the output of one-shot **36** causes ripple **96**, shown in FIGURE 3(*a*), in the voltage stored in storage unit **44**, but source V1 again brings the stored voltage to level **70**.

After the phase A initial interval has ended, flip-flop **208** remains in its set condition until the next initial interval signal from unit **26** passes through OR gate **212** to reset flp-flop **208**. During this period of time, the set output from flip-flop **208** enables AND gate **210** to pass further signals on line **214** from interval timer **28** to line **216** which connects to interval sequencing and memory unit **26**. Thus, signals from interval timer **28** marking the termination of other intervals in the timing sequence of the right-of-way period are not blocked by AND gate **210**. AND gate **210** is blocked only while the variable initial interval circuit is timing.

Operaton of the phase B variable initial interval timing circuitry is the same as that just described for phase A. Interval sequencing and memory unit **26** applies as inputs to the phase B circuitry (components **130** through **156** in FIGURE 2), the phase B detection pulses, and the signals BI, and B CALL. The voltage on phase B storage unit **144** passes through OR gate **202** and AND gate **204** to Schmitt trigger **206**, just as does the voltage from phase A storage unit **44**.

Each vehicle passing either phase A detector **12** or phase A detector **14** will cause the voltage on phase A storage unit **44** to be altered by a slight amount and will lengthen the variable initial interval. Since the phase A circuitry is not able to distinguish between vehicles passing detector **12** and vehicles passing detector **14**, the voltage on storage unit **44** is altered by the same amount when two northbound vehicles are waiting between detector **12** and the intersection as it is when one northbound vehicle and one southbound vehicle are waiting between detectors **12** and **14**, respectively, and the intersection. Thus, the variable initial interval will be of the same duration for two vehicles waiting in the same direction as it is one vehicle waiting in each direction. However, adjustments can be made via the rheostats **40** and **56** by the highway engineer to vary the effect which each waiting vehicle has on the variable initial interval to meet the requirements of each individual intersection. Thus, for example, if traffic engineering studies show that at a given intersection approximately 60% of the phase A traffic is northbound, then rheostats **40** and **56** can be adjusted so that each phase A detection pulse results in 60% of the necessary alteration in the initial interval. The particular adjustments made for a given intersection will be dependent upon traffic flow at that intersection.

While the above description is with reference to an intersection having two interfering traffic phases, it will be obvious that the traffic-actuated right-of-way control system of the present invention can be utilized at intersections having a greater number of interfering vehicle phases by utilizing an appropriate interval sequencing and memory unit **26** and an appropriate interval timer **28** to accommodate the desired number of phases and by including within the variable initial interval timer sets of phase-handling circuitry (e.g., components **30–56** utilized for phase A in FIGURE 2) for the deisred number of phases. Similarly, it can be utilized on a single phase of an intersection controlled by a semi-actuated

control system. The term multiphase traffic intersection thus describes all of these types of intersections.

In the above detailed description V1 and V2 have been sources of positive voltage and the one-shot 36 output has been a high voltage in the stable state and a low voltage in the unstable state. By appropriate selection of components, either V1 or V2 could be ground potential. Alternatively, in the quiescent condition a low voltage level could be on storage unit 44, with a controlled amount of voltage added to storage unit 44 from one-shot 36 each time a vehicle passes a detector. Additionally, gating has been provided by AND, OR and INHIBITED-AND gates, but other types of gates, for example, NOR and NAND gates could be utilized.

While in the above detailed description, each vehicle passing the phase A detector has altered the voltage stored on phase A storage unit 44 to lengthen the duration of the variable initial interval, flexibility can be achieved by making the detection pulse from the first vehicle to pass a phase A detector have no effect on the stored voltage. This can be easily accomplished by the simple method of inhibiting INHIBITED-AND gate 34 in the absence of the A CALL signal. Thus, for example, the A CALL signal on line 46 can be delayed and applied to another signal input (not shown) on INHIBITED-AND gate 34. Since the A CALL signal is not present prior to the first detection pulse, gate 34 will be blocked to this first pulse. Subsequent detection pulses will pass through gate 34, since the A CALL will enable the gate. In such a case, pulses occurring after termination of the A CALL signal, when phase A has right-of-way (e.g., pulses 86 and 92), will not trigger one-shot 36. Thus, flexibility can be achieved without complex switching and counting circuitry.

Thus, among others, the several objects of the invention as specifically afore-noted are achieved.

I claim:

1. A multiphase traffic intersection right-of-way control system for providing to a traffic phase in response to traffic-actuated signals a right-of-way period including an initial interval and at least one other interval, said control system comprising in combination:

(A) detection means for generating detection signals in response to vehicles approaching an intersection on a traffic phase which does not have right-of-way;

(B) apparatus means coupled to said detection means for receiving said detection signals and for sequentially stepping through prescribed intervals in response to control signals to bring right-of-way to said traffic phase, said apparatus generating for each traffic phase

(1) a detection pulse in response to each received detection signal for said traffic phase,

(2) a continuing signal indicating that at least one detection signal has been received for said traffic phase when said traffic phase does not have right-of-way, and

(3) an initial interval signal during the initial interval of right-of-way on said traffic phase;

(C) an interval timer connected to said apparatus to receive therefrom signals indicative of initiation of each interval of each right-of-way period and, after timing the appropriate interval, to generate a control signal;

(D) a variable initial interval timer including

(1) a set of phase circuitry for each traffic phase of said intersection comprising

(a) voltage storage means,

(b) first means coupled to said apparatus and to said voltage storage means and adapted for connection to a first voltage source to apply voltage from said first voltage source to said voltage storage means in the absence of both said continuing signal and said initial interval signal for said traffic phase,

(c) second means coupled to said apparatus and to said voltage storage means to alter in a controlled manner stored voltage on said voltage storage means in response to each of said detection pulses for said traffic phase occurring in the absence of said initial interval signal for said traffic phase,

(d) third means coupled to said apparatus and to said voltage storage means and adapted for connection to a second voltage source to apply voltage from said second voltage source to said voltage storage means when said initial interval signal is present for said traffic phase, the voltage from said second voltage source being of a magnitude different from the magnitude of the voltage from said first voltage source,

(e) said second means adapted to alter said stored voltage to cause the voltage difference between said altered stored voltage and the voltage from said second voltage source to be greater than the voltage difference between the voltage from said first voltage source and the voltage from said second voltage source;

(2) pulse generating means having an input coupled to the voltage storage means of each traffic phase, said pulse generating means generating a signal when there is applied to its input a voltage having a magnitude between the magnitudes of the voltages of said first and second voltage sources;

(E) switching means connected to said apparatus, to said interval timer, and to said pulse generating means and capable of assuming first and second stable states, said switching means assuming said first stable state when said pulse generating means initiates a signal and assuming said second stable state upon initiation of an initial interval signal for any traffic phase, said switching means applying said control signal to said apparatus when said switching means is in its first stable state to cause sequential stepping through the prescribed intervals of right-of-way periods.

2. A multiphase traffic intersection right-of-way control system for providing to a traffic phase in response to traffic-actuated signals a right-of-way period including an initial interval and at least one other interval, said control system comprising in combination:

(A) apparatus means for receiving detection signals indicative of vehicles approaching an intersection on a traffic phase which does not have right-of-way and for sequentially stepping through prescribed intervals in response to control signals to bring right-of-way to said traffic phase, said apparatus generating for each traffic phase

(1) a detection pulse in response to each received detection signal for said traffic phase,

(2) a continuing signal indicating that at least one detection signal has been received for said traffic phase when that traffic phase does not have right-of-way, and

(3) an initial interval signal during the initial interval of right-of-way on said traffic phase;

(B) an interval timer connected to said apparatus to receive therefrom signals indicating the initiation of each interval of each right-of-way period and, after timing the appropriate interval, to generate a control signal;

(C) a variable initial interval timer including

(1) a set of phase circuitry for each traffic phase comprising

(a) voltage storage means,

(b) first means coupled to said apparatus and to said voltage storage means and adapted

for connection to a first voltage source to apply voltage from said first voltage source to said voltage storage means in the absence of both said continuing signal and said initial interval signal for said traffic phase,

(c) second means coupled to said apparatus and to said voltage storage means to alter in a controlled manner stored voltage on said voltage storage means in response to each of said detection pulses for said traffic phase occurring in the absence of said initial interval signal for said traffic phase,

(d) third means coupled to said apparatus and to said voltage storage means and adapted for connection to a second voltage source to apply voltage from said second voltage source to said voltage storage means when said initial interval signal is present for said traffic phase, the voltage from said second voltage source being of a magnitude different from the magnitude of the voltage from said first voltage source,

(e) said second means adapted to alter said stored voltage to cause the voltage difference between said altered stored voltage and the voltage from said second voltage source to be greater than the voltage difference between the voltage from said first voltage source and the voltage from said second voltage source;

(2) pulse generating means having an input coupled to the voltage storage means of each traffic phase, said pulse generating means providing a signal when there is applied to its input a voltage having a magnitude between the magnitudes of the voltages of said first and second voltage sources;

(D) switching means connected to said apparatus, to said interval timer, and to said pulse generating means and capable of assuming first and second stable states, said switching means assuming said first stable state when said pulse generating means initiates a signal and assuming said second stable state upon initiation of an initial interval signal for any traffic phase, said switching means applying said control signal to said apparatus when said switching means is in its first stable state to cause sequential stepping through the prescribed intervals of right-of-way periods.

3. A multiphase traffic intersection right-of-way control system as claimed in claim 2 in which said second means includes a monostable multivibrator which is triggered to its unstable state in response to each of said detection pulses and which has its output coupled to said voltage storage means to alter in controlled manner voltage stored on said voltage storage means when said monostable multivibrator is in its unstable state.

4. A multiphase traffic intersection right-of-way control system as claimed in claim 2 in which said switching means includes a bistable multivibrator capable of assuming first and second stable states and includes gating means, said bistable multivibrator coupled to said pulse generating means and to said apparatus to cause said bistable multivibrator to assume its first stable state when said pulse generating means initiates a signal and to assume its second stable state when an initial interval signal is initiated for any traffic phase, said gating means connected to said bistable multivibrator, to said interval timer, and to said apparatus to apply said control signal to said apparatus when said bistable multivibrator is in its first stable state to cause sequential stepping through the prescribed intervals of right-of-way periods.

5. A multiphase traffic intersection right-of-way control system for providing to a traffic phase in response to traffic actuated signals a right-of-way period including an initial interval and at least one other interval, said control system comprising in combination:

(A) apparatus means for receiving detection signals indicative of vehicles approaching an intersection on a traffic phase which does not have right-of-way and for sequentially stepping through prescribed intervals in response to control signals to bring right-of-way to said traffic phase, said apparatus generating for each traffic phase

(1) a detection pulse in response to each received detection signal for said traffic phase,

(2) a continuing signal indicating that at least one detection signal has been received for said traffic phase when that traffic phase does not have right-of-way, and

(3) an initial interval signal during the initial interval of right-of-way on said traffic phase;

(B) an interval timer connected to said apparatus to receive therefrom signals indicative of initiation of each interval of each right-of-way period and, after timing the appropriate interval, to generate a control signal;

(C) a set of phase circuitry for each traffic phase and including

(1) voltage storage means,

(2) first gating means coupled to said apparatus and to said voltage storage means, and adapted for connection to a first voltage source to apply voltage from said first voltage source to said voltage storage means in the absence of both said continuing signal and said initial interval signal for said traffic phase,

(3) second gating means connected to said apparatus and to said voltage storage means, and adapted for connection to a second voltage source to apply voltage from said second voltage source to said voltage storage means when said initial interval signal is present for said traffic phase, the voltage from said second voltage source being of a magnitude different from the magnitude of the voltage from first voltage source;

(4) a monstable multivibrator having an input and an output,

(5) third gating means coupled to said apparatus and to said monostable multivibrator input to pass detection pulses from said apparatus to said input in the absence of said initial interval signal to cause said monostable multivibrator to assume its unstable state at the occurrence of each detection pulse,

(6) said monostable multivibrator output coupled to said voltage storage means to alter voltage stored on said voltage storage means so that the voltage difference between said altered stored voltage and the voltage from said second voltage source is greater than the voltage difference between the voltage from said first voltage source and the voltage from said second voltage source;

(D) pulse generating means having an input coupled to the voltage storage means of each set of phase circuitry, said pulse generating means generating a signal when there is applied to its input a voltage having a magnitude between the magnitudes of the voltages of said first and second voltage sources;

(E) bistable multivibrator capable of assuming first and second stable states and connected to said pulse generating circuit to cause said bistable multivibrator to assume its first stable state when said pulse generating circuit initiates a signal, said bistable multivibrator coupled to said apparatus to cause said bistable multivibrator to assume its second stable state when an initial interval signal is initiated for any traffic phase;

(F) gating means connecting to said bistable multivibrator to said interval timer, and to said apparatus to apply said control signal to said apparatus when said bistable multivibrator is in its first stable state.

6. In a multiphase traffic intersection right-of-way control system which provides to a traffic phase in response to traffic-actuated signals a right-of-way period including an initial interval and at least one other interval and which includes

(A) apparatus for receiving detection signals indicative of vehicles approaching an intersection on a traffic phase which does not have right-of-way and for sequentially stepping through prescribed intervals in response to control signals to bring right-of-way to said traffic phase, said apparatus generating for each traffic phase

(1) a detection pulse in response to each received detection signal for said traffic phase,

(2) a continuing signal indicating that at least one detection signal has been received for said traffic phase when said traffic phase does not have right-of-way, and

(3) an initial interval signal during the initial interval of right-of-way on said traffic phase; and

(B) an interval timer connected to said apparatus to receive therefrom signals indicative of initiation of each interval of each right-of-way period and, after timing the appropriate interval, to generate a control signal;

the improvement comprising a variable initial interval timer including:

(A) a set of phase circuitry for each traffic phase comprising

(1) voltage storage means,

(2) first means coupled to said apparatus and to said voltage storage means and adapted for connection to a first voltage source to apply voltage from said first voltage source to said voltage storage means in the absence of both said continuing signal and said initial interval signal for said traffic phase,

(3) second means coupled to said apparatus and to said voltage storage means to alter in a controlled manner stored voltage on said voltage storage means in response to each of said detection pulses for said traffic phase occurring in the absence of said initial interval signal for said traffic phase,

(4) third means coupled to said apparatus and to said voltage storage means and adapted for connection to a second voltage source to apply voltage from said second voltage source to said voltage storage means when said initial interval signal is present for said traffic phase, the voltage from said second voltage source being of a magnitude different from the magnitude of the voltage from said first voltage source;

(5) said second means adapted to alter said stored voltage so that the voltage difference between said altered stored voltage and the voltage from said, second voltage source is greater than the voltage difference between the voltage from said first voltage source and the voltage from said second voltage source;

(B) pulse generating means having an input coupled to the voltage storage means of each traffic phase, said pulse generating means generating a signal when there is applied to its input a voltage having a magnitude between the magnitudes of the voltages of said first and second voltage sources;

(C) switching means connected to said apparatus, to said interval timer, and to said pulse generating means and capable of assuming first and second stable states, said switching means assuming said first stable state when said pulse generating means initiates a signal and assuming said second stable state upon initiation of an initial interval signal for any traffic phase, said switching means applying said control signal to said apparatus when said switching means is in its first stable state to cause sequential stepping through the prescribed intervals of right-of-way periods.

7. The improvement claimed in claim 6 in which said second means includes a monostable multivibrator which is triggered to its unstable state in response to each of said detection pulses and which has its output coupled to said voltage storage means to alter in controlled manner voltage stored on said voltage storage means when said monostable multivibrator is in its unstable state.

8. The improvement claimed in claim 6 in which said switching means includes a bistable multivibrator capable of assuming first and second stable states and includes gating means, said bistable multivibrator coupled to said pulse generating means and to said apparatus to cause said bistable multivibrator to assume its first stable state when said pulse generating means initiates a signal and to assume its second stable state when an initial interval signal is initiated for any traffic phase, said gating means connected to said bistable multivibrator, to said internal timer, and to said apparatus to apply said control signal to said apparatus when said bistable multivibrator is in its first stable state to cause sequential stepping through the prescribed intervals of right-of-way periods.

9. A variable initial interval circuit for use with a multiphase traffic intersection right-of-way control system which provides to a traffic phase in response to traffic actuated signals a right-of-way period including an initial interval and at least one other interval and which includes:

(A) apparatus means for receiving detection signals indicative of vehicles approaching an intersection on a traffic phase which does not have right-of-way and for sequentially stepping through prescribed intervals in response to a control signal to bring right-of-way to said traffic phase, said apparatus generating for each traffic phase

(1) a detection pulse in response to each received detection signal for said traffic phase

(2) a continuing signal indicating that at least one detection signal has been received for said traffic phase when that traffic phase does not have right-of-way, and

(3) an initial interval signal during the initial interval of right-of-way on said traffic phase;

(B) an interval timer connected to said apparatus to receive therefrom signals indicative of initiation of each interval of each right-of-way period and, after timing the appropriate interval, to generate a control signal;

said circuit comprising:

(A) a set of phase circuitry for each traffic phase and including

(1) voltage storage means,

(2) first gating means coupled to said voltage storage means and adapted for connection to said apparatus and to a first voltage source to apply voltage from said first voltage source to said voltage storage means, in the absence of both said continuing signal and said initial interval signal for each traffic phase,

(3) second gating means coupled to said voltage storage means and adapted for connection to said apparatus and to a second voltage source to apply voltage from said second voltage source to said voltage storage means when said initial interval signal is present for said traffic phase, the voltage from said second voltage source being of a magnitude different from the magnitude of the voltage from said first voltage source;

(4) a monostable multivibrator having an input and an output,

(5) third gating means coupled to said monostable multivibrator input and adapted for connection to said apparatus to pass detection pulses from said apparatus to said input in the absence of said initial interval signal to cause said monostable multivibrator to assume its unstable state at the occurrence of each detection pulse,

(6) said monostable multivibrator output coupled to said voltage storage means to alter voltage stored on said voltage storage means so that the voltage difference between said altered stored voltage and the voltage from said second voltage source is greater than the voltage difference between the voltage from said first voltage source and the voltage from said second voltage source;

(B) pulse generating means having an input coupled to the voltage storage means of each set of phase circuitry, said pulse generating means generating a signal when there is applied to its input a voltage having a magnitude between the magnitude of the

voltages of said first and second voltage sources;

(C) a bistable multivibrator capable of assuming first and second stable states and connected to said pulse generating circuit to cause said bistable multivibrator to assume its first stable state when said pulse generating circuit initiates a signal, said bistable multivibrator adapted for connection to said apparatus to cause said bistable multivibrator to assume its second stable state when an initial interval signal is initiated for any traffic phase;

(D) gating means connected to said bistable multivibrator and adapted for connection to said interval timer and to said apparatus to apply said control signal to said apparatus when said bistable multivibrtor is in its first stable state.

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