United States Patent [19]

De Lyria

[11] **3,852,718**

[45] **Dec. 3, 1974**

[54] **APPARATUS FOR INTERPRETING NUMERICALLY CODED PULSE GROUPINGS IN A LINE**

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[22] Filed: **Oct. 25, 1973**

[21] Appl. No.: **409,766**

[52] **U.S. Cl.** ..... **340/164 R,** 340/293, 340/286

[51] **Int. Cl.** **G08b 25/00**

[58] **Field of Search** ..... 340/164 R, 167 R, 168 R, 340/293, 213 R

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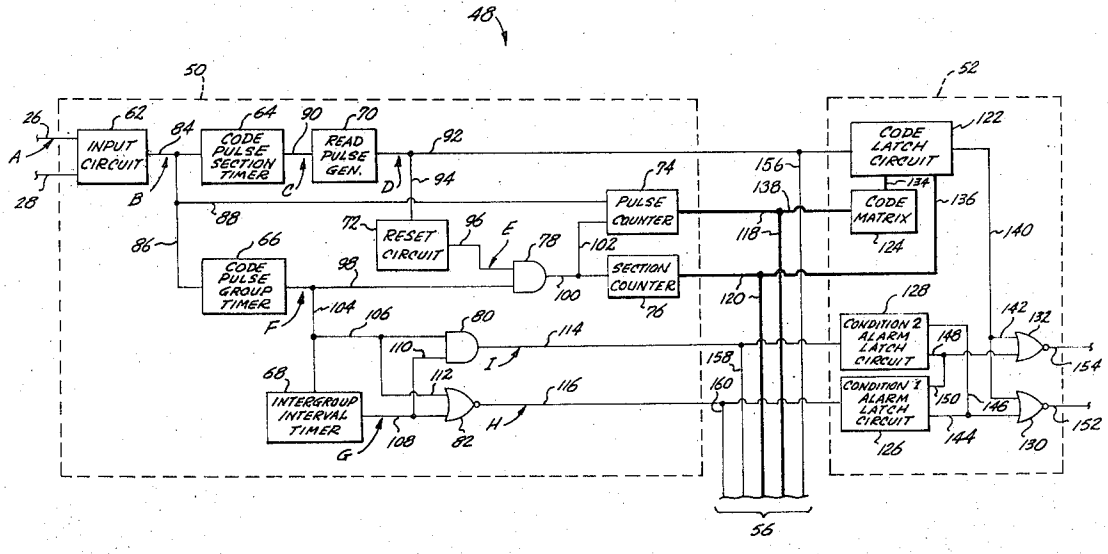
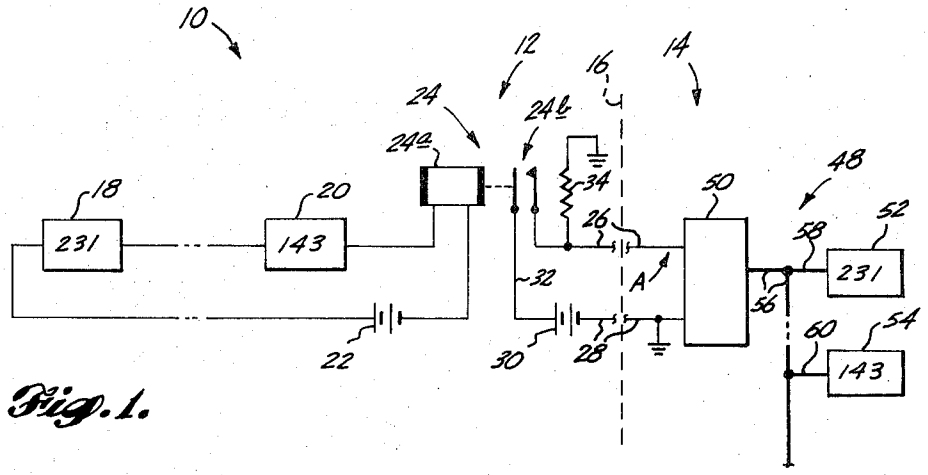
Attorney, Agent, or Firm—Kolisch, Hartwell, Dickinson & Stuart

[57] **ABSTRACT**

An electrical supervisory signaling system employing a plurality of McCulloh-type pulse transmitters which are operable selectively to transmit over a line one or more like groups, or "rounds," of time-spaced, numerically coded pulses. Single-"round" and multiple-"round" transmissions are used to indicate different monitored conditions. Receiving these pulses in the system is an interpreter which, through examining the time spacings between successive pulses, both distinguishes the transmissions from the different transmitters, and indicates whether a transmission from a given transmitter contains one or more "rounds" of pulses.

6 Claims, 5 Drawing Figures




10
12
14
16
24
24a
24b
18
20
231
143
34
26
50
48
52
58
231
32
A
56
60
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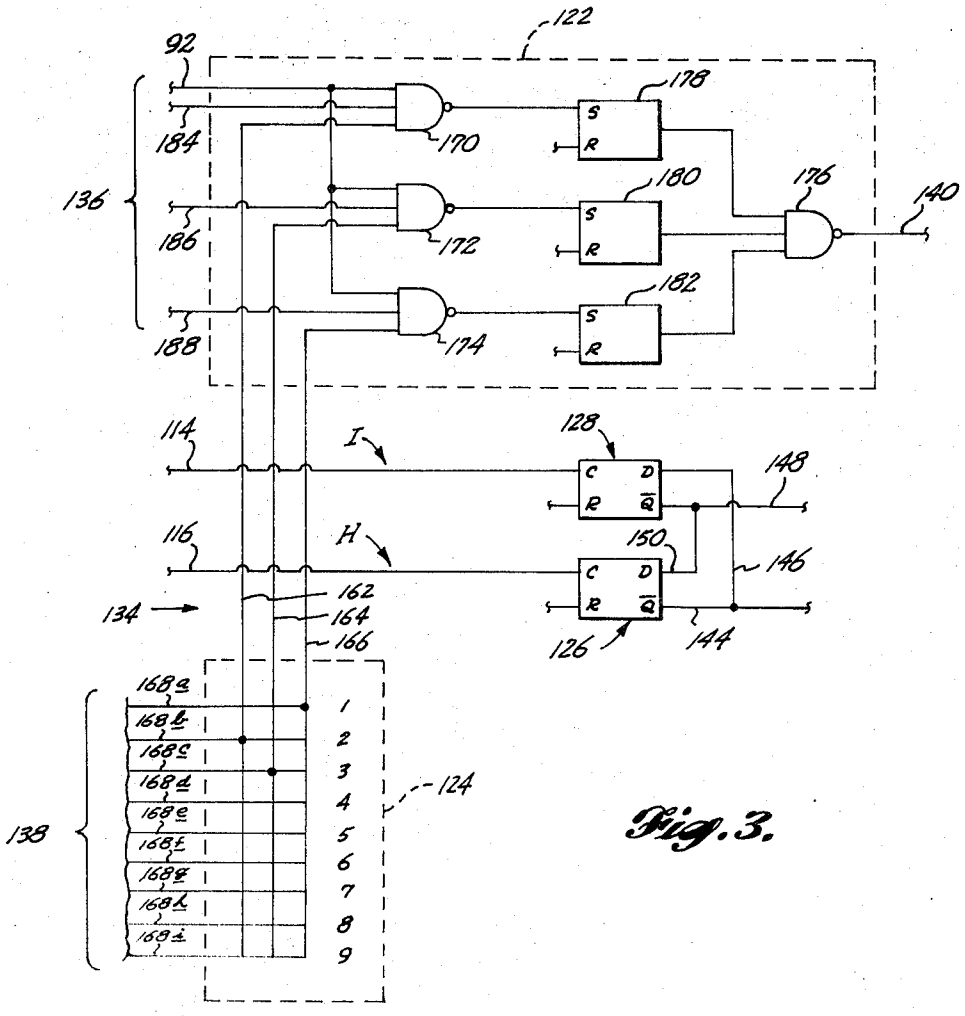
30
28

Fig. 1.


122
92
136
184
186
188
170
172
174
178
180
182
176
140
S
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114
116
I
H
128
148
150
146
144
126
C
D
Q
134
162
164
166
168a
168b
168c
168d
168e
168f
168g
168h
168i
124
138
1
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9

Fig. 3.

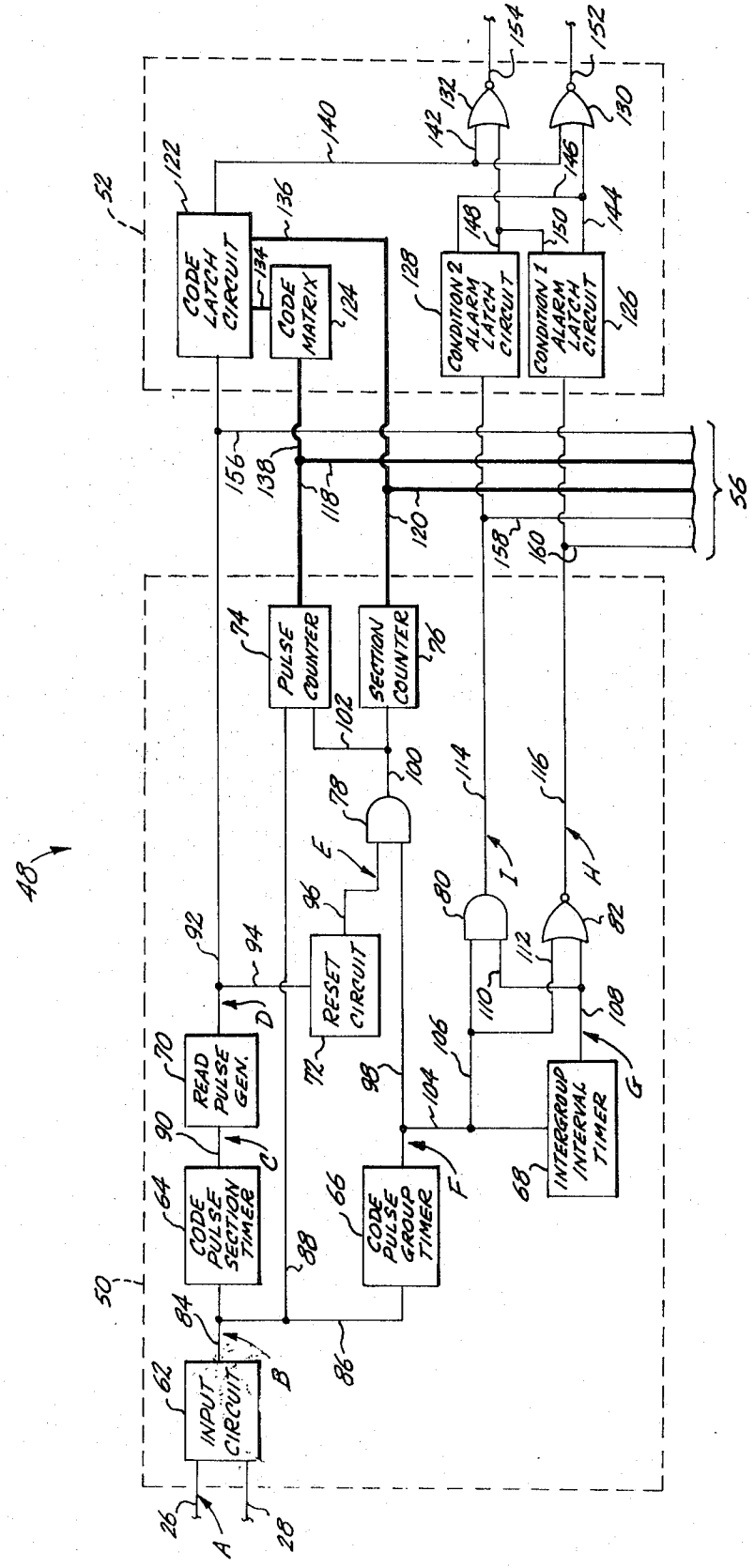
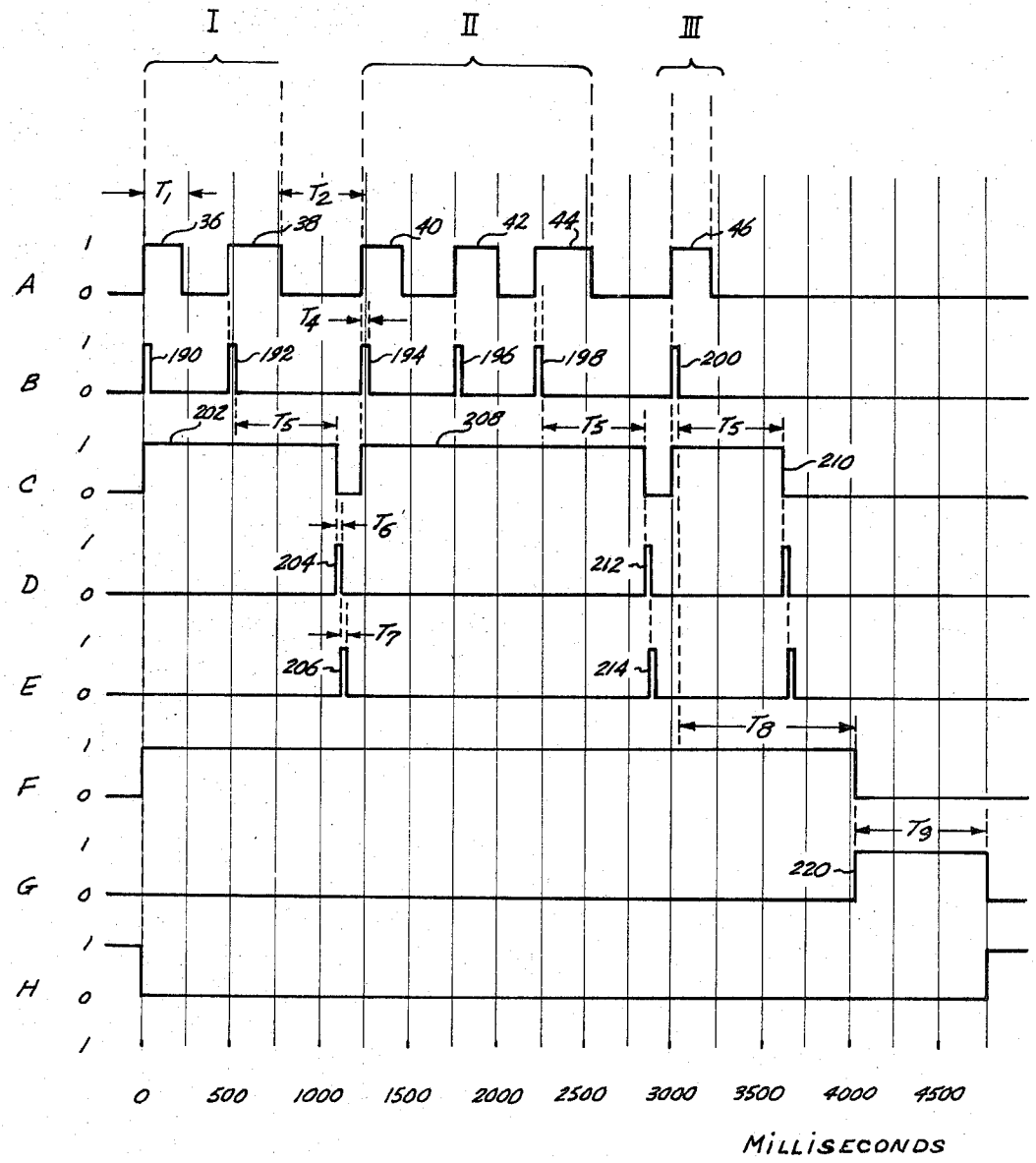

48
52
50
CODE LATCH CIRCUIT
122
CODE MATRIX
124
134
136
140
CONDITION 2 ALARM LATCH CIRCUIT
128
CONDITION 1 ALARM LATCH CIRCUIT
126
142
132
154
146
130
152
148
150
144
156
138
118
120
158
160
56
PULSE COUNTER
74
SECTION COUNTER
76
102
100
78
E
96
RESET CIRCUIT
72
92
94
D
READ PULSE GEN.
70
90
C
CODE PULSE SECTION TIMER
64
88
84
B
INPUT CIRCUIT
62
26
A
28
CODE PULSE GROUP TIMER
66
86
98
104
106
F
INTERGROUP INTERVAL TIMER
68
108
G
80
I
112
110
114
82
H
116

Fig. 2.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T7
T8
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192
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196
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212
206
214
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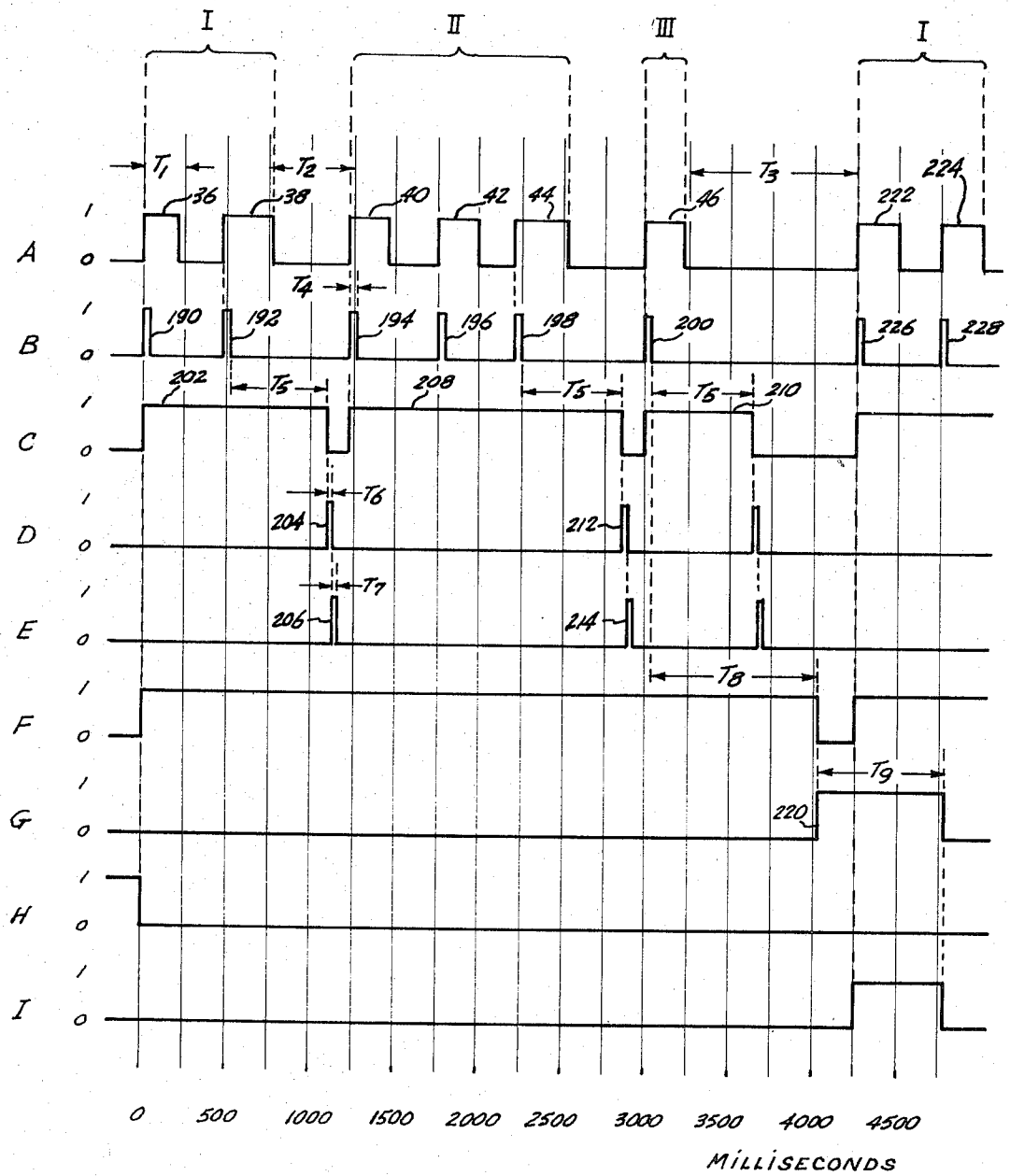
4500
MILLISECONDS

Fig. 4.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196
198
200
226
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202
208
210
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212
206
214
220
A
B
C
D
E
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I
1
0
0
500
1000
1500
2000
2500
3000
3500
4000
4500
MILLISECONDS

Fig. 5.

APPARATUS FOR INTERPRETING NUMERICALLY CODED PULSE GROUPINGS IN A LINE

BACKGROUND AND SUMMARY OF THE INVENTION

This invention pertains to an electrical supervisory signaling system of the type employing a plurality of McCulloh-type pulse transmitters. More particularly, it relates to an interpreter usable in such a system for automatically and reliably sorting out and interpreting the various transmissions therein of the different transmitters employed in the system.

A typical McCulloh-type transmitter includes a notched rotary wheel which may be turned selectively by a motor, such as by an electric or a spring-wound motor. The notches and lands in the wheel, with the latter turning, alternately open and close an associated electrical switch, which action is used to generate electrical voltage pulses in a line, such as in a conventional telephone line.

The arrangement of notches and lands provided in such a wheel defines a numerical pulse "code" for a transmitter. A typical code includes a group, or "round," of pulses divided into three sections, with each section containing one or more pulses. As an illustration, one code might be **2-3-1**, resulting in a pulse group containing a first section including two time-spaced pulses, a second section containing three time-spaced pulses, and a third and final section containing a single pulse.

A transmitter of the type just generally described is often set up to operate in two different modes so as to be able to respond to two different monitored conditions. In one mode of operation, the transmitter transmits but a single round of pulses, and in the other mode transmits two or more rounds. To illustrate, a transmitter set up to monitor the condition of a fire sprinkler system might be arranged to transmit but a single round if a non-fire-induced break occurs in the system, and more than one round in the event of the system turning on to handle a fire.

Further explaining what is conventional, within a coded round of pulses, it is usually intended that successive pulses within a section in the round be spaced apart by one uniform preselected time, and that successive sections in the round be spaced apart by another, longer preselected uniform time. Further, it is normally the case that successive rounds transmitted by a transmitter are spaced apart longer than the spacings between successive sections within a round. All of this practice, of course, is to aid in distinguishing rounds, and in distinguishing pulse sections within a round. With McCulloh-type transmitters, individual pulses normallly last between about .25–1.5-seconds, with the spaces between adjacent pulses in a section being the same width as the pulses. Further, it is usually the case that the time spacing used between successive sections in a round is about twice the spacing used between pulses in a section. The same two-to-one relationship normally typifies the length of the space between successive rounds as compared with the length between successive sections in a round. Thus, the pulses in a coded round might, for example, each be about 0.25-seconds long, with the gaps between pulses in a section also being about 0.25-seconds, and the gaps between sections in the round being about 0.5-seconds. Were the transmitter which is capable of producing such a round operated so as to produce successive rounds, the time spacings therebetween would typically be about 1-second for the example just described.

One of the problems with transmitters of the type just outllined is that the pulse widths, and the different pulse spacings, associated with a transmitter are not uniform, even within the transmission of a single round of pulses. This is partly due to the mechanical tolerances permitted in the manufacture of a notched wheel in a transmitter, and also partly due to the fact that the wheel when turned may not be rotated at a constant speed. As a consequence, the electrical pulse waveform transmitted by such a transmitter is not entirely predictable, and can be difficult to interpret.

A further problem is that transmitters of the type outlined have typically been used heretofore in systems wherein recording-type receivers, such as rolled paper tape recorders, have been used. What is recorded by such a recorder must be monitored by a person, and interpreted by him so as to distinguish different codes that may be transmitted in a system. Such an arrangement introduces considerable delay in obtaining desired information, and is quite prone to errors.

A general object of the present invention, therefore, is to provide novel means usable in a signaling system with transmitters of the type above outlined to receive and interpret transmissions therefrom in a manner avoiding the difficulties just mentioned.

More specifically, an object of the invention is to provide a novel electrical interpreter which is capable of ignoring pulse width and pulse spacing irregularities in the transmission from such a transmitter, and which is further capable of accurately and reliably distinguishing the coded transmissions of different transmitters which may be used in a system.

Still another object of the invention is to provide such an interpreter which is capable of determining whether the transmission from a given transmitter includes, on the one hand, a single coded round of pulses, or on the other hand, more than one round of pulses.

According to a preferred embodiment of the invention, an interpreter is proposed which accomplishes the above-stated objectives through examining major differences in the time spacings between successive pulses transmitted over a line in a system, thus to determine the beginnings and endings of different rounds, as well as the beginnings and endings of different pulse sections in a round. Included in the interpreter, for each transmitter employed in the system with which the interpreter is used, is a programmed memory capable of responding to, but only to, the coded transmission of but one of the transmitters in the system.

The interpreter of the invention continuously, and without the need for human intervention, monitors the signal conditions in a line in a system, and essentially immediately reports on each transmission in the system, with each such report specifically identifying which transmitter has operated, and what information it transmitted.

These and other objects and advantages attained by the invention will become more fully apparent as the description which follows is read in conjunction with the accompanying drawings.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a simplified diagram partially showing a sig-

naling system employing McCulloh transmitters and a receiving interpreter as contemplated by the present invention.

FIG. **2** is a block diagram illustrating details of the interpreter used in the system of FIG. **1.**

FIG. **3** is a block diagram illustrating, in greater detail, a portion of the interpreter of FIG. **2.**

And, FIGS. **4** and **5** are similar graphs illustrating, along a time base, several different voltage waveforms which appear at different points in the interpreter of FIG. **2** during two different modes of operation of the interpreter.

DETAILED DESCRIPTION OF THE INVENTION

1. Explanation of Terminology

Explaining briefly certain terminology which will be used in the description which follows, various components shown in the drawings operate in a response to a pair of voltage levels. More specifically, one of these levels corresponds to a certain positive voltage (typically about +5 volts) which will be referred to hereinafter as a 1 state. The other level corresponds essentially to ground, and will be called hereinafter a 0 state. A terminal or a conductor having one of these voltage levels on it will be referred to as being in, or as having on it, either a 1 or a 0 state.

2. Description of the Logic Gates Used

Among the components illustrated in the drawings which respond to the two voltage levels just mentioned are certain logic gates. More specifically, four different types of gates, all conventional in construction, are employed. These are referred to as AND, NAND, OR and NOR gates.

An AND gate functions as follows: with a 0 state on any input of the gate, the output thereof is held in a 0 state; with all inputs in 1 states, the output is placed also in a 1 state.

In a NAND gate: with a 0 state on any input, the output is held in a 1 state; with all inputs in 1 states, the output is placed in a 0 state.

In an OR gate: if any input is in a 1 state, the output of the gate is held also in a 1 state; if all inputs are in 0 states, then the output is also in a 0 state.

Finally, a NOR gate functions whereby: if any input is in a 1 state, the output is held in a 0 state; if all inputs are placed in 0 states, then the output is placed in a 1 state.

The operations of other components shown in the drawings which respond to these two voltage levels will be explained as such components are encountered in the description which follows.

3. The Signaling System Generally

Turning now to the drawings, and referring first to FIG. **1,** indicated generally at **10** is what is referred to herein as a conductive signaling system including remotely located transmitting and receiving portions **12, 14,** respectively, which are represented in FIG. **1** as being separated by a dashed line **16.** System **10** herein is used for reporting fire status and sprinkler system status information with respect to a plurality of facilities, such as storage warehouses, that are located remote from the receiving portion of the system. The term "fire status" is used herein to mean whether or not a fire exists; and the term "sprinkler system status" is intended to mean whether or not a sprinkler system is operative.

Included in the transmitting portion of system **10** are a plurality of conventional, electric-motor-driven McCulloh transmitters, or signalers, such as the two shown in block form at **18, 20.** Each such transmitter is employed with respect to a different facility herein, and each is set up to operate in either of two different modes of operation. In one of these operating modes, a transmitter produces a single round, or group, of coded pulses-- this being done to indicate that the sprinkler system in the associated facility has become inoperative. In the other operating mode, a transmitter transmits, one after another, a plurality of rounds of pulses to indicate that a fire exists at the associated facility. The way in which the transmitters in system **10** are connected to perform in such a manner is entirely conventional, and forms no part of the present invention. In general terms, the transmitters are suitably operatively connected to appropriate sensors which monitor the selected conditions of interest, and which operate to energize the motors in the transmitters to transmit the correct number of rounds.

McCulloh transmitters and the like typically take two different forms-- referred to as "normally open" and "normally closed" transmitters. In a normally open transmitter, the switch which is actuated by the wheel in the transmitter is normally open, and produces pulses by successive closures of this switch with turning of the wheel. Such transmitters, in a given system, are usually connected in parallel with one another. A normally closed transmitter is characterized by just the reverse operation, and in a given system, such transmitters are usually connected in series. The particular transmitters used in system **10** are of the normally closed type, and in this system are connected in series with a battery **22** (or some other suitable source of DC power) and the coil **24***a* of a relay **24.** Relay **24** also includes a normally closed switch **24***b* which in FIG. **1** is shown open for a reason which will be explained shortly.

Information in system **10** is transmitted over a suitable two-conductor line, such as a conventional telephone line. The particular telephone line used in system **10** includes conductors **26, 28.** Conductor **26** connects directly with one side of switch **24***b*. Conductor **28,** which is grounded, connects with one side of a battery (or other suitable DC power source) **30**--the other side of which is connected through a conductor **32** to the other side of switch **24***b*. Conductor **26** is connected through a resistor **34** to ground.

System **10** is shown in FIG. **1** with the switches in its transmitters all closed. As a consequence, and because of the series connection mentioned earlier, coil **24***a* is energized, and holds switch **24***b* open. Under these circumstances, conductor **26** is essentially at ground potential, or in a 0 state. With operation of a transmitter, it will be evident that switch **24***b* is alternately closed and opened to produce successive positive voltage square wave pulses (i.e., 1 states) on conductor **26.**

The particular different transmitters in system **10** are constructed to produce different coded rounds of pulses, with each round containing three pulse sections. These pulse sections each include on or more pulses. For example, transmitter **18** herein is associated with the numerical code **2-3-1,** and when operated to transmit a round of pulses, transmits a round containing a first pulse section containing two time-spaced pulses, a second pulse section containing three time-spaced

pulses, and a third section containing a single pulse. Thus, the number 231 is printed in FIG. 1 on the block representing transmitter **18**, as an indication of its associated code. Transmitter **20** is constructed to transmit rounds with the code **1-4-3.** Accordingly, the number 143 appears in the block in FIG. 1 representing transmitter **20.**

Each transmitter in system **10** is intended to transmit pulses having a duration of 0.25-seconds, with successive pulses in a section in a round separated by the same amount of time. It is further intended that successive sections in a round be separated by 0.5-seconds, and that successive rounds (when a transmitter is operated to produce a plurality of rounds) be separated by 1-second. However, because of the tolerance and operational speed problems mentioned earlier, these times may actually vary within about plus or minus 10 percent.

Considering for a moment FIG. **4,** Graph A therein illustrates a typical single round of coded pulses produced in conductor **26** by operation of transmitter **18.** As can be seen, this round includes three pulse sections, indicated by the three brackets and designated I, II, III. Section I contains two pulses **36, 38,** section II three pulses **40, 42, 44,** and section III a single pulse **46.** The reference character T_1 indicates the nominal or intended pulse width of 0.25-seconds. It will be recalled that this same time is the nominal or intended time between pulses in a section. The reference character T_2 indicates the nominal or intended time between pulse sections of 0.5-seconds.

In Graph A, an effort has been made to depict a round of pulses wherein the times, as would be experienced in actual practice, do not conform to the nominal or intended times. Thus, in section I, pulse **36** is somewhat shorter than, and pulse **38** somewhat longer than 0.25-seconds. The interval between these pulses is somewhat longer than 0.25-seconds. In section II, pulse **40** is somewhat shorter than, pulse **42** about equal to, and pulse **44** considerably longer than, 0.25-seconds. The gap between pulses **40, 42** exceeds, whereas the gap between pulses **42, 44** is less than, 0.25-seconds. Pulse **46** in section III is shorter than 0.25-seconds. Considering the intervals between the pulse sections, both of these intervals are somewhat less than 0.5-seconds.

Returning to FIG. **1,** included in the receiving portion of system **10** is a receiving interpreter, shown generally at **48,** which is constructed in accordance with the present invention. Interpreter **48** may be thought of, and is depicted in FIG. **1,** as containing a block of components **50** connected directly to conductors **26, 28,** and blocks, such as blocks **52, 54,** connected to block **50,** and each associated particularly with a different one of the transmitters in the system.

Bllocks **52, 54** herein are associated with transmitters **18, 20,** respectively, and accordingly, bear the code numbers 231, 143, respectively. Block **52** is connected to block **50** through multiple-conductor cables represented by the heavy lines shown at **56, 58.** Block **54** is connected to block **50** through cable **56** and a cable **60.** Other blocks, like blocks **52, 54,** are provided for the other transmitters in the system.

Explaining very briefly, and only in very general terms, how system **10** operates, should a breakdown occur in the sprinkler system located at the facility monitored by transmitter **18,** this transmitter is immediately operated to produce in conductor **26** a single round of coded pulses, with the code **2-3-1.** This transmission is received by interpreter **48,** which functions, as will be explained in detail later, to interpret this transmission correctly as being one from transmitter **18,** and as comprising but a single round of pulses. On determining that the transmission was made by transmitter **18,** and that it consists of a single round of pulses, block **52,** and only block **52,** provides one type of an output signal immediately indicating this situation.

In the case of a fire at the same location, transmitter **18** is operated to produce multiple successive rounds of pulses which are also received by the interpreter, and again interpreted thereby as correctly coming from transmitter **18.** Further, the interpreter determines that in this case the transmission received comprises multiple rounds of pulses, by which determination it ascertains that what is being indicated by transmitter **18** is that there is a fire. In this case, block **52,** again alone, produces another type of output signal to indicate this situation.

Similar operations take place with respect to transmissions made by each other transmitter in system **10.**

4. Details of the Interpreter

The overall construction of interpreter **48** is shown in FIGS. **2** and **3,** and reference is now made particularly to these figures.

Included within block **50** in the interpreter, such block being illustrated in dashed lines in FIG. **2,** and shown in block form therein, are an input circuit **62,** three timers, or timing circuits, **64, 66, 68,** a read pulse generator **70,** a reset circuit **72,** and a pair of counters **74, 76** which are referred to herein respectively as a pulse counter and a section counter. Also included within block **50** are three two-input logic gates including two AND gates **78, 80,** and a NOR gate **82.**

Timer **64** is also referred to herein as a code pulse section timer, timer **66** as a code pulse group timer, and timer **68** as an intergroup interval timer. In addition, timer **64,** generator **70,** and counters **74, 76** are referred to collectively as a code-reading circuit, and timer **68** along with gates **80, 82** are referred to collectively as an interval decision circuit. Further, timers **66, 68** along with gates **80, 82** constitute a pulse-group-spacing-monitoring circuit.

Previously mentioned conductors **26, 28** are connected to the input side of circuit **62**--the output of this circuit being connected through a conductor **84** to the input of timer **64,** through conductor **84** and a conductor **86** to the input of timer **66,** and through conductors **84, 86** and a conductor **88** to the counting terminal of counter **74.** Connecting the output of timer **64** and the input of generator **70** is a conductor **90.** A conductor **92** connects with the output of generator **70.** Connecting conductor **92** with the input of reset circuit **72** is a conductor **94.** The output of this circuit is connected through a conductor **96** to the upper input of gate **78.** And a lower input of gate **78** in connected via a conductor **98** to the output of timer **66.**

Further describing the interconnections existing between components in block **50,** gate **78** has its output connected via a conductor **100** to the counting terminal of counter **76.** A conductor **102** interconnects conductor **100** and the reset terminal of counter **74.** Conductor **98** is connected through a conductor **104** to the

input of timer **68**, and is connected through conductor **104** and a conductor **106** to the upper input of gate **80**. The output of timer **68** is coupled through a conductor **108** to the lower input of gate **82**. The lower and upper inputs of gates **80, 82**, respectively, are connected via conductors **110, 112**, respectively, to conductors **108, 106**, respectively. The outputs of gates **80, 82** are connected to conductors **114, 116**, respectively.

Input circuit **62**, timer **68**, generator **70**, and reset circuit **72** herein each comprise conventional monostable multivibrators. Circuit **62** responds to a state change from 0 to 1 on conductor **26**, and on such a state change occurring, produces at its output a positive, controlled-duration, square wave voltage pulse, called herein a follower pulse, which lasts about 0.05-seconds. Timer **68**, generator **70** and reset circuit **72**, on the other hand, respond to state changes from 1 to 0 on their respective inputs to produce at their outputs similar positive, controlled-duration, square wave voltage pulses. In particular, timer **68** produces a pulse which lasts about 0.75-seconds, and generator **70** and reset circuit **72** each produce a pulse which lasts about 0.015-seconds.

Timers **64, 66** are similar in construction-- each comprising a conventional retriggerable monostable multivibrator. Each of these timers responds to a state change from 0 to 1 on its input to produce a 1 state at its output, which 1 state lasts throughout the application of a 1 state at its input, plus an additional predetermined time interval. More particularly, with the application of a 1 state to the input of timer **64**, the output of this timer switches to a 1 state, and remains therein until about 0.6-seconds after removal of the 1 state from the input. Similarly, with application of a 1 state to the input of timer **66**, the output of this timer switches to a 1 state, wherein it remains until about 1-second after removal of the 1 state from its input. The term "retriggerable" as used herein respecting these timers means that a timer may be held in a condition placing a 1 state on its output, so long as successive 0 to 1 state changes recur on its input before completion of the "time-out" interval for the timer following the last preceding return of the input to a 0 state.

Counters **74, 76** are conventional decimal-output binary counters. Counter **74** is constructed to count from **0-9**, inclusive. This counter includes ten separate output terminals (not specifically shown in the drawings) each related to a different one of the ten different counts which may be stored in the counter. To each of the nine of these output terminals which are associated with the counts **1-9**, inclusive, is connected a separate conductor-all of which conductors are illustrated as a single heavy-line cable **118** in FIG. **2**. With counter **74** in a zero-count condition, each of these nine output terminals is in a 0 state, with the other terminal in a 1 state. The counter responds to each state change from 1 to 0 on its counting terminal to change the count in the counter. For example, with the counter in a zero-count condition, on the first such state change occurring on the counting terminal, the counter places a 1 state on its single output terminal which is associated with the count of "one"—all other output terminals then being in 0 states. On the second 1 to 0 state change occurring on the counting terminal, the counter places a 1 state on its output terminal associated with the count of "two"—all other output terminals then being in 0 states; and so on. A state change from 1 to 0 on its reset terminal returns the counter to a zero-count condition.

Counter **76** is similar in construction and operation to counter **74**, except that counter **76** includes but three output terminals (not specifically shown) associated with the counts **1-3** inclusive. To each of these separate output terminals is connected a separate conductor—all of which conductors are included within a cable shown at **120** in FIG. **2**. Counter **76** is normally in a condition storing a count of "one," with a 1 state existing on its output terminal associated with this count. Its other two output terminals are normally in 0 states. With the first count thereafter made by counter **76**, a 1 state is placed on its output terminal associated with the count of "two," and the other two output terminals are placed in 0 states. Similarly, when the next count is recorded, a 1 state is placed on the output terminal associated with the count of "three," and the other two output terminals are placed in 0 states. On the next count being recorded, counter **76** returns a 1 state to its output terminal associated with the count of "one"—the other two output terminals then being placed in 0 states. Such operation recurs in cycles with successive counts recorded by the counter.

Continuing with a description of what is shown in FIG. **2**, included within previously mentioned block **52** (shown in dashed lines in FIG. **2**) are a code latch circuit, or memory, **122**, a code matrix **124**, a pair of alarm latch circuits **126, 128**, and a pair of NOR gates **130, 132**.

Circuit **122** and matrix **124** are referred to herein collectively as a code-discriminating circuit. As will be more fully explained later, this combined circuit is programmed herein to respond only to a coded round of pulses transmitted by transmitter **18**. As can be seen in FIG. **2**, circuit **126** is also referred to as a "Condition **1** Alarm Latch Circuit," and circuit **128** as a "Condition **2** Alarm Latch Circuit." These two circuits, along with gates **130, 132** comprise an output circuit in interpreter **48**. As will become apparent, circuit **126** and gate **130** are employed in the production of an output signal to indicate a transmission from transmitter **18** consisting of but a single round of pulses, whereas circuit **128** and gate **132** are employed in effecting another type of output signal in the case of such a transmission containing more than one round of pulses.

Previously mentioned conductors **92, 114, 116** are connected to input sides of circuits **122, 128, 126**, respectively. Also connected to the input side of circuit **122** are cables **134, 136**. As will be explained more fullly shortly, cable **134** includes three conductors connected to the output side of code matrix **124**. Cable **136** includes three conductors, each connected to a different one of the three conductors previously mentioned in cable **120**. A nine-conductor cable **138** connects the input side of the code matrix with the nine different conductors previously mentioned in cable **118**.

The output of code latch circuit **122** is connected via a conductor **140** to the upper input of gate **130**, and via conductor **140** and a conductor **142** to the upper input of gate **132**. Circuits **126, 129** each include a pair of outputs. The lower output of circuit **126** is connected by a conductor **144** to the lower input of gate **130**, and also is connected through this conductor and a conductor **146** to the upper output of circuit **128**. The lower output of circuit **128** connects with the lower input of

gate 132 through a conductor 148, and connects through conductor 148 and a conductor 150 with the upper output of circuit 126. Conductors 146, 148 constitute inhibiting means herein. The outputs of gates 130, 132 are connected to conductors 152, 154, respectively.

Connected with conductors 92, 114, 116, and extending downwardly therefrom in FIG. 2 between blocks 50, 52, are conductors 156, 158, 160, respectively.

As a final correlation between FIGS. 1 and 2, the horizontal portion of cable 56 shown in FIG. 1 includes those portions of conductors 92, 114, 116, and of cables 118, 120, which extend horizontally into block 50 in FIG. 2. The vertical portion of cable 56 in FIG. 1 includes conductors 156, 158, 160, and the vertical portions of cables 118, 120, in FIG. 2. Cable 58 in FIG. 1 includes those portions of conductors 92, 114, 116, and of cables 136, 138, which extend into block 52 in FIG. 2.

Turning now to FIG. 3, this illustrates details of several of the components shown within block 52 in FIG. 2. Code matrix 124 is shown at the bottom of FIG. 3, and is depicted therein as a rectangular grid of crossed conductors including three vertically extending conductors 162, 164, 166, and nine horizontally extending conductors 168*a*-168*i*, inclusive. Where these conductors cross in the matrix, the presence of a black dot indicates a connection between the two crossing conductors, and the absence of such a dot indicates the absence of such a connection. Conductors 162, 164, 166 comprise the three conductors mentioned earlier which form cable 134. Conductors 168*a*-168*i* comprise the nine conductors mentioned earlier within cable 138.

Appearing to the right of the grid just described, adjacent the right ends of conductors 168*a*-168*i*, is a column containing the numbers 1-9, inclusive. These numbers have been included in the drawing to indicate the associations between conductors 168*a*-168*i* and the nine output terminals of pulse counter 74. In particular, conductor 168*a* is associated with that output terminal of the pulse counter which is placed in a 1 state with a count of "one" stored in the counter; conductor 168*b* is associated with that output terminal of the pulse counter on which a 1 state is placed with the counter storing a count of "two"; and so on. Such 1 states on the output terminals of the pulse counter result in 1 states also beiing placed on the respective associated ones of conductors 168*a*-168*i*.

It will be apparent that with a matrix such as that just described, programming is possible in accordance with the different codes that may be used by transmitters, simply through selection of the three locations where crossed wires in the matrix are connected. Matrix 124 is shown programmed for the code 2-3-1 which, of course, is associated with transmitter 18. Thus, connections exist between conductors 168*b*, 162, between conductors 168*c*, 164, and between conductors 168*a*, 166.

Code latch circuit 122 includes four three-input NAND gates 170, 172, 174, 176, and three conventional set-reset circuits shown as blocks 178, 180, 182.

The upper inputs of gates 170, 172, 174, are each connected as shown to previously mentioned conductor 92. The middle inputs of gates 170, 172, 174 are connected to conductors 184, 186, 188, respectively, which are the three conductors previously mentioned making up cable 136. The lower inputs of gates 170, 172, 174 are connected to previously mentioned conductors 162, 164, 166 respectively.

Conductors 184, 186, 188 are each connected to a different one of the three conductors previously mentioned within cable 120 (see FIG. 2). More specifically, conductor 184 is connected to that conductor in cable 120 which connects with the output terminal of counter 76 that is placed in a 1 state with a count of "one" stored in the counter; conductor 186 is connected to that conductor in cable 120 which is connected to the output terminal of the counter on which a 1 state is applied when the count of "two" is stored in the counter; and, conductor 188 is connected to that conductor in cable 120 which is connected to the other output terminal of counter 76.

The outputs of gates 170, 172, 174 are connected to the set terminals, marked S in FIG. 3, of circuits 178, 180, 182, respectively. The reset terminals of these circuits, marked R, are connected together to a suitable manual reset circuit (not shown) which may be operated, as will later be explained, to effect resetting of the circuits. The outputs of circuits 178, 180, 182 are connected as shown to the three inputs of gate 176. The output of gate 176 is connected to previously mentioned conductor 140.

Considering briefly the operation of the set-reset circuits, with such a circuit in a reset condition, a 0 state exists on its output. On a state change from 1 to 0 occurring at the set terminal of the circuit, the circuit is placed in a so-called set condition, wherein its output is placed in a 1 state. This situation remains until there is applied to the reset terminal in the circuit a state change from 1 to 0, whereupon the output of the circuit is returned to a 0 state.

Completing a description of what is shown in FIG. 3, previously mentioned alarm latch circuits 126, 128 comprise conventional electronic devices known as clocked-D flip-flops. Such a device typically includes set, reset, clock, and D inputs, and Q and $\overline{Q}$ outputs. In interpreter 48 herein, only four of such terminals are used, these being the reset, clock and D inputs, and the $\overline{Q}$ output. The reset inputs are marked by R, the clock inputs by C, the D inputs simply by D, and the $\overline{Q}$ outputs by $\overline{Q}$.

Explaining briefly how these devices perform, with such a device in a so-called reset condition, a 1 state exists on the $\overline{Q}$ output. With a state change of 0 to 1 occurring at the clock input, the $\overline{Q}$ output is placed in the opposite of whatever state then exists on the D input. For example, had a 0 state then been present on the D input, the voltage state on the $\overline{Q}$ output (initially in a 1 state) would remain unchanged. However, had the state on the D input been 1, the $\overline{Q}$ output would switch to a 0 state. A state change from 0 to 1 on the reset input returns the device to a reset condition.

The clock inputs of flip-flops 126, 128 are connected to previously mentioned conductors 116, 114, respectively. The reset inputs are suitably connected together to a suitable manual reset circuit like that mentioned above in connection with circuits 178, 180, 182. The D inputs of flip-flops 126, 128 are connected to conductors 150, 146, respectively, and the $\overline{Q}$ outputs of these devices are connected to conductors 144, 148, respectively.

The contents of block **54** (see FIG. **1**), and of the other such blocks in interpreter **48** which are associated with transmitters in the system other than transmitters **18, 20,** are substantially identical with those which have been described as being within block **52.** These other blocks differ from block **54** only with respect to the specific programmings provided in the code matrices therein which correspond to matrix **124.** In other words, these other code matrices are specially coded to relate to the specific codes associated with the different transmitters in the system. For example, the code maxtrix in block **54** is programmed in accordance with the code **1-4-3.** Considering how such programming would affect connections within a matrix, and referring back for a moment to FIG. **3,** had such a code been programmed into matrix **124,** conductor **168***a* would have been connected to conductor **162,** conductor **168***d* to conductor **164,** and conductor **168***c* to conductor **166.**

Finally, also connected to all of the reset terminals in all of the set-reset circuits and locked-D flip-flops in the interpreter, is a conventional, gated, automatic reset circuit (not specifically shown), which responds to each state change from 1 to 0 produced at the output of timer **66** to reset only those devices not then associated with an output block, such as block **52,** then producing an output signal. This arrangment positively places all such other devices in conditions properly to respond to succeeding transmissions.

5. Operational Description

Explaining now how system **10** and interpreter **48** therein perform, let us assume initially that no transmitter in the system is transmitting. Under such a condition, a 0 state exists on conductor **26,** as well as on conductors **84, 90, 92, 96, 98, 108.** The outputs of gates **78, 80** place 0 states on conductors **100, 114,** respectively, and the output of gate **82** places a 1 state on conductor **116.** With respect to pulse counter **74,** its nine output terminals which are associated with counts **1-9,** inclusive, are in 0 states, and this results in conductors **168***b*, **168***c*, **168***a* placing 0 states via conductors **162, 164, 166,** respectively, on the lower inputs of gates **170, 172, 174,** respectively. The other output terminal of counter **74** is in a 1 state. In counter **76,** only that output terminal associated with the count of "one" in the counter is in a 1 state--the other two output terminals each being in a 0 state. Thus, conductor **184** applies a 1 state to the middle input of gate **170,** and conductors **186, 188** apply 0 states to the middle inputs of gates **172, 174,** respectively.

The 0 state on conductor **92** is applied to each of the upper inputs of gates **170, 172, 174.** The 0 state on conductor **114** is applied to the clock input of flip-flop **128.** And, the 1 state on conductor **116** is applied to the clock input of flip-flop **126.**

The outputs of gates **170, 172, 174** are in 1 states, those of circuits **178, 180, 182** are in 0 states, and that of gate **176** is in a 1 state. The $\overline{Q}$ and D terminals of the flip-flops are all in 1 states. Consequently, the outputs of gates **130, 132** are each in a 0 state.

Considering what happens if a breakdown occurs in the sprinkler system which is being monitored by transmitter **18,** transmitter **18** is operated to produce in the telephone line a single round of pulses, with the code **2-3-1.** Such pulses, as they are produced on conductor **26,** are represented in Graph A in FIG. **4.** It should be appreciated that while each pulse shown in Graph A is represented as a true square wave pulse, in actual practice such pulses might have distinctly rounded corners, and other irregularities causing them to deviate from true square waves.

The positive-going or leading edge of each pulse on conductor **26** causes input circuit **62** to generate a corresponding controlled-duration follower pulse. Such follower pulses are shown in Graph B in FIG. **4,** and include pulses **190, 192, 194, 196, 198, 200** which are produced as the result of pulses **36, 38, 40, 42, 44, 46,** respectively, shown in Graph A. The time alignments between pulses in Graphs A and B are clearly apparent in FIG. **4.** Each pulse in Graph B has a closely controlled duration (shown at T_4) of about 0.05-seconds, as has been mentioned earlier.

One of the important advantages of employing circuit **62** to produce such follower pulses, is that the duration-controlled follower pulses serve to minimize the potential error-producing effects of the time irregularities present in the actual pulses present on conductor **26.**

With initiation of pulse **190,** timers **64, 66** are triggered, whereupon they place 1 states on conductors **90, 98,** respectively. This situation is illustrated in Graphs C and F, respectively, in FIG. **4** which show the voltage conditions in conductors **90, 98,** respectively. This state change on conductor **98** causes a 1 state to be applied via conductors **104, 106, 112** to the upper inputs of gates **80, 82,** whereupon gate **82** places a 0 state on conductor **116.** This situation is illustrated in Graph H in FIG. **4** which depicts the voltage condition on conductor **116.** The output of gate **80** remains 0. No other change of consequence occurs at this time.

The negative-going or trailing edge of pulse **190** causes a state change from 1 to 0 on the counting terminal of pulse counter **74,** which action results in counter **74** counting up to a count of "one." As a consequence, a 1 state is applied through conductors **168***a*, **166** to the lower input of gate **174** in code latch circuit **122.** However, this state change produces no consequential effect.

Timers **64, 66** remain in conditions with 1 states on their outputs until the occurrence of the next follower pulse, **192,** because of the fact that the time intervals between pulses **190, 192** is less than the respective "time-out" times of these timers. More specifically, the time interval between pulses **190, 192** is about 0.45-seconds. The time-out time of timer **64,** shown at T_5 in Graph C, is about 0.6-seconds, and the time-out time of timer **66,** shown at T_8 in Graph F, is about 1-second.

Initiation of pulse **192** retriggers timers **64, 66,** and their outputs remain in 1 states. The outputs of gates **80, 82** remain in 0 states. The trailing edge of pulse **192** increases the count in counter **74** to the count of "two." This change results in the lower input of gate **174** returning to a 0 state, and in the application via conductors **168***b*, **162** of a 1 state to the lower input of gate **170.**

Because of the considerably larger time gap which exists between pulses **38, 40** as compared with the gap between pulses **36, 38,** follower pulse **194,** which is related to pulse **40,** begins too late in time to retrigger timer **64** soon enough to maintain the output terminal of this timer in a 1 state. Referring to Graph B in FIG. **4,** the time interval between pulses **192, 194** is about 0.7-seconds. Thus, and as can be seen in Graph C, at

about 0.6-seconds after the end of pulse **192**, timer **64** times out, and a state change from 1 to 0 occurs on its output and on conductor **90**.

There thus results in Graph C a pulse **202** which serves to identify and distinguish the completion of a single pulse section (section I) in the round of pulses now being transmitted by transmitter **18**. The state change just mentioned which occurs at the trailing edge of pulse **202** triggers read pulse generator **70**, which then produces a positive pulse shown at **204** in Graph D in FIG. **4**. The duration of this pulse, indicated by T_6, is about 0.015-seconds.

Pulse **204** places a momentary 1 state on both conductors **92, 94**. As a consequence, there is a momentary situation where 1 states exist simultaneously on all three of the inputs of gate **170**. The 1 state on the upper input of this gate results, of course, from the momentary 1 state on conductor **92**. The 1 state on the middle input of the gate results from the 1 state initially applied, and still applied, via conductor **184** from the output terminal of section counter **76** associated with the count of "one" in this counter. The 1 state on the lower input of the gate results, as was previously mentioned, from the fact that a count of "two" now exists in counter **74**.

The result of this situation is that a momentary 0 state is applied by gate **170** to the set input of circuit **178**, whereupon the output of this circuit switches to and latches in a 1 state, which is applied to the upper input of gate **176**.

Thus, the circuitry just discussed in interpreter **48** has correctly distinguished the first pulse section in the transmission from transmitter **18**, has read the number of pulses in this section, which number is stored as the count of "two" in counter **74**, has compared this number of pulses with that for which the various blocks, like block **52**, have been programmed to respond to, and has produced what might be thought of as a memorized response in block **52**. It will be apparent that no such memorized response would have occurred in block **52** had this block been programmed for a first code number other than 2, or had the first-read pulse section contained other than two pulses.

The trailing edge of pulse **204** triggers reset circuit **72**, which then produces a pulse such as that shown at **206** in Graph E in FIG. **4**. Pulse **206** has a duration, indicated at T_7, of about 0.015-seconds.

As a consequence, a momentary 1 state is applied to the upper input of gate **78**. The lower input of this gate is also now in a 1 state because of the fact that code timer **66** is still in a condition supplying a 1 state to conductor **98**. The reason for this, of course, is that the time interval between follower pulses **192, 194** (about 0.7-seconds) is less than the time-out time (about 1-second) of timer **66**. Thus, a momentary 1 state is applied to the output of gate **78**, and via conductors **100, 102** to the counting and reset terminals, respectively, of counters **76, 74**, respectively. Counter **74** is then reset to a zero-count condition, and counter **76** counts up to a count of "two." This change in counter **76** results in a 0 state being placed on conductor **184**, and a 1 state being placed on conductor **186**.

The various operations which then take place within the interpreter, as the second and third sections of pulses in the transmission from transmitter **18** are received, are similar to those which have just been described. Thus, and referring to Graph C in FIG. **4**, timer **64** produces a pulse **208** which identifies and distinguishes section II, and a later pulse **210** which identifies and distinguishes section III. Throughout the production of these other two pulses in Graph C, timer **66** continues to supply a 1 state at its output, and gates **80, 82** continue to supply 0 states at their outputs.

During receipt of the second section of the transmission, which section contains pulses **40, 42, 44**, pulse counter **74** counts up to a count of "three," whereupon it places a 1 state via conductors **168c**, **164** to the lower input of gate **172**. As was previously mentioned, because of the fact that section counter **76** now stores a count of "two," a 1 state is applied via conductor **186** to the middle input of gate **172**. At the conclusion of pulse **208** in Graph C, read pulse generator **70** is again triggered, this time to produce a pulse **212** which is like pulse **204**, and which places a momentary 1 state on the upper input of gate **172**. Thereupon, circuit **180** latches into a condition supplying a 1 state to its output, and to the middle input of gate **176**. At the conclusion of pulse **212**, reset circuit **72** is again triggered, and produces a pulse **214** which is like previously mentioned pulse **206**. Pulse **214** results in the application of a pulse from the output of gate **78** which resets counter **74** to a zero-count condition, and places counter **76** in a condition storing the count of "three."

Thus, the second section of pulses is identified, read, and responded to in the code latch circuit. Similar action takes place with respect to the third section containing pulse **46**. Identifying and reading of this third section ultimately results in circuit **182** latching in a condition applying a 1 state to its output terminal, and to the lower input of gate **176**. And, at this time, the output of gate **176** switches from 1 to 0 which state change is sustained and applied via conductors **140, 142** to the upper inputs of gates **130, 132**. However, no change as yet occurs on the outputs of these two gates.

The reset pulse which results following identification and reading of pulse section III, resets counter **74** again to a zero-count condition, and returns a count of "one" to counter **76**. Thus, counter **76** is returned to a proper condition for monitoring the first pulse section of another round of pulses.

In the system operation which has just been described, it will be recalled that transmitter **18** transmitted but a single coded round of pulses. Therefore, follower pulse **200** was the last follower pulse to be generated. Accordingly, about 1-second after the end of this pulse, timer **66** times out, and returns a 0 state to its output, and to conductor **98**. This is clearly illustrated in Graph F in FIG. **4**. The state change from 1 to 0 which thus occurs on conductor **98** is applied to the input of timer **68**, to the lower input of gate **78**, and to the upper inputs of gates **80, 82**.

With respect to gate **78**, the return of a 0 state to its lower input closes the gate, and, in effect, locks the output of the gate in a 0 state. This assures that counter **76** will remain in the condition to which it has been returned (and which it had initially) storing a count of "one." With respect to timer **68**, the state change from 1 to 0 on the output of timer **66** triggers timer **68** into producing a positive voltage pulse shown at **220** in Graph G in FIG. **4**, which pulse lasts about 0.75-seconds, indicated by T_9. Thus, there is now a 1 state applied from the output of timer **68** to the lower inputs of gates **80, 82**, and a 0 state applied to the upper inputs

of these gates. As a consequence, the ouput of gate **80** remains in a 0 state--the state which it has had all along--and the output of gate **82** remains in a 0 state---the state to which it was initially switched on initiation of follower pulse **190.**

No further action of interest occurs until completion of pulse **220,** whereupon timer **68** returns a 0 state to its output terminal, which state is then applied to the lower inputs of gates **80, 82.** The output of gate **80** remains in a 0 state. However, and as is illustrated in Graph H, the output of gate **82** is switched from 0 to 1. Such switching results in clocking of device **126,** with consequent placement of a 0 state on its $\overline{Q}$ output. This 0 state is applied via conductor **144** to the lower input of gate **130,** and via conductor **144** and conductor **146** to the D input of device **128.**

A situation now exists with 0 states applies to both inputs of gate **130,** whereupon the output of this gate switches from 0 to 1 and applies a 1 state to conductor **152.** Such switching is referred to herein as an output signal from the interpreter of one type, which output signal may be utilized in any suitable fashion to indicate the information just transmitted by transmitter **18.** The application of a 0 state to the D input of device **128** inhibits this device from producing any change on its $\overline{Q}$ output should anything effect clocking of device **128.** Such inhibiting is important in preventing an improper output signal from now being produced through gate **132.** The output of gate **132** remains in a 0 state.

At the completion of such operation, and when the output signal just produced has been noted, the manual reset circuits mentioned earlier are operated to reset circuits **178, 180, 182,** and devices **126, 128.**

FIG. **5** illustrates what happens in the event of transmitter **18** operating to transmit a plurality of successive rounds of pulses, as in the case of its reporting a fire. As can be seen from a comparison of FIGS. **4** and **5,** the operation within the interpreter up through the beginning of pulse **220** is identical in both cases. Immediately following the leading edge of pulse **220:** gate **78** is closed by virtue of there being a 0 state on its lower input; a 1 state is applied to the lower inputs of gates **80, 82,** and a 0 state to the upper inputs of these gates; and the outputs of gates **80, 82** are in 0 states. Conductors **140, 142** apply 0 states to the upper inputs of gates **130, 132,** and the $\overline{Q}$ outputs of devices **126, 128** apply 1 states to the lower inputs of gates **130, 132,** respectively.

Graph A in FIG. **5,** at the right side thereof in the figure, shows the beginning of the next successive round of coded pulses transmitted by transmitter **18.** More specifically, this graph shows the beginning of a new section I in such a round, including pulses **222, 224.** With transmittier **18** constructed as was previously described, the nominal or expected time between successive rounds, shown at T_3 in graph A, is about 1-second. However, as can be seen in Graph A, the actual time between the end of pulse **46** and the beginning of pulse **222** is somewhat greater than this nominal time.

For each of pulses **222, 224,** circuit **62** produces a related follower pulse, such being shown at **226, 228,** respectively, in Graph B. It is the leading edge of pulse **226** which is significant at this time. This leading edge results in triggering of timer **66** to return a 1 state to its output. This is shown in Graph F. Such return of a 1 state results in the placement of 1 states on the upper inputs of gates **80, 82.** This change has no effect with respect to gate **82,** which continues to supply a 0 state at its output. However, in gate **80,** its output is switched from 0 to 1, as indicated by Graph I in FIG. **5.**

This action, then results in clocking of device **128** to produce a 0 state on its $\overline{Q}$ output. As a consequence, a 0 state is applied both to the lower input of gate **132,** and to the D input of device **126.** Placement of such a state on the D input of device **126** inhibits any change in the 1 state now existing at the $\overline{Q}$ output of device **126.** Placement of a 0 state on the lower input of gate **132** causes the output of this gate to switch to a 1 state which is applied to conductor **154.** Such switching constitutes another type of output signal from the interpreter, which may be utilized in any suitable manner to indicate the specific information transmitted from transmitter **18.**

With noting of this output signal, manual resetting, as mentioned above, is performed.

It will thus be apparent that the interpreter of the present invention, through examining the major time differences which exist between successive pulses transmitted in a system, accurately and reliably discerns different groups or rounds of pulses, different sections within rounds, and the code numbers associated with such sections. For each different transmitter in a system it provides two different discrete outputs for indicating, both, which specific transmitter has transmitted, and what specific information it has conveyed.

The interpreter immediately indicates whether a transmission from a given transmitter comprises one round, or more than one round. Human intervention is not required in the interpreting operation.

While a preferred embodiment of the invention has been described herein, it is appreciated that variations and modifications may be made without departing from the spirit of the invention.

It is claimed and desired to secure by letters patent:

1. An interpreter for use in an electrical signaling system of the type which includes a transmission line and a plurality of coded signalers operatively connected to said line, each signaler being operable selectively to produce and transmit over said line one or more like-coded groups of time-spaced electrical pulses, with each such group including a plurality of pulse sections each containing one or more pulses depending upon the particular code associated with the signaler, with the times between adjacent pulses in a section under all circumstances being shorter than the times between adjacent sections in a group, and with the latter-mentioned times under all circumstances being shorter than the times between successive groups produced by the signaler, said interpreter in operative condition comprising

a code-reading circuit operatively coupled to said line and constructed to read the particular code of each coded group of pulses transmitted in the line,

a code-discriminating circuit for each different signaler in the system, each operatively connected to said code-reading circuit and operable to indicate a reading by the latter of the particular code associated with the code-reading circuit's associated signaler,

a pulse-group-spacing-monitoring circuit operatively coupled to said line and constructed to respond to

the transmission therein of coded groups of pulses, and to generate, following the completion of such a group, a response of one type if another coded group of pulses follows within a preselected time span, and a response of another type if no such successive group follows within said preselected time span, and

an output circuit for each code-discriminating circuit operatively connected thereto and to said pulse-group-spacing-monitoring circuit, each operable, with its associated code-discriminating circuit indicating a reading of its associated code, to produce an output signal of one type on said pulse-group-spacing-monitoring circuit generating a response of said one type, and to produce an output signal of another type on the pulse-group-spacing-monitoring circuit generating a response of said other type,

each output circuit including means inhibiting the simultaneous production thereby of both types of output signals.

2. The interpreter of claim **1** which further includes an input circuit operatively connected between said line and said code-reading and pulse-group-spacing-monitoring circuits for processing pulses transmitted in the line for inputting into the latter-mentioned two circuits, said input circuit being constructed to generate, for each pulse transmitted by a signaler in the system, a time-related, controlled-duration follower pulse.

3. The interpreter of claim **1,** wherein said code-reading circuit includes: a timing circuit for discerning and identifying the different pulse sections in a coded group of pulses through monitoring the time spacings between successive pulses in a group to locate a spacing greater than that expected between adjacent pulses in a section but less than that expected between adjacent sections in a group; a read pulse generator operatively connected to said timing circuit for generating a read pulse on the timing circuit identifying a section in a group; a resettable pulse counter operatively connected both to said line and to said read pulse generator, constructed to count pulses transmitted in the line, and to be reset to a zero-count condition on each occurrence of a read pulse; and a resettable section counter operatively connected to said read pulse generator for counting read pulses generated thereby.

4. The interpreter of claim **3,** wherein each code-discriminating circuit comprises a memory programmed in accordance with the code associated with the code-discriminating circuit, each memory being operatively connected to said read pulse generator and to said counters, and being operable to produce a sustained indication following, but only following, receipt over said line of a group of pulses coded in accordance with the code associated with the memory.

5. The interpreter of claim **1,** wherein said pulse-group-spacing-monitoring circuit includes: a timing circuit for discerning and identifying different successive coded groups of pulses through monitoring the time spacings between successive pulses transmitted in the line to locate a spacing greater than that expected between adjacent sections in a group but less than that expected between successive like groups transmitted by a signaler; and an interval decision circuit operatively connected to said timing circuit for following the intervals between successive pulse group identifications by said timing circuit, said interval decision circuit effecting generation by said pulse-group-spacing-monitoring circuit of a response of said one type on said timing circuit identifying the beginning of a new pulse group within a preselected interval following its previous identification of a pulse group, and effecting a response by said pulse-group-spacing-monitoring circuit of said other type under all other circumstances.

6. In an electrical signaling system of the type which includes a transmission line, and a plurality of coded signalers operatively connected to said line, each signaler being operable selectively to produce and transmit over said line one or more like-coded groups of time-spaced electrical pulses, with each such group including a plurality of pulse sections each containing one or more pulses depending upon the particular code associated with the signaler, with the times between adjacent pulses in a section under all circumstances being shorter than the times between adjacent sections in a group, and with the latter-mentioned times under all circumstances being shorter than the times between successive groups produced by the signaler, an interpreter comprising

a code-reading circuit operatively coupled to said line and constructed to read the particular code of each coded group of pulses transmitted in the line,

a code-discriminating circuit for each different signaler in the system, each operatively connected to said code-reading circuit and operable to indicate a reading by the latter of the particular code associated with the code-reading circuit's associated signaler,

a pulse-group-spacing-monitoring circuit operatively coupled to said line and constructed to respond to the transmission therein of coded groups of pulses, and to generate, following the completion of such a group, a response of one type if another coded group of pulses follows within a preselected time span, and a response of another type if no such successive group follows within said preselected time span, and

an output circuit for each code-discriminating circuit operatively connected thereto and to said pulse-group-spacing-monitoring circuit, each operable, with its associated code-discriminating circuit indicating a reading of its associated code, to produce an output signal of one type on said pulse-group-spacing-monitoring circuit generating a response of said one type, and to produce an output signal of another type on the pulse-group-spacing-monitoring circuit generating a response of said other type,

each output circuit including means inhibiting the simultaneous production thereby of both types of output signals.

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