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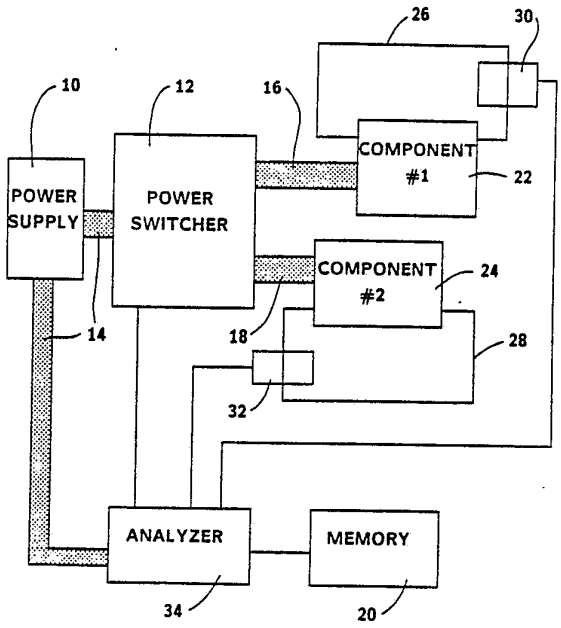
(54) Title: ADAPTIVE ELECTRICAL POWER MANAGEMENT SYSTEM




(57) Abstract

An electrical power management system for electronic devices (22 and 24) which includes partitioned power buses (16 and 18) that power various components (component ,1 and component ,2) within the electronic device (22 and 24) such that power supply (10) to such components (component ,1 and component ,2) can be independently controlled. The system monitors (34) use of such components (component ,1 and component ,2) and provides power to such components (component ,1 and component ,2) only as needed.

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# ADAPTIVE ELECTRICAL POWER MANAGEMENT SYSTEM

## Background of the Invention

### Field of Invention

This invention relates generally to electrical power systems in battery-operated electronic devices, and more particularly to an electrical power management system that controls power consumption of various components within an electronic device so as to conserve power use and prolong battery operation.

### Description of Prior Art

Numerous electronic devices today can be operated on battery power. Due to electrical demands within the such devices, e.g., portable computers, to power components such as disc drives, display screens, back light elements, etc., operation of such devices on battery power alone is limited.

Prior art in computer technology allows the user to manually turn off various elements within the computer which are not needed (e.g., modems can be deactivated by the user in most portable computers) and some computers allow the display screen to be powered down after a specified time period during which the computer receives no user input (this is called a time-out procedure).

It would be desirable to have an electrical power management system that automatically powers components of an electronic device on and off, or reduces power

consumption of such components based on the operational requirements of the device and the needs of the user.

Summary of the Invention

The invention provides a means to conserve power consumption in a battery operated electronic device by determining when a component within the device is not required to be fully powered, a determination that is based on the operation of the electronic device. The invention involves monitoring operation of the electronic device and analyzing the power consumption of components within the device. The invention uses algorithms to recognize information which indicates that a given component or group of components is not operationally required and can be powered down. The power supply to the component or group of components is partitioned so that the component or group of components can be powered down without affecting the power consumption of other components within the electronic device.

As used in this specification, powered down includes turning power completely off or any other power conservation state that is less than full power on (such as reducing the clock speed in a computer which affects the power consumption of components interrelated to the clock speed).

The algorithms employed in the invention can analyses a broad variety of software instructions without any prior knowledge or experience with such software permitting the power management system to automatically operate while running most software that is used today.

In addition, the invention may employ adaptive techniques which allow the user to instruct the power management system when it has made an error in a power management decision; once instructed, the power management system adapts itself so that the proper power management decision is made the next time.

Components within the electronic device are powered on or down as needed during operation of the device. This yields prolonged operation of the electronic device on battery power.

Brief Description of the Drawings

FIG. 1 is a block diagram of a partitioned power circuit showing two partitioned power buses controlled by an analyzer and power switcher, and two components, one connected to each of the two partitioned power buses.

FIG. 2 is a flow chart of the operation of the adaptive electrical power management system.

Detailed Description of the Preferred Embodiments

Referring now to the drawings, therein like numerals represent like or corresponding elements throughout the several views, there is shown in FIG. 1 the elements of an electronic device which incorporates the invention, showing a main power supply 10, a main power bus 14, a power switcher 12 which controls power to two partitioned power buses 16 and 18, each partitioned power bus being connected to a component 22 and 24 respectively, and the analyzer 34 which controls the power switcher.

Main power to the electronic device is supplied by the main power supply 10 which constitutes a battery operated type power supply. The main power supply 10 feeds electrical power to the main power bus 14 which supplies electrical power to the power switcher 12 and the analyzer 34.

Hardware implementations of the analyzer 34 could include a processor, an auxiliary microprocessor (such as a Motorolla 68HC11); a logic cell array (such as a conventional Xylink M2018 logic cell array); a macro cell array (such as a conventional LSI Logic Corporation LL3020 macro cell array); an application-specific integrated circuit; a gate array; or other forms of mask programmable logic. The analyzer controls power consumption of the

components. As shown in FIG. 1 the control of power consumption of the components is a function of controlling the partitioned power buses. This method of control is the basis for the description that follows. However, the analyzer 34 could control other elements such as a switch on the component itself, or an element such as the clock in a computer, that would control the rate of power consumption of a component as a means of managing power consumption.

Components or elements of the electronic device 22 and 24 are connected to the partitioned power buses, 16 and 18 respectively, and are independently powered by such buses.

The path of instruction flow for each component is shown on FIG. 1 as 26 and 28 respectively. Each path is monitored by the analyzer 34 through instruction detectors 30 and 32.

The analyzer 34 monitors all systems within the device to determine whether components are needed or not for operation of the device. FIG. 1 shows just two components within the device. There could be many more components or groups of components that are monitored.

A memory element 20 is also controlled by the analyzer 34. The memory stores the state of a component prior to that component being powered down so that that state can be reinstalled in the component prior to its being powered up. The memory function is only used if the state of a component needs to be saved and restored during a power down cycle.

FIG. 2 is a flow chart showing the operation of the adaptive power management system. At step 100 a given component within the device is powered on. At step 101 the analyzer monitors information related to the operation of the device. The analyzer looks for a pattern that indicates that a component is not being used. The analyzer's ability to recognize such a pattern is based on algorithms. Recognition of such a pattern answers the

question of whether the component is needed or not, step 102.

If the component is needed, step 103, the analyzer continues to monitor operation of the device to determine if the component continues to be needed, step 101. If the component is not needed, step 104, the component power down sequence commences, step 105.

If the component's state is needed once the component is powered on again, the state of the component is saved in memory before the component is powered down so that that state can be reinstalled prior to re-establishing power to the component, step 105. Once the component state is saved, the component is powered down either through the power bus that serves the component or at the component itself. Components on the main power bus and other partitioned power buses are not affected.

In step 106, the analyzer continues to monitor operation of the device for information indicating that the component is needed again. The analyzer continually checks to see whether the component is needed, step 107. If the component is not needed, the analyzer continues its monitoring function, step 106.

If the component is needed, step 108, the component power up sequence commences, step 109. If the state of the component had been stored in memory, that state is reinstalled in the component and the power to the partitioned bus serving the component is re-established. The component returns to a powered on status, step 111.

The process of monitoring and analyzing operation information and powering components up and down continues during operation of the electronic device. Components are only powered down when they are inactive or not needed. The result is less power consumption by the electronic device.

Claims

1. An electrical power management system for a battery powered electronic device, comprising:

a. at least one component the power consumption of which can be controlled;

b. monitoring and analyzing means for determining when said component is not required to be fully powered;

c. means for regulating the power consumption of said component.

2. The apparatus defined in claim 1 wherein the monitoring and analyzing means comprises a device selected from the group consisting of a processor, microprocessor, a logic cell array, a macrocell array, an application-specific integrated circuit, a gate array, and a mask programmable logic device

3. The apparatus defined in claim 1 wherein the monitoring and analyzing means comprises resident software.

4. The apparatus defined in claim 1 wherein the monitoring and analyzing means further comprises memory means for storing the state of a said component prior to powering down said component and for restoring the state of said component upon power up of said component.

5. The apparatus defined in claim 1 wherein the means for regulating the power consumption of said component further comprises:

a. at least one partitioned electrical power bus to which said component is operatively connected; and

b. a regulator means which can control the electrical power to said partitioned electrical power bus.

6. The apparatus defined in claim 1 wherein the means for regulating the power consumption of said component comprises means for changing the components rate of operation.

7. The apparatus defined in claim 1 wherein the means for regulating the power consumption of said component comprises a switch on said component.

8. A method of managing the consumption of electrical power in a battery powered electronic device comprising the steps of:

a. monitoring operation of said device to determine whether said component is required;

b. recognizing when a component is not required;

c. saving the state of the component in the computer's memory, if such state is necessary when the component is powered on again;

d. reducing power consumption of said component;

e. recognizing when said component is required;

f. restoring the state of said component if said state had previously been saved; and

g. restoring power to said component

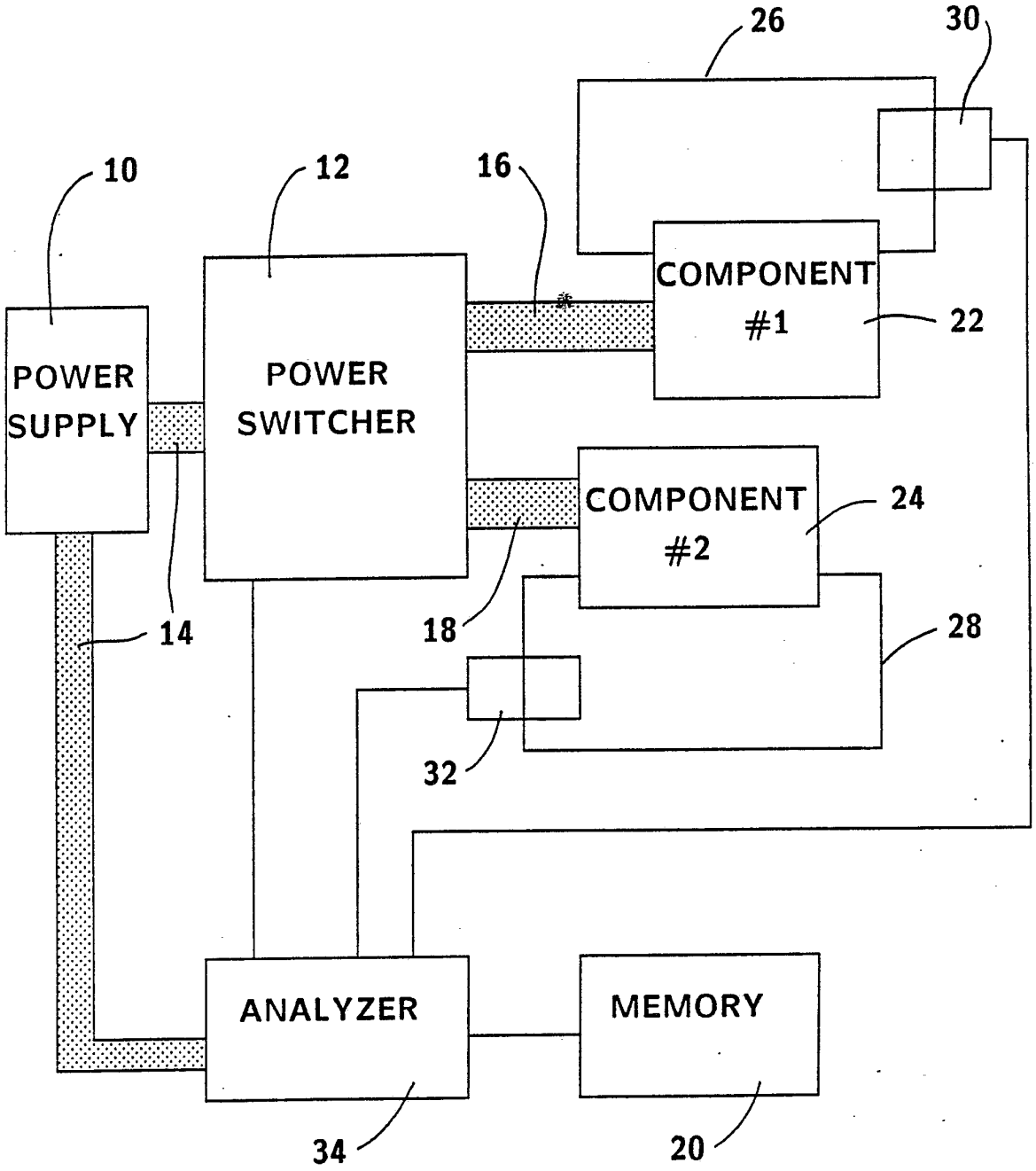
26
30
10
12
16
COMPONENT
#1
22
POWER
SUPPLY
POWER
SWITCHER
COMPONENT
#2
24
14
18
28
32
ANALYZER
MEMORY
34
20

FIG. 1

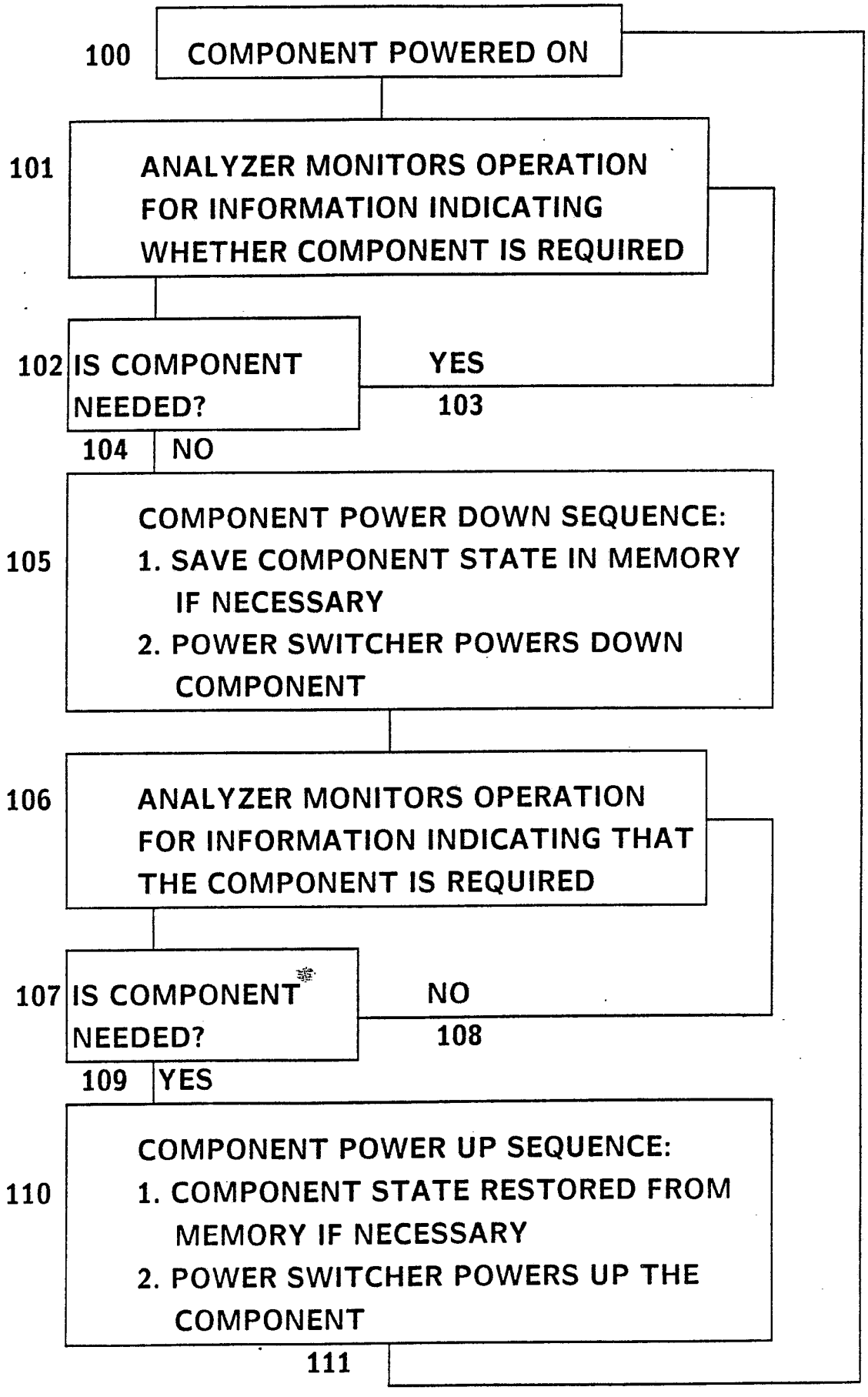


FIG. 2

SUBSTITUTE SHEET

# INTERNATIONAL SEARCH REPORT

International Application No. PCT/US89/05661

## I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC (5) H02J 3/14

U.S. CL. 307/126

## II FIELDS SEARCHED

Minimum Documentation Searched [7]

| Classification System | Classification Symbols |
|---|---|
| U.S. | 307/34-40, 10.7, 126<br>340/310R, 310CP, 310A<br>365/226, 227, 228, 229 |

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

## III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

| Category * | Citation of Document, [11] with indication, where appropriate, of the relevant passages [12] | Relevant to Claim No. [13] |
|---|---|---|
| X | US,A, 4,747,041 (Engel et al)<br>24 MAY 1988 ( SEE ENTIRE SPECIFICATION) | 1-8 |
| X | US,A, 4.639,609 (Floyd et al)<br>27 January 1987 ( SEE ENTIRE SPECIFICATION) | 1-8 |
| A | US,A, 4,593,349 (Chase et al)<br>03 June 1986 (SEE ENTIRE SPECIFICATION) | NONE |
| A | US,A, 4,371,789 (Chen et al)<br>01 February 1983 ( SEE ENTIRE SPECIFICATION) | NONE |
| A | US,A, 4,137,557 (Ciarniello et al)<br>30 January 1979 (SEE ENTIRE SPECIFICATION) | NONE |

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## IV. CERTIFICATION

| Date of the Actual Completion of the International Search | Date of Mailing of this International Search Report |
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