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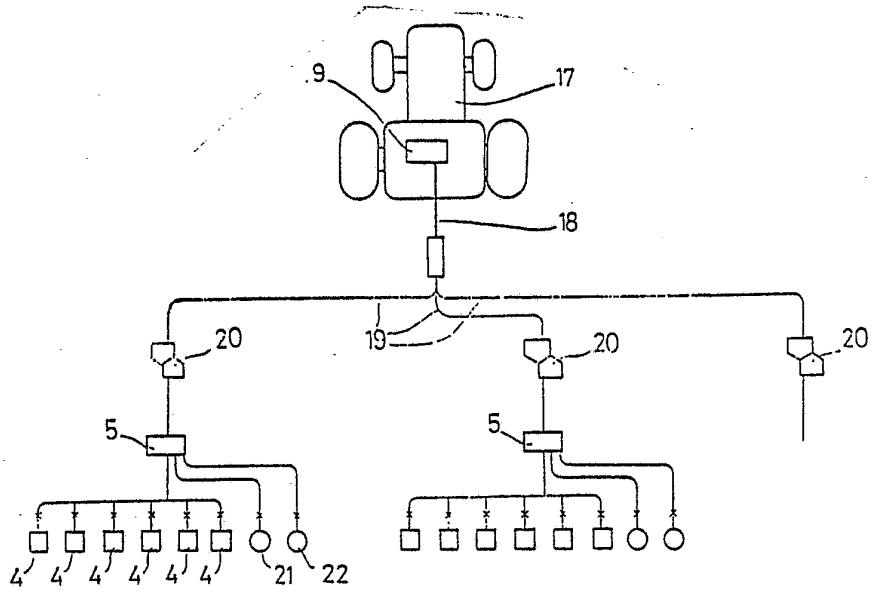
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(54) Title: SEED CONTROL APPARATUS WITH A MICROPROCESSOR



(57) Abstract

The seed control apparatus contains photoelectric seed-detectors, devices for measuring the distance covered, display and operating organs, data and control busses, buffer memories, a power supply unit, as well as a microprocessor system consisting of the microprocessor, program and data memories and the interface circuit inserted between the data bus and the detecting organs. In addition of the performance of the usual functions the microprocessor is programmed for counting operations. Between the microprocessor system and the detecting organs a programmable parallel input/output interface circuit interfacing the outputs of the detecting organs to the data bus of the microprocessor, as well as a signal level interface circuit each for the single detectors are inserted.

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Seed control apparatus with a microprocessor

Technical field

The invention relates to an apparatus with a microprocessor for the control of seeders. The apparatus contains photoelectric seed detectors, a device for measuring the path covered, display and operating organs, data and control busses, buffers, a power supply unit as well as a microprocessor system consisting of the interface circuits being inserted between the detector organs and the data bus.

Background art

Several solutions have been developed for the control of seeding machines during operation, some of them are described in the publication "Heavy-duty seeding machines" (Harangozó L. and al., Agricultural Publishing House, Budapest, 1980. pages 154-161). With these equipments fall through of the seeds is controlled by photocells or by the aid of photoelectric means, while the electric pulses generated in this way are forwarded to a central unit. Recently seed control apparatus based on microprocessor

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control are available, e.g. the type H 216 of Hessel (GFR). The aim of the known solutions has been to promote the precise performance of seeding technologies at the rows and stocks, simultaneously to enable seeding work at night. To fulfil the task set, the seed control apparatus has to deliver a series of information to the operator in course of the seeding process. In case of a failure, e.g. the clogging of the seed-pipe, the number of the seeds being less or more, than the prescribed quantity, the serial number of the defective furrow splitter, the effective number of stocks and stock distance, in case of a multiple failure the number of the defective furrow splitters are to be signalled visually and/or acoustically.

In course of normal operation, the following informations are needed by all means: the number of the seeds sown for each furrow splitter since starting the process, the effectively covered distance and the average number of seeds pro hectare. In addition to these, the seed control apparatuses must be compatible with several types of seeding machines, i.e. they could be adapted to different furrow splitter numbers and diverse diameters of the land wheels.

In general, the seed control apparatuses are meeting the requirements enumerated above in such a manner that the parameters qualifying the performance of seeding technologies are controlled by counting the pulses coming from the photoelectric seed detectors and the signal transmitters measuring the distance covered, and in case of failures the occurence, the place and extent are signalled visually and/or acoustically. In the known apparatuses the usual

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components, i.e. the programmable counter circuits recommended by the manufacturers of the microprocessor are used for performing the counting functions. These counter circuits - contained in a house - comprise one to three relatively high speed counter stages of 8 to 16 bits. Since with a seed control apparatus the pulses of a plurality of signal sources (detectors) are to be counted, the known solutions working with the usual components require a lot of circuit elements resulting in a voluminous apparatus. If in addition to this the electric characteristics of the signal sources are not even µP-compatible, due to the high number of the required interface circuits a further increase in the number of elements is to be reckoned with.

When a task cannot be solved with a counter of usual capacity, i.e. 16 bits, further supplementary circuits are needed. It goes without saying that increase in volume and numbers of elements disadvantageously influences investment costs and operational safety.

Disclosure of invention

The aim of the invention is to eliminate the above mentioned drawbacks and to develop a seed control apparatus which is able to realize the required functions with less components, accordingly with a lower cost expenditure with the simultaneous increase of operational safety.

In accordance with the invention, the microprocessor is programmed in addition to the usual functions for counting operations, furtheron between the microprocessor system and the dececting organs a programm-

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able parallel input/output interface circuit for interfacing the output of the detecting organs to the microprocessor as well as for each of the detecting organs a signal level interface unit are inserted.

A preferred embodiment of the invention contains signal level interface units which are formed as pulse shaping units.

With a further preferred embodiment of the invention monostable flip-flops are applied as signal level interfaces or pulse shaping units respectively.

Brief Description of Drawings

The invention will be described in details by means of a preferred embodiment, by the aid of the enclosed drawings, wherein:

Figure 1 is a block diagram showing a traditional counter interface inserted between the detectors and the microprocessor system,

Figure 2 is a block diagram showing the interface circuit according to the invention,

Figure 3 the time diagram of the pulse train output of a detector,

Figure 4 is a block diagram showing the seed control apparatus containing the interface circuit according to the invention,

Figure 5 shows schematically the connections between the seed control apparatus with the microprocessor according to the invention and the seeding machine.

Best Mode of Carrying out the Invention

The traditional counter interface circuit demonstrat-

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ted in figure 1 is processing, e.g. in case of a corn seeder with eighteen furrow splitters, the output signals of the signal transmitters - not shown here - of eighteen seed detectors for the microprocessor system and contains 18 + 2 interface elements 1, 18 precounters 2 and 6 + 1 programmable counter interfaces 3 comprising three 16-bit counter stages. The price of the totally seven programmable counter interfaces 3 represents a considerable proportion of the investment costs of the apparatus. At the same time, the capacity of these expensive circuits, at least as regards to the counter frequency, is far not utilized, since the frequency of the output pulses of the seed detectors are generally of the order of magnitude of 1o.....100 Hz. Counting of the signals of a relatively low frequency can be solved far cheaper by using the data-memory of the microprocessor combined with a software-promoted cyclical sampling, if an information-receiving interface circuit according to the invention is applied which requires elements in a minimal number and minimal volume, the block diagram of which is illustrated in Figure 2. With this arrangement the output signals of the signal transmitters of the detectors - not illustrated here - arrive via twenty-four signal level interface units 4 to the inputs of the programmable parallel interface circuit 5, i.e. to the input/output pins thereof. This latter circuit alone is able to interface twenty-four input signals to the data bus 6 leading to the microprocessor not illustrated here. The microprocessor informs said interface circuit 5 via the control bus 7 which input 8 out of the twenty-four inputs should be enabled in a given moment. When compared to the traditional solution according to Figure 1, it becomes obvious that

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considerably less components are needed, in particular, when considering that the twenty-four signal level interface units 4 can be assembled of two inverters each, consequently, merely twelve IC (e.g. of type CD 4011) containing four NAND-gates or eight IC containing inverters (e.g. of type CD 4009) are required.

Accordingly, by using the circuit shown in Figure 2, one programmable interface IC 3 (e.g. INTEL 8255) enables the input of sixteen to twenty-four signals. In case, when the detectors are delivering too narrow pulses, it seems to be expedient to design the signal level interface units 4 so that they should be suitable for pulse shaping when operated e.g. in a monostable mode of operation.

In order to ensure that all the pulses arriving from a detecting organs be counted, the time constant t_m of the monostable circuit, i.e. the increased pulse width should surpass the original pulse width t_j, but should be shorter, than the half of the period of repetition T, at the same time, the periodical time of sampling T_m should be shorter, than t_m. These corrédations are shown in Figure 3, wherein

T = the minimal periodical time of the signal to be processed,

t_j = the original width of the signalling pulse,

t_m = the period of the signal, increased by the monoflop circuit,

T_m = periodical time of sampling.

The instruction execution time being characteristic for the microprocessor, the number of the signal transmitters and detectors, the magnitude, number

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and time requirement of the task set for the microprocessor are restricting the period of sampling to be obtained by interrupts and thus the highest frequency of the signal to be received.

One of the embodiments of the seed control apparatus containing the interface circuit according to the invention is based on a microprocessor and the belonging program and data memories fitting into the system, together with the programmable parallel interfaces with the programmable 22 + 24 lines, the display and operating organs. The block diagram of the apparatus is shown in Figure 4, while Figure 5 illustrates the connection thereof with the seeder.

As mentioned above, Figure 4 shows the block diagram of the seed control apparatus 9. As shown, the signals coming from the seed detectors (not illustrated here) arrive at the signal level interface unit 4, the inputs 8 of which are connected to the programmable parallel interface circuit 5. The interface unit 21 for the output measuring the rotation of the land wheel, as well as the interface unit 22 detecting the elevated position of the seeding machine are also connected to the interface circuit 5.

The interface circuit 5 is connected to the microprocessor 10 via the data bus 6 and the control bus 7, the microprocessor contains the program memory 11 and the data memory 12. The address bus 13 forwards the addresses required for the operation of the program memory 11 and the data memory 12, respectively.

The parallel interface 14 is also connected to the

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microprocessor 10, via the busses mentioned above, and displays 15 and the operating organs 16 are connected thereto.

At last, Figure 5 shows the block diagram of the completely assembled seeding machine system. The seed control apparatus 9 itself is arranged on the trailer 17 and it is connected via the collecting cable 18, the connecting cable 19 and the connectors 20 to the interface circuits 5 belonging to the single groups of furrow splitters; the interface circuits are furthermore connected to the signal level interface units 4 of the seed detectors (not illustrated here), to the interface units 21 measuring the distance covered and the matching units 22 sensing the elevated position.

The apparatus according to the invention solves in an economical manner the processing of the pulse train of a frequency of max. 50 Hz, arriving from the seed detectors of the seeder with eighteen furrow splitters and of further six informations, it performs the shift of the eighteen decimal counters each with six characters and two characters, respectively, simultaneously delivering various informations requiring relatively complicated arithmetic routines.

Summirizing the advantageous features of the apparatus according to the invention it can be stated that in comparison with the known solutions, by using considerably less components, with a decreased volume and reduced costs higher operational safety could be obtained. In addition to these advantages, the embodiment herein described yields a surplus service, in so far as not only clogging of the seeding-pipe, but also the percentage of the deviation from the prescribed distance are signalled.

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C L A I M S

1. Seed control apparatus with a microprocessor containing photoelectric seed detectors, devices for measuring the path covered, display and operating organs, buffer memories, a power supply unit, as well as a microprocessor system consisting of the microprocessor, the program and data memories, furtheron of the interface circuit being connected between the detecting organs and the data bus, c h a r a c t e r i z e d in that in addition to the usual functions the microprocessor (9) is programmed for couting operations too, furtheron between the microprocessor system and the detecting organs a programmable parallel input/output interface circuit (5) interfacing the outputs of the detecting organs to the data bus (6) of the microprocessor (9) and for each detector a signal level interface unit (4) are inserted.

2. Seed control apparatus as claimed in claim 1, c h a r a c t e r i z e d in that the signal level interface units (4) are formed as pulse shaper units.

3. Seed control apparatus as claimed in claim 2, c h a r a c t e r i z e d in that said signal level interface resp. pulse shaper units are monostable circuits.

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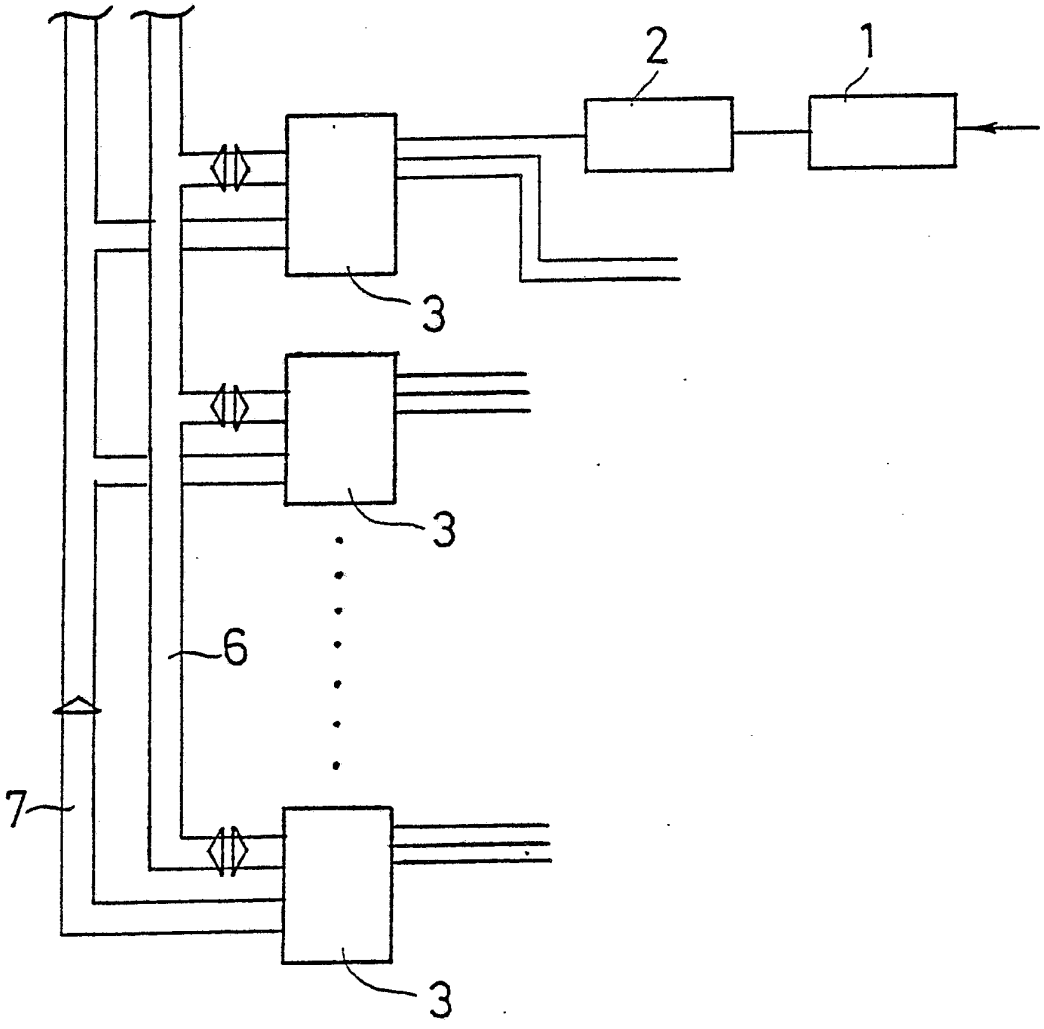


Fig.1

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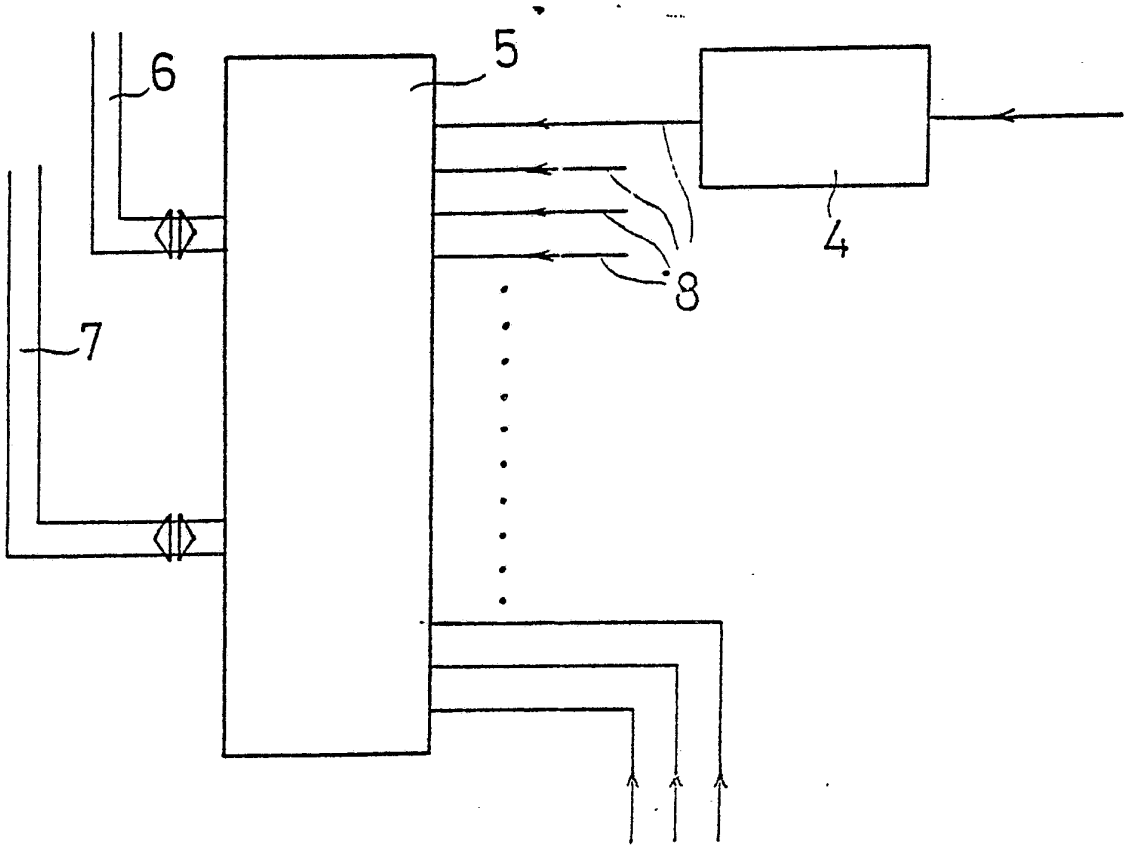


Fig.2

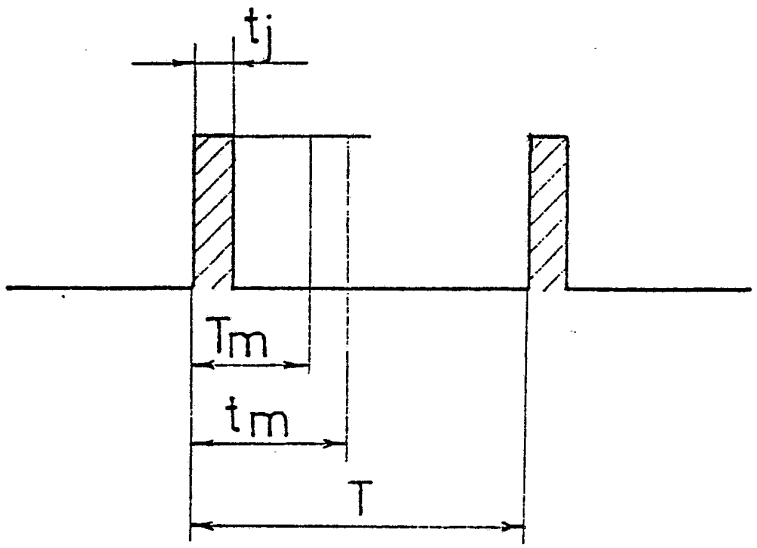


Fig.3

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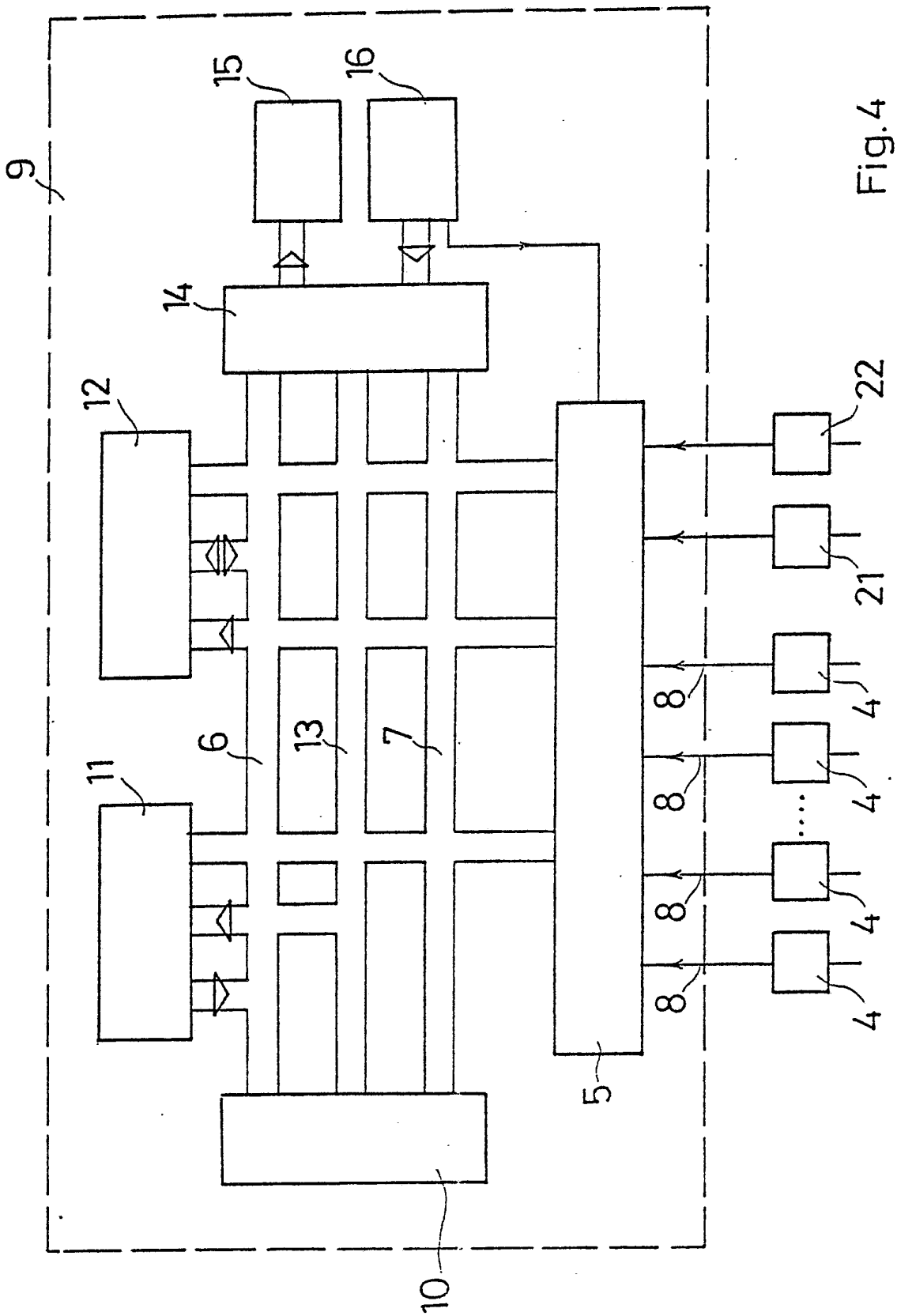


Fig.4

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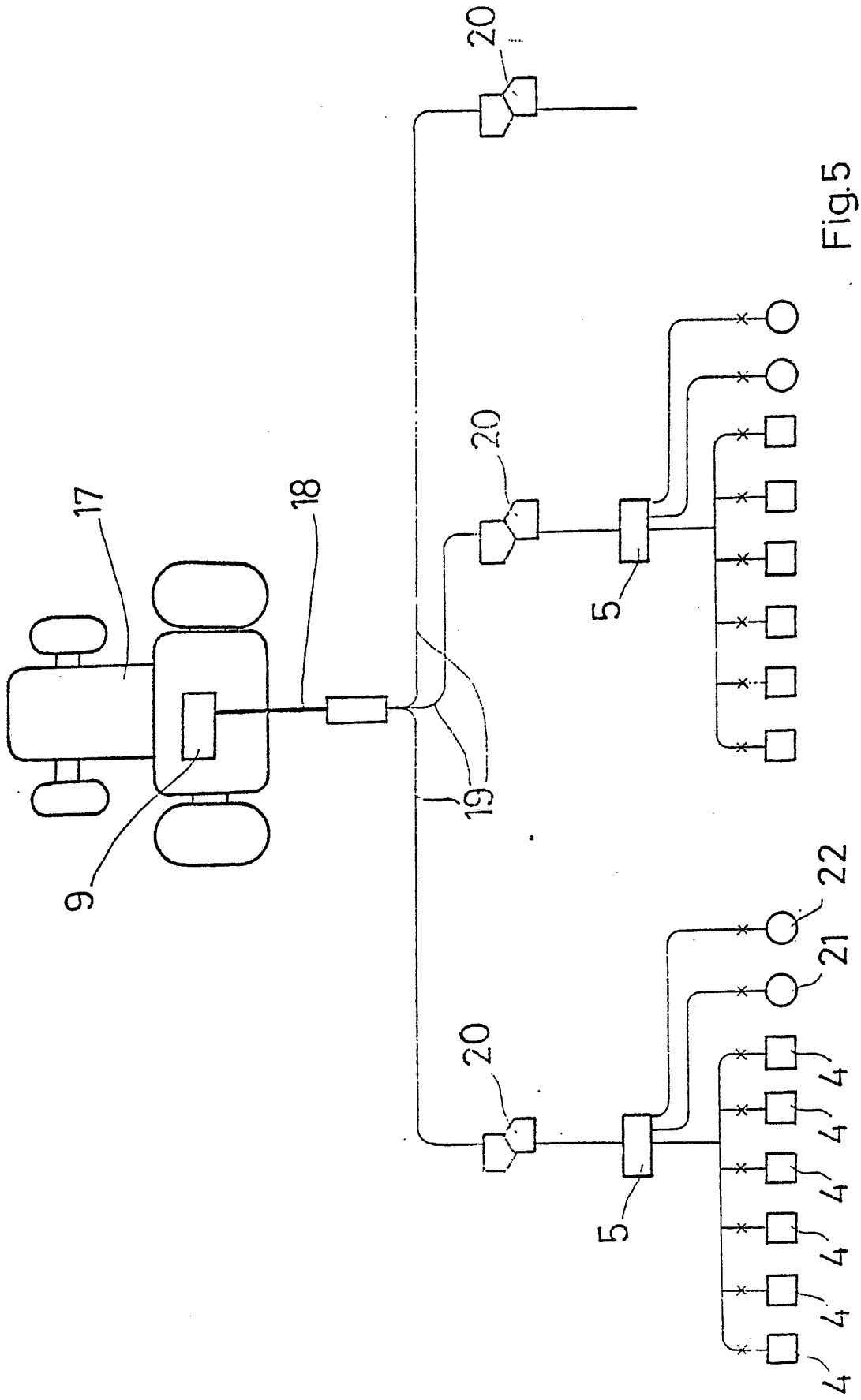


Fig.5

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INTERNATIONAL SEARCH REPORT

International Application No PCT/HU82/00058

I. CLASSIFICATION OF SUBJECT MATTER (If several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

G06F 15/00; A01C 7/00; A01C 7/18

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
IPC[3]	G06F 15/00, A01C 7/00, A01C 7/18

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
A	I.V. Prangishvili "Mikroprotsessory i mikro-EVM", 1979, Publishing House "Energia" (Moscow), see pages 5-10	1-3
A	B.M. Kagan, V.V. Stashin "Mikroprotsessory v tsifrovykh sistemakh", 1979, Publishing House "Energia" (Moscow), see pages 21-23	1-3
A	"Mikroprotsessornye BIS i mikro-EVM. Postroenie i primenenie", edited by A.A. Vasenkov, 1980, Publishing House "Sovetskoe radio", (Moscow), see pages 32-35; 45-46	1-3
A	SU, A, 587898 (V.K. Khoroshenkov et al), 15 January 1978 (15.01.78)	1
A,P	SU, A, 917744 (V.D. Erhova et al), 07 April 1982 (07.04.82)	1
A	US, A, 3855953 (Dickey-John Corporation), 24 December 1974 (24.12.74)	1
A	US, A, 4009799 (Dickey-John Corporation), 01 March 1977 (01.03.77)	1

* Special categories of cited documents: [15]

"A" document defining the general state of the art which is not considered to be of particular relevance

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
12 January 1983 (12.01.83)	28 January 1983 (28.01.83)
International Searching Authority [1]	**Signature of Authorized Officer [20]**
ISA/SU	(V. Kazankov)

Form PCT/ISA/210 (second sheet) (October 1981)

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE [10]

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. ☐ Claim numbers _____, because they relate to subject matter [12] not required to be searched by this Authority, namely:

—

2. ☒ Claim numbers 1, because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out [13], specifically: in the part, characterizing units, included into a structure of a microprocessor system, shown at fig.4

VI. ☐ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING [11]

This International Searching Authority found multiple inventions in this international application as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.

2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:

3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

4. ☐ As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest

☐ The additional search fees were accompanied by applicant's protest.

☐ No protest accompanied the payment of additional search fees.