Abstract: A monolithic integrated circuit comprising at least one relatively deep trench (14) etched into the rear or lower surface of a semiconductor wafer (1) to create a membrane in or on which low voltage logic circuitry for control and protection may be provided. At least one power device area (10) is also provided adjacent to the trench (14). The or each trench (14) is covered with an insulating material (3) and then filled with another material (4). A second, relatively shallow trench (12) is provided on the front or upper surface of the semiconductor wafer (1), in communication with the layer of insulating material (3) and located between adjacent devices or a power device (10) and the low voltage circuitry (2). A monolithic integrated circuit comprising a semiconductor (SOI) wafer is also disclosed.
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Power Integrated Circuits

This invention relates to semiconductor devices and technology and, more precisely, to power integrated circuit technology.

In recent years, Power Integrated Circuits (PICs) have gained huge interest in system integrations. PICs consist of high-voltage power devices and low-voltage control circuitry integrated on to the same semiconductor substrate (usually silicon). Lateral devices have generally been used for this type of application as they are easily integrated into existing processes and they have all their terminals available at the surface. The Lateral Doubled Diffused power MOSFET (LDMOSFET) transistors or the lateral IGBT are typically used.

Conventional extended drain LDMOSFETs are used for applications requiring voltages up to around 100V. However, the introduction of the Reduced Surface Field devices (RESURF LDMOSFET) in the early eighties allowed voltages to be significantly increased up to 700V. Such devices are majority carrier devices, which means all the current is carried by one carrier type and therefore switch very quickly. For lower on-state resistances it is possible to replace the LDMOS transistor with a lateral IGBT (LIGBT), which will have a lower on-state resistance, but as it is a bipolar device will have a much slower switching speed. Junction Isolation (JI) is usually used to separate such devices from each other and from the low-voltage circuitry.

Other technologies such as bipolar - CMOS-DMOS allow the integration of a single DMOS transistor with low-voltage control functionality. Here the DMOS is a vertical device with a drain contact on the backside of the wafer. This technology is extensively used at higher voltages, but at lower voltages or where several devices are needed alternatives such as the JI-LDMOS solution are sought.

Junction isolation is not ideal, since under certain transient conditions high injection conditions may well occur. Under such conditions, high levels of minority carriers will be injected into the substrate and will lead to interference with the low-voltage circuitry. To
tackle this problem Silicon on insulator (SOI) technologies have been developed to provide dielectric isolation.

Despite the big improvement made in lateral power devices, their performances (current and voltage handling capabilities) are still far behind those of the vertical power devices. The vertical power devices have bottom contacts (drain - VDMOSFET, Anode - IGBT), these making integration of the more than one device impossible using existing isolation techniques. Some designers use very deep sinkers to bring those contacts on the wafer top surface, the manufacture of those deep sinkers being a limiting factor.

We have now devised an arrangement which addresses the issues referred to above, and overcomes some of the problems raised thereby.

Thus, in accordance with a first aspect of the present invention there is provided an integrated circuit comprising a semiconductor wafer having a front or upper surface and an opposing rear or bottom surface, the circuit further comprising a first trench in the rear or bottom surface of the wafer which defines a membrane in or on which one or more low voltage circuits or components are provided, said first trench being at least partially covered or filled with an insulating material, a second trench in the front or upper surface of the wafer, said second trench being in communication with said insulating material, and at least one high voltage circuit or device provided in or on said semiconductor wafer, said second trench being provided between said membrane and said high voltage circuit or device so as to isolate them from each other.

Also in accordance with the first aspect of the present invention, there is provided a method of fabricating an integrated circuit comprising the steps of providing a semiconductor wafer having a front or upper surface and an opposing rear or bottom surface, forming a first trench in said rear or bottom surface of said wafer which defines a membrane, providing one or more low voltage circuits or components in or on said membrane, at least partially covering or filling said first trench with an insulating material, and providing at least one high voltage circuit or device in or on said wafer, forming a second trench in said front or upper surface of said wafer between said membrane and said high voltage circuit or device such that said
second trench is in communication with said first trench and isolates said one or more low voltage circuits or components and said high voltage circuit or device from each other.

Still further in accordance with the first aspect of the present invention there is provided a method of isolating a high voltage power device and a low voltage circuit provided on a semiconductor wafer from each other, the method comprising the steps of forming a first trench in a rear or bottom surface of said wafer so as to define a membrane in or on which said low voltage circuit or component is provided, at least partially covering or filling said first trench with an insulating material, and forming a second trench in a front or upper surface of the wafer between said high voltage power device and said low voltage circuit or component such that said second trench is in communication with said first trench and said high voltage power device and said low voltage circuit or component are isolated from each other.

In accordance with a second aspect of the present invention, there is provided an integrated circuit comprising a semiconductor wafer having a front or upper surface and an opposing rear or bottom surface, the circuit further comprising a first trench in the rear or bottom surface of the wafer on either side of which is provided a respective first and second high voltage power devices, said first trench being at least partially covered or filled with an insulating material, a second trench in the front or upper surface of the wafer, said second trench being located between said first and second high voltage power devices and in communication with said insulating material, so as to dielectrically isolate said first and second high voltage power devices from each other.

Also in accordance with the second aspect of the present invention, there is provided a method of fabricating an integrated circuit comprising the steps of providing a semiconductor wafer having a front or upper surface and an opposing rear or bottom surface, forming a first trench in said rear or bottom surface of said wafer, providing respective first or second high voltage power devices on either side of said first trench, at least partially covering or filling said first trench with an insulating material, forming a second trench in said front or upper surface of said wafer between said first and second high voltage high voltage power devices such that said second trench is in communication with said first trench and isolates said first and second high voltage power devices from each other.
Still further in accordance with the second aspect of the present invention, there is provided a method of isolating first and second high voltage power devices provided on a semiconductor wafer from each other, the method comprising the steps of forming a first trench in a rear or bottom surface of said wafer, said first and second high voltage power devices being provided on either side of said first trench, at least partially covering or filling said first trench with an insulating material, and forming a second trench in a front or upper surface of the wafer between said first and second high voltage power devices such that said second trench is in communication with said first trench and said first and second high voltage power devices are isolated from each other.

Thus, in accordance with the first and second aspects of the present invention, it is possible to integrate one or more vertical power devices (and, more particularly, high voltage power transistors and the like) into the same integrated circuit, with the method of isolation enabling dielectric isolation of the high voltage power devices from the low voltage control and protection circuitry (typically comprised of CMOS or BiCMOS devices) and from adjacent devices (i.e. each other), and also enabling the multiple power devices and the low voltage control logic to be fabricated simultaneously to form a monolithic integrated circuit, and all of this at an acceptably low processing cost.

In a preferred embodiment, the first trench is relatively significantly deeper than the second trench, and is preferably substantially completely covered and/or filled with an insulating material. It will be appreciated that the first trench may be etched to form a membrane in the conventional MEMS processes. The second trench is preferably also at least partially covered or filled with an insulating material. The power devices would typically (but not necessarily exclusively) be vertical power transistors, such as vertical IGBT’s, vertical trench IGBT’s, VDMOSFET’s, trench MOSFET’s, and the like.

Within the last decade, Power Integrated Circuits (PICS) have gained huge interest in system integrations. In the PICs, high voltage/power devices are fabricated on a common semiconductor substrate (usually silicon) used for low voltage logic circuits. A very complex functionality of the power IC is combined with higher switching speed, higher reliability, and less weight and size. At the beginning, pure bipolar technologies were used for power ICs implementation. These days, Lateral DMOSFETs are preferably used because of their fast
switching characteristics and the possibility of controlling them by voltage rather than current. Conventional LDMOSFETs are used for up to 100V applications. The introduction of Reduced Surface Field devices (RESURF LDMOSFET) in the early eighties made these devices applicable for the higher voltage applications (up to 700V). These are majority carrier devices and Junction Isolation (JI) can be used to separate them from a low voltage circuitry. The junction isolation technique is based on reverse biased p-n junctions, and it is a low self-heating and relatively cheap technique. On the negative side, JI involves parasitic currents causing interference thus leading to a low speed and high leakage current.

For applications higher than 700V, IGBT devices have to be integrated with the low voltage circuitry. Full integration of the lateral IGBT devices is a much more complex task since a high level of the minority carriers injected into the substrate will lead to interference with a low voltage (logic) circuits for junction isolated devices. Alternatively SOI (silicon oxide) technologies, such as SOI-SIMOX, SOI-Wafer Bonding or SOI-Unibond can be employed to adequately protect low voltage devices from carrier injection. Consequently, sol devices have very low interference between adjacent devices, high speed and low area consumption, but they are more expensive, and they involve self-heating problems (thermal conductivity of the silicon-dioxide is about 100 times larger than silicon).

In spite of big improvements being made in the last decade regarding lateral power devices, their performances (current and voltage handling capabilities) are still far behind those of the vertical power devices. The vertical power devices have bottom contacts to the back of the wafer (drain - VDMOSFET, Anode - IGBT), these making integration of more than one device impossible using existing isolation techniques. Some designers use very deep sinkers to bring these contacts on the wafer top surface, manufacturing of deep sinkers being a limiting factor. Some effort has been made to achieve Smart Power Integration (one power device with gate control logic) of the vertical power device into SOI wafer, but there is no present isolation technique which allows monolithic integration of more than one vertical power device with low voltage circuitry in the SOI wafer.

We have now devised an arrangement which addresses the issues referred to above, and overcomes some of the problems raised thereby.
Thus, in accordance with a third aspect of the present invention there is provided an integrated circuit comprising a semiconductor wafer comprising upper and lower layers of semiconductor material bonded together with a layer of insulating material therebetween, said wafer having a front or upper surface and an opposing rear or bottom surface, the circuit further comprising a trench in the rear or bottom surface of the wafer which trench extends into the lower layer of semiconductor material but does not extend beyond said layer of insulating material, said trench being at least partially covered or filled with an insulating material, said lower layer of semiconductor material being for receiving one or more high voltage power devices adjacent said trench and said upper layer of semiconductor material being for receiving one or more low voltage circuits or components, said layer of insulating material providing electrical insulation between said upper and lower layers.

Also in accordance with the third aspect of the present invention, there is provided a method of fabricating an integrated circuit comprising the steps of providing a semiconductor wafer comprising upper and lower layers of semiconductor material bonded together with a layer of insulating material therebetween, said wafer having a front or upper surface and an opposing rear or bottom surface, the method further comprising the steps of forming a trench in the rear or bottom surface of the wafer which extends into the lower layer of semiconductor material but does not extend beyond said layer of insulating material, at least partially covering or filling said trench with an insulating material, providing one or more high voltage power devices in or on said lower layer of semiconductor material adjacent said trench and providing one or more low voltage circuits or components in or on said upper layer of semiconductor material, said layer of insulating material providing electrical insulation between said upper and lower layers.

Still further in accordance with the third aspect of the present invention there is provided a method of isolating from each other a high voltage power device and a low voltage circuit provided on a semiconductor wafer comprising upper and lower layers of semiconductor material bonded together with a layer of insulating material there between, wherein at least one high voltage power device is provided in or on said lower layer of semiconductor material and at least one low voltage circuit or component is provided in or on said upper layer of semiconductor material, the method comprising the steps of forming a trench in a rear or bottom surface of said wafer which extends into the lower layer of semiconductor material but
does not extend beyond said layer of insulating material, and at least partially covering or filling said first trench with an insulating material.

Thus, in accordance with the third aspect of the present invention, it is possible to integrate one or more vertical power devices (and, more particularly, high voltage power transistors and the like) into the same integrated circuit, with the method of isolation enabling dielectric isolation of the high voltage power devices from the low voltage control and protection circuitry (typically comprised of CMOS or BiCMOS devices) and from adjacent devices (i.e. each other), and also enabling the multiple power devices and the low voltage control logic to be fabricated simultaneously to form a monolithic integrated circuit, and all of this at an acceptably low processing cost.

The power devices would typically (but not necessarily exclusively) be vertical power transistors, such as vertical IGBT’s, vertical trench IGBT’s, VDMOSFET’s, trench MOSFET’s, and the like. It is preferred that the trench extends up to but not beyond the layer of insulating material and is substantially completely covered and/or filled with an insulating material, such that high voltage power devices provided in the lower layer of semiconductor material, on either side of the trench, are completely isolated from each other by the trench and from the low voltage circuitry provided in the upper layer of semiconductor material by the layer of insulating material.

The trench may be etched by, for example, wet chemical etching, reactive ion etching (RIE), or the like, and preferably tapers inwardly from the bottom surface of the wafer up. The layer of insulation material provides a natural etch stop layer.

The upper layer of semiconductor material may be etched to form one or more semiconductor islands, in or on which the low voltage circuitry may be provided (for example, CMOS or BiCMOS circuitry is preferred).

Embodiments of the present invention will now be described by way of examples only with reference to the accompanying drawings, in which:

Figure 1 is a schematic perspective view of a semiconductor wafer;
Figure 2 is a schematic perspective view of the semiconductor wafer of Figure 1 after the first trench has been formed in the rear or bottom surface thereof;

Figure 3 is a schematic perspective view of the semiconductor wafer of Figure 2 after the first trench has been covered with an insulating material;

Figure 4 is a schematic perspective view of the semiconductor wafer of Figure 3 after the first trench has been filled with an insulating material;

Figure 5 is a partial schematic cross-sectional view of the semiconductor wafer of Figure 4 after a second trench has been formed in the front or upper surface thereof;

Figure 6 is a schematic perspective view of the semiconductor wafer of Figure 5 after the second trench has been filled with an insulating material;

Figure 7 is a schematic perspective view of an integrated circuit according to an exemplary embodiment of the present invention;

Figure 8 is a partial schematic cross-sectional view of an integrated circuit according to a first specific exemplary embodiment of the present invention;

Figure 9 is a partial schematic cross-sectional view of an integrated circuit according to a second exemplary embodiment of the present invention;

Figure 10 is a partial schematic cross-sectional view of an integrated circuit according to a third exemplary embodiment of the present invention;

Figure 11 is a partial schematic cross-sectional view of an integrated circuit according to a fourth exemplary embodiment of the present invention;

Figure 12 is a schematic perspective view of a semiconductor (SOI) wafer;
Figure 13 is a schematic perspective view of the semiconductor wafer of Figure 12 after two trenches have been formed in the rear or bottom surface thereof;

Figure 14 is a schematic perspective view of the semiconductor wafer of Figure 13 after the trenches have been covered with an insulating material;

Figure 15 is a schematic perspective view of the semiconductor wafer of Figure 14 after the trenches have been filled with another material;

Figure 16 is a schematic perspective view of the semiconductor wafer of Figure 15 after the upper layer of semiconductor material has been etched;

Figure 17 is a schematic cross-sectional view of an integrated circuit according to a specific exemplary embodiment of the present invention;

Figure 18 is a schematic cross-sectional view of an integrated circuit according to another exemplary embodiment of the present invention;

Figure 19 is a schematic cross-sectional view of an integrated circuit according to yet another exemplary embodiment of the present invention;

Figure 20 is a schematic cross-sectional view of an integrated circuit according to yet another exemplary embodiment of the present invention; and

Figure 21 is a schematic plan view of a semiconductor chip according to an exemplary embodiment of the invention.

Thus, referring first to Figures 1 and 2 of the drawings, the starting material for an integrated circuit according to the invention is a semiconductor wafer 1. A silicon membrane 2 is formed in the wafer 1 by etching, and low voltage logic circuitry can be provided, either partially or completely in the membrane 2, whereas the power device area 10 remains intact and is reserved for a vertical power device.
As shown in Figures 3 and 4 of the drawings, the trench formed to provide the membrane 2 is covered with an insulating material 3 and then filled with another material 4, such as another insulating material, glass or metal.

Referring now to Figures 5 and 6, a second trench 12 is etched in the upper surface of the semiconductor wafer 1 until it reaches the layer 3 of insulating material covering the first trench. The second trench 12 is then filled with an insulating material, such that the low voltage area (provided by the membrane 2) is completely isolated from the power device area (in which a vertical power device is provided).

As shown in Figure 7 of the drawings, an integrated circuit according to one exemplary embodiment of the present invention comprises a semiconductor wafer 1 in which two sets of upper 12 and lower trenches 14 are etched (simultaneously) in the upper and lower surfaces respectively of the wafer, such that two power devices 10 can be integrated into the device. This process can, of course, be extended to three or more vertical power devices, as required. It will be appreciated that the devices 10 are completely isolated from each other as well as the low voltage circuitry.

Figure 8 of the drawings illustrates an integrated circuit according to a first specific exemplary embodiment of the present invention, in which a vertical IGBT 10 is integrated with the low voltage CMOS circuitry 20.

Figure 9 illustrates an integrated circuit according to a second specific exemplary embodiment of the present invention, in which a vertical trench IGBT 10 is integrated with the low voltage CMOS circuitry 20.

Figure 10 illustrates an integrated circuit according to a third specific exemplary embodiment of the present invention, in which a VDMOSFET 10 is integrated with the low voltage CMOS circuitry 20.
Figure 11 illustrates an integrated circuit according to a fourth specific exemplary embodiment of the present invention, in which a vertical trench MOSFET 10 is integrated with the low voltage CMOS circuitry 20.

Referring first to Figures 12 and 13 of the drawings, the starting material for an integrated circuit according to an exemplary embodiment of the third aspect of the present invention is a semiconductor (SOI) wafer 1, comprising a first, lower layer 100 of semiconductor material (typically silicon), a second layer 102 of insulating material (typically silicon oxide) and a third, upper layer of semiconductor material (again, typically silicon). The three layers are bonded together as shown, and this type of wafer structure is well known in the art.

Trenches 2 are formed by, for example, wet chemical etching, or reactive ion etching in the lower layer 100 of semiconductor material up to the insulating layer 102, which may be used as a natural etch stop layer.

As shown in Figures 14 and 15 of the drawings, the trenches 2 are covered with an insulating material 3 and then filled with another material 4, such as another insulating material, glass or metal.

Referring now to Figure 16, the upper layer 104 of semiconductor material is etched to form semiconductor islands 5, inside which low voltage (for example BiCMOS) circuitry can be completely provided.

Figure 17 of the drawings illustrates a structure in which two vertical IGBT's 10 are monolithically integrated with CMOS low voltage devices 20. It will be appreciated that the vertical power devices are completely isolated from each other and from the low voltage circuits.

Figure 18 of the drawings illustrates a structure in which two trench IGBT's 10 are monolithically integrated with CMOS low voltage devices 20. It will be appreciated once again that the vertical power devices are completely isolated from each other and from the low voltage circuits.
Figure 19 of the drawings illustrates a structure in which two vertical DMOSFET's 10 are monolithically integrated with CMOS low voltage devices 20. Once again, it will be appreciated that the vertical power devices are completely isolated from each other and from the low voltage circuits.

Figure 20 of the drawings illustrates a structure in which two vertical trench MOSFET's 10 are monolithically integrated with CMOS low voltage devices 20. It will once again be appreciated that the vertical power devices are completely isolated from each other and from the low voltage circuits.

Figure 21 is a schematic plan view of a semiconductor chip according to an exemplary embodiment of the first, second or third aspects of the present invention. In this particular case, the two top trenches 6 and 7 have been designed to create five semiconductor regions 1, 2, 3, 4 and 5 (although it will be appreciated by a person skilled in the art that any other combination can be assumed). Inside each of the semiconductor regions 1-5, a vertical device, one or more lateral devices, or CMOS circuitry can be placed. Isolation amongst the regions 1, 2, 3, 4 and 5 is achieved in combination by the present invention between the top trenches 6 and 7, the cut lines (kerfs) 8, 9, 10, and 11, and the bottom (back) trenches (not shown in the figure).

Embodiments of the present invention have been described above by way of examples only, and it will be appreciated that modifications and variations can be made to the described embodiments without departing from the scope of the present invention as defined by the appended claims.
Claims

1. An integrated circuit comprising a semiconductor wafer having a front or upper surface and an opposing rear or bottom surface, the circuit further comprising a first trench in the rear or bottom surface of the wafer which defines a membrane in or on which one or more low voltage circuits or components are provided, said first trench being at least partially covered or filled with an insulating material, a second trench in the front or upper surface of the wafer, said second trench being in communication with said insulating material, and at least one high voltage circuit or device provided in or on said semiconductor wafer, said second trench being provided between said membrane and said high voltage circuit or device so as to isolate them from each other.

2. A method of fabricating an integrated circuit comprising the steps of providing a semiconductor wafer having a front or upper surface and an opposing rear or bottom surface, forming a first trench in said rear or bottom surface of said wafer which defines a membrane, providing one or more low voltage circuits or components in or on said membrane, at least partially covering or filling said first trench with an insulating material, and providing at least one high voltage circuit or device in or on said wafer, forming a second trench in said front or upper surface of said wafer between said membrane and said high voltage circuit or device such that said second trench is in communication with said first trench and isolates said one or more low voltage circuits or components and said high voltage circuit or device from each other.

3. A method of isolating a high voltage power device and a low voltage circuit or component provided on a semiconductor wafer from each other, the method comprising the steps of forming a first trench in a rear or bottom surface of said wafer so as to define a membrane in or on which said low voltage circuit or component is provided, at least partially covering or filling said first trench with an insulating material, and forming a second trench in a front or upper surface of the wafer
between said high voltage power device and said low voltage circuit or component such that said second trench is in communication with said first trench and said high voltage power device and said low voltage circuit or component are isolated from each other.

4. An integrated circuit according to claim 1, comprising two or more high voltage circuits or devices are isolated from each other and from said low voltage circuit or component by respective one or more second trenches provided in said front or upper surface of said wafer.

5. An integrated circuit comprising a semiconductor wafer having a front or upper surface and an opposing rear or bottom surface, the circuit further comprising a first trench in the rear or bottom surface of the wafer on either side of which is provided a respective first and second high voltage power devices, said first trench being at least partially covered or filled with an insulating material, a second trench in the front or upper surface of the wafer, said second trench being located between said first and second high voltage power devices and in communication with said insulating material, so as to dielectrically isolate said first and second high voltage power devices from each other.

6. An integrated circuit according to claim 1, claim 4 or claim 5, wherein the first trench is relatively significantly deeper than the second trench.

7. An integrated circuit according to any one of claims 1, or claims 4 to 6, wherein second trench is at least partially covered or filled with an insulating material.

8. An integrated circuit according to any one of claims 1 or claims 4 to 7, wherein the or each power device comprises a vertical power transistor, such as a vertical IGBT, a vertical trench IGBT, a VDMOSFET, a trench MOSFET, or the like.
9. An integrated circuit according to any one of claims 1 or claims 4 to 8, wherein said one or more low voltage circuits or components comprise one or more CMOS or BiCMOS devices.

10. An integrated circuit according to any one of claims 1 or claims 4 to 9, wherein said one or more low voltage circuits or devices comprise low voltage logic circuitry.

11. A method according to claim 2 or claim 3, wherein two or more high voltage circuits or devices are provided in said semiconductor wafer, and including the step of forming a plurality of second trenches in said front or upper surface of said wafer so as to isolate the high voltage circuits or devices from each other and from said low voltage circuits or components.

12. A method of fabricating an integrated circuit comprising the steps of providing a semiconductor wafer having a front or upper surface and an opposing rear or bottom surface, forming a first trench in said rear or bottom surface of said wafer, providing respective first or second high voltage power devices on either side of said first trench, at least partially covering or filling said first trench with an insulating material, forming a second trench in said front or upper surface of said wafer between said first and second high voltage high voltage power devices such that said second trench is in communication with said first trench and isolates said first and second high voltage power devices from each other.

13. A method of isolating first and second high voltage power devices provided on a semiconductor wafer from each other, the method comprising the steps of forming a first trench in a rear or bottom surface of said wafer, said first and second high voltage power devices being provided on either side of said first trench, at least partially covering or filling said first trench with an insulating material, and forming a second trench in a front or upper surface of the wafer between said first and second high voltage power devices such that said second trench is in communication with said first trench and said first and second high voltage power devices are isolated from each other.
14. An integrated circuit comprising a semiconductor wafer comprising upper and lower layers of semiconductor material bonded together with a layer of insulating material therebetween, said wafer having a front or upper surface and an opposing rear or bottom surface, the circuit further comprising a trench in the rear or bottom surface of the wafer which extends into the lower layer of semiconductor material but does not extend beyond said layer of insulating material, said trench being at least partially covered or filled with an insulating material, said lower layer of semiconductor material being for receiving one or more high voltage power devices adjacent said trench and said upper layer of semiconductor material being for receiving one or more low voltage circuits or components, said layer of insulating material providing electrical insulation between said upper and lower layers.

15. A method of fabricating an integrated circuit comprising the steps of providing a semiconductor wafer comprising upper and lower layers of semiconductor material bonded together with a layer of insulating material therebetween, said wafer having a front or upper surface and an opposing rear or bottom surface, the method further comprising the steps of forming a trench in the rear or bottom surface of the wafer which extends into the lower layer of semiconductor material but does not extend beyond said layer of insulating material, at least partially covering or filling said trench with an insulating material, providing one or more high voltage power devices in or on said lower layer of semiconductor material adjacent said trench and providing one or more low voltage circuits or components in or on said upper layer of semiconductor material, said layer of insulating material providing electrical insulation between said upper and lower layers.

16. A method of isolating from each other a high voltage power device and a low voltage circuit provided on a semiconductor wafer comprising upper and lower layers of semiconductor material bonded together with a layer of insulating material therebetween, wherein at least one high voltage power device is provided in or on said lower layer of semiconductor material and at least one low voltage circuit or component is provided in or on said upper layer of semiconductor material, the
method comprising the steps of forming a trench in a rear or bottom surface of said wafer which extends into the lower layer of semiconductor material but does not extend beyond said layer of insulating material, and at least partially covering or filling said first trench with an insulating material.

17. An integrated circuit according to claim 14, wherein the trench extends up to but not beyond the layer of insulating material.

18. An integrated circuit according to claim 14 or claim 17, wherein the trench is substantially completely covered and/or filled with an insulating material.

19. An integrated circuit according to any one of claims 14, 17 or 18, wherein respective high voltage power devices are provided in the lower layer of semiconductor material, on either side of the trench.

20. An integrated circuit according to any one of claims 14 or 17 to 19, wherein the trench tapers inwardly from the bottom surface of the wafer up.

21. An integrated circuit according to any one of claims 14 or 17 to 20, wherein the upper layer of semiconductor material is etched to form one or more semiconductor islands, in or on which the low voltage circuitry may be provided.

22. An integrated circuit according to any one of claims 14 or 17 to 21, wherein two or more trenches are provided in said lower layer of semiconductor material.

23. An integrated circuit substantially as herein described with reference to the accompanying drawings.

25. A method of isolating from each other a high voltage power device and a low voltage circuit provided on a semiconductor wafer, the method being substantially as herein described with reference to the accompanying drawings.
FIG. 11
FIG. 14

FIG. 15

SUBSTITUTE SHEET (RULE 26)
# INTERNATIONAL SEARCH REPORT

## A. CLASSIFICATION OF SUBJECT MATTER

<table>
<thead>
<tr>
<th>IPC</th>
<th>Classification Code</th>
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According to International Patent Classification (IPC) or to both national classification and IPC.

## B. FIELDS SEARCHED

- Minimum documentation searched (classification system followed by classification symbols)
  - IPC 7
  - H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched.

- Electronic data base consulted during the international search (name of data base and, where practical, search forms used)
  - EPO-Internal, WPI Data, PAJ

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
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<tbody>
<tr>
<td>X</td>
<td>US 5 138 422 A (KUROYANAGI SUSUMU ET AL) 11 August 1992 (1992-08-11) column 10, line 3 - column 11, line 29; figures 6a-6g</td>
<td>2,3,12, 13</td>
</tr>
<tr>
<td>Y</td>
<td>WO 02/25700 A (CAMBRIDGE SEMICONDUCTOR LTD) 28 March 2002 (2002-03-28) page 25, line 26; figure 6c page 26, line 5 - line 23</td>
<td>1,4-11, 14-22</td>
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<tr>
<td>A</td>
<td>EP 0 328 331 A (TOKYO SHIBAURA ELECTRIC CO) 16 August 1989 (1989-08-16) figures 5A,5B</td>
<td>1-22</td>
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Further documents are listed in the continuation of box C. Patent family members are listed in annex.

- * Special categories of cited documents:
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Date of the actual completion of the international search: 19 April 2004
Date of mailing of the international search report: 27/04/2004

Name and mailing address of the ISA:
European Patent Office, P.O. Box 5002, 3000 A3 NL - 2280 NL, NL - 2280 NL
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Affidavit:

Authorized officer:
Agne, M

Form PCT/ISA/1.0 (second sheet) (January 2004)
INTERNATIONAL SEARCH REPORT

Box I  Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. □ Claims Nos.: because they relate to subject matter not required to be searched by this Authority, namely:

2. X Claims Nos.: 23–25
   because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:
   see FURTHER INFORMATION sheet PCT/ISA/210

3. □ Claims Nos.: because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II  Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. □ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. □ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. □ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. □ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

□ The additional search fees were accompanied by the applicant’s protest.

□ No protest accompanied the payment of additional search fees.
Continuation of Box I.2

Claims Nos.: 23-25

It is entirely unclear which of the various technical features mentioned in the description are meant to be included in the subject-matter of claims 23-25.

The applicant's attention is drawn to the fact that claims relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examining Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure. If the application proceeds into the regional phase before the EPO, the applicant is reminded that a search may be carried out during examination before the EPO (see EPO Guideline C-VI, 8.5), should the problems which led to the Article 17(2) declaration be overcome.
# INTERNATIONAL SEARCH REPORT

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