SECONDARY DETECTION CIRCUIT WITH
SHARP CUTOFF FOR SECURITY
VALIDATING

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ABSTRACT

A secondary detection circuit for a paper security validating device which device scanned a portion of one surface of the paper security. The secondary detection circuit compares the level of reflection of light from the reverse side of the security with a known level and, if the reflected level falls below a first value or exceeds a second greater value, the secondary detection circuit blocks the output of the primary detection circuit regardless of whether or not an authentic signal is produced by the primary circuit.

11 Claims, 2 Drawing Figures
SECONDARY DETECTION CIRCUIT WITH SHARP CUTOFF FOR SECURITY VALIDATING

The present invention relates to a paper security validating device and more particularly to a circuit for performing a secondary validation check on the security.

Devices which determine the validity of paper security such as currency by scanning a portion of the security are well known. One such device is shown in U.S. Pat. No. 3,457,421, issued July 22, 1969 for "Radiation Sensitive Paper Security Validation Apparatus." Since the physical condition of the paper security may vary greatly, the validation apparatus must have a range of acceptance. This is especially true where currency is being detected as the validation apparatus will frequently be presented with valid pieces of currency which are considerably worn and dirty. A lower limit on the detection range must be established, however, to avoid the acceptance of non-authentic documents such as high quality photocopies. As a result, a portion of the valid securities must be rejected to avoid the acceptance of invalid securities.

It is the primary object of the present invention to provide a secondary detection circuit for a paper security validating device which permits the device to accept low quality valid securities while rejecting high quality reproductions.

It is also an object of the present invention to provide a secondary detection circuit for a paper security validating device which senses the reverse side of the security from that scanned by the primary detection circuit to thereby eliminate all photocopies or other reproductions.

A further object of the present invention is the provision of a secondary detection circuit which may be added to an existing paper security validating device to permit the range of acceptance of valid securities by the device to be extended without increasing the possibility of acceptance of an invalid document.

The above and other objects of the invention which will become apparent in the following detailed description are achieved by providing a secondary detection circuit for a paper security validating device which consists, essentially, of a light source directed to the reverse side of the security from that scanned by the primary detection means, means to detect the light reflected from the security and to compare this level with a reference level, an amplifier for amplifying the result of the comparison, and high and low threshold detectors for determining when the amplified comparison signal falls within an acceptable range.

For a more complete understanding of the invention and the objects and advantages thereof reference should be had to the following detailed description and the accompanying drawing wherein there is shown a preferred embodiment of the invention.

In the drawing:

FIG. 1 is a schematic showing of the detection circuit of the present invention; and

FIG. 2 is a plan view of the sensor arrangement of the secondary detection circuit.

The security validating circuit of the present invention consists of two functional groups, the primary grid detection circuit 10 and the secondary detection circuit 12. It will be understood that the primary grid detection circuit 10 illustrated herein is illustrative of one type of detection circuit which may be used but the invention is not limited to the particular circuit disclosed.

In the primary detection circuit 10 an input signal is supplied over the conductor 14 from the security scanning means. The scanning means may, for example, be the sensing cell grid arrangement illustrated in the above-mentioned patent. A typical scanning assembly generates an AC signal by detecting the passage of radiation from a source 28 through a portion of the security 30 and through a grid or reticle 32 positioned close to the security while relative movement is effected between the grid 32 and the security 30. This input signal over the conductor 14 is connected through the capacitor C1 to the noninverting input of an amplifier IC1. The resistor R5 establishes the AC impedance at this point while the resistors R2 and R3 form an accurate divider across the supply voltage. The junction of the resistors R2 and R3 provides a reference equal to one half of the supply voltage. The capacitor C2 provides a low impedance AC path from the reference point to ground. Resistors R6 and R4 fix the gain of the amplifier IC1. Potentiometer R7 adjusts the operative bias of the amplifier IC1. The amplified AC signal generated by a valid scan is coupled through the capacitor C3 and resistor R8 to the base of a transistor Q1. Resistor R9 provides a return path to the ground for the base of the transistor Q1. The positive going portion of the AC signal overcomes the base-emitter voltage threshold of transistor Q1 and causes the collector of transistor Q1 to conduct heavily through the primary of transformer of T1. The collector of transistor Q1 is clamped at 30 volts by the zener diode D1 during the off portion of the cycle. The resulting primary signal of the transformer T1 is coupled to the secondary of the transformer and applied to lamp DS1. Several cycles of energy are required for the lamp DS1 to attain illumination. When illumination is obtained the light output then lowers the resistance of the light dependent cadmium sulfide cell R23. This applies a DC signal to the gate of the silicon control switch Q2, triggering conduction of the switch Q2. Conduction of Q2 establishes an output signal in the conductor 16 indicating the detection of a valid piece of currency. The resistor R11 provides a ground return for gate 1 of the switch Q2 and the capacitor C4 prevents any noise signal at gate 1. Resistor R12 provides off bias to gate 2 of the silicon control switch Q2.

In order to prevent the acceptance of a photocopy the secondary detection circuit 12 measures the reflections of the reverse side of the paper security. The secondary detection circuit includes a sensing unit designated generally by the reference numeral 18 and illustrated in FIG. 2. This unit includes a lamp 20 to provide illumination, preferably in the infrared region, to the rear side of the note. A pair of closely matched silicon solar cells 22 and 24 are positioned closely adjacent to the lamp 20. The assembly 18 is mounted on a suitable supporting board and positioned closely adjacent the rear side of the paper security so that the illumination from the lamp 20 is reflected to the silicon solar cell 22. The cell 24 is covered with a light vane 26 so that it receives uniform reflection of the illumination of the lamp 20. The amount of reflectance of an average note is determined empirically and the light vane 26 is adjusted so that the output of the silicon solar cells 22 and 24 are equal to zero. This is indicated at amplifier output as one half the supply voltage when measuring an average note. The silicon solar cells 22 and 24 are arranged in a series-aiding configuration. The differential
output of this circuit is applied to the inputs of a DC operational amplifier IC2. Both inputs are referenced to the precision divider formed of resistors R2 and R3 through the resistors R13 and R14. The gain of the amplifier IC2 is determined by negative feedback through the potentiometer R16 and resistor R15. The output of the amplifier IC2 will be low (toward ground) for a lighter (white) note and will be high (toward supply voltage) for a darker (black) note.

When the amplifier output approaches the high limit conduction occurs through the zener diode D3, resistor R21, and the base-emitter junction of transistor Q4. Transistor Q4 is thus forward biased and its collector clamps the base of transistor Q1 to ground. Therefore, an accept command from the primary grid detection circuit amplifier IC1 does not bias the transistor Q1 on and no signal is generated through the transformer T1.

Similarly, when the low limit is approached, conduction occurs through the zener diode D2, resistor R19, and base-emitter junction of the transistor Q3. Collector current of the transistor Q3 then flows through the resistor R20 and forward biases the transistor Q4 again clamping the base of the transistor Q1 to ground and preventing an authentic signal from being produced. The resistors R18 and R22 provide a return path for leakage of the zener diodes D2 and D3 and transistors Q3 and Q4. The diode D4 acts as a reverse voltage clamp for transistor Q4.

It will be understood that while particular reference has been made to the measurement of the reflectivity of the reverse side of the paper security from that scanned by the primary detection circuit, the invention is not limited thereto. Rather, the tests of reflectivity can be made on the same side of the security as is the primary test. However, measurement of the reflectivity of the reverse side of the security is preferable since the photopies are one sided and measurement of the reverse side permits accurate detection and rejection of such photopies.

While only the best known embodiment of the invention has been illustrated and described in detail herein it will be understood that the invention is not limited thereto or thereby. Reference should therefore be had to the appended claims in determining the true scope of the invention.

What is claimed is:
1. In a paper security validating apparatus having means for scanning a portion of the security to determine the authenticity thereof and to produce an output signal when the scanning indicates a valid security, the improvement comprising:
   means for illuminating a portion of the security;
   a first sensor for detecting the amount of illumination reflected from the illuminated portion of the security;
   a reference surface, illuminated by the means for illuminating and having substantially the same reflective qualities as the portion of the security being illuminated;
   a second sensor for detecting the amount of illumination reflected from the reference surface;
   means for comparing the output signals of the first and second sensors; and
   means responsive to the comparing means for blocking the output signal of the authenticity determining means when the output signals of the first and second sensors differ by more than a predetermined amount.
2. The improvement according to claim 1 wherein the first and second sensors are silicon solar cells.
3. The improvement according to claim 2 when the first and second sensors have closely matched characteristics and are connected in a series-aiding network.
4. The improvement according to claim 1 wherein the means for illuminating and the sensors are located on the opposite side of the paper security from the means for scanning.
5. The improvement according to claim 1 wherein the means for illuminating is an infrared light source.
6. Apparatus for determining the authenticity of a paper security, comprising:
   a first detection circuit including means to scan a portion of the security and means to produce an output signal when the scanning means detects an apparently authentic security; and
   a second detection circuit for scanning a second portion of the security and means to block the output signal of the first detection circuit when an invalid security is detected, the second detection circuit including means for illuminating the second portion of the security, a sensor for detecting the amount of illumination reflected from the second portion of the security, circuit means receiving the output of the sensor and operative to block the first detector circuit output signal when the output of the sensor deparls from a reference level by more than a predetermined amount, wherein the first detector circuit means to produce an output signal includes a first normally non-conductive transistor which becomes conductive when an apparently valid security is scanned, the circuit means of the second detection circuit including a second transistor which is normally non-conductive but becomes conductive upon detection of an invalid security by the second detection circuit, conduction of the second transistor holding the first transistor in a non-conductive state, wherein the circuit means of the second detector circuit includes a second sensor illuminated by reflection from the means for illuminating, the first and second sensors being connected in a series-aiding network, and where a reflective surface is provided to direct illumination from the means to illuminate uniformly to the second sensor.
7. Apparatus according to claim 6 wherein the sensors are silicon solar sensors having closely matched characteristics.
8. Apparatus according to claim 7 wherein the reflective surface is adjustably mounted to controllably vary the amount of reflected illumination to the second sensor.
9. Apparatus according to claim 6 further including an amplifier receiving the output of the sensor network and controlling the second transistor.
10. Apparatus according to claim 9 further including a zener diode in series connection between the amplifier and the second transistor to block current flow from the amplifier until the amplifier signal exceeds a predetermined level.
11. Apparatus according to claim 10 further including a third transistor which is normally non-conductive and which biases the second transistor to a conductive state when the third transistor conducts, a second zener diode being provided between the amplifier and the third transistor to permit current flow to the third transistor only when the amplifier output is below a second predetermined level.