

(19)



(11)

EP 3 381 038 B1

(12)

EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention
of the grant of the patent:

28.12.2022 Bulletin 2022/52

(51) International Patent Classification (IPC):

G11C 16/16 ^(2006.01) **G11C 16/32** ^(2006.01)
G11C 16/04 ^(2006.01)

(21) Application number: **16801256.5**

(52) Cooperative Patent Classification (CPC):
G11C 16/16; G11C 16/0483; G11C 16/32

(22) Date of filing: **25.11.2016**

(86) International application number:
PCT/EP2016/078823

(87) International publication number:
WO 2017/089546 (01.06.2017 Gazette 2017/22)

(54) **ELECTRONIC DEVICE WITH MEMORY ERASED BY PAGE**

ELEKTRONISCHE VORRICHTUNG MIT SEITENWEISER SPEICHERLÖSCHUNG

DISPOSITIF ÉLECTRONIQUE À MÉMOIRE EFFACÉE PAR PAGE

(84) Designated Contracting States:

**AL AT BE BG CH CY CZ DE DK EE ES FI FR GB
GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO
PL PT RO RS SE SI SK SM TR**

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(30) Priority: **26.11.2015 EP 15306881**

(43) Date of publication of application:

03.10.2018 Bulletin 2018/40

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Description

Field of the Invention:

[0001] The invention relates to an electronic device with memory erased by page. More particularly the invention is related to memory having an erasing by page with strong timing constraints.

Background of the Invention:

[0002] Electronic memories are today essential for electronic devices using a microprocessor. Non volatile memories are memory that retains information when power is switch off. Amongst the non volatile memories there are memories that are electrically erasable, well known under the name of EEPROM or E2PROM. Typically a floating gate memorizes an electrical charge when the power is off. The charged state and the discharged state of the gate are associated to a logical level, zero or one of a binary information called bit. The charging and the discharging of the floating gate are made according two different polarizations of the floating gate transistor. In term of memory management two operations are performed. An erasing operation is performed for placing the bit in a first state and a writing operation is made for placing the bit in the other state. For making these operations, the floating gate transistor must be selected and several selection transistors are required.

[0003] In view to make big matrix of memories, it is well known to reduce the number of selection transistors. The memory matrix is often divided in groups of bits that can be selected simultaneously. Groups of bits have different names like words, pages and blocks depending of the size. Commonly, a word corresponds to one or two bytes, a page comprises several words, for example 256 to 1024 words and a blocks may comprises several pages, for example 16 to 64 pages. The different groups are used depending of the memory size. Small E2PROM can be written and erased by word. Very large Flash memory are written by page and erased by block. Intermediate memory can be written and erased by pages. The time and consumption for writing or erasing operations depends of the size of the group of bits. The larger the group is, the larger the capacity to charge is. In view to limit current peaks, it is known to increase the time of the operation. Commonly, a page to erase can take 1 to 10 ms depending of the block size and around the same time to be write

[0004] In case of a memory managed by pages (and/or blocks), some status bits are associated to each page for indicating that the page is currently in use, is written but no more in use, or is erased. Andrew Birrell et al., "A design for highperformance flash disks", in ACM SIG-OPS Operating Systems Review, vol. 41, no. 2, pages 88-93, 1 April 2007, and US 2006/143365 A1 disclose Flash memories that are erasable by blocks. Commonly, the page management is made like the sectors of an hard

drive: a page is erased just before to be reuse, such a method authorizes to retrieve an "erased" file till the page is not re-used. For avoiding too much stress on the memory cells, it is known to manage the pages in a circular manner, i.e. all the pages have to be used before reusing a page.

[0005] According to a conventional memory management, when a data is to be modified inside a file, the corresponding page has to be re-written in another page with the modified data. The memory controller has to find the next available page that is erased or no more in use. After all pages are used at least once, the memory controller can only find pages that are no more in use. The writing time is transformed into the addition of an erasing time and a writing time.

[0006] Considering a contactless device compliant with ISO14443, the contactless device may have not got a battery or may work in a battery off mode. In that case the contactless device is powered by the electromagnetic field provided by a reader device. A contactless communication according ISO 14443 is very fast, in general it should be done in few hundreds of milliseconds. Sometimes, a request necessitates the rewriting of few data at different places. With a conventional memory management, when the all the memory has been write at least one, the time to perform such a request can be very long and as an example more than one second. To be sure to complete the request, the user of the device must maintain the contactless device inside the electromagnetic field preferably without move to be sure to have the optimal transmission. In case of a move before the completion of the request, an error transmission may occur in the last feed-back message and the request is to be re-send a second time.

Summary of the Invention:

[0007] The invention is defined by the features of independent claims. Preferred embodiments are set out in the dependent claims.

Brief Description of the Drawings:

[0008] The invention will be better understood after the reading of the following

[0009] Description of the Preferred Embodiments that makes references to the annexed drawings in which:

Figure 1 shows a schematic diagram of an example of device in which the invention is implemented,

Figures 2 to 4 show some example of structure of a memory array,

Figure 5 shows an example of memory mapping using the invention, and,

Figure 6 shows an example of index of the memory

mapping of the figure 5.

Description of the Preferred Embodiments:

[0010] As indicated before, the problem solved by the invention is related to the time needed for performing a transaction in some contactless transaction which are commonly used in the smartcard world. So the preferred example of device implementing the invention is a smartcard SC as shown on figure 1. Nevertheless, the example can be transposed to other kind of device comprising the similar component and having comparable time constraints.

[0011] The Smartcard SC comprises a microprocessor μ C coupled to a central bus BUS to which are connected a first interface 11, a second interface 12, a volatile memory RAM, a short and fast non volatile memory SNVM and a large non volatile memory LNVM. The first interface is for example a communication interface according to ISO7816 that can receive and answer to commands when the smartcard SC is plugged into a reader. The second interface is a for example a contactless interface according to ISO14443 that can receive and answer to commands when the smartcard SC is inside the electromagnetic field of a reader.

[0012] The volatile memory RAM is commonly used for storing temporarily part of the code and the data during the running of programs, for preparing the messages to send and also as buffer before data storage in the large non volatile memory LNVM. The small and fast non volatile memory SNVM is a non volatile memory that can be accessed in read write by words so it can be used like a volatile memory that can be saved when power is turned off. The SNVM is relatively expensive in term of space occupation so the operating system uses it for storing some parameters that change a lot and that should be memorized between two powered sessions. The large non volatile memory LNVM is used as a mass memory, as an example Flash memory is used. To have a high integration level, such a memory is accessed by block.

[0013] The memory structure of a block inside a Flash memory comprises a data area and metadata area, as disclosed on figure 2. Typically, the metadata are separated in two groups, a first group being dedicated to data integrity and a second group being dedicated to memory management. The example of figure 2 shows a memory block of 2 kBytes comprising additional 128 Bytes for metadata. The first group CS/ECC comprises Check Sum of the data and an Error Correction Code for retrieving the data in case some bits are altered in the data area. The second group may comprise a lot of information for retrieving the memory mapping, the block chaining and other information. Typically, the metadata are a duplication of information that enable to retrieve all the memory structure in case of lost of the file of memory management by the operating system or the memory controller.

[0014] For the following explanation, we take into con-

sideration that the memory is a NAND Flash, i.e. with erased state at level 1 for each bit. With such a memory it is possible to write several times a same block but in that case only the bits at level 1 can be write at level zero. Once a bit is at level 0, a complete erasing of the block is needed for putting the bit to level 1. Such a multiple write is commonly implemented for modifying bit by bit the metadata.

[0015] On figure 3, the second group is detailed for indicating the bits and Bytes of metadata that are used for the memory management according to the invention. A first bit indicates if the block is Used, this bit is written at low level once at least a part of the data area is written. A second bit NMU indicates that a block is no more use, this NMU bit is written at zero when the data area should be considered to be erased. Once the NMU bit is set to level 0, the block can be selected for its erasing. A first field Virt@ contains the virtual block address corresponding to the physical block address. Such virtual address Virt@ can be written only when the data area is written. The erasing of the virtual address is made only when the block is erased. The size of the field Virt@ is determined for addressing all the addresses, i.e. one Byte enable to address 256 blocks. A second field EQ Nb contains a number representative of the position of the block in the erasing queue. The second field EQ NB is written when the NMU bit is set to level 0, the value being the next value after the higher value recorded in one block. This number should be at least equal to the maximum number of blocks in the memory. Of course other information can be stored in the metadata area but they are not essential for the invention.

[0016] As indicated, a block can be subdivided into pages for the writing. Figure 4 shows an adaptation of the metadata area in the case the block contains 8 pages with an erasing made by block. The first group CS/ECC will be divided in 8 groups of 8 bytes, each group corresponding to one page. The first bit Used is transformed into a word of 8 bits Used[0-7], each bit being dedicated to one page. The bit NMU is transformed into a word of 8 bits NMU[0-7], each bit being dedicated to one page. The field Virt@ is also modified for comprising 8 field corresponding to the virtual address of each page. The field EQNb remains unchanged but it must be written only when the 8 bits of NMU[0-7] are set to level 0.

[0017] The man of the art will understand that other kind of memory structures can be used with the invention. In addition, the definition of the "memory block" in the invention correspond to the size used for the erasing of data and that, depending of the memory structure, it could be the same than a memory page. In addition the size of the memory will influence the size of the fields used for the address or the number in the erasing queue.

[0018] Now, it is explained in relation with figure 5 to 8 how the invention works. On figure 5, it is represented an example of memory implementing the invention. The figure 6 represents an index of the memory of figure 5 used as circular buffer. As it can be seen, the index may

comprise a lower number of blocks than the LNVM in such a way that several index can be managed on a same memory. The index is stored inside the RAM or inside the SNVM. If the RAM is used for storing the index, it should be stored before switching off the power or it should be reconstructed at each power on using the metadata of the LNVM. Such a reconstruction is not necessary if the index is stored in the SNVM.

[0019] The address @ corresponds to the physical address in the memory also indicated in the index as Phy@. The virtual address Virt@ corresponds to the address inside the index. In the index, the binary information Erased corresponds to the reverse of the bit Used in the memory, and the binary information TBE corresponds to the bit NMU.

[0020] In the index of figure 6, we show a reserve of 4 erased pages that the invention will try to maintain in a time independent of the writing operation. It is also indicated that the index already points on blocks to be erased that will be the next page to erase when the microprocessor has time to do it. So when a write operation is required, the index will take the first erased block to write the data, which is Virt@ 06. After the writing of the data this address is no more available as an erased address, as it can be seen on figure 7.

[0021] The processor performs the erasing operation only to maintain a predetermined number of erased page in such a way that a reserve of blocks always exists. Each time the number of erased blocks is below the predetermined number and each time the memory is not used, the microprocessor launches an erasing operation.

[0022] With a smart card compliant with ISO7816 or ISO14443, the reception of a command has a time duration that can be of the same time of a block erasing. During the reception of a command only the RAM is used for buffering the command. So each time the microprocessor detects the reception of a command on its interface I1 or I2, he can use the reception time as an idle time for erasing a block to be erased. In addition, after the sending of an answer, the microprocessor can try to launch an erasing before the reception of a next command but in that case there is a risk of tearing with a power cut off during the erasing. If the erasing is not performed completely, the bits of the LNVM and the index still indicate that the block is to be erased. So the erasing can be made again at the next command reception. Of course if a smart card is plug into a card reader without command reception, the microprocessor can try to erase as many blocks than needed.

[0023] On figure 7, the index indicates that only 3 blocks are erased while the predetermined number is 4. When the microprocessor μP detects an appropriate time for erasing a block, the next block to be erased is selected then erased. Preferentially, the oldest block to be erased is chosen by using the EQ Nb which indicates the position inside the erasing queue. As it can be seen on figure 7, the block with virtual address Virt@ 0A is the next block. After the erasing of this block, the index is updated as

indicated on figure 8.

[0024] The man of the art will understand that the example was done on a reduced size of index and limited number of pre-erased page for explanation purpose. In the practice, the indicated number can be strongly increased.

Claims

1. A method for managing a non-volatile memory (LNVM) erasable by block wherein the method comprises an index management of the memory blocks wherein the index indicates, in a first field, for each block whether the block is erased (Erased), and in a second field, whether the block is no more used, and therefore to be erased (TBE), **characterized in that** a memory manager performs a block erasing when the memory is not in use and a block is indicated by the index to be erased and when the index indicates that the number of erased blocks is lower than a predetermined number.
2. The method of claim 1, wherein the block erasing is made on the oldest available block that is not erased.
3. The method of claim 1, wherein the index management is made on a number of blocks lower than the total number of blocks of the memory.
4. The method of claim 1, wherein the memory is inside an electronic device receiving commands according ISO7816 or ISO14443, and wherein the block erasing is made during an idle time of said commands.
5. Electronic device (SC) comprising at least one electrically erasable non-volatile memory (LNVM) which is erasable by blocks and a memory controller (μP) wherein the memory controller comprises an index of the memory storing, in a first field, for each block an indication of whether the block is erased, and, in a second field, whether the block is no more used and therefore to be erased, **characterized in that** the memory controller performs a block erasing when the memory is not in use and a block is indicated by the index as to be erased and when the index indicates that the number of erased blocks is lower than a predetermined number.

Patentansprüche

1. Verfahren zum Verwalten eines nichtflüchtigen Speichers (LNVM), der in Blöcken löschar ist, wobei das Verfahren eine Indexverwaltung der Speicherblöcke umfasst, wobei der Index in einem ersten Feld für jeden Block anzeigt, ob der Block gelöscht ist (Gelöscht), und in einem zweiten Feld, ob der Block nicht

mehr verwendet und daher gelöscht werden soll (TBE), **dadurch gekennzeichnet, dass** ein Speichercontroller ein Blocklöschen durchführt, wenn der Speicher nicht in Verwendung ist und ein Block durch den zu löschenden Index angezeigt wird, und wenn der Index anzeigt, dass die Anzahl von gelöschten Blöcken niedriger als eine zuvor bestimmte Anzahl ist.

2. Verfahren nach Anspruch 1, wobei das Blocklöschen auf dem ältesten verfügbaren Block vorgenommen wird, der nicht gelöscht wird. 10
3. Verfahren nach Anspruch 1, wobei die Indexverwaltung auf einer Anzahl von Blöcken vorgenommen wird, die niedriger als die Gesamtanzahl von Blöcken des Speichers ist. 15
4. Verfahren nach Anspruch 1, wobei der Speicher in einer elektronischen Vorrichtung ist, die Befehle gemäß ISO7816 oder ISO14443 empfängt, und wobei das Blocklöschen während einer Leerlaufzeit der Befehle vorgenommen wird. 20
5. Elektronische Vorrichtung (SC), umfassend mindestens einen elektrisch löschbaren nichtflüchtigen Speicher (LNVM), der durch Blöcke löschar ist, und eine Speichersteuerung (μ P), wobei die Speichersteuerung einen Index des Speichers umfasst, der in einem ersten Feld für jeden Block eine Anzeige davon speichert, ob der Block gelöscht ist, und in einem zweiten Feld, ob der Block nicht mehr verwendet und daher gelöscht werden soll, **dadurch gekennzeichnet, dass** die Speichersteuerung ein Blocklöschen durchführt, wenn der Speicher nicht in Verwendung ist, und ein Block durch den zu löschenden Index angezeigt wird, und wenn der Index anzeigt, dass die Anzahl von gelöschten Blöcken niedriger als eine zuvor bestimmte Anzahl ist. 25 30 35

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Revendications

1. Procédé de gestion d'une mémoire non volatile (LN-VM) effaçable par bloc dans lequel le procédé comprend une gestion d'index des blocs de mémoire dans lequel l'index indique, dans un premier champ, pour chaque bloc, si le bloc est effacé (Erased), et dans un second champ, si le bloc n'est plus utilisé, et donc destiné à être effacé (TBE), **caractérisé en ce qu'un** gestionnaire de mémoire effectue un effacement de bloc lorsque la mémoire n'est pas en cours d'utilisation et qu'un bloc est indiqué par l'index à effacer et lorsque l'index indique que le nombre de blocs effacés est inférieur à un nombre prédéterminé. 45 50 55
2. Procédé selon la revendication 1, dans lequel l'effa-

cement de bloc est réalisé sur le bloc disponible le plus ancien qui n'est pas effacé.

3. Procédé selon la revendication 1, dans lequel la gestion d'index est réalisée sur un nombre de blocs inférieur au nombre total de blocs de la mémoire.
4. Procédé selon la revendication 1, dans lequel la mémoire est à l'intérieur d'un dispositif électronique recevant des commandes selon les normes ISO7816 ou ISO14443, et dans lequel l'effacement de bloc est réalisé pendant un temps de repos desdites commandes.
5. Dispositif électronique (SC) comprenant au moins une mémoire non volatile effaçable électriquement (LNVM) qui est effaçable par blocs et un contrôleur de mémoire (μ P) dans lequel le contrôleur de mémoire comprend un index de la mémoire stockant, dans un premier champ, pour chaque bloc, une indication indiquant si le bloc est effacé, et, dans un second champ, si le bloc n'est plus utilisé et donc destiné à être effacé, **caractérisé en ce que** le contrôleur de mémoire effectue un effacement de bloc lorsque la mémoire n'est pas utilisée et qu'un bloc est indiqué par l'index comme étant effacé et lorsque l'index indique que le nombre de blocs effacés est inférieur à un nombre prédéterminé.

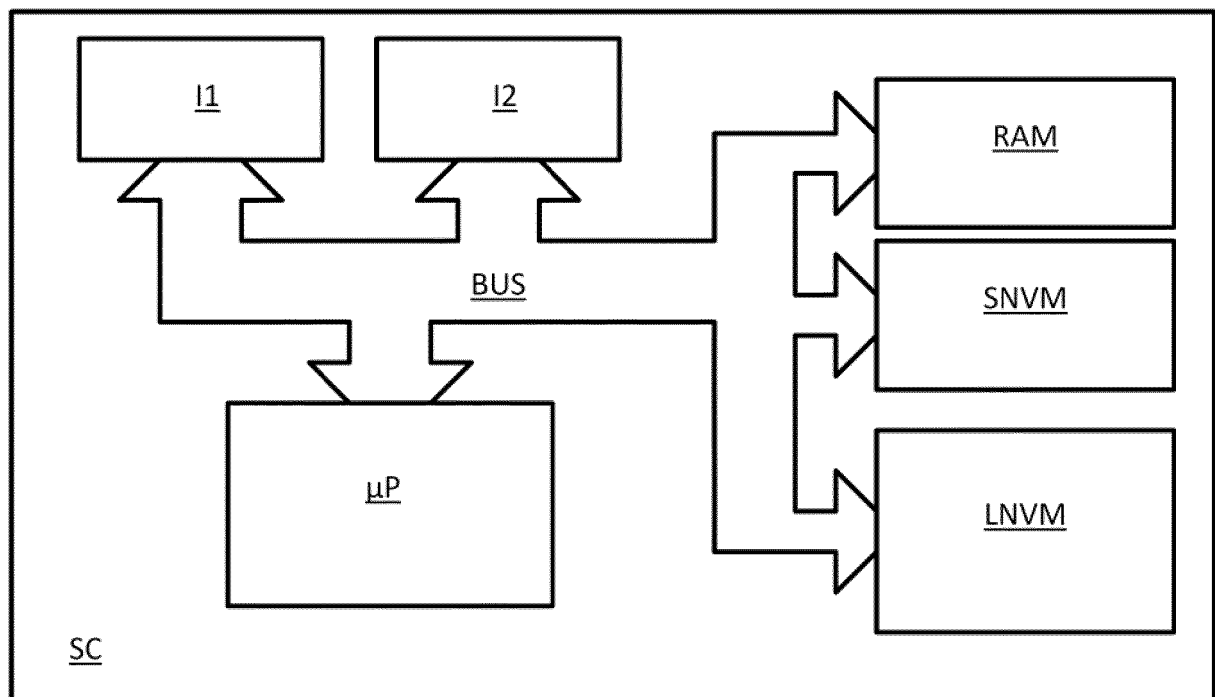


Figure 1

Data Area	Meta Data Area	
	CS/ECC	Memory Management
2048 Bytes	64 Bytes	64 Bytes

Figure 2

Meta Data Area					
CS/ECC	Used	NMU	Virt@	EQ Nb	Other
64 bytes	1 bit	1 bit	1 byte	1 byte	60 bytes and 6bits

Figure 3

Meta Data Area					
CS/ECC	Used[0-7]	NMU [0-7]	Virt@ [0-7]	EQ Nb	Other
8*8 bytes	1 byte	1 byte	12 bytes	1 byte	49 bytes

Figure 4

@	Data	ECC	Used	NMU	Virt@	EQ Nb
00	Written	Written	0	0	Not Val.	05
01	Written	Written	0	1	0F	FF
02	FF—FF	FF—FF	1	1	FF	FF
03	Written	Written	0	1	01	FF
04	Written	Written	0	1	02	FF
05	Written	Written	0	1	03	FF
06	FF—FF	FF—FF	1	1	FF	FF
07	Written	Written	0	1	00	FF
08	Written	Written	0	1	0E	FF
09	Written	Written	0	0	Not Val.	06
0A	Written	Written	0	0	Not Val.	08
0B	FF—FF	FF—FF	1	1	FF	FF
0C	Written	Written	0	1	04	FF
0D	Written	Written	0	0	Not Val.	07
0E	FF—FF	FF—FF	1	1	FF	FF
0F	Written	Written	0	1	05	FF
10	Written	Written	0	0	Not Val.	04
11	Written	Written	0	0	Not Val.	09
12	Written	Written	0	0	Not Val.	0A
13	Written	Written	0	0	Not Val.	0B

Figure 5

Virt@	Phy@	Erased	TBE
00	07	No	No
01	03	No	No
02	04	No	No
03	05	No	No
04	0C	No	No
05	0F	No	No
06	06	Yes	No
07	0B	Yes	No
08	02	Yes	No
09	0E	Yes	No
0A	10	No	Yes
0B	00	No	Yes
0C	09	No	Yes
0D	0D	No	Yes
0E	08	No	No
0F	01	No	No

Figure 6

Virt@	Phy@	Erased	TBE
00	07	No	No
01	03	No	No
02	04	No	No
03	05	No	No
04	0C	No	No
05	0F	No	No
06	06	No	No
07	0B	Yes	No
08	02	Yes	No
09	0E	Yes	No
0A	10	No	Yes
0B	00	No	Yes
0C	09	No	Yes
0D	0D	No	Yes
0E	08	No	No
0F	01	No	No

Figure 7

Virt@	Phy@	Erased	TBE
00	07	No	No
01	03	No	No
02	04	No	No
03	05	No	No
04	0C	No	No
05	0F	No	No
06	06	No	No
07	0B	Yes	No
08	02	Yes	No
09	0E	Yes	No
0A	10	Yes	No
0B	00	No	Yes
0C	09	No	Yes
0D	0D	No	Yes
0E	08	No	No
0F	01	No	No

Figure 8

REFERENCES CITED IN THE DESCRIPTION

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