

- [54] VAULT PROTECTED WITH ELECTRONIC TIME AND COMBINATION LOCK
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- [51] Int. Cl. .... E05b 49/00
- [58] Field of Search ..... 340/147 MD, 149 R, 164 R, 340/274; 307/40, 112, 133; 70/271, 272, 274

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## [57] ABSTRACT

A vault having a door controlled by an electronic time and combination lock. Access to the vault via the door is obtained by entering two separate and independent multi-digit combination sequences at or after a specified time of day which is preset in a 24-hour clock of a specified day which is preset in a day counter. The digits of each multi-digit sequence must be entered in

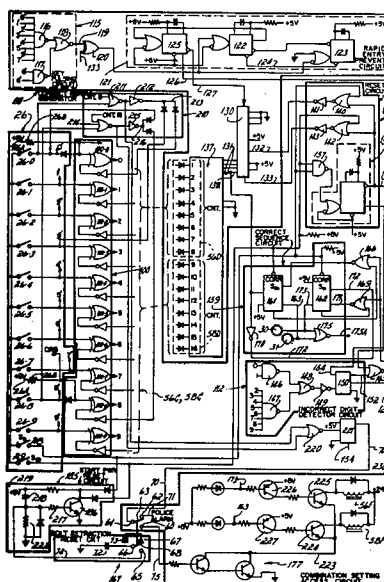
a predetermined order, although the digit sequences themselves may be entered in either order. Should authorized personnel possessing the multi-digit combination sequences be forced to open the vault at or after the preset time and day under threats of physical harm or the like, the vault can be opened by entry of slightly modified "duress" versions of the normal multi-digit combination sequences, which entries will also result in transmission of a secret alarm signal to a remote station, such as the police, alerting them to the forced entry condition.

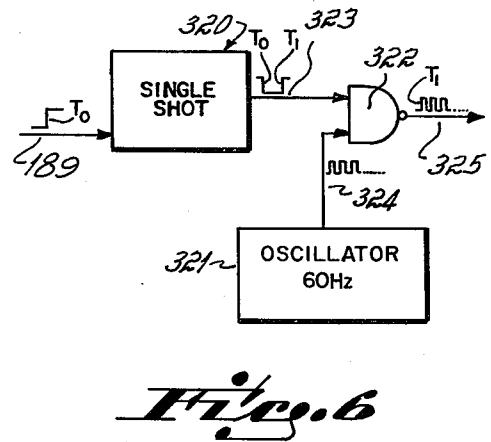
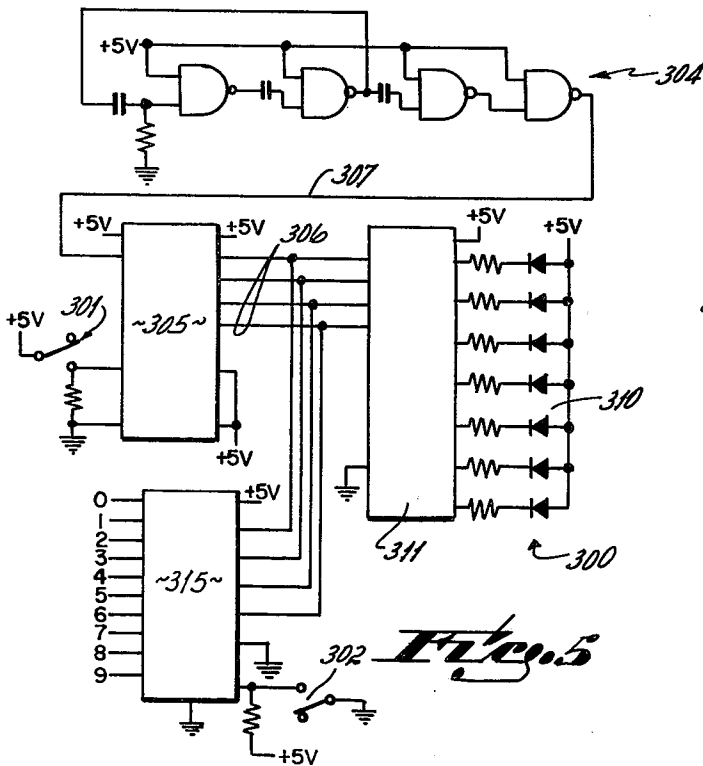
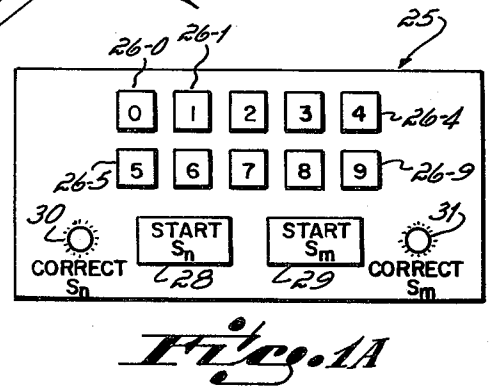
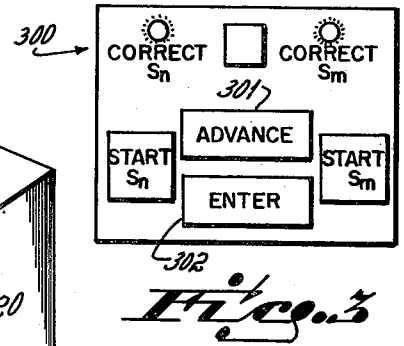
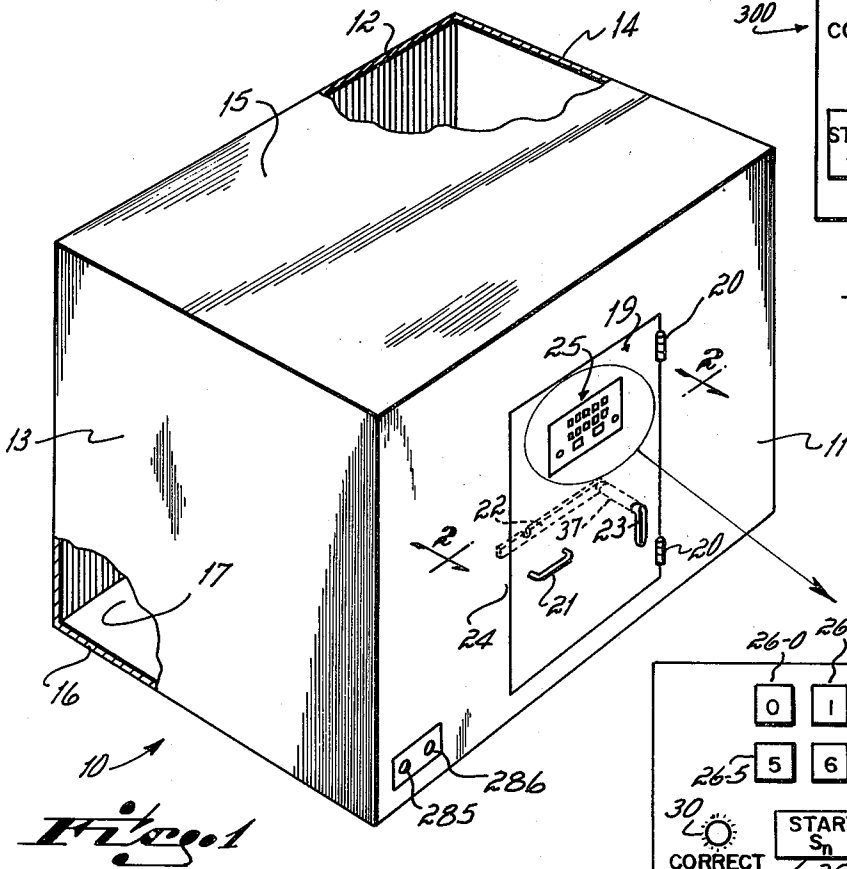
One or both of the combinations can be changed by correctly entering both combination sequences at the prescribed time and day, thereafter initiating access to the vault by, for example, retracting the bolt of the vault door, and thereafter entering the duress combination which, once accomplished, unlocks combination setting units mounted in the interior of the vault door.

In lieu of using a multi-digit keyboard to enter the various digits of the combination sequences, a variable single-digit display, display stepping key, and a digit entry key are provided. Sequential entry of different digits of a combination sequence is accomplished by sequentially stepping the display to display the different digits to be entered and as each digit to be entered is displayed actuating the digit entry key.

Other features are provided to accommodate various situations, such as occur when a person is inadvertently locked in the vault; an attempt is made to speed up the 24-hour clock and day counter to permit premature vault access; failure of the main power supply occurs; an attempt is made to rapidly enter different combination sequences, such as by computer means, to achieve access to the vault by trial-and-error digit entry techniques; etc.

17 Claims, 8 Drawing Figures





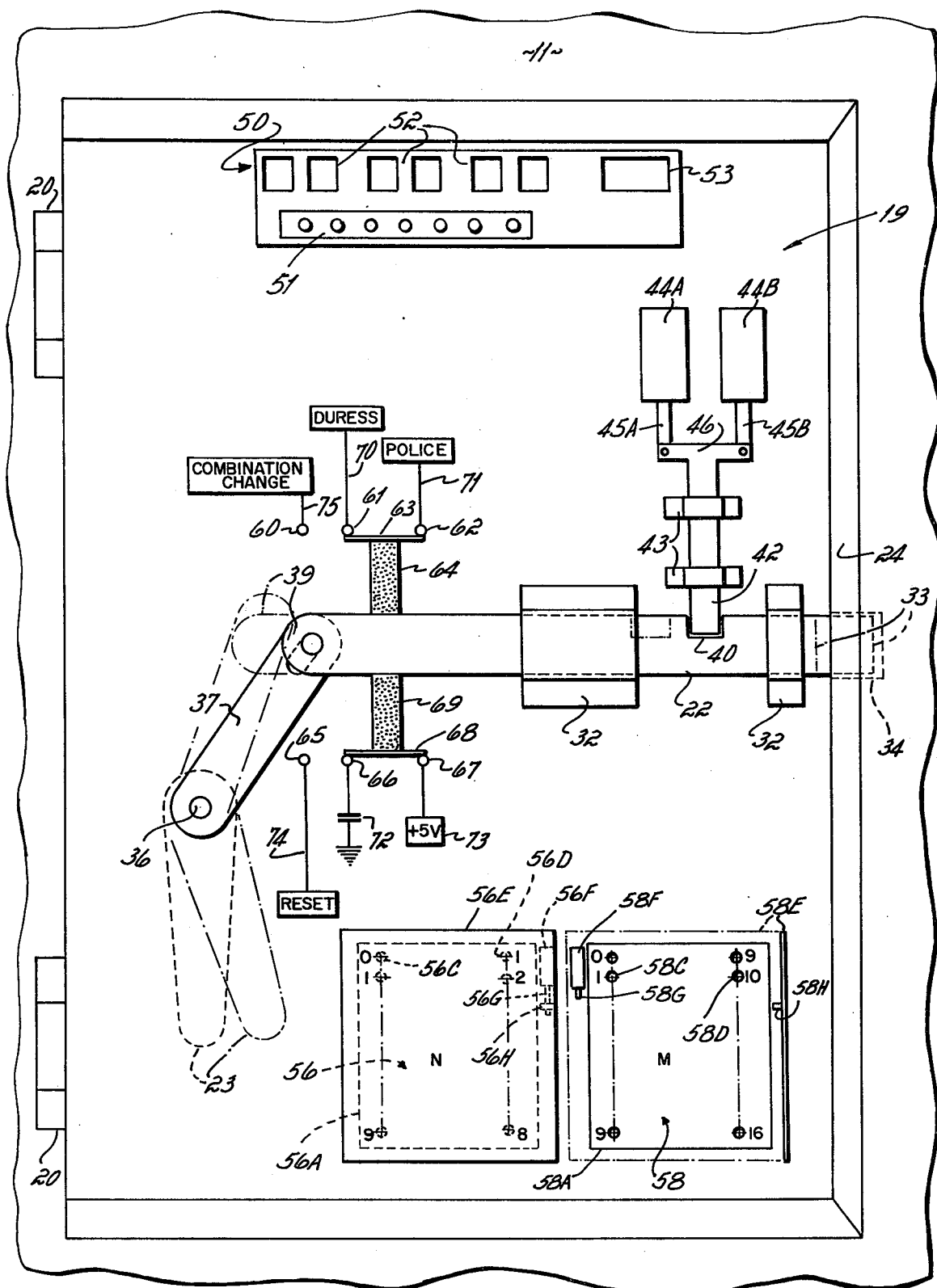
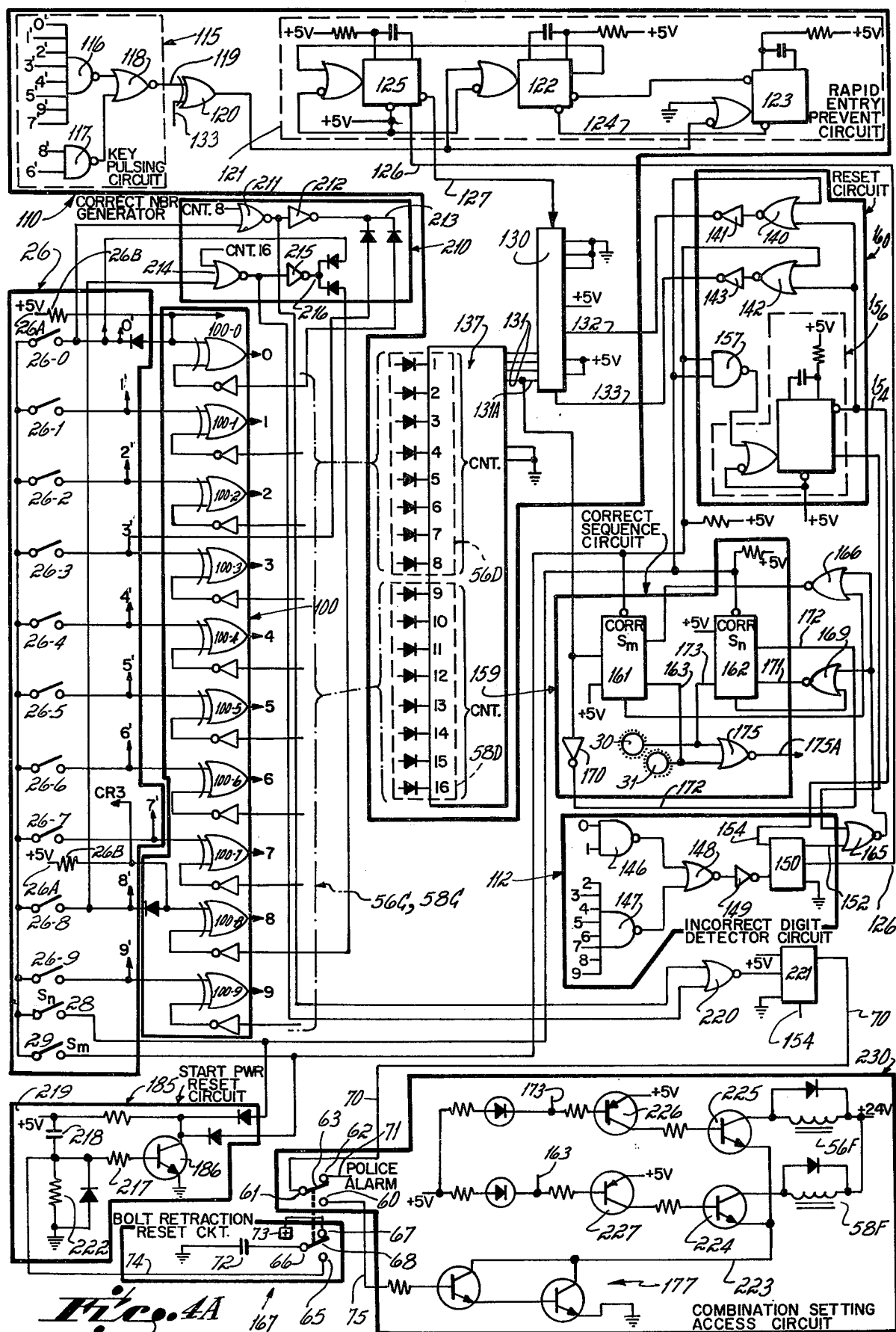


*Fig. 2*



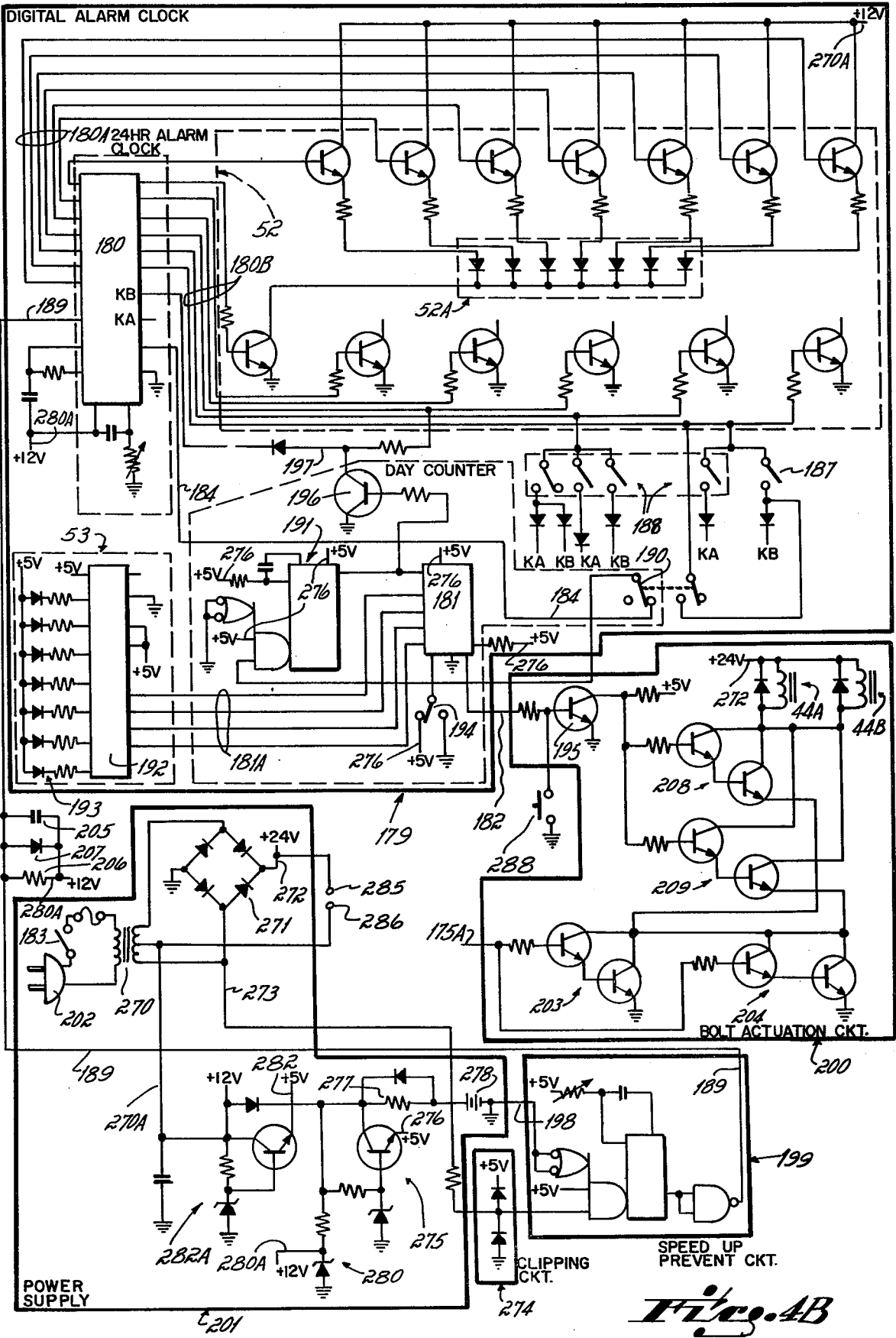


Fig. 4B

## VAULT PROTECTED WITH ELECTRONIC TIME AND COMBINATION LOCK

This invention relates to access control and more particularly to a vault or the like under control of an electronic time and combination lock.

As the sophistication of persons seeking unauthorized entry to a protected vault increases, it has become necessary to resort to more elaborate protective devices to avoid compromise of vault security. A vault protective system meeting present day standards against compromise by unauthorized personnel employing sophisticated equipment and techniques must necessarily be reasonably complex in structure and operation. However, its design must not be such that it is unduly complicated, rendering use by ordinary banking personnel not possessing substantial technical knowledge a difficult task.

It is also essential for a system, if to meet current standards of commercial acceptability, to accommodate reasonably foreseeable emergency situations without undue inconvenience. For example, it should be possible to operate an electronic timecontrolled vault at or after the specified time preset therein notwithstanding an intervening failure of the main electrical power supply. It should also be possible to access the vault without waiting for the present time to arrive should a person inadvertently become locked in the vault prior to the next preset time when it can be accessed. It is also important that a vault protective system accommodate for certain human errors, such as failure to reset the timing means prior to locking the vault to facilitate access at some future time and date. It is also desirable that combination changes be conveniently accomplished by authorized yet protection be provided against such change by unauthorized personnel. It is also desirable, in certain applications, to reduce the likelihood that unauthorized personnel observing entry of the digits of the correct combination will be able to determine the correct combination such that at a later time they could gain unauthorized access.

It has been an objective of this invention, therefore, to provide protection for a vault or the like which provides a high level of security against access by unauthorized personnel, and yet is relatively simple and convenient to use and accommodates for foreseeable mistakes by personnel using it.

The foregoing has been accomplished in accordance with certain principles of this invention by placing a vault door under the control of a combination and time lock which requires, at or after a specified time of a predetermined day preset in the system, correct entry, and in proper order, of the digits of two separate multi-digit combination sequences. In a preferred form, multiple digit keys corresponding to the different digits of the combination sequences are provided which, upon actuation, generate electrical signals corresponding to the digits being entered. These signals are then processed by validation means to determine if the digits entered and the order of entry thereof for both combinations are correct. Timing means presettable to a predetermined time of a specified day provide an electrical control signal which, in combination with an electrical control signal produced by the validation means upon proper entry of both combinations, causes an access signal to be produced for permitting access to the vault. The foregoing electronic time and combination lock

system provides a high degree of protection for a vault by reason of the fact that it requires correct entry and in proper order of the digits of two separate and independent multi-digit combination sequences, and further that both such sequences be correctly entered at or after a specified time and day preset in the system.

In a preferred form of the invention the timing device, which establishes the time and day when, or following which, correct entry of the digit combination sequences will be successful to permit access to the vault, is an electronic clock which is advanced at a predetermined rate in response to electrical reference pulses of fixed frequency derived from an external power supply of fixed frequency, e.g., a conventional 60Hz a.c. source. Assuming the timing device is set to provide an electrical time signal at and after 8:00 A.M. Monday morning, which signal in combination with the correct entry of both combination sequences will permit the vault to be accessed, a person seeking to compromise the vault protective system may attempt to accelerate the clock such that the timing signal, instead of being produced at and after 8:00 A.M. Monday when bank employees would customarily be present, is produced the preceding Sunday when bank employees are not ordinarily present. Were such efforts successful, the vault could conceivably be accessed on a Sunday by unauthorized personnel who surreptitiously gained knowledge of the combinations without interference by bank personnel. Premature generation of the time signal could be accomplished, for example, by substituting for the 60Hz power source a power supply operating at a much higher frequency. In this way, the clock timing means would be advanced at an above-normal rate, producing a timing signal on Sunday rather than Monday. To avoid this possibility and further enhance the security of the vault protection system, the electronic clock timing means of this invention is provided with an internal source of reference pulses of the desired frequency, e.g., 60Hz signals. Should the input to the clock timing means from an external source be altered to substantially exceed the normal pulse rate, the internal source responds to advance the clock at the predetermined normal rate at which it operates. Thus, any attempt to prematurely produce the clock timing signal by energizing the clock with power from a source of higher frequency than normal would be ineffective.

Personnel seeking to compromise the system may also attempt to enter the correct combination on a trial-and-error basis, for example, by rapidly entering in succession a vast number of combination sequences. Such could be accomplished with present-day technology by substituting a computer for the conventional keyboard entry device. In this way, a vast number of different multi-digit combination sequences could be entered in a methodical fashion, and in a manner of minutes, virtually assuring entry of the correct combination. To avoid the foregoing possibility and further enhance the security of the vault protection system, means are provided in this invention to limit system processing of digit signals to a rate not substantially in excess of the rate at which digits can be entered manually via a keyboard or the like. In a preferred form, the digit entry rate is limited by disabling the keyboard-operated digit signal generator for a brief interval, for example,  $\frac{1}{2}$  second, following entry of each digit. In this way, entry of a vast number of random digit combi-

nations to defeat the system on a trial-and-error basis would require weeks, if not months, and could not be accomplished on a weekend and go undetected by bank personnel.

In the event that an unauthorized person would seek to obtain access to the vault by forcing bank personnel to enter the correct combination at or after the specified time and day preset in the system, means are provided whereby the system is responsive to entry of a slightly modified form of the normal digit combination sequences herein termed the "duress sequences." Entry of the duress sequences simultaneously (a) opens the vault and thereby prevents possible harm to bank personnel who otherwise might resist, and (b) secretly transmits an electrical signal to a remote station, such as the police, indicating that the vault is being opened under force, or duress, conditions.

In accordance with a further aspect of the invention, the timing means which provides the timing signal, which timing signal in combination with correct entry of the two-digit sequences enables the vault to be accessed, includes a 24-hour clock and a day counter. The 24-hour clock can be preset to provide an electrical signal every 24 hours at a predetermined time, while the day counter can be preset to provide on the day to which the counter is preset, and thereafter unless reset, an electrical signal at the time preset in the 24-hour clock. Preferably the date counter is preset with a count corresponding to the day on which the time enabling signal is desired. For example, if the day counter is set at the close of the banking day on Friday and it is desired that the next time enabling signal be produced on Monday, the day counter is set to a count of 3. Upon the occurrence of each output from the 24-hour clock, which outputs occur at 24-hour intervals coincident with the time of day preset in the 24-hour clock, the day counter is decremented. When the 24-hour clock has been decremented to a count of zero, the time enabling signal is produced, which signal continues until the counter is reset to a nonzero count. An advantage of the foregoing approach, wherein a recycling 24-hour clock is used with and to decrement a day counter, is that should bank personnel fail to reset the day counter when locking the vault at the end of the day, and instead leave the day counter at zero, a time enabling signal will continue to be produced until the day counter is reset to a nonzero count. This permits the vault to be accessed at any time prior to counter reset by entry of the proper combination notwithstanding that the day counter has inadvertently not been set to a new day.

In accordance with a still further aspect of the invention and to facilitate convenient entry of the combination sequences, the system is provided with signal storage means which in effect store the fact that a combination sequence has been properly entered, which stored data is not cleared should the remaining combination fail to thereafter be correctly entered. Thus, if one of the combinations is correctly entered and an unsuccessful attempt is thereafter made to enter the second sequence, additional attempts can be made to enter the second sequence without the requirement that the first sequence be again correctly entered.

The invention includes a further convenience feature, namely, means for enabling the independent multi-digit combination sequences to be entered in either order. This is accomplished, in a preferred form of the

invention, by providing two separate and individual start keys respectively associated with each of the two independent combination sequences. The actuation of a particular one of the start keys effectively conditions the system for receipt and processing to determine validity of the digits of the sequence associated with the start key which was actuated. Depending upon the order in which the start keys are actuated, either one of the two combination sequences can be entered first.

To insure, once the vault has been accessed by correct entry of both multi-digit combination sequences, that subsequent accessing of the vault cannot be accomplished without re-entry of the correct combinations, automatic reset means are provided. In one form of the invention, switch means are associated with the bolt which locks and unlocks the vault door and, upon retraction of the bolt to place the vault in an open condition, a reset signal is generated which, among other things, clears the storage elements of the system which had previously stored signals reflecting the fact that the correct digit sequences have been entered. Thus, once access has been initiated by retraction of the bolt following entry of the correct digit sequences, access at a later date is not possible without again entering the correct digits. This automatic reset scheme eliminates the possibility of subsequent unauthorized access without re-entry of the correct digit sequences, as was possible with prior combination lock systems of the mechanical dial type wherein once the proper combination was mechanically entered via suitable dials, the vault remained unlocked and accessible until the combination dials were turned at random, or "scrambled," mechanically resetting the combination device.

In prior art multi-digit combination locks of the type wherein individual selectively actuatable digit keys are provided corresponding to each of the different possible digits which can be entered, it is possible by observing the keyboard location of the digits actuated by authorized personnel in entering the digits of a combination for an unauthorized person to determine the digits of the entered combination. To reduce this possibility of detection of the proper digits by observing entry thereof by an authorized person, an alternative form of keyboard is provided in accordance with a further aspect of the invention. Specifically, a visual display capable of displaying different digits, one-at-a-time, is provided which, in combination with a digit-enter key, enables entry of the digit displayed. Since entry of different digits is accomplished by actuating a sole digit-enter key, it is not possible to learn the identity of digits being entered by merely observing the location of the operator's finger as the keys are entered. Display of different digits such that, upon actuation of the sole digit entry key these different digits are entered, is accomplished with a second, or advance, key which, so long as it is actuated, cycles the display to successively display the different digits. When the digit which it is desired to enter is displayed, the advance key is released and the digit-enter key actuated, thereby entering the digit. Because of the extreme difficulty in correlating the digits being displayed with the actuation of the advance key, it is virtually impossible to determine the digits being entered by merely observing authorized personnel actuating the advance and digit-enter keys.

In a preferred form of the invention all electrical circuit components of the system, including the digit-entry signal generator, digit validator, timer, and the

means responsive to the validator and timer for permitting access to the vault upon coincidence thereof, are energized from a conventional 60Hz a.c. main power supply. Thus, under normal circumstances, i.e., when the main power supply is operative, the timer is advanced in response to a 60Hz reference signal derived from the main a.c. power supply. To enable the vault to be accessed at or after the specified time and day preset in the timer notwithstanding a power failure, a stand-by battery is provided which energizes, in the event of a main power failure, only the timer, thereby assuring that the timer is advanced as desired. In addition to the stand-by battery, connector means are provided accessible from outside of the vault for supplying, from an auxiliary power supply connected thereto, electrical power to the remaining components of the system, such as the digit entry signal generator, validator, and the circuit jointly responsive to the timer and the validator for permitting access to the vault.

In the event of a main power failure, the timer will advance in normal fashion under energization of the stand-by battery, to produce the time enable signal at the time and day preset in the timer. By connecting an auxiliary power supply to the remaining electrical components of the system from outside the vault via the connector provided, the remaining circuit components are energized, facilitating entry of the digits of the combination sequences, validation of the digits entered, and accessing of the vault should the correct digits be entered. As a consequence of this feature of the invention, should a power failure occur, for example during the course of a weekend when the bank is customarily closed, correct advancement of the timing means will not be hampered, and should the power failure still exist when the time enabling signal is produced, for example, at 8:00 A.M. the following Monday morning, the vault can nevertheless be opened at or after the desired time by connection of the auxiliary power supply from outside the vault and correct entry of the digits of the combination sequences.

Quite possibly, at the end of the business day and after the day counter has been reset to a nonzero count, the vault door could be closed and locked while a bank employee is still inside the vault. In such case it is desirable to permit the vault to be immediately re-opened by entry of the correct combinations without waiting for passage of the normal time period ordinarily necessary for production of the time enabling signal. To accomplish this, a manually operable switch is provided within the vault which, when actuated, simulates the time enabling signal. In this way, if, for example, a janitor sweeping out the vault and not having knowledge of either two combination sequences, is inadvertently locked in the vault at the close of the business day, the vault can immediately be opened by having (a) the janitor actuate the switch within the vault to simulate the time enable signal and (b) the bank personnel with knowledge of the combinations enter the correct digit sequences. Thus, the janitor is released without waiting until the time enable signal is produced in normal course, such as at 8:00 A.M. the following business day.

To facilitate convenient change of the combinations and yet restrict combination changing to authorized personnel, a further and equally important capability is incorporated in the preferred embodiment. Specifically, selectively lockable combination changing units are provided within the vault which, even if the vault

is open and access to its interior possible, are not accessible to permit changing the combinations since they are normally locked. To change a combination, it is first necessary to enter correctly, and at or after the preset time and day, both multi-digit combination sequences; thereafter initiate access to the vault by, for example, retracting the bolt, opening the door or the like; and finally enter the modified combination sequence customarily used in the duress mode. Depending upon which duress sequence is entered, access to that particular combination setting unit is provided. Since access to the vault interior following entry of the normal digit sequences has already occurred prior to entry of the duress sequence, entry of the duress sequence as an incident to obtaining access to the combination changing unit is ineffective to transmit an alarm signal to a remote station such as the police.

These and other advantages, features and objectives of the invention will become more readily apparent from a detailed description thereof taken in connection with the drawings in which:

FIG. 1 is a perspective view of a vault incorporating the electronic combination and time lock of this invention;

FIG. 1A is a front elevational view of the encircled area of FIG. 1 showing, in enlarged scale, the combination entry keyboard mounted in the outside wall of the vault door;

FIG. 2 is a rear elevational view taken generally along line 2—2 of FIG. 1 showing the interior of the vault door and contiguous vault wall structure showing the bolt operating mechanism and associated controls, the digital alarm clock and associated controls, and the combination setting unit;

FIG. 3 is a front elevational view of an alternative form of combination entry keyboard also useful with the electronic combination and time lock of this invention;

FIGS. 4A and 4B are schematic electrical circuit diagrams, partially in block format, of the electrical controls incorporated in a preferred embodiment of the electronic combination and time lock of this invention;

FIG. 5 is a schematic circuit, in block diagram format, of the digit entry device of FIG. 3; and

FIG. 6 is a schematic circuit diagram, in block format, of a circuit suitable for switching to an internal source of reference timing signals to advance the 24-hour clock should an attempt be made to speed-up the clock by providing reference signals of excessively high frequency to the 24-hour clock from an external source.

As shown in FIGS. 1 and 2, a typical vault 10 with which the electronic combination and time lock of this invention is useful includes front and rear walls 11 and 12, left and right side walls 13 and 14, ceiling 15 and a floor 16, which collectively establish a protected enclosure 17 selectively accessible via a door 19 under control of the electronic combination and time lock of this invention. The vault 10, including the door 19, can be constructed of conventional and known high strength materials designed to withstand forceable entry. The door 19 is mounted for pivotal swinging motion about one vertical side thereof by hinges 20. A handle 21 secured to the exterior surface of the door 19 is provided to facilitate opening and closing of the door when a bolt 22 is shifted to its retracted position shown in phantom. Bolt 22 is shiftable to its retracted

position shown in phantom in FIG. 2 in which it is disengaged from the door jamb 24 in response to pivoting a pivotal handle 23 also mounted to the exterior of the door 19.

Mounted in the exterior surface of the door above handles 21 and 23 is a combination entry keyboard, shown enlarged in FIG. 1A, which facilitates entry of the digits of the combination in a manner to be more fully explained hereinafter. The combination entry keyboard 25, in the preferred embodiment depicted in FIG. 1A, includes ten selectively actuatable decimal digit keys 26-0, 26-1, . . . 26-9. The digit keys 26-0, 26-1, . . . 26-9 are preferably spring-biased to an outward position in which a pair of electrical contacts associated therewith are open-circuited or electrically disconnected, but which upon depression, or actuation, close to electrically connect the pair of contacts associated with the depressed key. In a preferred form, the multi-digit combination which must be entered as one of the conditions for operating the electronic combination and time lock takes the form of two separate and independent multi-digit number sequences  $S_n$  and  $S_m$ , each consisting of eight decimal digits. The digits of each sequence  $S_n$  and  $S_m$ , as a condition for operating the electronic combination and time lock, must be entered in a predetermined digit sequence, although either sequence  $S_n$  or  $S_m$  may be entered first.

To facilitate entry of the digits of each of the two multi-digit combination sequences  $S_n$  and  $S_m$  in either of the two possible chronological orders, i.e., combination sequence  $S_n$  followed by sequence  $S_m$  or vice versa, a start  $S_n$  key 28 and a start  $S_m$  key 29 are provided. Start  $S_n$  and  $S_m$  keys 28 and 29 are actuated prior to entering the multi-digit combination sequences  $S_n$  and  $S_m$ , respectively, via the digit keys 26-0, 26-1, . . . 26-9. While the start  $S_n$  key 28 and the start  $S_m$  key 29 must be actuated before entry of the digits of their respectively associated multidigit combination sequence  $S_n$  and  $S_m$ , respectively, either sequence  $S_n$ ,  $S_m$ , and hence either start key 28 or 29, may be actuated first. To indicate proper entry in the correct sequence of the digits of each multi-digit combination sequence  $S_n$  and  $S_m$ , which preferably have eight digits per sequence, a correct  $S_n$  indicator light 30 and a correct  $S_m$  indicator light 31 are provided. These lights 30 and 31 become illuminated upon correct entry in the proper sequence of the digits of their respectively associated multi-digit combination sequence  $S_n$  and  $S_m$ .

As shown best in FIG. 2, which is an elevational view of the rear interior surface of the vault door 19, the bolt 22 is seen to take the form of an elongated rod which is mounted for horizontal sliding motion between lock and unlock positions by bracket 32 secured to the rear surface of the door. In the extended or lock position of bolt 22 (shown in solid lines) the free end 33 of the bolt projects into an appropriately located recess 34 formed in the door jamb 24 preventing opening of the door; while in the retracted or unlock position (shown in phantom) the outer end 33 of the bolt is disengaged from the door jamb recess 34, permitting the door to be opened.

To facilitate horizontal sliding motion of the bolt 22 between its lock and unlock positions upon correct entry of both combination sequences  $S_n$  and  $S_m$ , the pivotal handle 23 mounted at the front of the door 19 is provided. The handle 23 is fixed at one end to a horizontal actuating shaft 36 which extends through the

door 19, the other end of the shaft being fixed to the lower end of a lever 37 located adjacent the inner surface of the door. The lever 37 has its other end pinned to the inner end 39 of the bolt. When the handle 23 is pivoted counterclockwise, as viewed in FIG. 2, the shaft 36 and lever 37 which are rigidly secured to each other rotate about the axis of the shaft 36 in a counterclockwise direction shifting the bolt 22 from the extended, lock position (shown in solid lines) to the retracted, unlock position (shown in phantom lines). When the handle 23 is rotated in the clockwise direction, as viewed in FIG. 2, the shaft 36 and lever 37 operate to shift the bolt 22 from its retracted, unlock position to its extended, lock position in which its outer end 33 engages the door jamb 24.

To alternatively permit and prevent, on a selective basis, horizontal shifting motion of the bolt 22 between its lock and unlock positions, a notch 40 in the upper surface of the bolt 22 is provided in combination with a selectively operable vertically shiftable detent 42. The detent 42 is mounted by suitable brackets 43 secured to the interior of door 19 for vertical sliding motion between a lower position in which the bottom free end thereof engages the bolt notch 40 to prevent movement of the bolt from the lock position, and an upper position in which the lower end of the detent 42 is disengaged from the bolt notch 40 to facilitate movement of the bolt between the lock and unlock positions. A pair of solenoids 44A and 44B mounted to the interior of door 19 have vertically shiftable cores 45A and 45B connected at their lower ends to opposite ends of a horizontal bar 46, the midportion of which is secured to the upper end of the detent 42. Solenoids 44A and 44B are selectively energizable to raise the detent 42 from its lower position engaging the notch 40 of the bolt 22 to an upper position disengaged from the bolt notch to permit the bolt 22 to be moved from its lock position to its unlock position by the handle 23. Energization of solenoids 44A and 44B to permit unlocking of the vault door 19 occurs, in a manner to be described, when both combination sequences  $S_n$  and  $S_m$  have been properly entered during a specified time period of a specified day established by the setting of a digital alarm clock, in a manner also to be described in detail hereinafter.

Mounted to the interior of the door 19 is a control panel 50 for setting the digital alarm clock, which includes a 24-hour clock and a day counter, to the correct time of day, and for setting the specified day and period during such day, when the digital alarm clock will provide an output which, in combination will correct entry of the digit sequences  $S_n$  and  $S_m$  will enable the bolt 22 to be moved from its lock to its unlock position via handle 23 to open the vault. Also mounted on the rear surface of the door 19 is a digital read-out, or display 52, which displays in digital format, and on an alternative basis, either (a) the correct time of day in hours, minutes and seconds, or (b) the specified time period during the day preset in the 24-hour clock when the 24-hour clock provides a signal which, in combination with a similar signal from the day counter correlated to a specified day preset therein, facilitates opening the vault upon proper entry of both the digit sequences  $S_n$  and  $S_m$ . A second display or digital read-out 53 is mounted on the rear surface of the door 19 for providing a digital read-out of the number of days from the setting of the day counter which must elapse before the signal from the 24-hour clock is effective to enable

the vault to be opened upon correct entry of both combination sequences  $S_n$  and  $S_m$ . Switches 51 permit setting the day counter and 24-hour clock to the desired settings in a manner to be described.

For example, if at the end of the business day on Friday, it is desired to have the digital alarm clock produce a signal at 8:00 A.M. the following Monday to permit opening of the vault door (assuming the correct number sequences  $S_n$  and  $S_m$  are entered at that time), the 24-hour clock will be set for 8:00 A.M. and the day counter set for three days hence, i.e., Monday morning. Since the door unlock enabling time signal is to be provided at 8:00 A.M. on the third day, i.e., Monday following the day on which the digital alarm clock is set, i.e., Friday, the digital display 53 of the 24-hour clock will display either the correct time of day such as 5:00 P.M. when the digital alarm clock is being reset for Monday at 8:00 A.M., or the time of day when the 24-hour clock is to produce its output signal, namely, at 8:00 A.M. and thereafter. Instead of using the same display 52 to alternatively display the correct time of day and the time of day when the unlocking of the vault is to be permitted by proper entry of the number sequences  $S_n$  and  $S_m$ , two separate displays could be provided.

As indicated the vault door 19 is capable of being unlocked upon proper entry, following passage of the time interval established by the digital alarm clock, of both multi-digit number sequences  $S_n$  and  $S_m$ . Additionally, the vault door is capable of being unlocked if, following passage of the time interval established by the digital alarm clock, digit sequences  $S_n'$  and  $S_m'$  are both entered, these latter digit sequences being hereafter referred to as "duress" sequences. In order to avoid possible harm to bank employees having knowledge of the digit sequences  $S_n$  and  $S_m$ , who may be coerced or threatened by a person intent on gaining unlawful access to the vault, it is desirable to provide means whereby the bank employee can simultaneously unlock the vault and secretly transmit an electrical signal to a remote station, such as to the police, indicating that the bank is being opened forceably and under duress.

Accordingly, in addition to enabling the vault 10 to be unlocked by entry of the normal digit sequences  $S_n$  and  $S_m$  during the time period and day established by the digit alarm clock, in which case no remote police alarm is transmitted, it is also possible to open the vault at or after the time and day determined by the digital alarm clock as well as simultaneously transmit an alarm to a police station or the like, by entering duress digit sequences  $S_n'$  and  $S_m'$ . Digit sequence  $S_n'$  differs from digit sequence  $S_n$  in accordance with a preferred form of the invention, in that only the last digit of the sequence is altered. For example, if the normal sequence  $S_n$  is 5-2-3-9-4-7-6-3, the duress sequence  $S_n'$  will, in a preferred form, be 5-2-3-9-4-7-6-0, the last digit only being changed. Similarly, if the normal sequence  $S_m$  is 2-6-5-4-9-8-6-0, the duress sequence  $S_m'$  will be 2-6-5-4-9-8-6-8, with the last digit only being changed.

To facilitate changing the combination sequences  $S_n$  (and  $S_n'$ ) and/or  $S_m$  (and  $S_m'$ ), combination setting units 56 and 58, respectively, are provided. Each of the combination setting units 56 and 58 includes a patch board 56A and 58A, respectively. Each patch board 56A and 58A includes a row of digit sockets 56C and 58C, respectively, and a row of sequence sockets 56D and 58D, respectively. Depending upon the connec-

tions made by jumper cables or the like between the sequence sockets 56D and 58D and the respectively associated digit sockets 56C and 58C, the multi-digit combination sequences  $S_n$  (and  $S_n'$ ) and  $S_m$  (and  $S_m'$ ), respectively, will vary. For example, if the normal digit sequence  $S_n$  is 5-2-3-9-4-7-6-3 ( $S_n'$  being 5-2-3-9-4-7-6-0), jumper cables would be connected between sockets 1 and 5, 2 and 3, 3 and 3, 4 and 9, 5 and 4, 6 and 7, 7 and 6, and 8 and 3 of socket sets 56C and 56D, respectively, of patch panel 56A of the combination setting unit 56. Similarly, if the combination normal sequence  $S_m$  is 2-6-5-4-9-8-6-0 ( $S_m'$  being 2-6-5-4-9-8-6-8), interconnection with jumper cables of sockets 2 and 9, 6 and 10, 5 and 11, 4 and 12, 9 and 13, 8 and 14, 6 and 15, and 0 and 16 of socket sets 58C and 58D, respectively, of patch panel 56A of combination setting unit 58 would be made.

Each of the combination setting units 56 and 58 includes a closure of door 56E and 58E, respectively, which in their closed positions deny access to the combination setting sockets and jumper cables, and which in their open position permit such access for changing the number sequences  $S_n$  and  $S_m$ . Solenoids 56F and 58F have vertically shiftable cores 56G and 58G engageable in their lowermost position with apertured ears 56H and 58H mounted to the inner surface of doors 56E and 58E to selectively lock and unlock the doors 56E and 58E.

In order to gain access to one or both of these combination setting patch panels 56A and 58A to change one or both of the combination sequences  $S_n$  (and  $S_n'$ ) and  $S_m$  (and  $S_m'$ ) it is necessary that both digit sequences  $S_n$  (or  $S_n'$ ) and  $S_m$  (or  $S_m'$ ) be entered at or after the time and day established by the digital alarm clock and the bolt 22 retracted, whereupon the vault door can be opened to permit access to the rear of the vault door, and thereafter that the duress sequence  $S_n'$  and/or  $S_m'$  be correctly entered whereupon solenoids 56F and/or 58F are energized to unlock doors 56E and/or 58E, depending upon whether one or the other or both of the multi-digit number sequences  $S_n$  (and also  $S_n'$ ) and  $S_m$  (and also  $S_m'$ ) are to be changed. If only combination sequence  $S_n$  (and  $S_n'$ ) is to be changed, it is necessary that both digit sequences  $S_n$  (or  $S_n'$ ) and  $S_m$  (or  $S_m'$ ) be entered at or after the specified time and day established by the digital alarm clock, the bolt 22 thereafter placed in its unlock position to provide access to the rear of vault door 19, and that the duress sequence  $S_n'$  be entered to energize solenoid 56F to unlock door 56E. Similarly, if only sequence  $S_m$  (and  $S_m'$ ) is to be changed, it is necessary that both sequences  $S_n$  (or  $S_n'$ ) and  $S_m$  (or  $S_m'$ ) be entered at or after the time and day established by the digital alarm clock, that the bolt 22 be placed in its retracted position to facilitate access to the rear of the vault door, and thereafter that the duress sequence  $S_n'$  be entered to energize the solenoid 58F to unlock door 58E. If both digit sequences  $S_n$  (and  $S_n'$ ) and  $S_m$  (and  $S_m'$ ) are to be changed, it is essential that digit sequences  $S_n$  (or  $S_n'$ ) and  $S_m$  (or  $S_m'$ ) be entered at or after the time and day established by the digital alarm clock, that the bolt 22 be placed in its unlock position to facilitate access to the rear of vault door 19, and that thereafter both duress sequences  $S_n'$  and  $S_m'$  be entered to energize solenoids 56F and 58F to unlock doors 56E and 58E, respectively.

Mounted to the rear surface of the door 19 and associated with the horizontally shiftable bolt 22 are sta-

tionary electrical contacts 60, 61 and 62 which cooperate with a movable electrical contact 63 secured to the upper surface of the bolt via an electrically insulative bracket 64, and stationary contacts 65, 66 and 67 which cooperate with a movable electrical contact 68 secured to the lower surface of the bolt via an insulative bracket 69. When the bolt 22 is in the extended lock position, electrically conductive contact 63 connects stationary contacts 61 and 62 such that should a duress signal be present on line 70, as a consequence of entry when the door is closed of both duress sequences  $S_n'$  and  $S_m'$  during the time interval and day established by the digital alarm clock, indicating that a duress condition exists, the duress signal on line 70 will be connected to output line 71 to a police station or the like. Additionally, when the bolt 22 is in the extended lock position, contacts 66 and 67 are electrically connected by electrically conductive contact 68 to charge a capacitor 72 from a source of positive potential 73. When the bolt 22 is thereafter retracted and stationary contacts 65 and 66 connected via the contact 68 which has now shifted leftwardly, the capacitor 72 will discharge via a line 74 to reset the electronic lock circuitry. Resetting is effective to de-energize solenoids 44A and 44B enabling the detent 42 to drop vertically such that when the bolt 22 is once again moved to its extended position following opening of the door, the detent 42 and bolt notch 40 will automatically engage to lock the bolt in its extended position. Resetting is also effective to require that both digit sequences  $S_n$  (or  $S_n'$ ) and  $S_m$  (or  $S_m'$ ) again be entered during the time and day specified by the electronic alarm clock to facilitate access to the vault once the door has been closed and the bolt placed in its extended position wherein it is automatically locked by the detent 42 in the manner described.

When the bolt 22 is in its retracted, unlock position, stationary contacts 60 and 61 are electrically connected by the electrically conductive contact 63. The effect of this is to apply a duress signal appearing on line 70, produced by entry of one or both duress sequences  $S_n'$  or  $S_m'$  when the door is open and it is desired to change one or more of the sequences  $S_n$  (and  $S_n'$ ) or  $S_m$  (and  $S_m'$ ) to line 75 of a combination setting access circuit, to be described, which in a manner described previously permits doors 56E and/or 58E to be opened depending upon whether one or both of the patch boards 56A or 58A is to be accessed to permit changing of the combination sequences  $S_n$  (and  $S_n'$ ) and  $S_m$  (and  $S_m'$ ).

Assuming that the combination lock circuitry has been reset by return of the bolt 22 to its extended lock position and that the electronic alarm clock has been set via the control panel 50 to provide an enabling signal at and after a specified time during some future day, such as at or after 9:00 A.M. the day following setting of the day counter of the digital alarm clock, the sequence of operations involved in unlocking the vault door will now be briefly summarized. Specifically, at 9:00 A.M. the day following setting of the day counter, each of the multi-digit combination sequences  $S_n$  (or  $S_n'$ ) and  $S_m$  (or  $S_m'$ ) are entered via the combination entry keyboard 25. If digit sequence  $S_n$  (or  $S_n'$ ) is to be entered first, the start  $S_n$  key 28 is depressed, whereupon the digit keys of sequence  $S_n$  (or  $S_n'$ ) are sequentially momentarily depressed. For example, if digit sequence  $S_n$  is 5-2-3-9-4-7-6-3, digit keys 26-5, 26-2,

26-3, 26-9, 26-4, 26-7, 26-6 and 26-3 are sequentially momentarily actuated. Upon conclusion of this, lamp 30 becomes illuminated indicating that digit sequence  $S_n$  was correctly entered. Following correct entry of sequence  $S_n$  (or  $S_n'$ ) digit sequence  $S_m$  (or  $S_m'$ ) is entered. This is accomplished by first momentarily depressing the start  $S_m$  key 29, followed by sequential entry of the digit keys corresponding to sequence  $S_m$  (or  $S_m'$ ). If the digits of sequence  $S_m$  are 2-6-5-4-9-8-6-0, digit keys 26-2, 26-6, 26-5, 26-4, 26-9, 26-8, 26-6 and 26-0 are sequentially entered, whereupon lamp 31 becomes illuminated to indicate that sequence  $S_m$  has been correctly entered.

With both of the normal digit sequences  $S_n$  and  $S_m$  both correctly entered and such entry having taken place at or after the time and day set in the digital alarm clock, in this example, 9:00 A.M. of the day following setting of the day counter, the solenoids 44A and 44B are energized to retract their armatures 45A and 45B and in turn disengage the detent 42 from the bolt notch 40. With detent 42 and bolt notch 40 disengaged, the bolt 22 can be horizontally shifted by rotation of handle 23 in a counterclockwise direction as viewed in FIG. 2 to the retracted position shown in phantom lines, disengaging bolt end 33 from ramp recess 34. The door can now be opened by pulling handle 21 outwardly.

Movement of the bolt 22 from the extended lock position to the retracted unlock position shifts movable electrical contact 68 to connect stationary contact 65 and 66 enabling capacitor 72, now fully charged, to discharge via line 74 to a reset circuit. As a consequence, the electronic combination lock circuitry is reset to de-energize solenoids 44A and 44B, allowing detent 42 to drop atop the bolt between the notch 22 and the bolt end 33. When the door is later closed and the bolt 22 returned to its extended lock position, the detent 42 will automatically seat in the bolt notch 40 to prevent retraction of the bolt until the next successful entry of combination sequences  $S_n$  and  $S_m$  at the time and day prescribed by the electronic alarm clock. The discharge of capacitor 72 on line 74 to the reset circuit is also effective to destroy the circuit conditions of the electronic combination lock previously existing as a consequence of the correct entry of sequences  $S_n$  and  $S_m$  at or after the time and day set by the electronic alarm clock. It is now necessary to again enter the correct combination sequences  $S_n$  and  $S_m$  at or after the time and day prescribed by the electronic alarm clock before the solenoids 44A and 44B can again be energized to permit the bolt 22 to be retracted from a locked to an unlocked position.

While the foregoing examples assumed that digit sequence  $S_n$  was entered to digit sequence  $S_m$ , unlocking of the vault can be accomplished by entry of digit sequence  $S_m$  followed by correct entry of digit sequence  $S_n$ , providing that start  $S_m$  key 29 is actuated prior to entry of digit sequence  $S_m$  and further that start  $S_n$  key 28 is actuated prior to entry of digit sequence  $S_n$ , with the digit sequences and their respective start keys being actuated in the order of sequence  $S_m$  first and sequence  $S_n$  thereafter.

Further, had duress conditions existed, the vault door could have been unlocked at or after the time and day set by the electronic alarm clock, for example, at or after 9:00 A.M. the following day by setting of the day counter, by entry, in any order, of the duress sequences  $S_n'$  and  $S_m'$ . In addition to unlocking the vault door,

entry of the digit sequences  $S_n'$  and  $S_m'$  during the time interval and day set in the electronic clock would have been effective to generate an electrical signal on line 70 which would have been transmitted to the police station on line 71 by contact 63 which, until both duress sequences  $S_n'$  and  $S_m'$  are correctly entered and the bolt 22 shifted to its retracted position, is in its lock position bridging stationary contacts 61 and 62.

With reference to FIGS. 4A and 4B, the keyboard 26 includes ten digit keys 26-0, 26-1, . . . 26-9. Each digit key is normally open such that a logical 1 is present on each of the digit key output lines which are input to a comparator 100. The logical 1 signals are provided by a 5-volt potential source 26A connected to the digit key output lines via a resistor 26B. The connection to source 26A via resistor 26B is shown only for keys 26-0 and 26-8, although all digit keys 26-0 through 26-9 are so connected. Source 26A is supplied from power supply 201 to be described. Momentary actuation of any one of the digit keys 26-0, 26-1, . . . 26-9 connects the output line of the actuated digit key to ground potential 26C with the result that current flows through the associated resistor 26B to ground from the source of positive potential 26A, applying a voltage slightly above ground potential, or a logical 0 signal, to the output of the digit key actuated. Release of the momentarily actuated digit key restores the output of that key to a logical 1 level since current through associated resistor 26B, and the resulting voltage drop thereacross, decreases to zero when the digit key is released.

Start  $S_n$  key 28 and start  $S_m$  key 29 operate in the same manner as the digit keys 26-0, 26-1, . . . 26-9 to provide a logical 0 signal on their output lines when their respective output keys are momentarily actuated to a closed-circuit condition, and provide a logical 1 signal level on their respective output lines when in the unactuated, open-circuit condition. Isolating diodes 26D, 26D are connected in the output lines of digit keys 26-0 and 26-8, which particular keys are the duress keys for digit sequences  $S_n$  and  $S_m$ , respectively, between the respective digit key and the resistor 26B for reasons to become apparent hereafter in connection with the "duress" capability.

The comparator 100 includes ten Exclusive-Or circuits 100-0, 100-1, . . . 100-9 associated respectively with the ten digits, 0, 1, . . . 9 represented by digit keys 26-0, 26-1, . . . 26-9. Each of the Exclusive-Or gates of the comparator 100 has one of its two inputs connected to a respectively associated different digit key, and the other of its inputs connected via respectively associated different inverter to a respectively associated different output of a correct combination number sequence generator 110. During entry of a digit sequence  $S_n$  or  $S_m$ , if the digit is a correct digit and is being entered in proper order, a logical 0 level is input to the Exclusive-Or circuit associated with the correct digit from the correct digit key while a logical 1 is input to the Exclusive-Or circuit associated with the correct digit, following inversion, from the correct combination number sequence generator 110. For example, if sequence  $S_n$  is 5-2-3-9-4-7-6-3 and the second digit 2 thereof is being entered, Exclusive-Or gate 100-2 will have a logical 0 input to it from actuated digit key 26-2 and a logical 1 input to it as a consequence of a logical 0 being provided by the correct combination number sequence generator which is then inverted prior to input to the other terminal of Exclusive-Or gate 100-2. Thus, when

the correct digit of a sequence  $S_n$  or  $S_m$  is entered in proper order, the Exclusive-Or gate associated with that digit will provide on its output line a logical 1 signal.

If digit key 26-2 corresponding to the digit 2 is not actuated as the second digit of the illustrative sequence  $S_n$ , a logical 1 will be input to Exclusive-Or gate 100-2 from digit key 26-2. Since a logical 1 is input to the other terminal of Exclusive-Or gate 100-2 as a consequence of the logical 0 input to its associated inverter circuit from the correct combination sequence generator 110, a logical 0 will be provided at the output of Exclusive-Or gate 100-2. This logical 0 output from Exclusive-Or gate 100-2, in a manner to be apparent hereafter, will be sensed by an incorrect digit detector circuit 112.

Again assuming the correct second digit of sequence  $S_n$  is a digit 2, if during entry of the second digit a digit key other than the correct key 26-2 is actuated, such as digit key 26-3, a logical 0 signal will be provided on the output of Exclusive-Or gate 103 which, in a manner to be described hereafter, will be detected by the incorrect digit detector circuit 112.

Specifically, if digit key 26-3 corresponding to an incorrect digit is depressed instead of digit key 26-2, a logical 0 is input from depressed digit key 26-3 to one terminal of the Exclusive-Or gate 100-3, while a logical 0 is input to the other terminal of the Exclusive-Or gate as a consequence of inversion of a logical 1 signal provided by the correct combination of the sequence generator 110. With a logical 0 signal input to both terminals of Exclusive-Or gate 100-3, a logical 0 is provided at the output of this Exclusive-Or gate which, as noted, is detected by the incorrect digit detector circuit 112.

Similarly, if digit key 26-3 corresponding to an incorrect digit is actuated simultaneously with digit key 26-2 corresponding to a correct digit, a logical 0 will be produced from Exclusive-Or gate 100-3 which will be detected by incorrect digit circuit 112 notwithstanding that a logical 1 signal is produced by Exclusive-Or gate 100-2 reflecting the fact that the correct digit key 26-2 was actuated.

If during actuation of digit key 26-2, a correct key, none of the other digit keys are actuated, logical 1 signals will be provided from the Exclusive-Or gate 26-0, 26-1 and 26-3 through 26-9 reflecting the fact that no incorrect digit was entered. For example, assuming digit key 26-3, an incorrect digit, is not actuated, a logical 1 is input from this unactuated digit key to its respectively associated Exclusive-Or gate 100-3, while a logical 0 input to the other terminal of this Exclusive-Or gate as a consequence of inversion of a logical 1 signal provided by the correct combination number sequence generator 110, producing a logical 1 signal from the Exclusive-Or gate reflecting the fact that digit key 26-3, corresponding to an incorrect digit, was not actuated.

Summarizing, if during the entry of a digit of one of the digit sequences  $S_n$  or  $S_m$  the key corresponding to the correct digit and only that key is actuated, logical 1 signals will be provided at the outputs of all the Exclusive-Or gates 100-0, 100-1, . . . 100-9. If an incorrect key is actuated, either alone or simultaneously with actuation of the correct digit key, a logical 0 will be output from the Exclusive-Or gate associated with the incorrectly actuated key, which logical 0 signal will be detected by the incorrect digit detector circuit 112, in

a manner to be described. Thus, the circuit of this invention operates to detect actuation of a correct digit key in proper sequence, as well as actuation of an incorrect digit key. An "incorrect" digit key may be a key corresponding to a digit which is not contained in the correct digit sequence, such as the digit 1 in a sequence  $S_n$  having digits 5-2-3-9-4-7-6-3, or may be a key corresponding to a digit which is included in the digit sequence, but which actuation occurs out of sequence or order, such as occurs if digit key 26-2 corresponding to a 2 is actuated other than as the second digit of the sequence  $S_n$  comprising digits 5-2-3-9-4-7-6-3.

The correct combination sequence generator 110 provides logical 0 signals to the inverters associated with the Exclusive-Or gates 100-0, 100-1, . . . 100-9 of the correct digits. The Exclusive-Or gates 100-0, 100-1, . . . 100-9 associated with the correct digits of a digit sequence  $S_n$  or  $S_m$  receive their respective signals from the correct combination number sequence generator 110 on a sequential basis corresponding to the position in the sequence  $S_n$  of  $S_m$  on the respective digits with which the Exclusive-Or gates are associated. Thus, if digit sequence  $S_n$  is being entered into the keyboard 26, the correct combination number sequence generator 110 successively provides logical 0 signals to the inverters associated with digits 5-2-3-9-4-7-6-3, that is, to Exclusive-Or gates 100-5, 100-2, 100-3, 100-9, 100-4, 100-7, 100-6, and 100-3.

To accomplish the foregoing, a key pulsing circuit 115 is provided. This circuit includes two NAND-gates 116 and 117 whose individual inputs are connected to different ones of the outputs of the digit keys 26-0, 26-1, . . . 26-9, and a NOR-gate 118 connected to the outputs of NAND-gates 116 and 117. The key pulsing circuit 115 provides on its output line 119 a logical 0 pulse each time one or more of the digit keys 26-0, 26-1, . . . 26-9 is actuated. Output line 119 is input via an Exclusive-Or gate 120 to a rapid entry prevention circuit 121. Rapid entry prevention circuit 121 limits the processing of signals by the circuit of FIGS. 4A and 4B to a rate corresponding to that which occurs when digits are entered manually via the keyboard 26. This eliminates the possibility that, for example, someone attempting to unlawfully compromise the system would, instead of manually actuating the digit keys 26-0, 26-1, . . . 26-9 a multiplicity of different times in attempting to produce the correct combination sequence by trial and error, would instead connect a computer to the comparator 100 and in a few minutes simulate the entry of a very large number of different digit sequences in an effort to accelerate entry of the correct combination by trial and error methods.

Rapid entry prevention circuit 121 includes a single shot, or monostable multivibrator, circuit 122 responsive to the output of Exclusive-Or gate 120. Single shot 121 switches on the leading edge of the logical 1 signal output from Exclusive-Or gate 120 each time a digit key 26-0, 26-1, . . . 26-9 is actuated. Also included is a one shot circuit 123 which triggers on the trailing edge of a logical 1 output from the Exclusive-Or gate 120 each time a digit key is depressed. The output of one shot 123 is input on line 124 to one shot 122 preventing re-triggering of one shot 122 for the duration of the output pulse provided by one shot 123. A third one shot circuit 125 is responsive to the output of one shot circuit 122 and triggers on the rising edge of the

logical 1 pulse provided by one shot 122. One shot 125 provides complementary positive (1) and negative (0) pulses on lines 126 and 127 for the interval established by one-shot 125. The periods of one shots 122, 123 and 125 are 18, 22, and 7 milliseconds, respectively.

The logical 0 or negative pulse on line 127 from one shot 125 of the rapid entry prevention circuit 121 is input to a binary counter 130. Thus, each time a digit key 26-0, 26-1, . . . 26-9 is actuated an input is provided to binary counter 130 on line 127. Binary counter 130 also is responsive to a signal on line 132 produced as a consequence of momentarily actuating the start  $S_n$  key 28 and a signal on line 133 produced as a consequence of momentarily actuating the start  $S_m$  key 29.

The input on line 132 to the binary counter 130 is produced by applying the output of start  $S_n$  switch 28 to line 127 via a NOR-gate 140 and an inverter 141 which in combination constitute a logical OR-gate. Similarly, the input on line 133 to the binary counter 130 is produced by applying the output of start  $S_m$  switch 29 to line 133 via a NOR circuit 142 and an inverter 143 which collectively constitute a logical OR circuit.

If the start  $S_n$  key 28 has been actuated producing an input to counter 130 on line 132, as the counter is thereafter successively pulsed on line 127 coincident with the successive actuation of the digit keys 26-0, 26-1, . . . 26-9, the counter will provide on its output lines 131, in binary format, signals corresponding to successive counts of 1, 2, 3, 4, 5, 6, 7 and 8. Similarly, if the binary counter 130 is input with a signal on line 133 as a consequence of actuating the start  $S_m$  key 29, when the counter 130 is thereafter successively pulsed on line 127 as a consequence of successive actuation of the digit keys, the counter 130 will provide on its output lines 131 signals in binary format correlated successively to counts of 9, 10, 11, 12, 13, 14, 15 and 16.

The successive outputs on counter output lines 131 corresponding to successive counts of 1, 2, 3, 4, 5, 6, 7, and 8, if the start  $S_n$  key 28 is depressed, or counts of 9, 10, 11, 12, 13, 14, 15 and 16 if the start  $S_m$  key 29 is depressed, are input to a binary-to-hexadecimal converter 137 having sixteen output lines 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, and 16. Output lines 1, 2, 3, 4, 5, 6, 7 and 8, preferably in the form of patch board sockets, correspond to sockets 56D of combination setting unit 56 for setting the digits of combination sequence  $S_n$ , while output sockets 0, 10, 11, 12, 13, 14, 15 and 16 of converter 137 correspond to sockets 58D of patch board 58A of combination setting unit 58 for setting the digits of combination sequence  $S_m$ .

Assuming start  $S_n$  switch 28 has been actuated, as different ones of the digit keys are successively actuated and pulses successively applied to binary counter 130 on line 127, logical 0 pulses will be successively provided to outputs 1, 2, 3, 4, 5, 6, 7 and 8 of the converter 137. Similarly, assuming start  $S_m$  key 29 is actuated, successive actuation of digit keys producing successive negative pulses input to the binary counter 130 on line 127 will produce successive logical 0 signals at terminals 9, 10, 11, 12, 13, 14, 15 and 16 of the converter 137. Depending upon the particular digits of digit sequences  $S_n$  and  $S_m$  established by the jumper cable connections of patch boards 56A and 58A, the logical 0 pulses successively produced at terminals 1, 2, 3, . . . 15, 16 of converter circuit 137 in synchronism with the successive actuation of the digit keys following actua-

tion of start  $S_n$  and  $S_m$  switches 28 and 29 will be input to the Exclusive-Or gates 100-0, 100-1, . . . 100-9 of the comparator 100 in digit sequences corresponding to the digit sequences  $S_n$  and  $S_m$ .

Assuming sequence  $S_n$  is 5-2-3-9-4-7-6-3 and further that start  $S_n$  switch 28 was actuated, successive entry of any eight digits via the digit keys will result in the successive application of logical 0 signals from terminals 1, 2, 3, 4, 5, 6, 7 and 8 of converter 137 to the inverters associated with Exclusive-Or gates 100-5, 100-2, 100-3, 100-9, 100-4, 100-7, 100-6 and 100-3, respectively. Similarly, assuming the digits of sequence  $S_m$  are 2-6-5-4-9-8-6-0, and further that start  $S_m$  switch 29 was actuated, successive entry of any eight digits via the digit keys will result in the successive application of logical 0 pulses from terminals 9, 10, 11, 12, 13, 14, 15 and 16 of the converter 137 to the inverters associated with Exclusive-Or gates 100-2, 100-6, 100-5, 100-4, 100-9, 100-8, 100-6 and 100-0. If the digit keys corresponding to the correct digit of sequences  $S_n$  and  $S_m$  are entered in the correct order following actuation of the start  $S_n$  and start  $S_m$  switches 28 and 29, respectively, the successive application of logical 0 signals from terminals 1, 2, . . . 16 of the converter 137 will, in combination with successive entry of the correct digits in the proper order of sequences  $S_n$  and  $S_m$ , result in production of a sequence of logical 1 signals successive by Exclusive-Or circuits 100-0, 100-1, . . . 100-9 for each sequence  $S_n$  and  $S_m$ .

The incorrect digit detector circuit 112 includes two NAND-gates 146 and 147 which have their different inputs respectively connected to different ones of the outputs of comparator Exclusive-Or gates 100-0, 100-1, . . . 100-9. The outputs of NAND-gates 146 and 147 are input to a NOR-gate 148, the output of which in turn is input to an inverter 149. NAND-gates 146 and 147 in combination with NOR-gate 148 effectively monitor the outputs of all of the Exclusive-Or gates of the comparator 100 to detect entry of an incorrect digit during entry of digit sequences  $S_n$  and  $S_m$ . As it will be recalled, if during the entry of any digit of the sequences  $S_n$  and  $S_m$ , the correct digit key and only the correct digit key is actuated, logical 1 signals will be output from all of the comparator Exclusive-or, circuits 100-0, 100-1, . . . 100-9. If during entry of a digit of sequences  $S_n$  and  $S_m$  a digit key corresponding to an incorrect digit is actuated and/or the digit key corresponding to the correct digit key is not actuated, all outputs of the comparator Exclusive-Or circuits 100-0, 100-1, . . . 100-9 will not be at a logical 1 level and the output of NOR-gate 148 will be at a logical 0 level reflecting the fact that an incorrect key was actuated and/or that the correct key was not actuated.

If a logical 0 is output from NOR-gate 148 at any time during the entry of digit sequence  $S_n$  or digit sequence  $S_m$ , an incorrect number latch 150 will be set providing a logical 1 signal level on latch output line 152. For example, if a logical 0 is output from NOR-gate 148 corresponding to either actuation of an incorrect key or failure to actuate the correct key, a logical 1 will be input to the wrong number latch from the inverter 148 coincident with the presence of a pulse on line 126, which latter pulses enables the latch 150 to be switched in response to the presence of a logical 1 signal input thereto from inverter 149. With the incorrect digit latch 150 set, a logical 1 signal is present on line 152 which in a manner described hereafter is sampled

following entry of the last digit of sequence  $S_n$  and the last digit of sequence  $S_m$  to determine if one or more incorrect digits or failures to enter correct digits occurred during entry of sequences  $S_n$  and  $S_m$ . Incorrect digit latch 150 is reset by a signal on line 154 each time either the start  $S_n$  switch 28 or the start  $S_m$  switch 29 is actuated prior to entry of the digits of sequence  $S_n$  or sequence  $S_m$ . This enables the wrong digit latch 150 to be independently responsive to the entry of an incorrect digit or the failure to enter a correct digit during entry of digit sequence  $S_n$  and entry of the digits of sequence  $S_m$ .

The reset signal on line 154 which, as indicated, resets incorrect digit latch 150 prior to entry of sequence  $S_n$  in response to actuation of start  $S_n$  switch 28 and prior to entry of sequence  $S_m$  in response to actuation of start  $S_m$  switch 29, is produced by a reset circuit 160. Reset circuit 160, in addition to including OR circuit equivalent 140, 141 and OR circuit equivalent 142, 143, also includes a single shot circuit or monostable multivibrator 156 which is responsive to the output of a NAND-gate 157, which functions as a logical OR-gate, which in turn is responsive to the outputs of the start  $S_n$  switch 28 and start  $S_m$  switch 29. Each time either start  $S_n$  switch 28 or start  $S_m$  switch 29 is momentarily actuated prior to entry of the digits of sequences  $S_n$  and  $S_m$ , a signal is input to NAND-gate 157 which in turn triggers one shot 156, providing on output line 154 a negative reset pulse which, among other things, resets wrong digit latch 150. Thus, wrong digit latch 150 is reset prior to entry of the digits of sequence  $S_n$  and again prior to entry of the digits of sequence  $S_m$ .

To determine whether during the entry of digit sequences  $S_n$  and  $S_m$  an incorrect digit was entered or one of the correct digits not entered, a correct sequence circuit 159 is provided. The correct sequence circuit 159 includes a correct  $S_n$  latch 162 and a correct  $S_m$  latch 161. Correct  $S_n$  latch 162 and correct  $S_m$  latch 161 are reset in response to actuation of the start  $S_n$  and  $S_m$  switches, respectively.

Correct  $S_m$  latch 161 is also responsive to the output on line 152 of the incorrect number latch 150 via NOR-gates 165 and 166, and to the output line 131A of the binary counter 130 on which a logical 0 level is present when counter 130 has a count of 16 occurring after entry of the last digit of sequence  $S_m$  and on which a logical 1 signal appears when binary counter 130 has a count of 8 which occurs following entry of the last digit of sequence  $S_n$ . If upon conclusion of entry of the eight digits of sequence  $S_m$ , the wrong number latch 150 has not been set in response to either entry of an incorrect digit or the failure to enter a correct digit, the correct m latch 161 will be switched when the input on line 131A is at a logical 0. Under these conditions, the correct m latch 161 will provide on its output line 163 a logical 0 level indicating that the correct digits and only the correct digits of sequence  $S_m$  were entered and that such were entered in the correct order. This signal on line 163 will illuminate lamp 31 providing a visual indication that sequence  $S_m$  was correctly entered. If, however, during entry of sequence  $S_m$  the wrong number latch 150 is set as a consequence of either actuation of an incorrect digit key or the failure to operate a correct digit key, correct m latch 161 will not be switched following entry of the eighth digit of sequence  $S_m$ , providing a logical 1 signal on output line 163. Lamp 31 will not become illuminated.

Correct  $n$  latch 162 is responsive to the output on line 152 of the wrong number latch 150 via NOR-gate 165 and NOR-gate 169, as well as to the output of counter line 131A via an inverter 170. Assuming wrong number latch 150 has not been set during entry of sequence  $S_n$  by either actuation of an incorrect key or the failure to actuate a correct key, a logical 0 will be input to latch 162 on line 171 and a logical 0 will be input on line 172 upon conclusion of the entry of the eighth digit of sequence  $S_n$  with the result that latch 162 will be switched providing a logical 0 on latch output line 173. The logical 0 output on line 173 illuminates lamp 30 indicating that the sequence  $S_n$  was correctly entered. If, however, during the entry of sequence  $S_n$  either an incorrect key was actuated or a correct key not actuated, a logical 1 signal will be input to the latch 162 from the wrong number latch 150 on line 171, and upon occurrence of the logical 0 signal on line 172 upon entry of the eighth digit of sequence  $S_n$ , correct  $n$  latch 162 will not be switched providing a logical 1 on its output line 173.

Assuming both sequences  $S_n$  and  $S_m$  have been correctly entered, logical 0 level signals will be present on lines 163 and 173. These logical 0 level signals on lines 163 and 173, in addition to illuminating both lamps 30 and 31, are also input to a NOR-gate 175, providing a logical 1 signal on the output line 175a from this gate. Thus, if both sequences  $S_n$  and  $S_m$  have been correctly entered, a logical 1 signal will be output from NOR-gate 175 on line 175a.

NOR-gates 165, 166 and 169 interconnecting the output line 152 of wrong number latch 150 and the correct  $n$  and correct  $m$  latches 162 and 161 prevents these latter two latches from being switched when the wrong number latch is being reset which occurs each time the start  $S_n$  and start  $S_m$  switches 28 and 29 are actuated. Stated differently, NOR-gates 165, 166 and 169 render correct  $n$  and correct  $m$  latches 162 and 161 immune to the resetting of the wrong number latch 150. Additionally, these NOR-gates prevent clearing of the correct  $n$  and correct  $m$  latches 162 and 161 should any key, except the start  $S_n$  key 28 or the start  $S_m$  key 29 be actuated. Stated differently, NOR-gates 165, 166 and 169 cause latches 161 and 162 to remain in states they may be in as a consequence of the fact that sequence  $S_n$  or sequence  $S_m$  was correctly entered, notwithstanding actuation of a key other than the  $S_n$  and  $S_m$  keys 28 and 29.

The digital alarm clock 179 includes a 24-hours clock 180 and a day counter 181 which cooperate to provide a logical 0 level signal on line 182 at a specified time of day present in the clock 180 of a specific day subsequent to setting of the day counter, which day counter setting typically occurs at the end of a business day prior to closure of the vault door. The logical 0 signal on line 182 persists until the day counter 181 is reset to a nonzero count in a manner to be described later. For example, and in a manner also to be described, the 24-hour clock 180 and the day counter 181 can be set to provide a signal starting at 8:00 A.M. on the Monday following the close of business the preceding Friday. Alternatively the 24-hour clock 180 and the day counter 181 can be set to provide a logical 0 signal on output line 182 starting later the same day the day counter is set or starting at some specific time during the next day, 2 days hence, 3 days hence, etc. The logical 0 signal on output line 182 produced starting at the

time of day present in 24-hour clock 180 on the specified day preset in day counter 181, in combination with the logical 1 signal on output line 175a produced when both the correct  $S_n$  (or  $S_n'$ ) and  $S_m$  (or  $S_m'$ ) sequences have been entered, are input to the bolt actuator circuit 200, and function to energize solenoids 44A and 44B and permit opening of the vault door, in a manner to be described.

The 24-hour clock 180 is a conventional commercially available digital alarm clock circuit such as described in Mostek Corporation Product Descriptions Bulletin MK-5017AA/AN, incorporated herein by reference. The 24-hour clock 180 provides on its output lines 180A and 180B signals continuously correlated to the correct time of the day in hours, minutes and seconds, or alternatively the time preset therein, in hours, minutes and seconds, when an alarm tone will be produced on clock output line 184. The signals on clock output lines 180A and 180B are input to a six digit display 52. Each digit of the display 52, of which only one is shown, is of the well-known seven-segment display type. The outputs from the 24-hour clock 180 on lines 180A and 180B are pre-coded such that the seven light-emitting diode segments 52A of each digit display will cooperate to visually display its respective digit. Display 52 includes two digits to represent the 24 possible hours in a day, two digits to represent the sixth possible minutes in each hour, and two digits to represent the 60 seconds in each minute. As noted, only one such seven-segment digit display is shown, the seven-segment displays for the other five digits being identical. Normally, the 24-hour clock display 52 displays the correct time of day. However, if a switch 187, which is normally open, is closed the six-digit display 52 will display the time of day preset in clock 180 when a tone signal on line 184 will be produced.

To set the 24-hour clock 180 to the correct time of day, normally open switches 188 are closed. This advances the time of day setting of the clock 180. By visually observing the advancing time of day on the digital display 52 and selectively opening the switches 188 when the displayed time in hours, minutes and second corresponds to the correct time of day, the 24-hour clock 180 can be set to the correct time of day. Further, the preset time of day when the 24-hour clock 180 provides a tone on line 184 can be set as desired by closing both the switch 187 and the hour, minute and second switches 188. Closure of switch 187 causes the 24-hour clock display 52 to display the time presently preset in the 24-hour clock when the tone would be produced on line 184, while closing of switches 188 enables the preset time setting for production of the tone on line 184 to be advanced. By visually observing the preset tone time setting on display 52 and selectively closing the second, minute and hour switches 188 when the displayed tone time matches that desired, it is possible to set the 24-hour clock such that the tone on line 184 is produced at any desired time of day.

The 24-hour clock 180 preferably includes two counters, namely, a time of day counter and a tone time counter. The time of day counter is responsive to a 60Hz reference signal on input line 189 derived from a conventional a.c. power source and continuously counts 60Hz signals, providing at the output of the time of day counter a signal correlated to the correct time of day. This counter is initially set to the correct time via switches 188 in the manner described. The tone

time counter is responsive to the 60Hz reference signals on line 189 only when it is being set to a specified tone time in response to the joint actuation of switches 187 and 188. Once the tone time counter is set to a specified time of day when a tone signal on line 184 is desired, this counter no longer responds to 60Hz signals. When the continuously varying count in the time of day counter correlated to the correct time of day matches the preset count in the tone time counter correlated to a preset time when a tone is desired, a tone signal on line 184 is produced, indicating that the current time of day matches the preset time of day when the tone is desired. By providing appropriate coding circuitry between the output of the time of day counter and the digital display 52 and between the output of the tone time counter and the digital display 52, the continuously varying count of the time of day counter correlated to the correct time of day can be displayed on the display 52, as well as the preset count of tone time counter correlated to the preset time when the tone is desired, depending upon the position of switch 187.

The 24-hour clock 180, assuming it is set to provide a tone signal on line 184 at a preset time of day, such as 8:00 A.M., will provide a tone signal on line 184 every 24 hours at the preset time, that is, each day at 8:00 A.M. To produce a signal at a specified time of day of a specified day following setting of digital clock 179, such as at 8:00 A.M. Monday following setting of the clock the preceding Friday at the close of business, a day counter 181 is provided. The day counter 181 takes the form of a conventional binary counter, and is connected to the tone signal output line 184 of the 24-hour clock 180 via a normally closed switch contact 190 and a single shot circuit 191. Assuming the switch 190 is in the position shown, each time the logical 1 tone signal is provided on line 184 at the preset time each day, the single shot 191 is triggered to provide a logical 1 signal to the day counter 181. Assuming the time signal on line 182 is desired on the third day following the setting of the clock 179, the day counter 181 would be preset to a count of 3. As each day passes, a tone signal is provided on output line 184 of the 24-hour clock at the second, minute and hour tone time preset into the 24-hour clock. These signals on line 184 occurring at the preset tone time each day are input via the single shot 191 to the day counter 181 decrementing the day counter. When the day counter 181 decrements to a count of 0, the logical 0 signal on line 182 is provided indicating that the time of day is equivalent to the specified tone time preset in the 24-hour clock and further that the specified number of days preset in the day counter 181 have elapsed since the setting of the day counter 181. The logical 0 signal on line 182 remains until day counter 181 is reset to a nonzero count.

For example, if at the close of business on Friday the day counter 181 is preset to a count of 3, a signal will be provided on line 182 starting with receipt of three tone signals from the 24-hour clock on line 184. If the 24-hour clock 180 is for 8:00 A.M., the tone signals on line 184 will be produced at 8:00 A.M. Saturday, 8:00 A.M. Sunday and 8:00 A.M. Monday, each of which will decrement the day counter 181 a single count. When the third tone signal on line 184 is produced at 8:00 A.M. Monday, the day counter 181 will be decremented to 0 at which time a signal will be produced on line 182 indicating that it is 8:00 A.M. Monday. As

noted, this signal on line 182 persists until day counter 181 is reset to a nonzero count. Similarly, if the day counter 181 has been preset to counts of 2 or 1, a signal would be provided on line 182 starting at 8:00 A.M. Sunday or 8:00 A.M. Saturday, respectively.

The output lines 181A of the day counter 181 provide signals in binary format indicating the count presently in the day counter. These signals are input to a decoder 192 which conditions them for controlling a single digit seven-segment light-emitting diode display 193. The count to which the day counter 181 is preset can be increased or decreased to preset it to a different count. If the count currently in the day counter 181 is to be decreased, switch 194 is placed in the position shown and switch 190 is transferred from the position shown. The count now decreases and when the decreasing count in the day counter 181 as displayed by the display 193 reaches that desired, switch 190 is transferred to the position shown. Similarly, if it is desired to increase the count to which the day counter 181 is presently preset, the switch 194 is transferred from the position shown, as is the switch 190. The count now increases and when the increasing count in the day counter 181 as displayed in the display 193 reaches that desired, the switch 190 is transferred to the position shown.

The output of the single shot 191 on line 191A produced each time a tone signal is provided on line 184 from the 24-hour clock 180 is also coupled via a transistor switch 196 to an input line 197 of the 24-hour clock 180, terminating the tone.

In an effort to compromise the system, an unauthorized person may attempt to accelerate the time at which the signal is produced on line 182, for example, from Monday morning at 8:00 A.M. when bank employees are customarily present in the bank to some earlier time during the preceding weekend when the bank employees are not likely to be present. To avoid this, a clock speed-up prevention circuit 199 is employed. The circuit 199 is connected between the 60Hz reference signal line 189 input to the 24-hour clock and a power supply 201 from which the 60Hz reference signal is normally derived, the power supply 201 itself being connected via a suitable plug 202 to a conventional 60Hz source of power. Should the frequency of the signal from the power supply 201 input to the clock speed-up prevention circuit 199 on line 198 exceed 60Hz to any significant extent, the clock speed-up prevention circuit 199 provides on line 199 a continuous logical 1 signal causing the 24-hour clock 180 to switch to an internal 60Hz oscillator for reference purposes.

The circuit 199 is in the form of a single shot having a period slightly less than 1/60 second. Assuming the frequency of the a.c. signal from the power supply 201 input to the clock speed-up prevention circuit 200 on line 198 is approximately 60Hz, the one shot 199 will be triggered to provide logical 1 signal pulses on line 189 to the 24-hour clock 180 at a 60Hz rate. Since the duration of logical 1 pulse output from the one shot is less than 1/60 of a second, the output of the clock speed-up prevention circuit 199 on line 189 will drop to zero at the end of each one-shot pulse, but prior to the next 60Hz triggering signal from the power supply 201. When the output line of the circuit 199 drops to a logical 0, which occurs at a 60Hz rate assuming the a.c. frequency from the power supply 201 input to the circuit 199 is at 60hz, a capacitor 205 which has been

charging through a resistor 206 during the duration of the logical 1 single shot output from the circuit 199, will discharge through diode 207. However, should the frequency input to the 24-hour clock 180 via the circuit 199 be substantially above 60Hz, the output on line 189 of the single shot of circuit 199 remains at a logical 1, preventing capacitor 205 from discharging. As a result of the continued logical 1 level on line 189 to the 24-hour clock 180, this clock switches to an internal 60Hz reference signal source contained within the clock.

FIG. 6 depicts one possible form of circuit, which can be incorporated in 24-hour clock 180, for switching to an internal source of reference signals for advancing the 24-hour clock 180 should an attempt be made to speed up the 24-hour clock by connecting to it an external source of reference signals having a frequency substantially greater than that normally provided by the power supply 201, which typically would be 60Hz. The circuit includes a single shot 320 responsive to the signal input on line 189, a 60Hz free-running oscillator 321 which functions as an internal source of 60Hz signals, and a NAND-gate 322 which is responsive to the output of the single shot 320 on line 323 and the oscillator output on line 324.

As noted previously, if the source of reference pulses input to the clock speed-up prevention circuit 199 on line 273 substantially exceeds the desired reference signal frequency, for example 60Hz, the speed-up prevention circuit 199 provides on its output 189 a logical 1 signal level, the signal on line 189 normally being in the form of 60Hz pulses if the reference signals on line 273 are normal. Assuming that at time  $t_0$  the signal on line 189 switches from pulses to a logical 1 level in response to a change in frequency of the reference signals on line 273 from 60Hz to an excessive frequency, the single shot 320 is triggered at time  $t_0$  providing a logical 0 pulse on single shot output line 323. The pulse output from the single shot 320 on line 323 starts at time  $t_0$  corresponding to the point when the frequency of reference signals on line 189 became excessive and continues in time until time  $t_1$  when the single shot 320 times out. Assuming the single shot 320 still has a logical 1 signal input to it on line 189 due to the fact that the reference signal frequency on line 273 remains excessive, when the output from the single shot on line 323 reverts to a logical 1 level at time  $t_1$ , NAND-gate 322 is enabled, gating the 60Hz signals from free-running internal reference signal oscillator 321 to NAND-gate output line 325. The 60Hz reference signals on line 325 gated from the internal reference signal oscillator 321 continued until such time as the frequency of the reference signals from the external source on line 273 drop to an acceptable level whereupon the signal on line 189 reverts to a logical 0. The 60Hz output on line 325 present when the frequency of timing signals on line 273 is excessive advances the clock 180 in the same manner as the pulses on line 273 do when the frequency of reference signals on line 273 is not excessive.

The bolt actuator circuit 200, which includes solenoids 44A and 44B, is provided to raise the detent 42 and thereby disengage it from the bolt notch 40, allowing the vault door to be opened by turning the handle 23, when both combination sequences  $S_n$  (or  $S_n'$ ) and  $S_m$  (or  $S_m'$ ) have been properly entered at or after the predetermined time preset in the 24-hour clock 180 of

the specified day preset in day counter 181. The bolt actuator 200 is responsive to output line 175A of NOR-gate 175 which, as previously indicated, provides a logical 1 signal when both sequences  $S_n$  (or  $S_n'$ ) and  $S_m$  (or  $S_m'$ ) have been properly entered. The bolt actuator circuit 200 is also responsive to output line 182 of the day counter 181 on which there is a logical 0 signal at or after the specified time of day present in alarm clock 180 of the specified day preset in the day counter 181. The logical 1 level signal input to the bolt actuator circuit 20 on line 175A reflecting the fact that both sequences  $S_n$  (or  $S_n'$ ) and  $S_m$  (or  $S_m'$ ) have been correctly entered is resistor coupled to two parallel-connected transistor switches 203 and 204 in the form of Darlington circuits, each of which is connected in series with a different one of the solenoids 44A and 44B which, when energized, raise the detent 42 to disengage it from the bolt notch 40. The logical 0 signal input to the bolt actuator circuit 200 from the day counter 181 on line 182 produced at and after the time preset in 24-hour clock 180 of the day preset in counter 181, following inversion in a transistor 195, is input to two parallel-connected transistor switches 208 and 209, also Darlington circuits. Transistor switches 208 and 209 are connected in series with different ones of the solenoids 44A and 44B and different ones of the transistor switches 203 and 204 responsive to the signal on line 175A from the correct  $S_n$  (or  $S_n'$ ) and  $S_m$  (or  $S_m'$ ) NOR-gate 175. Assuming the correct sequences  $S_n$  (or  $S_n'$ ) and  $S_m$  (or  $S_m'$ ) have been entered at or after the specified time preset in the 240 hour clock 180 on the specified day preset in the day counter 181, the logical 1 and logical 0 signals input to the bolt actuator circuit 200 on lines 175A and 182, respectively, will switch the Darlington circuit transistor switches 203, 204 and 208, 209 to a conductive state, energizing solenoids 44A and 44B. With these solenoids energized, the bolt detent 42 is raised disengaging the bolt notch 40, allowing the bolt 22 to be moved to its unlock position by rotation of the handle 23 in a manner previously described. While both of the solenoids 44A and 44B will normally be energized in response to logical 0 and logical 1 signals input to the bolt actuator circuit 200 on lines 182 and 175A, respectively, energization of either one of the solenoids 44A and 44B will be sufficient to raise the detent 42 to disengage it from the bolt notch 40. The inclusion of two solenoids 44A and 44B in parallel is merely to provide a factor of safety should one solenoid become defective.

A duress circuit 210 is provided to permit remote signaling to a police station or the like should the bank employees be required, under threat of force, to open the vault. Specifically, the duress circuit 210 permits the vault door 19 to be opened while at the same time an alarm signal sent to a remote police station or the like should both duress sequences  $S_n'$  and  $S_m'$  be entered at or after the time of day preset in the 24-hour clock 180 on the specified day preset in the day counter 181. As it will be recalled, duress sequences  $S_n'$  and  $S_m'$  are identical to the normal sequences  $S_n$  and  $S_m$ , except that the last or eighth digit of each sequence is changed. Specifically, and by way of example only, the duress sequence  $S_n'$  is 5-2-3-9-4-7-6-0 instead of 5-2-3-9-4-7-6-3, while the duress sequence  $S_m'$  is 2-6-5-4-9-8-6-8 instead of 2-6-5-4-9-8-6-0. Obviously, more than one digit could be changed to modify the normal sequence to produce a duress sequence, or al-

ternatively digits could be added to or removed from the normal sequence to produce a duress sequence.

The duress circuit 210 includes a NOR-gate 211 and an inverter 212, the NOR-gate being responsive to the count seven output of the binary-to-decimal converter 137 and the zero digit key 26-0 of the keyboard 26. Should a zero be entered into the keyboard 26 by depressing key 26-0 as the eighth digit of a sequence  $S_n'$  following actuation of the start  $S_n$  key 28, a logical 0 signal will be input to both inputs of the NOR-gate 211 providing at the output 213 of inverter 212 a logical 0 signal. The logical 0 signal on line 213 is input via separate diodes to the inverter associated with the Exclusive-Or gate 100-0 of the depressed digit key 26-0, and the input line of Exclusive-Or gate 100-3 associated with digit key 26-3 which would normally have been actuated as the eighth digit of sequence  $S_n$  had the duress key 26-0 not been actuated. The input to Exclusive-Or gate 100-0 cancels, insofar as the incorrect digit detector circuit 112 is concerned, the fact that duress key 26-0 has been actuated as the eighth digit of the sequence  $S_n'$ . As will be recalled, the eighth digit of the normal sequence  $S_n$  is a 3 in the example herein, and under normal conditions actuation of the 0 digit key 26-0 following depression of start  $S_n$  key 28 as the eighth digit of a sequence instead of the digit key 26-3 will produce a logical 0 output from the Exclusive-Or gate 100-0 which when input to the incorrect digit circuit 112 will result in setting the incorrect number latch 150. By feeding the output of NOR-gate 211 following inversion in inverter 212 to Exclusive-Or gate 100-0, the output of Exclusive-Or gate 100-0 associated with duress key 26-0 will provide a logical 1 output to the incorrect digit detector circuit during entry of the eighth digit of duress sequence  $S_n'$  in much the same fashion as would have occurred had the normally correct eighth digit key 26-3 of sequence  $S_n$  been entered and the duress key 26-0 of sequence  $S_n'$  not actuated.

The inverted output of duress NOR-gate 211 is also input to Exclusive-Or gate 100-3 associated with digit key 26-3 which is the correct eighth digit for the normal sequence  $S_n$ . The input to Exclusive-Or gate 100-3 simulates the actuation during entry of the eighth digit of the duress sequence  $S_n'$  of the correct eighth digit of the normal sequence  $S_n$ . As a consequence, Exclusive-Or gate 100-3 provides a logical 1 at its output as would normally occur were the correct digit, 3 in the example assumed herein, had been entered as the eighth digit of the sequence  $S_n$ . This logical 1 signal from Exclusive-Or gate 100-3 is input to the incorrect digit detector circuit 112 preventing the wrong number latch 150 from being set even though the correct digit key 26-3 associated with normal sequence  $S_n$  had not been actuated. Thus, duress NOR-gate 211 and associated inverter 212, insofar as concerns the incorrect digit detector circuit 112, simulates actuation of the correct digit key of the normal sequence  $S_n$  and overrides the actuation of the duress key 26-0 which, while correct for the duress sequence  $S_n'$ , is incorrect for the normal sequence  $S_n$ .

A NOR-gate 214 and inverter 215 function in a similar manner with respect to the duress sequence  $S_m'$  as NOR-gate 211 and inverter 212 function with respect to the duress sequence  $S_n'$ . NOR-gate 214 is responsive to the count 15 terminal of the binary-to-decimal converter 137 and to the duress key 26-8 associated with the last digit of duress sequence  $S_m'$  to provide on in-

verter output line 216 a logical 0 signal when the duress digit 8 is actuated as the eighth digit of the duress sequence  $S_m'$  instead of the normal digit 0 constituting the last digit of the normal sequence  $S_m$ . The output line 216 of inverter 215 is input to Exclusive-Or gate 100-8 associated with the duress key 26-8 to effectively override, insofar as incorrect digit detector circuit 112 is concerned, the fact that the digit key 8 was actuated as the eighth digit of the sequence  $S_m'$ , preventing latch 150 from being set. The output of inverter 215 on line 216 is also input to Exclusive-Or gate 100-0 to effectively simulate the actuation of digit key 26-0 which corresponds to the last digit of the normal sequence  $S_m$ , thereby preventing the incorrect digit detector circuit 112 from setting latch 150 as a consequence of the actuation of duress key 26-8 rather than digit key 26-0 as the last digit of the sequence  $S_m$ .

The outputs 211A, 214A of the duress NOR-gates 211 and 214 are input to a NOR-gate 220, the output of which is input to a latch 221. Should either the duress key 26-0 be entered as the last digit of the duress sequence  $S_n'$  or the duress digit 26-8 be entered as the last digit of the duress sequence  $S_m'$ , a logical 0 output is provided from NOR-gate 220 to latch 221 setting this latch. Setting of latch 221 in turn provides a logical 1 signal on latch output line 70. The duress signal on line 70 is input, via contact 63 which is in the position shown when the bolt 22 is in the lock position, to a remote station, such as the police, connected to line 71. Thus, when at least the last of two sequences entered is a duress sequence, either  $S_n'$  or  $S_m'$ , and such sequences are entered at or after the specified time preset in the 24-hour clock 180 during the specified day preset in the day counter 181, not only are the bolt solenoids 44A and 44B energized to permit the bolt to be moved to its unlock position, but a signal is provided to a remote station, such as the police, to reflect the fact that the vault door is being opened under duress conditions.

To reset the various latch circuits such as the correct  $n$  latch 162, correct  $m$  latch 161, incorrect digit detector latch 150, and duress latch 221 a start power reset circuit 185 is included. The circuit 185 includes a transistor switch 186, the base of which is coupled via a resistor 217 and a capacitor 218 to a source of positive potential 219, which potential source 219 is included in power supply 201 to be described and is energized only when the power supply 201 is in an ON condition by reason of switch 183 being closed-circuited. The emitter of transistor 216 is coupled to the output of the start  $S_n$  switch 28 and the output of the start  $S_m$  switch 29. When power supply 201 is turned ON by closure of a power ON switch 183 to be described, the power supply 219 is energized providing bias to the base of transistor 216 to place this transistor in a conductive state. Conduction of transistor 216 brings the emitter thereof to ground potential with the result that a logical 0 or lower level signal is applied to the output of start  $S_n$  switch 28 and start  $S_m$  switch 29. These signals in turn reset correct  $n$  latch 162 and correct  $m$  latch 161 and via the reset circuit 160 resets the wrong number 150 and the duress latch 221. Following charging of the capacitor 218, transistor 216 is switched to a nonconductive state terminating the reset signals applied from the emitter of transistor 216 to the output line of start  $S_n$  switch 28 and start  $S_m$  switch 29.

The start power reset circuit 185 is also responsive to a bolt retraction reset circuit 167. When the bolt 22 is switched from its lock position to its unlock position, movable contact 68 switches from the position shown in which capacitor 72 is charging from a source of positive potential 73 to a position in which contacts 65 and 66 are electrically connected. This enables the charged capacitor 72 to discharge through a resistor 222 via line 74. This causes the transistor 186 to be temporarily switched to a conductive state. Conduction of transistor 186 resets the correct *n* latch 162, correct *m* latch 16, duress latch 221, and the wrong number latch 150 in the same manner described in connection with the initial energization of power supply 201 by the closure of normally open switch 183. When the capacitor 72 has fully discharged, transistor switch 186 is again rendered non-conductive to terminate the reset function. Thus, by virtue of the bolt retraction reset circuit 167 which, via circuit 185 and reset circuit 160, resets the latches 150, 221, 161 and 162 when the bolt is placed in its unlock or open condition, the control circuit is automatically reset each time the vault door is opened, requiring, once the door has been closed, and before it can be again opened, that the sequences  $S_n$  (or  $S_n'$ ) and  $S_m$  (or  $S_m'$ ) be entered at or after the specified time preset in the 24-hour clock 180 of the specified day preset in the day counter 181.

To facilitate energization of one or both of the solenoids 56F and 58F to permit access to the patch board 56A and 58A of the combination setting units 56 and 58, a combination setting access circuit 230 is provided. As it will be recalled, access to one or the other or both of the combination setting units 56 and 58 is possible by entering one or the other or both of the duress sequences  $S_n'$  and/or  $S_m'$  following (a) entry of both normal sequences  $S_n$  and  $S_m$  at or after the specified time preset into the 24-hour clock 180 during the specified day counter 181 and (b) retraction of bolt 22. Access to combination change units 56 and/or 58 can also be obtained if, before retracting bolt 22 and opening the door, the duress sequences  $S_n'$  and  $S_m'$  are entered instead of the normal sequences  $S_n$  and  $S_m$ .

When both sequence  $S_n$  (or  $S_n'$ ) and sequence  $S_m$  (or  $S_m'$ ) are entered and the bolt 22 placed in its retracted position to permit access to the rear of door 19, movable contact 63 is transferred from the position shown such that it electrically connects stationary contacts 60 and 61. When one or the other of the duress sequences  $S_n'$  or  $S_m'$ , or both, are entered following retraction of the bolt 22 to the open position and transfer of the contact 63 from the position shown, the duress signal on line 70 provided by the duress latch 221, which has been set in the manner previously described as a consequence of entry of one or the other or both of the duress sequences  $S_n'$  or  $S_m'$ , is applied to line 75. The duress signal on line 75 switches a normally nonconductive Darlington transistor switch 177 to its conductive state, applying a logical 0 level signal to line 223. The logical 0 signal on line 223 is effective to ground the emitters of transistor switches 224 and 225 which are normally nonconducting. If the correct duress sequence  $S_n'$  is entered, the logical 0 level output on line 173 from the correct *n* latch 162 is input to the base of a transistor switch 226 placing this normally nonconducting switch in a conductive state. Similarly, if the correct duress sequence  $S_m'$  is entered, the logical 0 level signal output on line 163 from the correct *m* latch

161 is input to the base of a normally nonconducting switch 227 rendering this transistor conductive. With the emitters of transistors 225 and 224 at ground potential as a consequence of line 223 being grounded due to application of the duress signal on line 70 via the bolt-controlled, transferred contact 63, a logical 0 signal input to transistor 226 switches transistor 225 to a conductive state energizing solenoid 56F permitting access to combination changing unit 56, while a logical 0 input to the base of transistor 227 reflecting correct entry of the duress sequence  $S_m'$  switches transistor switch 224 to a conductive state energizing solenoid 58F to permit access to the combination changing unit 58. If logical 0 signals are simultaneously input to transistor 226 and 227 indicating that both the correct duress sequence  $S_n'$  and correct duress sequence  $S_m'$  have been entered following retraction of bolt 22, both solenoids 56F and 58F will be energized to permit access to both combination setting units 56 and 58.

The power supply 201 includes an input plug 220 which is normally connected to a conventional 11-volt/60Hz power source. The switch 183 permits the available power input at plug 202 to be applied to the circuit 201 as desired. A transformer 270 and full wave rectifier 271 provide on line 272 24-volt full-wave rectified d.c. power which is used to energize various of the solenoids 44A, 44B, 56F and 58F. One side of the transformer secondary winding is connected via line 273 and a clipping circuit 274 to the input of the clock speed-up prevention circuit 199 to provide a 60Hz reference signal to the 24-hour clock 180 in a manner previously described. The center tap terminal of the transformer secondary winding is at approximately 12 volts for application of energizing potential to the 24-hour clock display 52 via line 270A. Additionally, the center tapped potential of the secondary winding of transformer 270 is applied to a regulator circuit 275 which at its output 276 provides a regulated 5-volt d.c. potential for energizing the day counter 181. The center tapped potential of secondary winding of transformer 270 is also applied to a 12-volt d.c. regulator circuit 280 for providing regulated 12-volt power to the 24-hour clock 180.

The center tapped voltage output from secondary winding of transformer 270 is further input via a charging resistor 277 to a stand-by battery 278.

Normally, the 24-hour clock 180 and the day counter 181 are energized from regulated supplies 275 and 280 of appropriate potentials present on lines 276 and 280A which derive their power from an external supply via plug 202. Should, however, the external supply to which plug 202 is connected fail, the day counter 181 and the 24-hour clock 180 will be energized by the stand-by battery 278.

The remaining logic circuit components of the control circuit of FIGS. 4A and 4B are normally energized from a suitably regulated 5-volt d.c. supply 282A taken at line 282 which in turn is derived from power from an external source via plug 202. Should the external source to which plug 202 is connected fail, these remaining logic circuit components will be de-energized. Further, should the external power supply to which plug 202 is connected fail, the various solenoids 44A, 44B, 56F, 58F, which are normally energized via the full-wave rectifier 271 output on line 272, will become de-energized. Additionally, the 24-hour clock display 52 normally energized from the center tap of the second

dary winding of transformer 270 will cease to be energized if the external source to which plug 202 is connected fails. Thus, all circuit components, with the exception of the clock 180 and day counter 181 energized from lines 280A and 276 by a stand-by battery 278, will cease to be energized as a consequence of a failure of power at plug 202.

As noted, should the power supply to which plug 202 is connected fail, the 24-hour clock 180 and the day counter 181 will continue to be advanced by the stand-by battery 278. However, all remaining logic circuitry as well as the solenoids will be without electrical power. To enable these unpowered circuit components and solenoids to be powered from outside of the vault to facilitate opening of the vault at the predetermined hour preset in the 24-hour clock 180 on the predetermined day preset in the day counter 181, the 24-volt line 272 and the center tap 270A of the secondary winding of transformer 270 are connected to sockets 285 and 286 which are accessible from the exterior of the vault as, for example, by flush-mounting the sockets in the exterior surface of the vault 10. With sockets 285 and 286 accessible from the exterior of the vault 10, an auxiliary power supply (not shown) could be connected thereto to provide power to lines 270A and 272 from the exterior of the vault, thereby enabling the vault door to be opened upon proper entry of sequences  $S_n$  (or  $S_n'$ ) and  $S_m$  (or  $S_m'$ ) when the 24-hour clock 180 and day counter 181 are advanced to their respective preset time and day settings under the power provided by stand-by source 278, notwithstanding a failure of the external supply connected to the plug 202.

Should a person inadvertently become locked in the vault, a normally open switch 288 connected between the base of transistor 195 and ground potential is provided, which is accessible from the interior of the vault. Closure of switch 288 applies a logical 0 level signal to input line 182 of the bolt actuator circuit 200 to simulate the condition produced when both the 24-hour clock 180 has arrived at the predetermined time preset therein and the day counter has arrived at the predetermined day preset in it. With a logical 0 signal present on line 182 as a consequence of closure of normally open switch 288 by the person locked in the vault 10, to unlock the vault door by energization of the solenoids 44A and 44B it is only necessary to enter the correct combinations  $S_n$  (or  $S_n'$ ) and  $S_m$  (or  $S_m'$ ) using the keyboard 26. Thus, if a person is inadvertently locked in the vault, the vault door can be opened, assuming switch 288 is closed, by proper entry of the combination sequences  $S_n$  (or  $S_n'$ ) and  $S_m$  (or  $S_m'$ ) in keyboard 26 without waiting until the 24-hour clock 180 and day counter 181 arrive at the time of day and day settings preset therein.

In lieu of providing ten separate digit keys 26-0, 26-1, . . . 26-9 for each of the ten digits 0, 1, . . . 9, the single digit key keyboard shown in FIG. 3 and the circuit depicted in FIG. 5 may be provided. This keyboard and circuit includes a single digit display 300 which at any given time displays a single one of the digits 0, 1, . . . 9. The particular digit being displayed in display 300 can be changed at will by actuation of an advance digit switch 301. Entry into the system of the digit displayed in the display 300 is accomplished by momentary actuation of an enter digit switch 302. To enter the multiple digits of a sequence  $S_n$ ,  $S_n'$ ,  $S_m$ , or  $S_m'$ , the advance switch 301 is successively utilized to successively cause

the single digit display 300 to display the successive digits of the particular digit sequence being entered. When the display 300 contains a digit it is desired to enter, the digit enter switch 302 is actuated. For example, if the normal sequence  $S_n$  consisting of digits 5-2-3-9-4-7-6-3 is to be entered, the advance switch 301 is actuated to cause the numeral 5 to be displayed by display 300 whereupon the enter digit switch 302 is actuated to enter this digit. Thereafter, the advance switch 301 is operated to display numeral 2 in the display 300 following which the enter digit switch 302 is actuated to enter the second digit 2 of the sequence. This procedure is repeated until all eight digits of a sequence have been displayed in the display 300 and the displayed digits entered by the enter digit switch 302.

The circuit of FIG. 5 affords a greater degree of security for entering the digits of the combination sequences  $S_n$ ,  $S_n'$ ,  $S_m$  and  $S_m'$  than the multi-digit keyboard 26. Specifically, with the keyboard 26, an observer attempting to learn the digits of the combination sequences can, by observing the location of the switches being successively actuated, determine the identity of the digits of the sequence. Whereas, with the circuit of FIG. 5, entry of a digit is accomplished by actuating the same switch, namely, digit switch 302 while observing a display 300 visible only to the person entering the number, which display is controlled by the advance switch 301. Hence, it is not possible to determine the digits being entered by noting the position of the operator's finger as he successively actuates different ones of the digit switches 26.

The circuit of FIG. 5 includes a binary counter 305 which is connected to a source of low frequency pulses 306, e.g., 2Hz, via a line 307. The pulse source 304 may be any free-running multivibrator having a relatively low frequency. The counter 305 is also responsive to the normally open advance switch 301. When the advance switch 301 is closed, that is, transferred from the normally open position shown, the 2Hz clock pulses continuously present on line 307 are entered into the counter 305 causing the counter to repeatedly cycle through counts of 0, 1, . . . 9, the counting and recycling continuing so long as the switch 301 is closed. The output of the binary counter 305 on lines 306 at any given time reflects the counts then stored in the counter 305.

The output of the counter 305 on line 306 is input to the digit display 300 which preferably takes the form of a conventional seven-segment LED display 310 via a coding unit 311 which converts the binary signals on line 306 indicative of the count in counter 305 into a form suitable for illuminating the seven light-emitting diode segments of the display 310. Thus, the count in counter 305 at any given time is displayed by the display circuit 300, and as the counter 305 cycles in response to the 2Hz signals input thereto on line 307 when the advance switch 301 is closed, the display 300 will change to reflect the changing count in the counter 305.

By observing the digit displayed in the display 300, it is possible, by actuating the switch 301, to arrest the counter 305 at a count corresponding to a particular digit it is desired to enter into the system. For example, if it is desired to enter a 5 into the system, the advance switch 301 is closed to cycle the counter 305. When the counter 305 contains a count of 5 as indicated visually by the display 300, the switch 301 is actuated, termi-

nating further advance of the counter 305, in which event the counter 305 remains at a count of 5. The enter digit switch 302 is then actuated to cause the output of the counter 305, which is in binary format on lines 306, to be read out and converted to decimal by a binary-to-decimal converter 315 to energize a particular one of the ten decimal outputs 0, 1, 2, . . . 9 of the converter 315.

If it is now desired to enter the digit 8, the advance switch 301 is closed until the count of the counter 305 as displayed by the display 300 has advanced to a count of 8 under the action of the 2Hz clock pulses provided by oscillator 306. When this has occurred, the switch 301 is returned to its open condition, freezing the count in the counter 305 at a count of 8. The enter digit switch 302 is now closed to convert the counter output on line 306, which is in the binary format, to a decimal output from the binary-to-decimal converter 315 which in this case results in energization of the output line 8 thereof. This process is repeated until all digits of the sequence being entered have been displayed in the display 300 and entered via momentary closure of the enter digit switch 302. The ten output lines 0, 1, 2, . . . 9 of the binary-to-decimal converter 315 correspond to the digits 0, 1, 2, . . . 9 and when the circuit of FIG. 5 is used instead of the keyboard 26, these outputs 0, 1, 2, . . . 9 of the binary-to-decimal converter 315 are connected to the input terminal of comparator Exclusive-Or gates 100-0, 100-1, 100-2, . . . 100-9 which, when the keyboard 26 is used, are connected to the output of the digit keys 26-0, 26-1, . . . 26-9.

The start  $S_n$  and start  $S_m$  keys and correct  $S_n$  and correct  $S_m$  lamps in FIG. 3 operate in the same manner as their counterparts in FIG. 1A.

While the invention has been described in accordance with a preferred embodiment in which two multi-digit combination sequences must be entered to facilitate operation of the vault bolt, those skilled in the art will realize that certain of the principles of the invention can be utilized to construct a system requiring the entry of more or less combination sequences with a corresponding increase or decrease, respectively, in the security provided. For example, certain of the principles of this invention could be utilized to construct a system requiring the entry of three separate multi-digit sequences, in which case an additional start key, decoder, plug board, and "correct latch" would be utilized. Alternatively, a system could be constructed utilizing certain of the principles of this invention in which only a single combination sequence would be required to permit access to the vault in which event certain elements of the existing circuit of FIGS. 4A and 4B could be eliminated such as one of the correct  $S_m$  or correct  $S_n$  latches, one of the start keys, one of the plug boards, and a portion of the decoder.

Having described the invention, it is claimed:

1. An electronic time and combination lock system for permitting access to persons correctly entering the digits of a predetermined multi-digit combination at a predetermined time of day of a specific day, comprising:

digit entry means for entering multiple digits when access is desired, said digit entry means generating electrical signals correlated to the digits entered, validation means responsive to the electrical signals generated by said digit entry means for determining if the entered digits correctly correspond to pre-

terminated multi-digit combination and generating a first electrical control signal upon correct correspondence,

an alarm clock presettable to a predetermined future time of day of a specific day to provide a second electrical control signal when said predetermined future time of day of said specific day arrives, said present future time being independent of said digits of said combination, and

means responsive to the coincidence of said first and second electrical control signals for generating an electrical signal permitting access.

2. The system of claim 1 wherein said digit entry means is operative to enter multiple digits on a sequential basis, and wherein said validation means determines if the entered digits correctly correspond to the digits of said predetermined multi-digit combination and were entered in a predetermined sequence, said first electrical control signal being produced if said entered digits both correctly correspond to said predetermined combination and are entered in said predetermined sequence.

3. The system of claim 2 wherein said digit entry means includes:

- display means for displaying at a given time only a selected one of a multiplicity of different digits, said display means being sequentially operable to sequentially display different selected digits,
- digit signal generating means for generating electrical signals correlated to the digit displayed by said display means, and
- actuator means actuatable by a person entering a digit into said system to cause digit signals correlated to the displayed digit to be output from said digit entry means.

4. The system of claim 1 wherein said alarm clock is advanced to successively later times at a rate dependent upon the frequency of reference timing signals input thereto,

said system further comprising:

an external source of reference timing signals of predetermined frequency connectable to said alarm clock to advance said alarm clock at a specified rate,

an internal source of reference timing signals of said predetermined frequency connected to said alarm clock to advance said alarm clock at said specified rate, and

frequency responsive circuit means associated with said alarm clock and responsive to said external source for advancing said alarm clock under control of said internal source should the frequency of signals input to alarm clock substantially exceed said predetermined frequency, whereby advancement of said alarm clock at a rate substantially exceeding said specified rate is prevented.

5. The system of claim 1 wherein said alarm clock includes:

a 24-hour clock presettable to provide a time signal each day at a predetermined time of day, and

a day counter responsive to said 24-hour clock and presettable to provide said second electrical control signal at said predetermined future time of day of said specific day correlated to the setting of said day counter,

whereby said predetermined future time of day and specific day can be separately preset in said alarm clock.

6. The system of claim 5 wherein said day counter is decremented each day in response to each said time signal output from said 24-hour clock to produce said second control signal coincident with receipt of the timing signal which decrements said day counter to a count of zero, whereby subsequent time signals input to said day counter is ineffective, without resetting said day counter to a count exceeding zero, to produce subsequent second control signals coincident with the subsequent production of time signals by said 24-hour clock.

7. The system of claim 1 further including circuit means cooperating with at least one of said digit entry means and validation means for preventing digit entry and determination of correct correspondence thereof at a rate substantially in excess of that at which digits can be entered manually.

8. The system of claim 7 wherein said circuit means is connected to said digit entry means for disabling said digit entry means for a specified interval following entry of each digit to prevent digit entry at a rate substantially in excess of that at which digits can be entered manually.

9. The system of claim 1 further including: storage means responsive to said validation means for storing said first electrical control signal, said coincidence means being responsive to the coincidence of said stored first electrical control signal and said second electrical control signal for generating an electrical signal permitting access, and reset means for resetting said storage means to clear said stored first electrical signal as an incident to access, whereby the correct digits must again be entered and the resultant first electrical control signal again stored before access can again be permitted.

10. The system of claim 9 further including: a physically movable lock member positionable between lock and unlock positions and controlled by said access signal for permitting movement from said lock position to said unlock position to facilitate access, switch means responsive to movement of said lock member toward said unlock position for controlling said reset means for clearing said storage means upon movement of said lock member toward said unlock position as an incident to access, and means associated with said lock member for automatically locking said lock member in said lock position to prevent access when said lock member is moved to said lock position following clearing of said storage means as an incident to previous movement of said lock member toward said unlock position.

11. The system of claim 1 further including: a vault having a door controlled by said access signal for permitting access to the interior of said vault from outside thereof upon generation of said access signal, said digit entry means including means operable from outside vault for entering said digits, and manually actuable means operable from within said vault interior to simulate, in response to actuation

thereof from within said vault, said second electrical control signal whereby said access signal can be generated at times other than said predetermined future time of day of said specific day upon entry of said predetermined multi-digit combination.

12. The system of claim 1 further including: a vault having a door controlled by said access signal for permitting access to the interior of said vault from outside thereof upon generation of said access signal,

a main power supply connected to normally energize said digit entry means, said validation means, said timing means and said access signal generating means,

a stand-by power supply connected to energize only said timing means upon failure of said main power supply, whereby said timer is advanced at a normal rate to provide said second electrical control signal when said predetermined future time of day of said specific day time arrives notwithstanding failure of said main power supply, and

electrical connector means accessible from outside said vault and connected to said digit entry means, said validation means and said access signal generating means for enabling an auxiliary power supply to be connected to power said digit entry means, said validation means and said access signal generating means upon failure of said main power supply, whereby said access control signal can be generated upon proper entry of said predetermined digit combination at said predetermined future time of day of said specific day notwithstanding prior failure of said main power supply.

13. An electronic combination lock system for permitting access to persons correctly entering a predetermined multi-digit combination, comprising:

a vault having a door for permitting access to the interior of said vault from outside thereof,

digit entry means located outside said vault for entering multiple digits when access is desired, said digit entry means generating electrical signals correlated to the digits entered,

first validation means responsive to the electrical signals generated by said data entry means for determining if the digits entered correspond correctly to said predetermined multi-digit combination and generating a first electrical control signal upon correct correspondence,

door control means responsive to said first electrical control signals for permitting access to the interior of said vault via said door,

means located within said vault interior for changing said combination,

protective means normally denying access to said combination changing means,

second validation means responsive to electrical signals generated by said data entry means for determining if digits entered correspond correctly to a second predetermined multi-digit combination and generating a second control signal upon correct correspondence,

means for generating a third control signal as an incident to accessing said vault interior through said door following generation of first control signal, and

means responsive to said second and third control signals for generating a fourth control signal for op-

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erating said protective means to permit access to said combination changing means, whereby said combination can be changed from within said vault only upon entry of said first combination followed by initiating access through said door, and thereafter entry of said second combination.

14. An electronic combination lock system for permitting access to persons correctly entering, in predetermined order, the digits of a first predetermined multi-digit combination sequence and the digits of a second predetermined multi-digit combination sequence, said system comprising:

digit entry means for entering multiple digits when access is desired, said digit entry means generating electrical signals correlated to the digits entered, validation means responsive to the electrical signals generated by said digit entry means for separately determining

- a. correct correspondence between the digits entered and said first multi-digit sequence and producing a first control signal upon correct correspondence thereof, and
- b. correct correspondence between the digits entered and said second multi-digit sequence and producing a second control signal upon correct correspondence thereof,

storage means for storing at least the first to occur of said first and second control signals, said storage means retaining storage of said first-occurring control signal associated with correct entry of one of said first and second multi-digit combination sequences notwithstanding subsequent incorrect entry of the other of said first and second multi-digit combination sequences, and

means jointly responsive to said storage means and to said validation means for providing an access signal to allow access upon correct entry, in any order, of said first and second combination sequences.

15. The system of claim 14 further including means

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responsive to the electrical signals generated by said digit entry means for detecting incorrect correspondence between digits entered and said first and second digit sequences and producing an incorrect digit signal as a consequence of detection of an incorrectly entered digit, and wherein said storage means retains storage of said first-occurring control signal notwithstanding subsequent production of an incorrect digit signal upon subsequent incorrect entry of the other of said first and second digit sequences.

16. The system of claim 15 further comprising:

manually operable means to alternatively generate a first start signal and a second start signal on a selective basis,

said validation means being responsive to said first and second start signals to determine correct correspondence between said entered digits and said first and second digit combination sequences, respectively, whereby said first and second combination sequences can be entered and correct correspondence thereof determined in the order in which said first and second start signals are manually generated.

17. The system of claim 13 further comprising:

alarm means responsive to said second validation means for transmitting an alarm to a remote station upon correct entry of said second predetermined sequence and generation of said second control signal prior to accessing said vault, said alarm means being ineffective to transmit said alarm if said second control signal is generated subsequent to accessing said vault, said door control means also being responsive to said second validation means for permitting access to the interior of said vault via said door, whereby entry of said second predetermined combination is susceptible of controlling multiple functions including vault access, alarm transmission and combination changing.

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