



- (51) International Patent Classification:
G02F 1/1343 (2006.01) *G02F 1/1362* (2006.01)
- (21) International Application Number:
PCT/CN2015/097023
- (22) International Filing Date:
10 December 2015 (10.12.2015)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
201510333832.X 16 June 2015 (16.06.2015) CN
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(81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

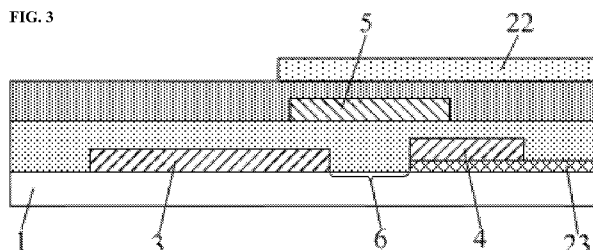
(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: ARRAY SUBSTRATE, DISPLAY PANEL AND DISPLAY DEVICE HAVING THE SAME, AND METHOD THERE-OF

FIG. 3



(57) Abstract: An array substrate (8), comprises a base substrate (1), a row of a plurality of pixel units (2), and a first gate line (3) and a first common electrode line (4) adjacent to the row of the plurality of pixel units (2) and on a first side thereof in plan view of the array substrate (8). The first gate line (3) and the first common electrode line (4) are spaced apart by a gap (6); and a light shield (5) at least partially covers the gap (6) for reducing light leakage from the gap (6).



ARRAY SUBSTRATE, DISPLAY PANEL AND DISPLAY DEVICE HAVING THE SAME, AND METHOD THEREOF

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to Chinese Patent Application No. 201510333832.X, filed June 16, 2015, the contents of which are incorporated by reference in the entirety.

FIELD

[0002] The present invention relates to display technology, more particularly, to an array substrate, a display panel and a display device having the same, and a manufacturing method thereof.

BACKGROUND

[0003] Liquid crystal display panel has found a wide variety of applications. Typically, a liquid crystal display panel includes a color filter substrate and an array substrate facing each other. Thin film transistors, gate lines, data lines, pixel electrodes, common electrodes, and common electrode lines are disposed on the array substrate and color filter substrate. Between the two substrates, a liquid crystal material is injected to form a liquid crystal layer. One common problem associated with the liquid crystal display panel is light leakage. To prevent light leakage, a black matrix is placed on the color filter substrate. A liquid crystal display panel having a larger black matrix can better prevent light leakage. However, an aperture ratio of the liquid crystal display device is reduced by using a black matrix with a larger area.

SUMMARY

[0004] In one aspect, the present invention provides an array substrate, comprising a base substrate; a row of a plurality of pixel units; and a first gate line and a first common electrode line adjacent to the row of the plurality of pixel units and on a first side of the row of the plurality of pixel units in plan view of the array substrate. The first gate line and the first common electrode line are spaced apart by a gap. The array substrate further comprises a light shield at least partially covering the gap for reducing light leakage from the gap.

[0005] Optionally, the light shield is above the gap.

[0006] Optionally, the light shield is below the gap.

[0007] Optionally, the light shield has a width which is substantially equal to a width of the gap and less than a total width of the gap, the first gate line and the first common electrode line.

[0008] Optionally, the array substrate further comprises a first layer comprising the first gate line and the first common electrode line and a second layer comprising the light shield.

[0009] Optionally, each of the plurality of pixel units comprises a thin film transistor comprising a gate electrode, an active layer, a source electrode, and a drain electrode; the first layer further comprising the gate electrode connected to the first gate line; the second layer comprising the light shield, the source electrode and the drain electrode.

[0010] Optionally, each of the plurality of pixel units comprises a pixel electrode above the light shield, the pixel electrode substantially completely covers the light shield in plan view of the array substrate.

[0011] Optionally, each of the plurality of pixel unit comprises a common electrode below the first gate line and the first common electrode line, and connected to the first common electrode line.

[0012] Optionally, each of the plurality of pixel units comprises a pixel electrode on top of a common electrode, the common electrode is above the light shield, the common electrode substantially completely covers the light shield in plan view of the array substrate.

[0013] Optionally, each of the plurality of pixel units comprises a common electrode on top of a pixel electrode, the pixel electrode is above the light shield, the pixel electrode substantially completely covers the light shield in plan view of the array substrate.

[0014] In another aspect, the present invention also provides a display panel comprising an array substrate described herein.

[0015] In another aspect, the present invention also provides a display device comprising a display panel described herein.

[0016] In another aspect, the present invention further provides a method of manufacturing an array substrate comprising forming a row of a plurality of pixel units on a base substrate; forming a first gate line and a first common electrode lines adjacent to the row of the plurality of pixel units and on a first side of the row of the plurality of pixel units in plan view of the base substrate, wherein the first gate line and the first common electrode line are spaced apart

by a gap; and forming a light shield, wherein the light shield at least partially covers the gap for reducing light leakage from the gap.

[0017] Optionally, the light shield is above the gap.

[0018] Optionally, the light shield is below the gap.

[0019] Optionally, the gate line and the common electrode line are made of a same material and formed in a first patterning process in a first layer, and the light shield is formed in a second patterning process in a second layer.

[0020] Optionally, the step of forming the row of the plurality of pixel units comprises forming a thin film transistor, comprising forming a gate electrode; forming an active layer; and forming a source electrode and a drain electrode. The gate electrode, the gate line, and the common electrode line are made of a same material and formed in the first patterning process; the light shield, the source electrode and the drain electrode are formed in the second patterning process.

[0021] Optionally, the step of forming the row of the plurality of pixel units further comprises forming a pixel electrode, the pixel electrode is above the light shield, the pixel electrodes substantially completely covers the light shield in plan view of the array substrate.

[0022] Optionally, the step of forming an array of a plurality of pixel units further comprises forming a pixel electrode and a common electrode. The common electrodes is on top of the pixel electrode, the pixel electrode is above the light shield, the pixel electrode substantially completely covers the light shield in plan view of the array substrate.

[0023] Optionally, the step of forming an array of a plurality of pixel units further comprises forming a pixel electrode and a common electrode. The pixel electrode is on top of the common electrode, the common electrode is above the light shield, the common electrode substantially completely covers the light shield in plan view of the array substrate.

BRIEF DESCRIPTION OF THE FIGURES

[0024] The following drawings are merely examples for illustrative purposes according to various disclosed embodiments and are not intended to limit the scope of the present invention.

[0025] FIG. 1 is a cross-sectional view of a conventional liquid crystal display panel.

[0026] FIG. 2 is a diagram illustrating the structure of an array substrate in plan view in an embodiment.

[0027] FIG. 3 is a cross-sectional view of the array substrate taken along section line A-A of FIG. 2.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0028] The disclosure will now describe more specifically with reference to the following embodiments. It is to be noted that the following descriptions of some embodiments are presented herein for purpose of illustration and description only. It is not intended to be exhaustive or to be limited to the precise form disclosed.

[0029] FIG. 1 is a cross-sectional view of a conventional liquid crystal display panel. The conventional liquid crystal display panel includes a color filter 7 and an array substrate 8. Referring to FIG. 1, the array substrate 8 in a conventional display panel includes a plurality of gate lines 3 and a plurality of common electrode lines 4. The gate lines 3 and the common electrode lines 4 are parallel to each other and are spaced apart by a gap 6. Light leakage occurs in the gap 6 between the gate line 3 and the common electrode line 4. In a conventional display panel, as shown in FIG. 1, light leaking out from the gap 6 sometimes cannot be blocked by a black matrix 71. For example, in response to external pressure placed on the color filter 7, the color filter 7 of the display panel may shift relative to the array substrate 8, resulting in light passing through.

[0030] FIG. 2 is a diagram illustrating the structure of an array substrate in plan view in an embodiment. FIG. 3 is a cross-sectional view of the array substrate taken along section line A-A of FIG. 2. Referring to FIGs. 2 and 3, the array substrate in the embodiment includes a base substrate 1, an array of a plurality of pixel units 2 disposed on the base substrate 1, a plurality of gate lines 3, a plurality of common electrode lines 4, and a plurality of light shields 5. The gate lines 3 define rows of pixel units 2. Each row of the plurality of pixel units 2 corresponds to one gate line 3 (i.e., a first gate line 3) and one common electrode line 4 (i.e., a first common electrode line 4). The first gate line 3 and the first common electrode line 4 are adjacent to and are on a same side of the row of the plurality of pixel units 2 in plan view of the array substrate. The first gate line 3 and the first common electrode line 4 are spaced apart by a gap 6. The light shield 5 is disposed on the base substrate at a position corresponding to the gap 6 between the first gate line 3 and the first common electrode line 4 (e.g., above or below the gap 6). In FIG. 3, the light shield 5 is disposed on top of the gap 6 to reduce light leakage from the gap 6. The projection of light shield 5 covers the gap 6 in plan view of the array substrate. By covering the gap 6 between the first gate line 3 and the first common electrode line 4 with a light shield 5, light leakage can be reduced or

eliminated. In some embodiments, the light shield 5 at least partially covers the gap 6 for reducing light leakage from the gap 6.

[0031] In some embodiments, the light shield 5 has a width which is equal to or larger than a width of the gap 6 but less than the total width of the gap 6, the first gate line 3 and the first common electrode line 4 altogether. A light shield 5 having such a width can effectively prevent light leakage in the gap 6. At the same time, the light shield 5 having such a width minimally affects light transmission in light transmitting areas of the array substrate.

Consequently, the aperture ratio of the display panel is not compromised by having a light shield 5. Optionally, the width of the light shield 5 equals to the width of the gap 6. In some embodiments, the width of the light shield 5 is less than the width of the gap 6 but still allows sufficient reduction of light leakage in the gap 6. In some embodiments, the width of the light shield 5 is larger than (e.g., slightly larger) the total width of the gap 6, the first gate line 3 and the first common electrode line 4 to ensure complete light blocking. Optionally, the array substrate includes a first layer having the first gate line 3 and the first common electrode line 4, and a second layer having the light shield 5. The second layer having the light shield 5 can be disposed either above or below the first layer having the first gate line 3 and the first common electrode line 4.

[0032] As used herein, the term “same layer” refers to the relationship between the layers simultaneously formed in the same step. In one example, two electrodes are on the same layer when the two electrodes are formed as a result of one or more steps of a same patterning process performed on a same layer of material. In another example, the first gate line 3 and the first common electrode line 4 can be formed in the same layer by simultaneously performing the step of forming the first gate line 3 and the step of forming the first common electrode line 4. The term “same layer” does not always mean that the thickness of the layer or the height of the layer in a cross-sectional view is the same.

[0033] Referring to FIG. 2, the pixel unit 2 in the embodiment includes a thin film transistor 21. The thin film transistor 21 includes a gate electrode 210, an active layer 211, a source electrode 212, and a drain electrode 213. The gate electrode 210 and the first gate line 3 are connected to each other. Optionally, the first layer includes the gate electrode 210, the first gate line 3, and the first common electrode line 4. Optionally, the second layer includes the light shield 5, the source electrode 212 and the drain electrode 213 made of a same material. Accordingly, the source electrode 212, the drain electrode 213, and/or the light shield 5 can be formed in a same patterning process. The thin film transistor 21 as shown in FIG. 2 can be a bottom gate type thin film transistor (as shown in FIG. 2) or a top gate type

thin film transistor. The second layer can be disposed above the first layer (as shown in FIG. 2) or below the first layer.

[0034] Optionally, the light shield 5 is integrally formed as a single body with the drain electrode 213 of the thin film transistor 21. For example, the light shield 5 can be formed by extending the drain electrode pattern to the area corresponding to the gap 6.

[0035] In the embodiment as shown in FIGs. 2 and 3, the light shield 5 has a width which is equal to or larger than a width of the gap 6 but less than the total width of the gap 6, the first gate line 3 and the first common electrode line 4 altogether. The light shield 5 partially overlaps with the first gate line 3 and the first common electrode line 4, and forms capacitance with them. During image display, the voltages on the first gate line 3 and the first common electrode line 4 induce an electrical field with the light shield 5. The induced electrical field causes disturbance in the liquid crystal layer of the display panel.

[0036] Referring to FIGs. 2 and 3, the pixel unit in the embodiment further includes a pixel electrode 22 above the light shield 5. For example, the pixel electrode 22 can be on top of the light shield 5 to shield the liquid crystal layer from electrical field induced by the light shield 5. To optimize the electrical field shielding effect, the pixel electrode 22 may be disposed to substantially completely cover the light shield 5 in plan view of the array substrate. By having a pixel electrode 22 that substantially completely covers the light shield 5, the induced electrical field can be effectively shielded. The disturbance in the liquid crystal layer can be effectively reduced or eliminated, thereby enhancing display quality.

[0037] Referring to FIGs. 2 and 3, the pixel unit in the embodiment further includes a common electrode 23 below the first gate line 3 and the first common electrode line 4, and connected to the first common electrode line 4.

[0038] Optionally, the pixel unit in the embodiment further includes a common electrode 23 disposed at a position corresponding to the pixel electrode 22. The common electrodes 23 are disposed on top of the pixel electrodes 22. Each of the plurality of pixel electrodes 22 is above each of the light shield 5. For example, each of the pixel electrodes 22 can be on top of each of the plurality of light shields 5 to shield the liquid crystal layer from electrical field induced by the light shield 5. To optimize the electrical field shielding effect, each of the plurality of pixel electrodes 22 may be disposed to substantially completely cover each of the plurality of light shields 5 in plan view of the array substrate. Optionally, the light shields 5 are above the first layer having the gate lines 3 and the common electrode lines 4. Optionally,

the light shields 5 are below the first layer having the gate lines 3 and the common electrode lines 4.

[0039] Optionally, the pixel unit in the embodiment further includes a common electrode 23 disposed at a position corresponding to the pixel electrode 22. The pixel electrodes 22 are disposed on top of the common electrodes 23. Each of the plurality of common electrodes 23 is above each of the light shield 5. For example, each of the common electrodes 23 can be disposed on top of each of the plurality of light shields 5 to shield the liquid crystal layer from electrical field induced by the light shield 5. To optimize the electrical field shielding effect, each of the plurality of common electrodes 23 may be disposed to substantially completely cover each of the plurality of light shields 5 in plan view of the array substrate. Optionally, the light shields 5 are disposed above the layer having the gate lines 3 and the common electrode lines 4. Optionally, the light shields 5 are disposed below the layer having the gate lines 3 and the common electrode lines 4.

[0040] The array substrate in the embodiment is an Advanced Super Dimension Switch (ADS) mode array substrate. In an ADS mode display panel, the color filter is prone to shift relative to the array substrate in response to external pressure. As a result, the black matrix on the color filter also shifts relative to the array substrate, and no longer covers the gap area 6 between the first gate line 3 and the first common electrode line 4. By covering the gap 6 between the first gate line 3 and the first common electrode line 4 with a light shield 5, light leakage can be reduced or eliminated when the leaking light cannot be blocked by the black matrix. Optionally, the array substrate may be an array substrate of other modes, e.g., a Twisted Nematic (TN) mode array substrate. In a TN mode array substrate, the common electrode 23 is disposed on the color filter.

[0041] In some embodiments, the display panel is a touch display panel, e.g., a resistive, capacitive, optical, sound wave, or electromagnetic touch display panel.

[0042] The present disclosure also provides a method of manufacturing an array substrate. In some embodiments, the method includes forming an array of pixel units, gate lines, and common electrode lines on a base substrate, and forming light shields. The plurality of gate lines defines a plurality of rows of pixel units (FIG. 2), and each row of the pixel units corresponds to one gate line (i.e., a first gate line) and one common electrode line (i.e., a first common electrode line). In some embodiments, the method includes forming a row of a plurality of pixel unitson a base substrate, forming a first gate line and a first common electrode lines, and forming a light shield.The first gate line and the first common electrode

line are adjacent to and are on the same side (e.g., a first side) of a row of the pixel units in plan view of the array substrate. The first gate line and the first common electrode line are spaced apart by a gap. The light shield is disposed at a position corresponding to the gap for reducing light leakage from the gap, e.g., the projection of light shield covers the gap in plan view of the array substrate. The light shield can be disposed either above or below the layer having the first gate line and the first common electrode line. The gate lines and the common electrode lines can be made of a same material and formed in a same patterning process. In some embodiments, the light shield at least partially covers the gap for reducing light leakage from the gap.

[0043] The process of forming an array of pixel units includes a process of forming an array of thin film transistors, e.g., forming gate electrodes, active layers, source electrodes and drain electrodes. The gate electrodes and the gate lines can be made of a same material and formed in a same patterning process. Optionally, the gate lines, the common electrode lines, and the gate electrodes of the thin film transistor are all made of a same material and formed in a first patterning process (i.e., a first layer). The source electrodes and the drain electrodes can be made of a same material and formed in a same patterning process. Optionally, the light shields, the source electrodes, and the drain electrodes are all made of a same material and formed in a second patterning process (i.e., a second layer). Optionally, an insulating layer is disposed between the second layer having the light shields and the first layer having the gate lines and the common electrode lines. The first patterning process can be conducted prior to the second patterning process. As a result, the second layer is above the first layer. Alternatively, the second patterning process is conducted prior to the first patterning process. Consequently, the second layer is below the first layer.

[0044] The process of forming pixel units also includes a process of forming pixel electrodes. In some embodiments, each of the pixel electrodes is on top of each of the light shields, and substantially completely covers each of the corresponding light shields in plan view of the array substrate. As discussed above, the light shield partially overlaps with and forms capacitance with the gate line and the common electrode line. During image display, the voltages on the gate line and the common electrode line induce an electrical field with the light shield. By forming a pixel electrode that substantially completely covers the light shield, the induced electrical field can be effectively shielded. The disturbance in the liquid crystal layer can be effectively reduced or eliminated, thereby enhancing display quality.

[0045] Optionally, a passivation layer is disposed between the pixel electrodes and the light shields. The passivation layer may include a via through which the pixel electrode is connected to the drain electrode of the thin film transistor.

[0046] In some embodiments, the process of forming an array of pixel units includes a process of forming an array of common electrodes and forming an array of pixel electrodes. The pixel electrodes are above the light shield. For example, the pixel electrode can be disposed on top of the light shield to shield the liquid crystal layer from electrical field induced by the light shield. To optimize the electrical field shielding effect, each of the pixel electrodes may be disposed to substantially completely cover each of the light shields in plan view of the array substrate.

[0047] In some embodiments, the common electrodes are below the gate lines and the common electrode lines. Optionally, the light shields are above the gate lines and the common electrode lines. Optionally, the light shields are below the gate lines and the common electrode lines.

[0048] In some embodiments, the process of forming pixel units includes a process of forming common electrodes and forming pixel electrodes. The common electrodes are disposed on top of the pixel electrodes. Each of the plurality of pixel electrodes is above each of the light shield. For example, each of the pixel electrodes can be on top of each of the plurality of light shields to shield the liquid crystal layer from electrical field induced by the light shield. To optimize the electrical field shielding effect, each of the plurality of pixel electrodes may be disposed to substantially completely cover each of the plurality of light shields in plan view of the array substrate. Optionally, the light shields are above the first layer having the gate lines and the common electrode lines. Optionally, the light shields are below the first layer having the gate lines and the common electrode lines.

[0049] In some embodiments, the process of forming pixel units includes a process of forming common electrodes and forming pixel electrodes. The pixel electrodes are disposed on top of the common electrodes. Each of the plurality of common electrodes is above each of the light shield. For example, each of the common electrodes can be disposed on top of each of the plurality of light shields to shield the liquid crystal layer from electrical field induced by the light shield. To optimize the electrical field shielding effect, each of the plurality of common electrodes may be disposed to substantially completely cover each of the plurality of light shields in plan view of the array substrate. Optionally, the light shields are disposed above the layer having the gate lines and the common electrode lines. Optionally,

the light shields are disposed below the layer having the gate lines and the common electrode lines.

[0050] The present disclosure also provides a display panel having an array substrate described herein or manufactured by a method described herein. The present disclosure further provides a display device having a display panel described herein. The display device can be of any type, e.g., a mobile phone, a laptop, a television, a display device, a computer, a digital photo album, a gps, etc.

[0051] The foregoing description of the embodiments of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form or to exemplary embodiments disclosed. Accordingly, the foregoing description should be regarded as illustrative rather than restrictive. Obviously, many modifications and variations will be apparent to practitioners skilled in this art. The embodiments are chosen and described in order to best explain the principles of the invention and its best mode practical application, thereby to enable persons skilled in the art to understand the invention for various embodiments and with various modifications as are suited to the particular use or implementation contemplated. It is intended that the scope of the invention be defined by the claims appended hereto and their equivalents in which all terms are meant in their broadest reasonable sense unless otherwise indicated. Therefore, the term “the invention”, “the present invention” or the like does not necessarily limit the claim scope to a specific embodiment, and the reference to exemplary embodiments of the invention does not imply a limitation on the invention, and no such limitation is to be inferred. The invention is limited only by the spirit and scope of the appended claims. Moreover, these claims may refer to use “first”, “second”, etc. following with noun or element. Such terms should be understood as a nomenclature and should not be construed as giving the limitation on the number of the elements modified by such nomenclature unless specific number has been given. Any advantages and benefits described may not apply to all embodiments of the invention. It should be appreciated that variations may be made in the embodiments described by persons skilled in the art without departing from the scope of the present invention as defined by the following claims. Moreover, no element and component in the present disclosure is intended to be dedicated to the public regardless of whether the element or component is explicitly recited in the following claims.

WHAT IS CLAIMED IS:

1. An array substrate, comprising:
a base substrate;
a row of a plurality of pixel units; and
a first gate line and a first common electrode line adjacent to the row of the plurality of pixel units and on a first side of the row of the plurality of pixel units in plan view of the array substrate, wherein the first gate line and the first common electrode line are spaced apart by a gap; and
a light shield at least partially covering the gap for reducing light leakage from the gap.
2. The array substrate of claim 1, wherein the light shield is above the gap.
3. The array substrate of claim 1, wherein the light shield is below the gap.
4. The array substrate of claim 1, wherein the light shield has a width which is substantially equal to a width of the gap and less than a total width of the gap, the first gate line and the first common electrode line.
5. The array substrate of claim 1, comprising a first layer comprising the first gate line and the first common electrode line and a second layer comprising the light shield.
6. The array substrate of claim 5, wherein each of the plurality of pixel units comprises a thin film transistor comprising a gate electrode, an active layer, a source electrode, and a drain electrode; the first layer further comprising the gate electrode connected to the first gate line; the second layer comprising the light shield, the source electrode and the drain electrode.
7. The array substrate of claim 5, wherein each of the plurality of pixel units comprises a pixel electrode above the light shield, the pixel electrode substantially completely covers the light shield in plan view of the array substrate.
8. The array substrate of claim 5, wherein each of the plurality of pixel units comprises a common electrode below the first gate line and the first common electrode line, and connected to the first common electrode line.

9. The array substrate of claim 5, wherein each of the plurality of pixel units comprises a pixel electrode on top of a common electrode, the common electrode is above the light shield, the common electrode substantially completely covers the light shield in plan view of the array substrate.

10. The array substrate of claim 5, wherein each of the plurality of pixel units comprises a common electrode on top of a pixel electrode, the pixel electrode is above the light shield, the pixel electrode substantially completely covers the light shield in plan view of the array substrate.

11. A display panel comprising an array substrate of any one of claims 1-10.

12. A display device comprising a display panel of claim 11.

13. A method of manufacturing an array substrate, comprising:
forming a row of a plurality of pixel units on a base substrate;
forming a first gate line and a first common electrode lines adjacent to the row of the plurality of pixel units and on a first side of the row of the plurality of pixel units in plan view of the base substrate, wherein the first gate line and the first common electrode line are spaced apart by a gap; and
forming a light shield, wherein the light shield at least partially covers the gap for reducing light leakage from the gap.

14. The method of claim 13, wherein the light shield is above the gap.

15. The method of claim 13, wherein the light shield is below the gap.

16. The method of claim 13, wherein the gate line and the common electrode line are made of a same material and formed in a first patterning process in a first layer, and the light shield is formed in a second patterning process in a second layer.

17. The method of claim 16, wherein the step of forming the row of the plurality of pixel units comprises forming a thin film transistor, comprising:
forming a gate electrode;
forming an active layer; and
forming a source electrode and a drain electrode;

wherein the gate electrode, the gate line, and the common electrode line are made of a same material and formed in the first patterning process; the light shield, the source electrode and the drain electrode are formed in the second patterning process.

18. The method of claim 16, wherein the step of forming the row of the plurality of pixel units further comprises:

forming a pixel electrode, the pixel electrode is above the light shield, the pixel electrodes substantially completely covers the light shield in plan view of the array substrate.

19. The method of claim 16, wherein the step of forming an array of a plurality of pixel units further comprises:

forming a pixel electrode and a common electrode;

wherein the common electrodes is on top of the pixel electrode, the pixel electrode is above the light shield, the pixel electrode substantially completely covers the light shield in plan view of the array substrate.

20. The method of claim 16, wherein the step of forming an array of a plurality of pixel units further comprises:

forming a pixel electrode and a common electrode;

wherein the pixel electrode is on top of the common electrode, the common electrode is above the light shield, the common electrode substantially completely covers the light shield in plan view of the array substrate.

FIG. 1

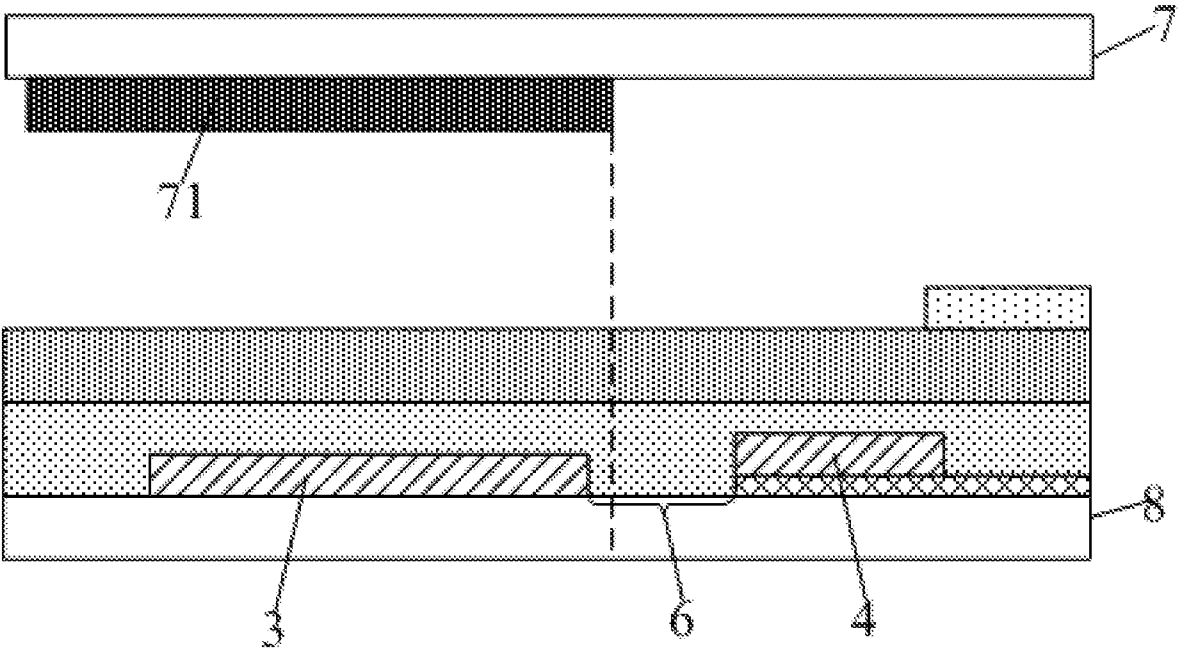


FIG. 2

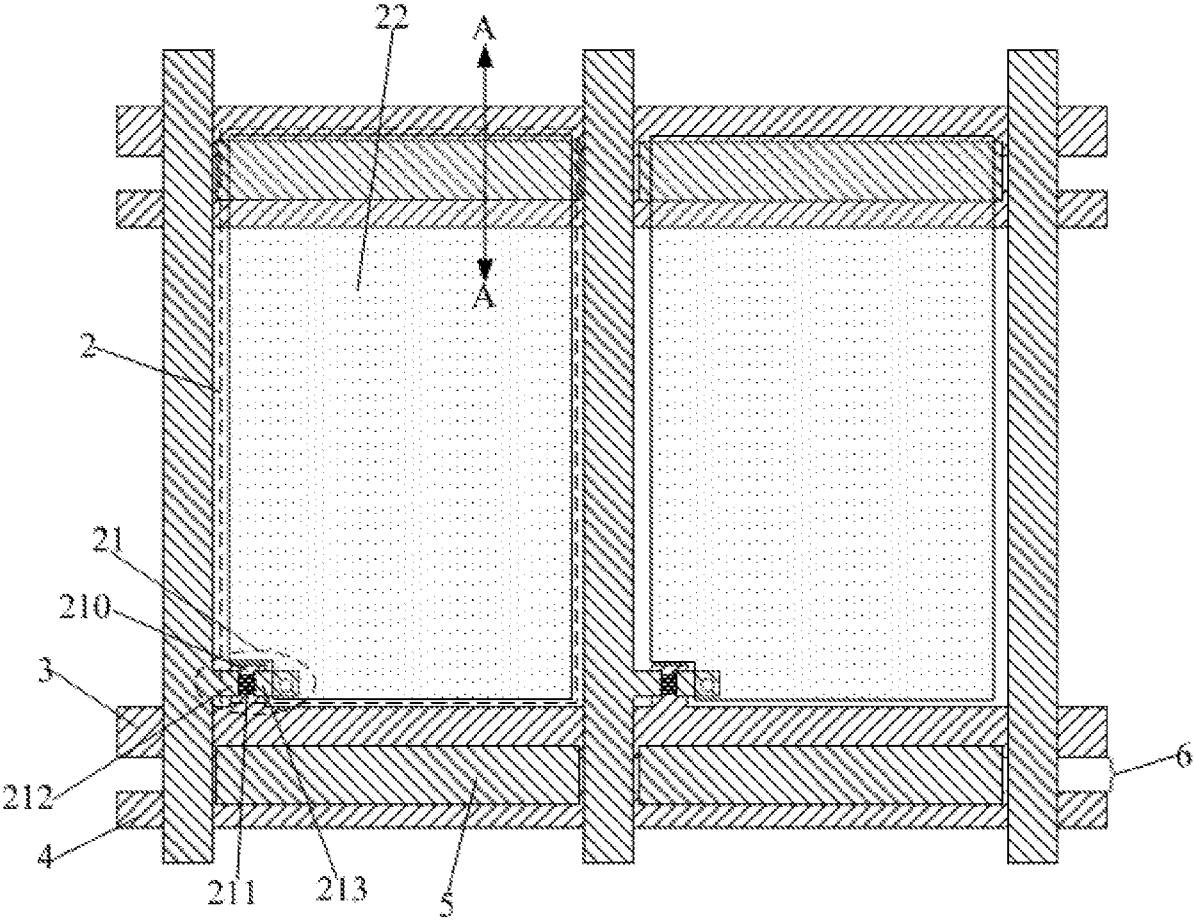
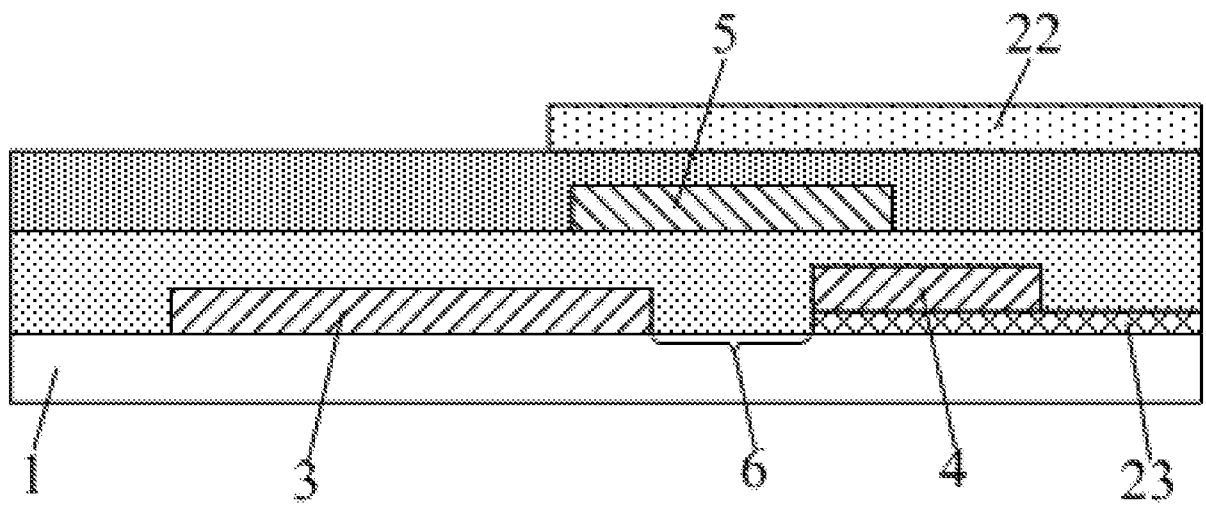


FIG. 3



INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2015/097023

A. CLASSIFICATION OF SUBJECT MATTER

G02F 1/1343(2006.01)i; G02F 1/1362(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G02F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

VEN, CNABS, CNTXT: gate, scan+, common, shield, light leakage, gap

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2009002294 A1 (EPSON IMAGING DEVICES CORP) 01 January 2009 (2009-01-01) description, paragraphs [0054]-[0066], figures 1-3	1-2, 5, 13-14, 16
X	CN 101122694 A (EPSON IMAGING DEVICES CORP) 13 February 2008 (2008-02-13) description, page 16, paragraph 6 – page 23, paragraph 3, figures 1-9	1-2, 5, 13-14, 16
PX	CN 104880852 A (BOE TECHNOLOGY GROUP CO LTD ET AL) 02 September 2015 (2015-09-02) claims 1-16	1-20
A	CN 104597643 A (BOE TECHNOLOGY GROUP CO LTD ET AL) 06 May 2015 (2015-05-06) the whole document	1-20
A	CN 103941499 A (SHANGHAI TIANMA MICROELECTRONICS CO LTD ET AL) 23 July 2014 (2014-07-23) the whole document	1-20

☐ Further documents are listed in the continuation of Box C.
 ☒ See patent family annex.

* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance

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“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

15 March 2016

Date of mailing of the international search report

23 March 2016

Name and mailing address of the ISA/CN

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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2015/097023

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				KR	20080013744	A	13 February 2008
				US	2008284962	A1	20 November 2008
				US	7787091	B2	31 August 2010
CN	104880852	A	02 September 2015	None			
CN	104597643	A	06 May 2015	None			
CN	103941499	A	23 July 2014	None			