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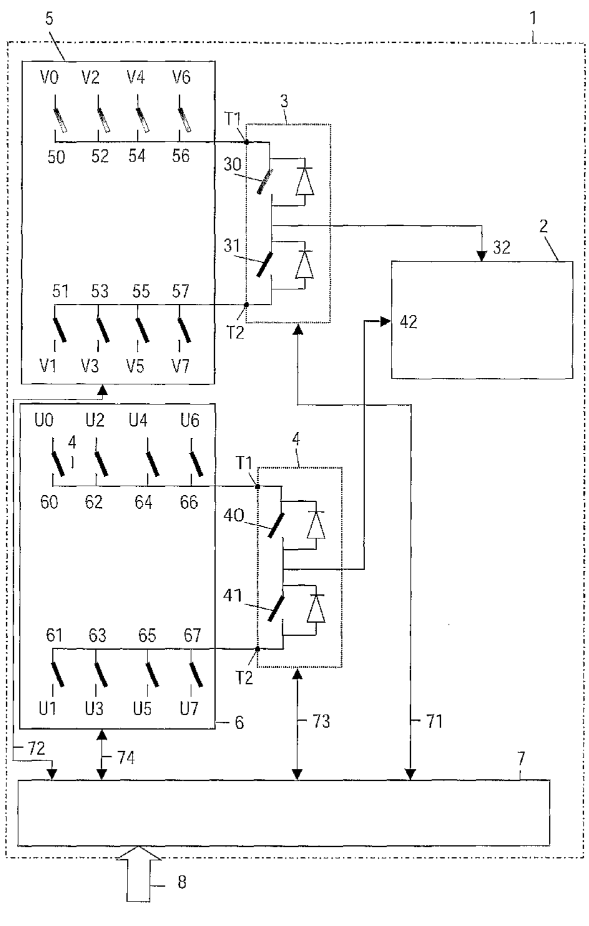
(54) Title: DISPLAY DEVICE COMPRISING A DISPLAY PANEL AND A DRIVER-CIRCUIT



(57) Abstract: The display device (1) comprises a display panel (2), a driver circuit (3,4) for driving at least one part of the display panel (2) and at least one switching circuit (5,6). The at least one switching circuit (5,6) comprises at least three switches (50-57,60-67) for coupling supply voltages (V0-V7,U0-U7) to the driver circuit (3,4) for driving the at least one part of the display panel (2) with the supply voltages (V0-V7,U0-U7). The switching circuit (5,6) enables the use of low cost and well available two-level driver integrated circuits (3,4) for generating multi-level outputs.

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Display device comprising a display panel and a driver-circuit

The invention relates to a display device comprising a display panel and a driver circuit for driving at least one part of the display.

The invention also relates to a switching circuit, and to a method of driving at least a part of a display panel.

The display device may be a mobile phone, PDA, a computer monitor, a television receiver, a disc player/recorder or a display module.

US 6,078,319 disclose a video display device comprising circuitry for driving a display. Via a switching circuit, in a low speed mode (lower resolution, pixel depth and refresh rate) 3.3 Volts DC is supplied to the circuitry, and in a high speed mode (higher resolution, pixel depth and refresh rate) 5 Volts DC is supplied to the circuitry. The known display device is disadvantageous, inter alia, due to having insufficiently flexible drive circuitry: the output circuitry generates 0 -5 Volts for a first kind of display, or 0-3.3 Volts for a second kind of display, and generally generates a fixed operating voltage for a given display type.

It is an object of the invention to provide a display device having driver circuitry enabling flexible multi-level driving of a display panel. The invention is defined by the independent claims. The dependent claims define advantageous embodiments.

The display device according to the invention comprises a display panel, a driver circuit for driving at least one part of the display panel and at least one switching circuit comprising at least three switches for coupling supply voltages to the driver circuit for driving the at least one part of the display panel with the supply voltages.

By providing the switching circuit with three or more switches, the display panel may be driven with three or more voltage levels, so that even the most recent display panels requiring three or more voltage levels can now be driven advantageously. In addition, these switches may be turned on an off rapidly, thereby allowing to change frequently the supply voltages for the driver circuit. So, the display device according to the invention gives more flexibility when designing addressing schemes for the driving by allowing frequent changes between the available voltage levels. A cost-effective two-level drive circuit may be used, which in combination with the switching circuit is able to provide drive waveforms with three or more voltage levels.

Such a two-level driver circuit may deliver as output voltage level the voltage present at its first terminal or the voltage level present at its second terminal. When at least two switches are coupled to the first terminal, at least two voltage levels can be applied to the first terminal. By coupling two other switches to the second terminal also two voltage levels can be applied to the second terminal.

The display panel may be a dynamic-foil display or any other display requiring to be driven with three or more voltage levels.

Such a dynamic-foil display comprises a flexible and transparent foil clamped between two glass plates. In the back plate, light is coupled in and captured by internal reflection. If the foil sticks to the front plate, no light is coupled out, if the foil sticks to the back plate, light is coupled out. The display comprises a matrix of rows and columns of conductive material. At each crossing of a row and a column a pixel is formed. By flipping the foil through driving the rows and columns of the dynamic-foil display with appropriate drive voltages, an image is displayed.

By providing the column-witching circuit with, for example, eight switches for switching at least six different supply voltages for driving the columns of the display at one or more of at least six different voltage levels, four switches are used for displaying images, and four switches are used for reset purposes. Due to the fact that a dynamic-foil display represents a capacitance, it needs to be controlled with non-inverted voltage levels during positive frames and with inverted voltage levels during negative frames and vice versa. Therefore, of the four switches for displaying images, the two upper switches coupled to the first terminal switch the first set of supply voltages, for example, 0 Volt and +20 Volts respectively, and the two lower switches coupled to the second terminal switch the second set of supply-voltages for example -20 Volts and 0 Volt respectively. Of the four switches for resetting purposes, the two upper switches coupled to the first terminal switch for example +50 Volts and -50 Volts respectively, and the two lower switches coupled to the second terminal switch for example +50 Volts and -50 Volts respectively.

When providing the row-switching circuit with four switches for driving the rows of the display, two upper switches coupled to the first terminal may switch the first set of supply voltages, for example +30 Volts and -05 Volts respectively, and two lower switches coupled to the second terminal may switch the second set of supply voltages for example +05 Volts and -30 Volts respectively.

Alternatively, the switches necessary for resetting purposes can be shifted from the column-switching circuit to the row-switching circuit.

Embodiments of the switching circuit according to the invention and of the method according to the invention correspond with the embodiments of the display device according to the invention.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments(s) described hereinafter.

In the drawings:

Fig. 1 is a block diagram of a display device according to the invention comprising switching circuits according to the invention;

Fig. 2 is a general timing diagram of the display device according to the invention based upon a simple addressing scheme;

Fig. 3 is a timing diagram for supplying column driver circuits based upon the simple addressing scheme;

Fig. 4 is a timing diagram for supplying row driver circuits based upon the simple addressing scheme;

Fig. 5 is a timing diagram for supplying row driver circuits based upon a more efficient addressing scheme; and

Fig. 6 is a block diagram of a switch to be used in a switching circuit according to the invention.

The display device 1 according to the invention may be a product such as a mobile phone, PDA, a computer monitor, a television receiver or a disc player/recorder comprising a display panel 2 and driver circuits. The display device 1 may also be a display module for use in a product and comprising a display panel 2 such as, for example, a dynamic-foil display (DFD) and driver-circuits. In the embodiment of figure 1 the display device 1 is a display module comprising a display panel 2, also called a DFD 2, a column driver circuit 3 and a row driver circuit 4. The column driver circuit 3 and the row driver circuit 4 may each be a two-level driver integrated circuit like the TEA6205 (Philips Semiconductors) for driving the columns and rows of the DFD 2.

Column driver circuit 3 comprises two serial driver switches 30,31, of which a common point is coupled to the output of column driver circuit 3. This output is coupled to a column input 32 of DFD 2. In a first mode, driver switch 30 is conducting and the common point is coupled to a first terminal T1 of column driver circuit 3. This first terminal T1 is further coupled to one side of four switches 50,52,54,56, of which the other sides are coupled to four supply voltages V0,V2,V4,V6, respectively . In a second mode, driver switch 31 is conducting and the common point is coupled to a second terminal T2 of column driver circuit 3. This second terminal T2 is further coupled to one side of four switches 51,53,55,57 respectively, of which the other sides are coupled to four supply voltages V1,V3,V5,V7, respectively. The switches 50-57 form (part of) a column switching circuit 5.

Row driver circuit 4 comprises two serial driver switches 40,41, of which a common point is coupled to the output of row driver circuit 4. This output is coupled to a row input 42 of the DFD 2. In a first mode, driver switch 40 is conducting and the common point is coupled to a first terminal T1 of row driver circuit 4. This first terminal T1 is further coupled to one side of four switches 60,62,64,66, of which the other sides are coupled to four supply voltages U0,U2,U4,U6, respectively. In a second mode, driver switch 41 is conducting and the common point is coupled to a second terminal T2 of row driver circuit 4. This second terminal T2 is further coupled to one side of four switches 61,63,65,67, of which the other sides are coupled to four supply voltages U1,U3,U5,U7, respectively. The switches 60-67 form (part of) row switching circuit 6.

In a third mode like a tri-state mode or a floating mode, each of the driver switches 30,31,40,41 of the driver circuits 3,4 is non-conducting. Each driver circuit 3,4 comprises two diodes, one of the diodes being coupled anti-parallel to one of the serial driver switches 30,31,40,41 and the other one of the diodes being coupled anti parallel to the other one of the serial driver switches 30,31,40,41.

For the sake of clarity, only one column driver circuit 3 with two driver switches 30,31 and only one row driver circuit 4 with two driver switches 40,41 have been shown. Usually, a two-level driver integrated circuit comprises, for example, 3x32=96 separate drivers each comprising two driver switches, and more than one two-level driver integrated circuit may be used to drive more than 96 columns/rows in the same display.

A controller 7 receives image information 8 and controls column driver circuit 3 via a coupling 71 and column switching circuit 5 via a coupling 72 and row driver circuit 4 via a coupling 73 and row switching circuit 6 via a coupling 74.

The DFD 2 comprises a foil, which is flipped by driving the rows and columns with the correct voltage levels. The unselect level of a row is for example +5 Volts, and selecting a row is done by for example +30 Volts. If a certain row is scanned, the columns are driven with the video data to be displayed. If a column is driven with -20 Volts, pixels corresponding to the selected row are switched on (the foil flips from the front plate to the back plate). For pixels which have to remain in their off-state, the corresponding columns are driven with 0 Volt (for these pixels the foil remains sticking to the front plate). Row by row is selected (which is also called scanning) and, while a row is selected, the columns are driven with the video data for the pixels in that row. At the end of a scan sequence, the correct pixels are switched on and emit light, for displaying the intended images.

In figure 1, for example, V0 corresponds to 0 Volt, V1 to -20 Volts, V2 to +20 Volts, V3 to 0 Volt, V4 to +50 Volts, V5 to +50 Volts, V6 to -50 Volts, V7 to -50 Volts, U0 to +30 Volts, U1 to +05 Volts, U2 to -05 Volts, U3 to -30 Volts, U4 to +05 Volts, U5 to -20 Volts, U6 to +20 Volts and U7 to -05 Volts.

The general timing diagram for the display device 1 according to the invention shown in figure 2 illustrates in figure 2a the display voltage Vd (in other words the voltage at the foil), and illustrates in figure 2b row voltages Vr, and illustrates in figure 2c the first column voltage Vc1, and illustrates in figure 2d the second column voltage Vc2, for a positive frame pos and for a negative frame neg. Due to the fact that the DFD represents a capacitance (foil between two (glass)plates), it needs to be controlled with non-inverted supply levels during positive frames and with inverted supply levels during negative frames, and vice versa, to avoid the summing of charges with a same polarity.

During the first (positive) frame, the foil receives the display voltage Vd of +50 Volts, and the rows are scanned one after the other by increasing the voltage to be supplied to the row to be scanned from +05 Volts to +30 Volts. This is illustrated in figure 2b for a first row with the first pulse of +30 Volts and for a second row by a second pulse of +30 Volts having dotted lines. Per scanned row, a column to be driven addressed by decreasing the voltage to be supplied to the column from 0 Volt to -20 Volts. In figure 2c a column voltage Vc1 of a first column is decreased while the first row is selected, while that same column is not addressed when the second row is selected. In figure 2d a column voltage Vc2 of a second column is not addressed while the first row is selected, but is addressed while the second row is selected.

During the second (negative) frame, the foil receives -50 Volts, and the rows are scanned one after the other by decreasing the voltage to be supplied to the row to be scanned from -05 Volts to -30 Volts. Per scanned row, a column is addressed by increasing the voltage to be supplied to the column from 0 Volt to +20 Volts.

So, in this example four different voltage levels are necessary for driving the rows, and another three different voltage levels are necessary for driving the columns.

The timing diagram for addressing column-drivers shown in figure 3 comprises eight time intervals I-VIII. During the first positive frame, pos, comprising time intervals I-IV, DFD 2 is erased by pulling all columns to the foil voltage of +50 Volts. This is done by simultaneously activating switches 54 and 55. Both the first terminal T1 and the second terminal T2 are connected to the same +50 Volts (time interval I). In the next time interval II, some pixels will have to remain in their off-state (0 Volt), and others will have to be switched on (-20 Volts). By activating switches 50 and 51, columns can be driven with either 0 Volt or -20 Volts. Then, for time interval III, DFD 2 is erased again by activating switches 54 and 55, and another scan sequence is performed in the following time interval IV, through activating switches 50 and 51, with the off-state here being indicated by "m" and with the on-state here being indicated by "n". So, in this example two subframes, indicated by II and IV, are present in the positive frame pos. Each of those subframes may have a different duration for generating different levels of light output and are preceded by an erase period I, III .

During the second negative frame, neg, comprising time intervals V-VIII, all voltages change polarity. The DFD 2 is erased by pulling all columns to the foil voltage of -50 Volts. This is done by simultaneously activating switches 56 and 57. Both the first terminal T1 and the second terminal T2 are connected to the same -50 Volts (time interval V). In the next time interval VI, some pixels will have to remain in their off-state (0 Volt), and others will have to be switched on (+20 Volts). By activating switches 52 and 53, columns can be driven with either 0 Volt or +20 Volts. Then, for time interval VII, the DFD 2 is erased again by activating switches 56 and 57, and another scan sequence is performed in the following time interval VIII, through activating switches 52 and 53, with the off-state here being indicated by "q" and with the on state here being indicated by "p". So, in this example are also two subframes present during the negative frame neg.

The timing diagram shown in figure 4 for addressing row driver circuits comprises the same eight time intervals I-VIII, where rows can be driven during the first (positive) frame with either +05 Volts or +30 Volts via switches 60 and 61 and during the second (negative) frame with either -05 Volts or -30 Volts via switches 62 and 63.

The timing diagrams shown in figures 2, 3 and 4 are all based upon the same simple addressing scheme, which, however, requires quite some time and comprises some unnecessary switching. Therefore, a more efficient addressing scheme will require less time and will not comprise any unnecessary switching.

The timing diagram of a row voltage Vr1 for addressing row drivers based upon such a more efficient addressing scheme is shown in figure 5 and discloses three supply voltages: firstly, +05 Volts is supplied, secondly (time interval "a") -20 Volts is supplied, then thirdly (time intervals "b","c" and "d") +05 Volts is briefly supplied, and fourthly +30 Volts is finally supplied (time interval "e").

Rows are set at an unselect level of, for example, +05 Volts. To set pixels off for a certain row, the row has to be driven at for example -20 Volts. To switch pixels on, the row has to be driven at for example +30 Volts. Pixels corresponding to a previous image may be switched off and may immediately be followed by switching other pixels on corresponding to the new image. Both actions follow each other in time but take place for the same row, for example as in the following very efficient addressing scheme.

For time interval "a", switches 64 and 65 are activated (conducting), and driver switch 41 is activated (conducting) and driver switch 40 is not activated (non-conducting), in other words row driver circuit 4 is in the second mode.

For time interval "b", switches 64 and 65 are activated (conducting), and driver switch 41 is not activated (non-conducting) and driver switch 40 is activated (conducting), in other words row driver circuit 4 is in the first mode.

For time interval "c", switches 60-67 are all non-activated (non-conducting), and driver switches 40 and 41 are not activated (non-conducting), in other words row driver circuit 4 is in the third (tri-state) mode.

For time interval "d", switches 60 and 61 are activated (conducting), and driver switch 40 is not activated (non-conducting) and driver switch 41 is activated (conducting), in other words row driver circuit 4 is in the second mode.

For time interval "e", switches 60 and 61 are activated (conducting), and driver switch 40 is activated (conducting) and driver switch 41 is not activated (non-conducting), in other words row driver circuit 4 is in the first mode.

The unselect level of +05 Volts is present in two cases: when pixels are switched on and when pixels are switched off. Via all driver switches 40 all rows but one (for example row "one") are connected to the first terminal T1s for receiving +05 Volts. Row "one" is driven via its driver switch 41 to the second terminal T2 for receiving -20 Volts (switches 64 and 65 are activated). The appropriate pixels for this row are switched off via the column driver circuits, by driving the columns between +20 Volts and 0 Volt. Then all rows including the selected one are driven by driver switches 40 to the +05 Volts unselect level. All switches 60-67 are deactivated and the row driver circuit 4 is set in its tri-state mode. All rows are now floating, but will remain at +05 Volts due to the presence of row capacitances. With DFD 2 being not driven, this +05 Volts will be stable.

Then the switches 60 and 61 are activated, and simultaneously all driver switches 41 are activated and all rows are driven with the +05 Volts unselect level. Since the rows were already floating at this +05 Volts level, this should go without any spikes. The same row as before is selected (row "one") and driven by driver switch 40. The columns in turn are driven in correspondence with the video data to switch the correct pixels on, by driving the columns between 0 Volt and -20 Volts.

Summarizing, for the more efficient addressing scheme, each time that pixels for a row are switched on or off, the supply for the row driver circuits and for the column driver circuits has to be changed, requiring the following actions:

x) drive all rows with +05 Volts unselect voltage via driver switch 40 or 41 and drive all columns with 0 Volt via driver switch 30 or 31;

y) deactivate all switches 60-67, set the row driver circuit in tri-state, deactivate all switches 50-53, set the column driver circuit in tri-state;

z) activate the proper switches, drive all rows with +05 Volts unselect voltage via driver switch 40 or 41, activate the proper switches, drive all columns with 0 Volt via driver switch 30 or 31.

The switch 90 shown in figure 6 and to be used in a switching circuit 5,6 according to the invention, is an embodiment of one of the switches 50-57,60-67 and comprises a MOST 96 of which a control electrode is coupled via an impedance 95 to one side of a serial circuit comprising a capacitor 92 and an impedance 91 and to one side of a parallel circuit comprising an impedance 93 and a zener diode 94 (cathode coupled to impedance 95). The other side of the serial circuit receives a control pulse (control contact of switch 90), and the other side of the parallel circuit is coupled to a main electrode of MOST 96 and to an anode of a diode 98 (an internal back-gate diode usually forming part of MOST

96), of which a cathode is coupled to another main electrode of MOST 96 and to a cathode of a diode 97. An anode of diode 97 forms a first main contact of switch 90, and the anode of diode 98 (or the main electrode of MOST 96) forms the second main contact of switch 90.

Unilateral switch 90 (a switch which can conduct current in one direction) is extremely fast, and allows the supply voltages for the driver circuits to be changed rapidly. In case of a bilateral switch being needed (a switch which can conduct current in two directions), a switch 100 not shown but being identical to switch 90 should be placed in anti-parallel to switch 90 (with both control contacts then needing to receive the same control pulse).

The expression “for” in for example “for A” and “for B” does not exclude that other functions “for C” are performed as well, simultaneously or not. The expressions “X coupled to Y” and “a coupling between X and Y” and “coupling/couples X and Y” etc. do not exclude that an element Z is in between X and Y. The expressions “P comprises Q” and “P comprising Q” etc. do not exclude that an element R is comprised/included as well.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. Use of the verb "to comprise" and its conjugations does not exclude the presence of elements or steps other than those stated in a claim. The article "a" or "an" preceding an element does not exclude the presence of a plurality of such elements. The invention may be implemented by means of hardware comprising several distinct elements, and by means of a suitably programmed computer. In the device claim enumerating several means, several of these means may be embodied by one and the same item of hardware. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.

The invention is based upon an insight, inter alia, that prior art display devices are insufficiently flexible, and is based upon a basic idea, inter alia, that the flexibility is increased by providing the switching circuit with three or more switches for selecting three or more supply voltages. Simple and cost-effective two-level driver ICs may be used in combination with such a switching circuit for selecting the supply voltages to be coupled to the driver ICs. The combination provides multi-level outputs, which may be selected alternately by means of the three or more switches in dependence on the desired drive waveforms.

The invention solves the problem, inter alia, of providing a more flexible display device, and is advantageous, inter alia, in that even the most recent display panels requiring three or more supply levels can now be driven. In addition, the display device according to the invention gives more freedom when designing addressing schemes for the driving. Further, the low cost and well available two-level driver integrated circuit can now be operated at three or more supply levels.

CLAIMS:

1. Display device (1) comprising a display panel (2); a driver circuit (3,4) for driving at least one part of the display panel (2); and at least one switching circuit (5,6) comprising at least three switches (50-57,60-67) for coupling supply voltages (V0-V7,U0-U7) to the driver circuit (3,4) for driving the at least one part of the display panel (2) with the supply voltages (V0-V7,U0-U7) .

2. Display device (1) according to claim 1, wherein the driver circuit (3,4) comprises a first terminal (T1) for receiving a first set of the supply voltages (V0,V2,V4,V6,U0,U2,U4,U6) and a second terminal (T2) for receiving a second set of the supply voltages (V1,V3,V5,V7,U1,U3,U5,U7), at least two switches (50,52,54,56,60,62,64,66) of the at least three switches (50-57,60-67) being coupled to the first terminal (T1) and at least two other switches (51,53,55,57,61,63,65,67) of the at least three switches (50-57,60-67) being coupled to the second terminal (T2).

3. Display device (1) according to claim 1, wherein the display panel (2) comprises a dynamic-foil display having rows and columns.

4. Display device (1) according to claim 3, wherein the driver circuit (3,4) comprises a column driver circuit (3) for driving a column of the display panel (2).

5. Display device (1) according to claim 4, wherein the at least one switching circuit (5,6) comprises a column switching circuit (5) comprising at least six switches (50-57) for coupling at least six supply voltages (V0-V7) to the column driver circuit (3).

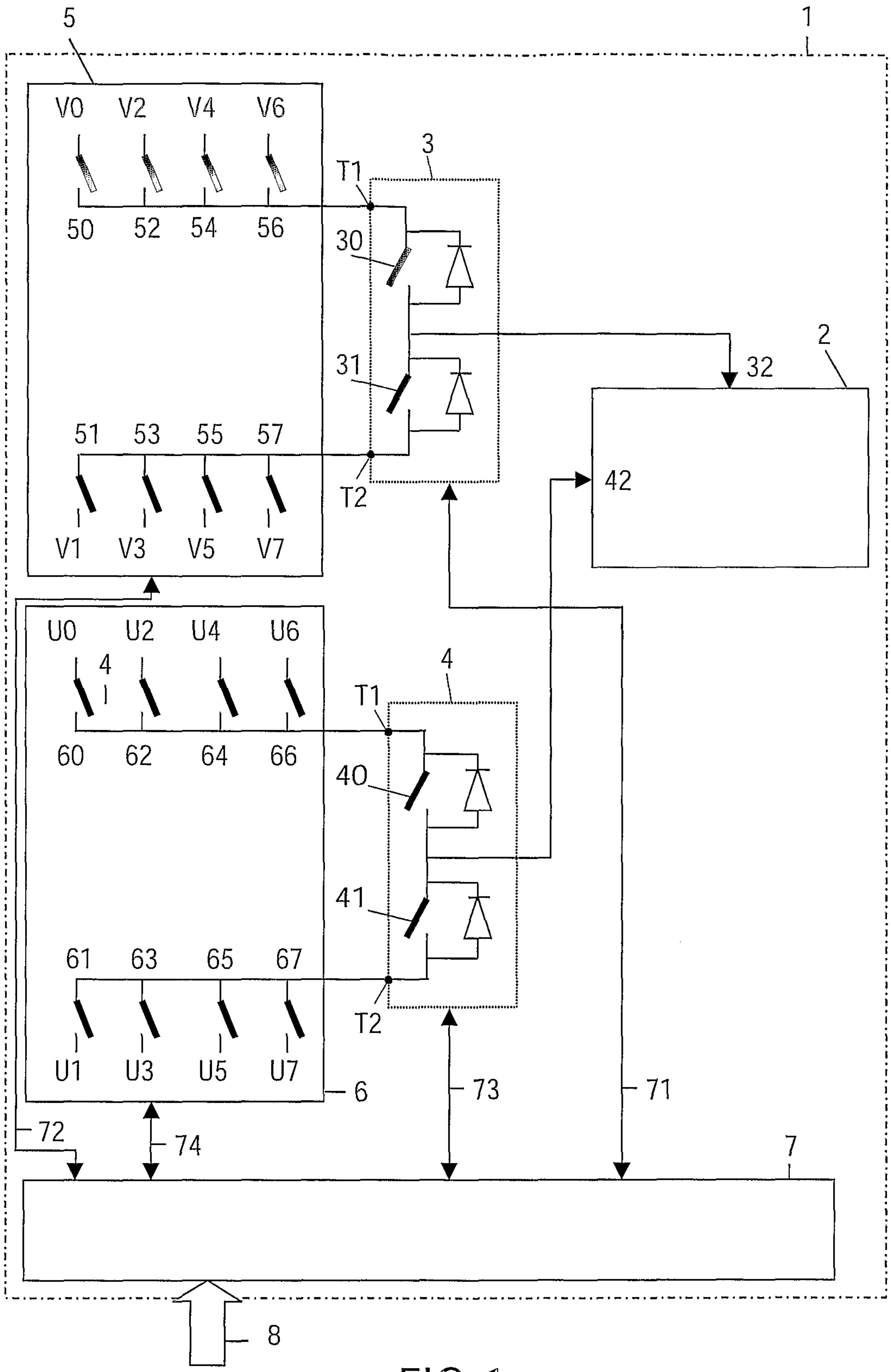
6. Display device (1) according to claim 3, wherein the driver circuit (3,4) comprises a row driver circuit (4) for driving a row of the display panel (2).

7. Display device (1) according to claim 6, wherein the at least one switching circuit (5,6) comprises a row switching circuit (6) which comprises at least three switches

(60-67) for coupling at least three different supply voltages (U0-U7) to the row driver circuit (4).

8. Switching circuit (5,6) comprising at least three switches (50-57,60-67) for coupling corresponding supply voltages (V0-V7,U0-U7) to a driver circuit (3,4) for driving at least one part of a display panel (2) with the respective supply voltages (V0-V7,U0-U7).

9. Method of driving at least one part of a display panel (2) with a driver circuit (3, 4) comprising the step of: alternately coupling supply voltages (V0-V7,U0-U7) to the driver circuit (3,4) for driving the at least one part of the display panel (2) with the respective supply voltages (V0-V7,U0-U7).


5
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V0
V2
V4
V6
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T1
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56
30
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55
57
42
T2
V1
V3
V5
V7
U0
U2
U4
U6
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T1
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41
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FIG.1

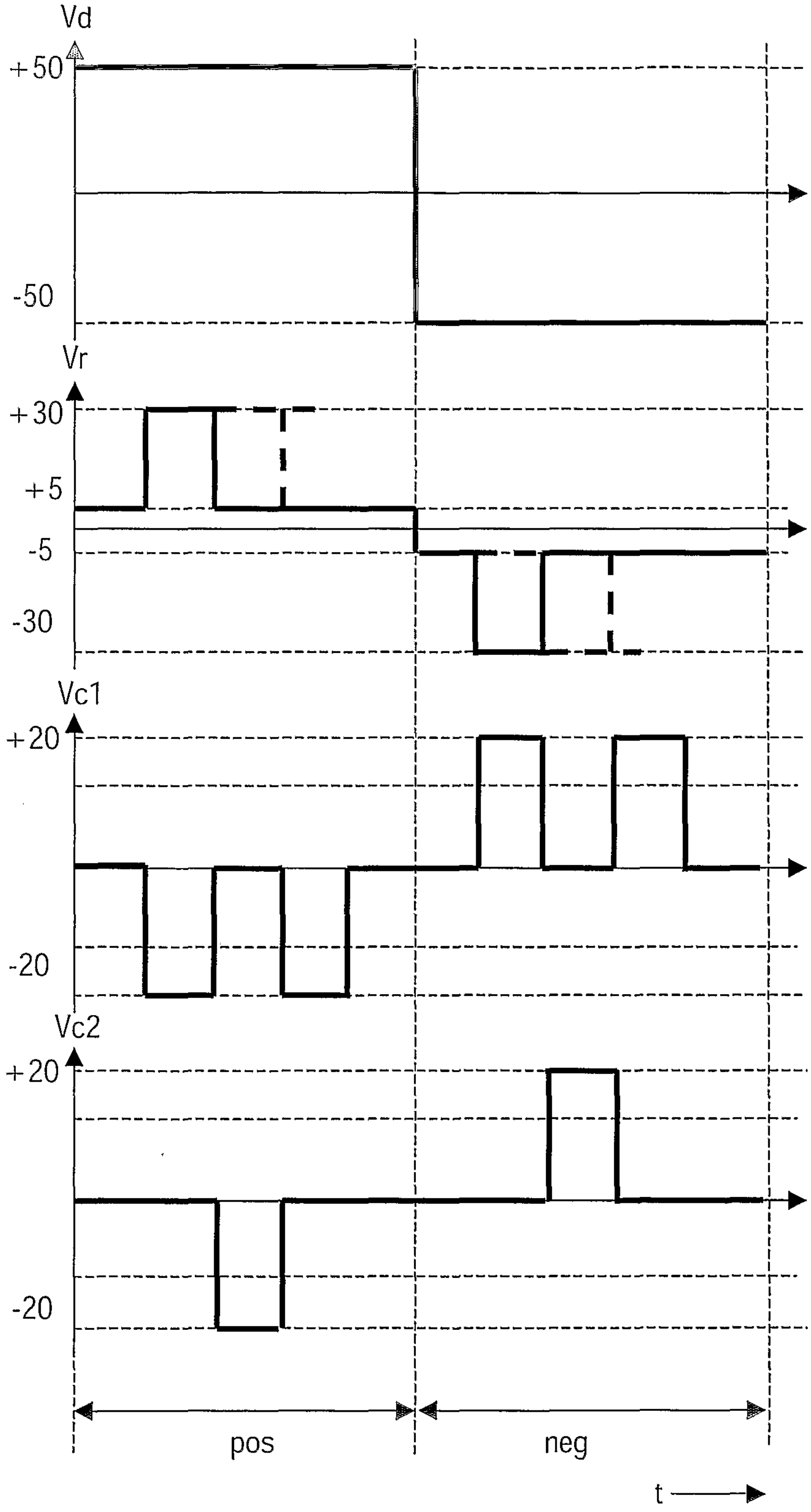
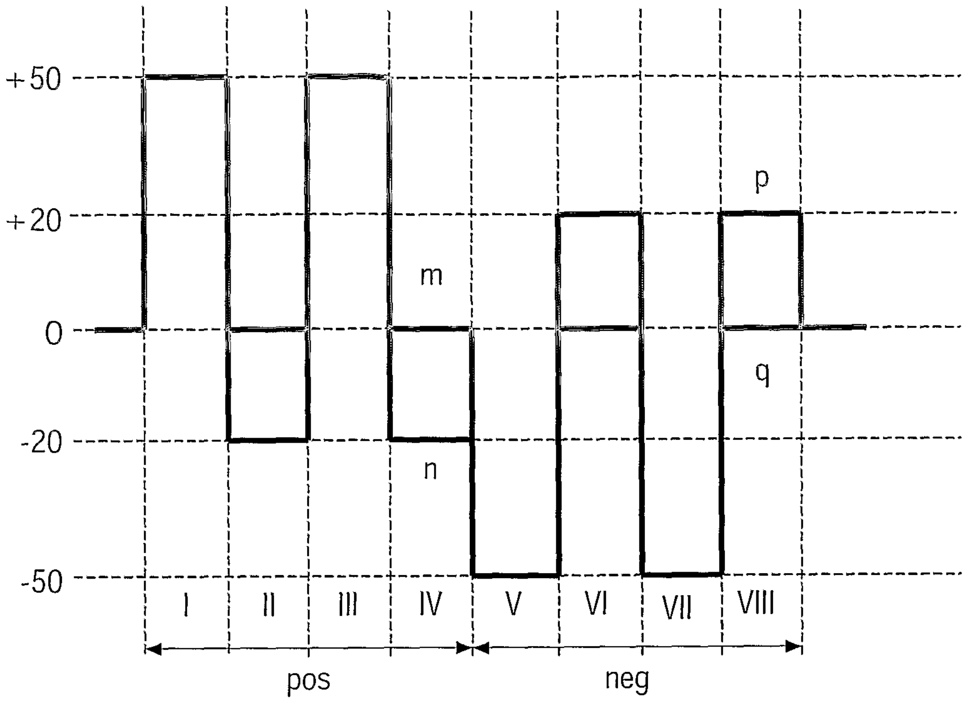


FIG.2a

FIG.2b

FIG.2c

FIG.2d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V
VI
VII
VIII
pos
neg

FIG.3

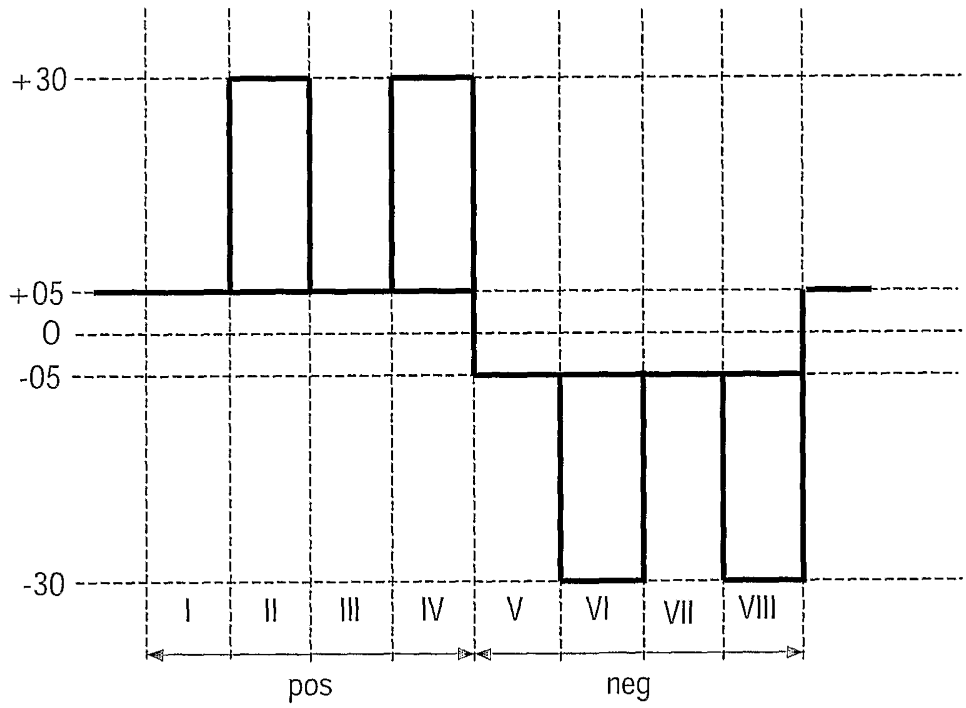
+30
+05
0
-05
-30
I
II
III
IV
V
VI
VII
VIII
pos
neg

FIG.4

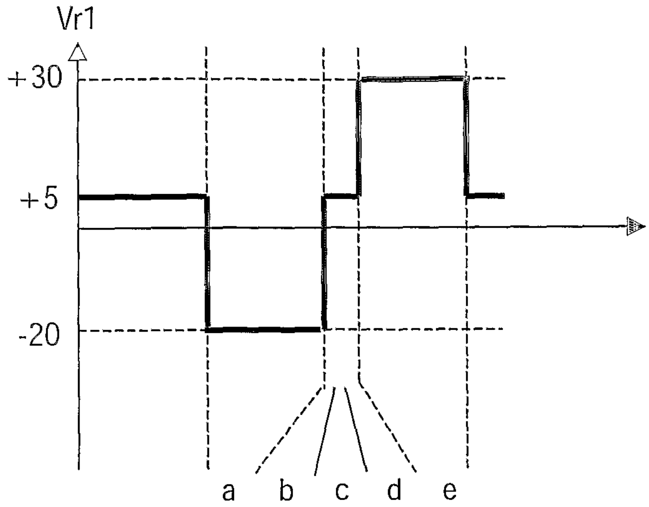

FIG.5

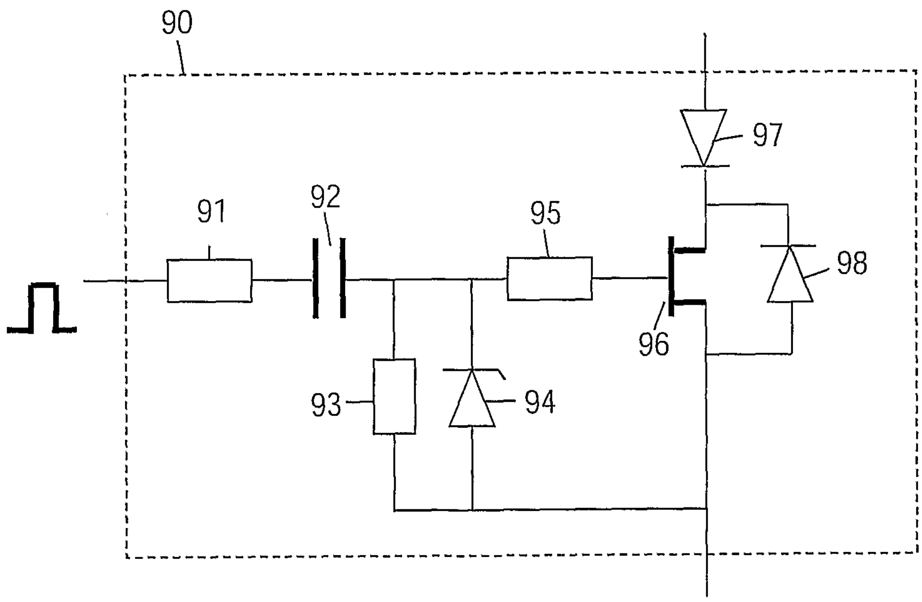

FIG.6