



- (51) **International Patent Classification:**
H01L 29/737 (2006.01) *H01L 21/336* (2006.01)
- (21) **International Application Number:**
PCT/US2013/057317
- (22) **International Filing Date:**
29 August 2013 (29.08.2013)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**
13/597,439 29 August 2012 (29.08.2012) US
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- (81) **Designated States** (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM,

AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

- (84) **Designated States** (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))
- as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))

Published:

- with international search report (Art. 21(3))

(54) **Title:** SEMICONDUCTOR DEVICE WITH JFET WIDTH DEFINED BY TRENCH ISOLATION

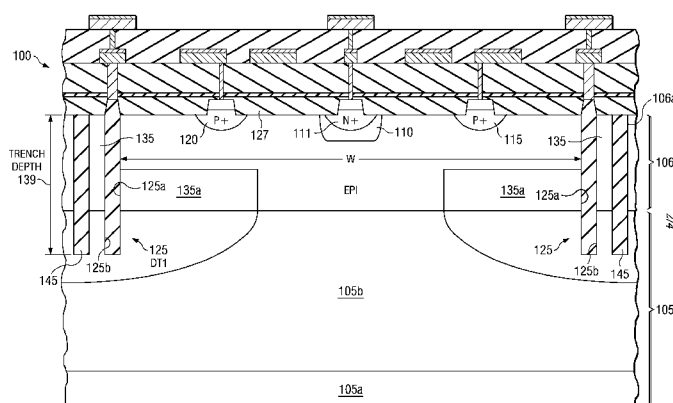


FIG. 1B

(57) **Abstract:** A semiconductor device having a junction field-effect transistor (JFET) (100) includes a substrate (105) having a first-type semiconductor surface (106) including a topside surface (106a), and a top gate (110) of a second-type formed in the semiconductor surface. A first-type drain (120) and a first-type source (115) are formed on opposing sides of the top gate. A first deep trench isolation region (125) has an inner first trench wall (125a) and an outer first trench wall (125b) surrounding the top gate, the drain and the source, and extends vertically to a deep trench depth (139) from the topside surface. A second-type sinker (135) formed in semiconductor surface extends laterally outside the outer first trench wall. The sinker extends vertically from the topside surface to a second-type deep portion which is both below the deep trench depth and laterally inside the inner first trench wall to provide a bottom gate.



SEMICONDUCTOR DEVICE WITH JFET WIDTH DEFINED BY TRENCH ISOLATION

[0001] This relates to semiconductor devices in general and in particular to such devices including junction field-effect transistors (JFETs).

BACKGROUND

[0002] A JFET is the simplest type of field-effect transistor (FET). In operation, to pinchoff the normally conducting channel of a JFET, a certain minimum gate-to-source reverse bias (V_{GS}) is applied to the gate and source junction. JFETs can include a heavily doped vertical sinker coupled to a bottom (or back) gate to improve performance of the JFET, including a lower pinchoff voltage and faster switching.

SUMMARY

[0003] This disclosure relates to improvements in integrated circuit semiconductor devices and processes for their manufacture. Disclosed embodiments include junction field-effect transistors (JFETs) having a width defined by an enclosing trench isolation region referred to herein as the "first deep trench isolation region". The JFET includes a substrate having a first-type semiconductor surface including a topside surface, and a top gate of a second-type formed in the semiconductor surface. A first-type drain and a first-type source are formed on opposing sides of the top gate. As used herein, the "first-type" and "second-type" refer to the doping type, where one of the types has n-type doping and the other type has p-type doping.

[0004] The first deep trench isolation region has an inner first trench wall and an outer first trench wall surrounding the top gate, the drain and the source, and extends vertically a deep trench depth from the topside surface. A second-type sinker formed in semiconductor surface includes a portion which extends laterally outside the outer first trench wall. The sinker extends vertically from the topside surface to a second-type deep portion which is both below the deep trench depth and extends laterally inside the inner first trench wall to provide a bottom gate for the JFET.

[0005] Disclosed JFETs can be used as a high voltage tolerant JFET in ICs, such as for analog ICs, and for non-destructive process monitoring purposes on an IC. Monitoring embodiments include monitoring the deep trench depth and the extent (length) of the lateral diffusion of the bottom gate out from the inner first trench wall.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] FIG. 1A is a depth enhanced top view depiction of an example JFET.

[0007] FIG. 1B is a cross-sectional depiction of the JFET of FIG. 1A.

[0008] FIG. 2 is a top view depiction of an example JFET having a bottom gate configured in a checkerboard layout.

[0009] FIG. 3 shows an example relation for drain to source current vs. JFET width (W) in μm that can be used to estimate the lateral diffusion of the deep n^+ (for a p-JFET) or deep p^+ (for an n-JFET) from the inner trench wall that provides the bottom gate for the JFET.

[0010] FIG. 4 shows a plot of diode breakdown voltage from an n^+ bottom gate to the p-semiconductor surface vs. trench depth (in μm) for a p-JFET that can be used to monitor the trench depth.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0011] FIGS. 1A - 1B illustrate an example JFET 100 which may be configured as a p-type JFET (p-JFET) or an n-type JFET (n-JFET). When JFET 100 is a p-JFET 100, first dopant type (the dopant type for the substrate surface and channel, source and drain) is p-type and the second dopant type (for the gate) is n-type. JFET 100 embodied as a p-JFET comprises a substrate 105 having a p-type semiconductor surface 106 including a topside surface 106a. When the JFET 100 comprises an n-JFET, the dopant types are simply reversed relative to a p-JFET.

[0012] The substrate 105 can comprise a bulk substrate, or include an epitaxial layer on a substrate. The substrate 105 can comprise silicon, silicon-germanium, or other substrate that provides a semiconductor surface 106.

[0013] Trench isolation 127 can comprise trench isolation such as shallow trench isolation (STI), or local oxidation (LOCOS). The top gate 110 shown comprises a n-type diffusion (n-well) formed in the semiconductor surface 106, having an n^+ contact 111 inside the top gate 110.

[0014] A drain 120 and source 115 both p^+ doped for a p-JFET are formed on opposing sides of the top gate 110 in the semiconductor surface 106. A first trench isolation region referred to herein as a first deep trench isolation (DT1) 125 includes an inner first trench wall

125a and an outer first trench wall 125b. DT1 125 is configured to enclose (or surround) the top gate 110, drain 120 and source 115, and extend vertically from the topside surface 106a to a deep trench depth 139 as shown in FIG. 1B, such as from 1.5 μm to 4 μm . The width of the JFET 100 shown as W is the space between the inner first trench walls 125a as shown in the x-direction. The length of the JFET 100 shown as L is also defined by the space between the inner first trench walls 125a as shown in the y-direction. DT1 125 thus defines the area of the JFET 100.

[0015] A sinker 135 doped n⁺ for the p-JFET is formed in semiconductor surface 106 laterally outside the outer first trench wall 125b. As shown in FIG. 1B the sinker 135 extends vertically from the topside surface 106a, and due to a high temperature diffusion (e.g., 1100 °C to 1200 °C drive) during processing diffuses out from the bottom of the DT1 125 into the semiconductor surface 106 to provide a second-type deep portion (bottom gate) 135a being n⁺ doped for the p-JFET, which is both below the deep trench depth 139 of the DT1 125 and laterally inside the inner first trench wall 125a.

[0016] An optional second deep trench isolation region 145 is shown positioned laterally outside the outer first trench wall 125b which also extends vertically to the trench depth 139. The sinker 135 is thus between the outer first trench wall 125b and the second deep trench isolation region 145. JFET 100 may be used for high voltage applications, such as for a 20 to 40 V application, and can be implemented in a trench isolated analog or Bipolar CMOS DMOS (BCD) process generally without any extra masks.

[0017] In FIG. 1B the substrate 105 is shown comprising a portion 105a doped p-type having a buried layer 105b doped n-type thereon for a p-JFET. The semiconductor surface 106 is shown as an epitaxial (epi) layer. There is an electrical contact shown to DT1 125. Although not shown, the DT1 125 can have a polysilicon filled center region which allows electrical contact thereto for optional biasing of DT1 125. Although there is an electrical contact provided to sinker 135 to provide contact to the bottom gate 135a, for simplicity, no contact is shown in FIG. 1A or FIG. 1B.

[0018] FIG. 2 depicts an example JFET 200 having a sinker 135 in a checkerboard layout. Having the sinker 135 in a checkerboard layout provides a checkerboard patterned bottom gate 135a after its formation following high temperature diffusion. The pinchoff voltage of the JFET 200 can be tuned by varying the layout pattern of the sinker 135 which then effects the layout of the bottom gate 135a. If the sinker 135 is discontinuous, such as in a checkerboard layout, the

amount of lateral diffusion of the bottom gate 135a will be reduced as compared to as continuous sinker 135 resulting in less diffusion to form the bottom gate 135a, which will function to raise the $|pinchoff\ voltage|$ of the JFET.

[0019] As noted above, besides being useful as JFETs within the functional circuitry on ICs, such as for performing the switching function, disclosed JFETs can also be used for non-destructive process monitoring. In one embodiment, described for p-JFETs, disclosed JFETs can be used to electrically monitor the extent (length) of lateral diffusion (length) of the bottom gate 135a measured from the inner first trench wall 125a. Known spreadsheet resistance measurements cannot provide the length of lateral diffusion of the bottom gate 135a from the inner first trench wall 125a.

[0020] In one embodiment, the source to drain current, I_{SD} , is used to estimate the length of the lateral diffusion of the bottom gate 135a from the inner first trench wall 125a. A relatively low voltage (e.g., $< |0.5V|$), can be used so that there is minimal depletion effects. The source to drain current decreases as the length of lateral diffusion of the bottom gate 135a from the inner first trench wall 125a increases, and the Inventors have recognized when two (2) times the lateral diffusion length approaches the width (W) of the JFET (as noted above W of the JFET 100 is the space between the inner first trench walls 125a of DT1 125 in the x-direction), pinchoff occurs (the bottom gate 135a shorts to the top gate 110), and as a result the source to drain current is reduced several orders of magnitude from its pre-pinchoff value (where a current path is present between source and drain) to a very low level. For example, FIG. 3 described below shows a p-JFET having a W of 4 μm pinches off when the lateral diffusion length is larger than 1.5 μm .

[0021] The term B_{vds} for a JFET refers to the breakdown voltage (defined at some predetermined current level, such as at 1 μa) between the drain and the source terminals, when the gate and the source terminals are shorted together. The B_{vds} value is generally between 20 and 50 volts. The Inventors have recognized for a given W, B_{vds} decreases as the length of lateral diffusion of the bottom gate 135a from the inner first trench wall 125a increases.

[0022] A calibration relation between source to drain current or B_{vds} for a disclosed JFET as a function of length of the lateral diffusion of the bottom gate 135a from the inner first trench wall 125a can be generated at a predetermined set of conditions including a bias condition. Empirical data is one way to generate this data, although simulation is also possible. For example, for the source to drain current embodiment, for an expected range of lateral diffusion of

1.5 to 2.5 μm , a plurality of disclosed JFETs having different W's can be provided, such as 2, 3, 4, 5 and 6 μm , and these devices are all measured after metallization. If the JFETs having W's of 2, 3 and 4 μm all have low source to drain current, while the JFETs having W's of 5 μm and 6 μm have high source to drain current, it can be concluded that the lateral diffusion of the bottom gate 135a from the inner first trench wall 125a in the final IC is from 1.5 μm to 2.0 μm .

[0023] For example, FIG. 3 shows an example relation for drain to source current vs. JFET W for a p-JFET (in μm). The discontinuity in current at about $W=4\mu\text{m}$ indicates the lateral diffusion of the bottom gate 135a from the inner first trench wall 125a is a bit larger than 1.5 μm . For $W < 4\mu\text{m}$, the drain to source current decreases abruptly (due to no longer a drain to source current path), since two times the lateral diffusion of the bottom gate 135a from the inner first trench wall 125a is about 3.5 μm to 4 μm .

[0024] In another monitoring embodiment, described for p-JFETs, a disclosed JFET can be used to electrically monitor the deep trench depth 139 of a deep trench. There is no inline tool or method available for monitoring deep trench depth known in the art. SEM cross-section analysis is the only known way to characterize deep trench depth, but is a destructive and time consuming process. This embodiment is based on the Inventor's recognition the breakdown voltage of the bottom gate 135a to the semiconductor surface 106 shown as epi in FIG. 1B correlates with the deep trench depth, because the curvature of bottom gate 135a near bottom of the DT1 125 increases with increasing deep trench depth. As known in device physics, junction curvatures enhance the electric field in the curved parts of the associated depletion regions, and the enhanced electric field reduces the breakdown voltage below that predicted by one-dimensional junction theory.

[0025] Calibration data for the breakdown voltage from the bottom gate 135a to the semiconductor surface 106 shown as epi in FIG. 1B as a function of deep trench depth can be obtained by obtaining breakdown voltage on test JFETs, and then directly measuring the corresponding deep trench depth, such as using SEM cross section analysis. This allows a calibration relation to be generated and stored. Upon completion of the process steps to form an IC including metallization, the breakdown voltage from the bottom gate 135a to the semiconductor surface 106 can be measured, and the calibration relation used to determine the deep trench depth. The deep trench depth can thus be estimated electrically and statistical results can be obtained by using a plurality of JFETs. For example, by placement of disclosed JFETs

spread across the area of a wafer, a full wafer map can be obtained to evaluate deep trench depth uniformity across the wafer.

[0026] FIG. 4 shows a plot of diode breakdown voltage from the bottom gate 135a doped n⁺ to the semiconductor surface 106 doped p- vs. trench depth (in μm) for a p-JFET. The breakdown voltage can be seen to decrease from about 42 V to about 34V as the trench depth increases from 2.1 μm to 2.9 μm , since the curvature of bottom gate 135a near bottom of the DT1 125 increases with increasing trench depth.

[0027] Disclosed embodiments can be integrated into a variety of assembly flows to form a variety of different semiconductor integrated circuit (IC) devices and related products. The assembly can comprise single semiconductor die or multiple semiconductor die, such as PoP configurations comprising a plurality of stacked semiconductor die. A variety of package substrates may be used. The semiconductor die may include various elements therein and/or layers thereon, including barrier layers, dielectric layers, device structures, active elements and passive elements including source regions, drain regions, bit lines, bases, emitters, collectors, conductive lines, conductive vias, etc. Moreover, the semiconductor die can be formed from a variety of processes including bipolar, CMOS, DMOS, BiCMOS and MEMS.

[0028] Those skilled in the art to which this disclosure relates will appreciate that many other embodiments and variations of embodiments are possible within the scope of the claimed invention..

CLAIMS

What is claimed is:

1. A semiconductor device including a junction field-effect transistor (JFET), comprising:
 - a substrate having a first-type semiconductor surface (semiconductor surface) including a topside surface;
 - a top gate comprising a second-type formed in the semiconductor surface;
 - a first-type drain and a first-type source formed on opposing sides of the top gate in the semiconductor surface;
 - a first deep trench isolation region having an inner first trench wall and an outer first trench wall surrounding the top gate, the drain and the source and extending vertically to a deep trench depth from the topside surface;
 - a second-type sinker formed in the semiconductor surface laterally outside the outer first trench wall, the sinker extending vertically from the topside surface to a second-type deep portion which is both below the deep trench depth and extends laterally inside the inner first trench wall to provide a bottom gate.
2. The device of claim 1, further comprising a second deep trench isolation region positioned laterally outside the outer first trench wall extending vertically to the deep trench depth, wherein the sinker is between the outer first trench wall the second deep trench isolation region.
3. The device of claim 1, wherein the deep portion is in a discontinuous pattern.
4. The device of claim 1, wherein the JFET comprises a p-JFET.
5. The device of claim 1, wherein the JFET comprises an n-JFET.
6. The device of claim 1, further comprising shallow trench isolation (STI) within the inner first trench wall surrounding the top gate, the source, and the drain.
7. A method of forming a semiconductor device including a junction field-effect transistor (JFET), comprising:
 - providing a substrate having a first-type semiconductor surface (semiconductor surface) including a topside surface;
 - forming a top gate comprising a second-type in the semiconductor surface;

forming a first-type drain and a first-type source on opposing sides of the top gate in the semiconductor surface;

forming a first deep trench isolation region having an inner first trench wall and an outer first trench wall surrounding the top gate, the drain and the source and extending vertically to a deep trench depth from the topside surface, and

forming a second-type sinker in the semiconductor surface laterally outside the outer first trench wall, the sinker extending vertically from the topside surface to a second-type deep portion which is both below the deep trench depth and laterally inside the inner first trench wall to provide a bottom gate.

8. The method of claim 7, wherein the deep portion is in a discontinuous pattern.

9. The method of claim 7, further comprising forming a second deep trench isolation region positioned laterally outside the outer first trench wall extending vertically to the deep trench depth, wherein the sinker is between the outer first trench wall and the second deep trench isolation region.

10. The method of claim 7, further comprising forming shallow trench isolation (STI) within the inner first trench wall, wherein the STI surrounds the top gate, the source, and the drain.

11. A method of using junction field-effect transistors (JFETs) to determine a lateral diffusion length out from trench isolation, comprising:

measuring electrical data comprising current from a source to a drain (source to drain current) or a breakdown voltage between the drain and the source (B_{vdss}) for at least one JFET formed on an integrated circuit (IC) including a substrate having a first-type semiconductor surface (semiconductor surface) including a topside surface, the JFET including:

a top gate comprising a second-type formed in the semiconductor surface;

the source and the drain being first-type formed on opposing sides of the top gate in the semiconductor surface;

a first deep trench isolation region having an inner first trench wall and an outer first trench wall surrounding the top gate, the source and the drain and extending vertically a deep trench depth from the topside surface; and

a second-type sinker formed in the semiconductor surface laterally outside the outer first trench wall, the sinker extending vertically from the topside surface to a second-

type deep portion which is both below the deep trench depth and extends laterally inside the inner first trench wall to provide a bottom gate, and

determining a length of a lateral diffusion of the bottom gate relative to the inner first trench wall from the electrical data using stored characterization data.

12. The method of claim 11, wherein the electrical data comprises the source to drain current and the stored characterization data comprises the source to drain current as a function of spacing between the inner first trench wall which defines a width for the JFET.

13. The method of claim 11, wherein the electrical data comprises the Bvdss and the stored characterization data comprises the Bvdss versus the length of the lateral diffusion of the bottom gate relative to the inner first trench wall.

14. A method of using junction field-effect transistors (JFETs) to monitor trench depth, comprising:

measuring electrical data comprising a breakdown voltage between a bottom gate and a first-type semiconductor surface (semiconductor surface) for at least one JFET formed on an integrated circuit (IC) including a substrate having the semiconductor surface including a topside surface, the JFET including:

a top gate comprising a second-type formed in the semiconductor surface;

a source and a drain being first-type formed on opposing sides of the top gate in the semiconductor surface;

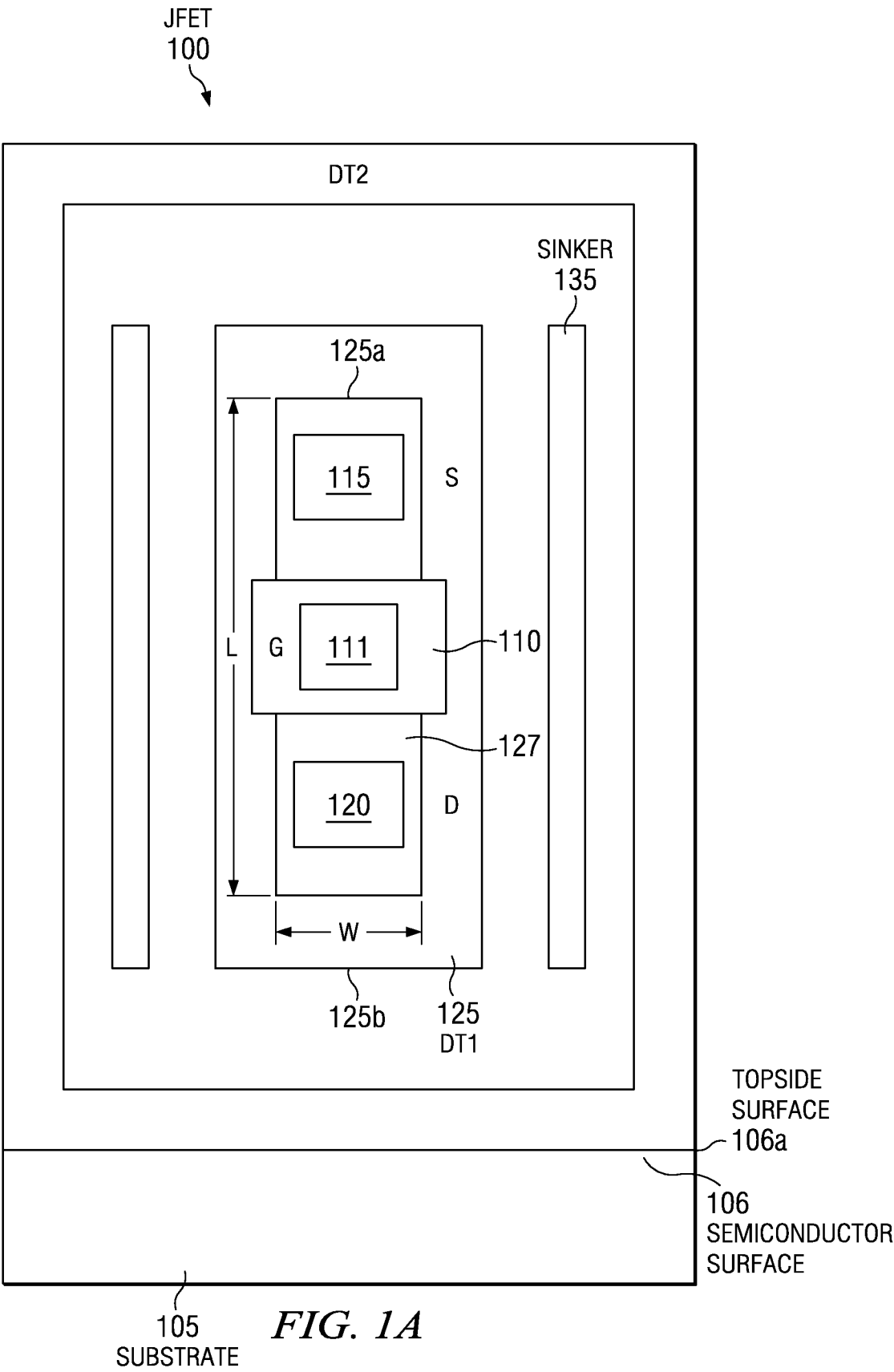
a first deep trench isolation region having an inner first trench wall and an outer first trench wall surrounding the top gate, the source and the drain extending vertically a deep trench depth from the topside surface; and

a second-type sinker formed in the semiconductor surface laterally outside the outer first trench wall, the sinker extending vertically from the topside surface to a second-type deep portion which is both below the deep trench depth and extends laterally inside the inner first trench wall to provide the bottom gate, and

determining the deep trench depth using stored characterization data relating the breakdown voltage between the bottom gate and the semiconductor surface and the deep trench depth.

15. The method of claim 14, wherein the substrate comprises a wafer and the at least one JFET comprises a plurality of the JFETs spread across an area of the wafer; and further

comprising generating a wafer map which evaluates a uniformity of the deep trench depth across the wafer.



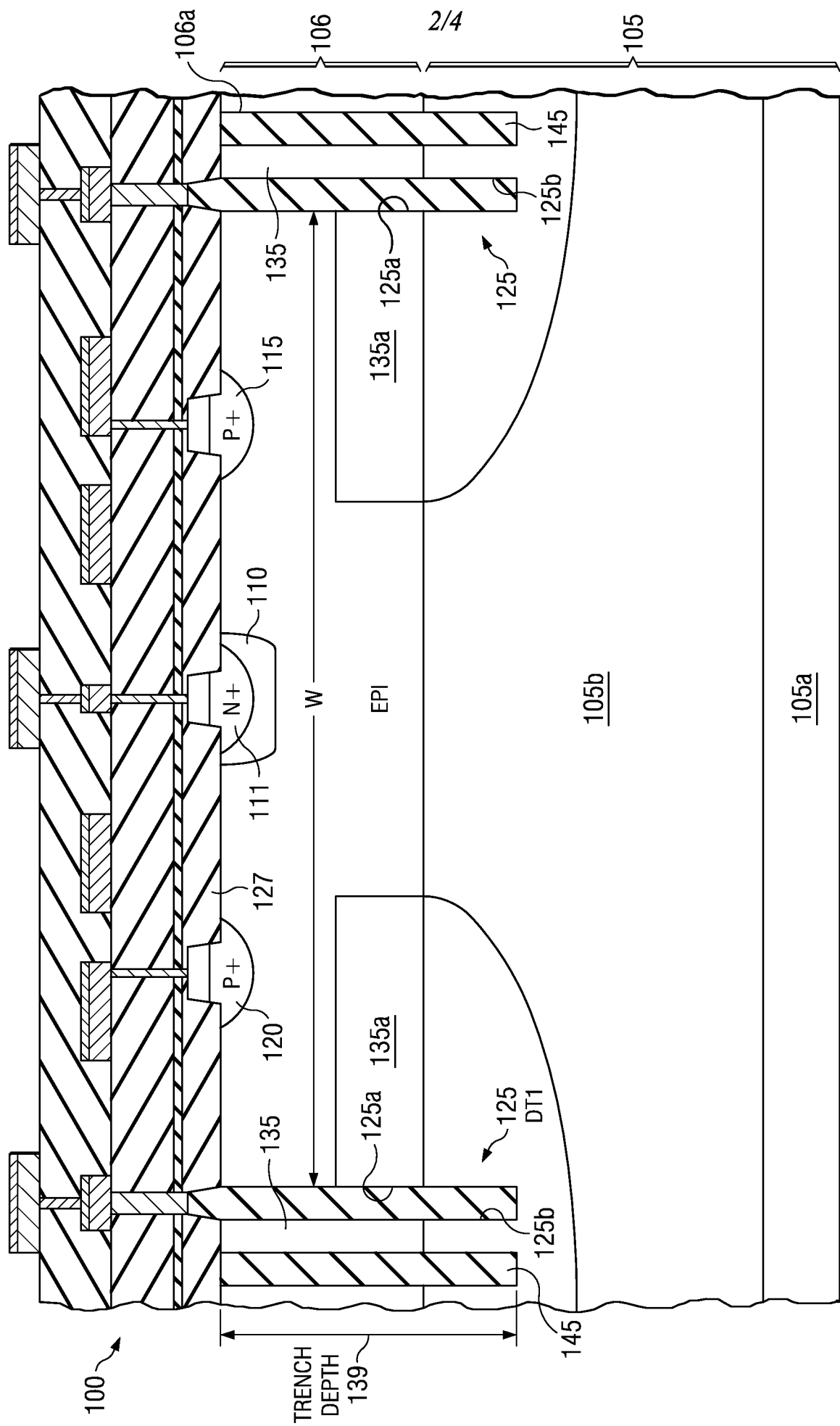
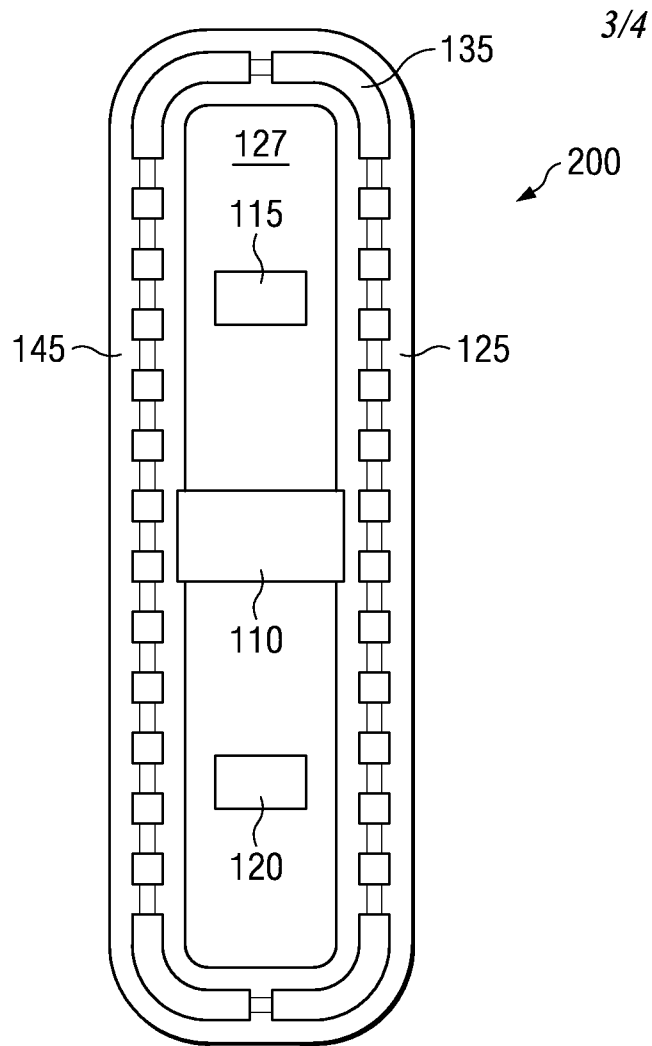
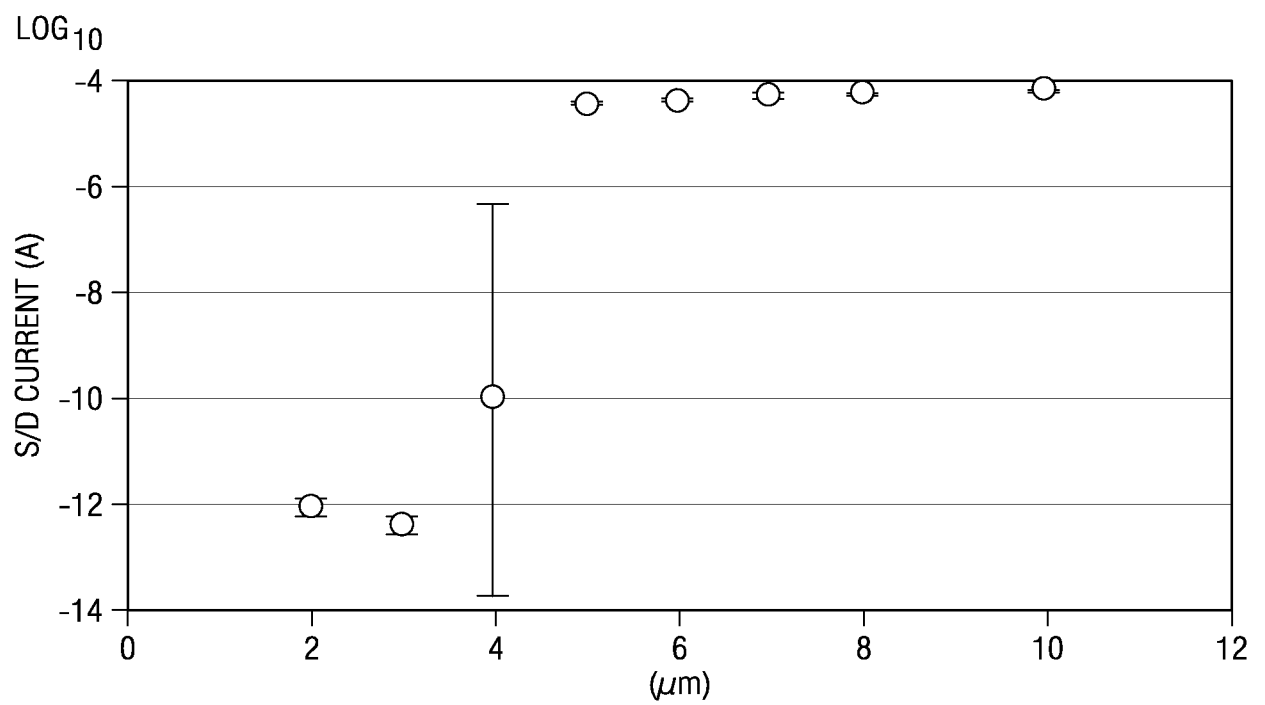
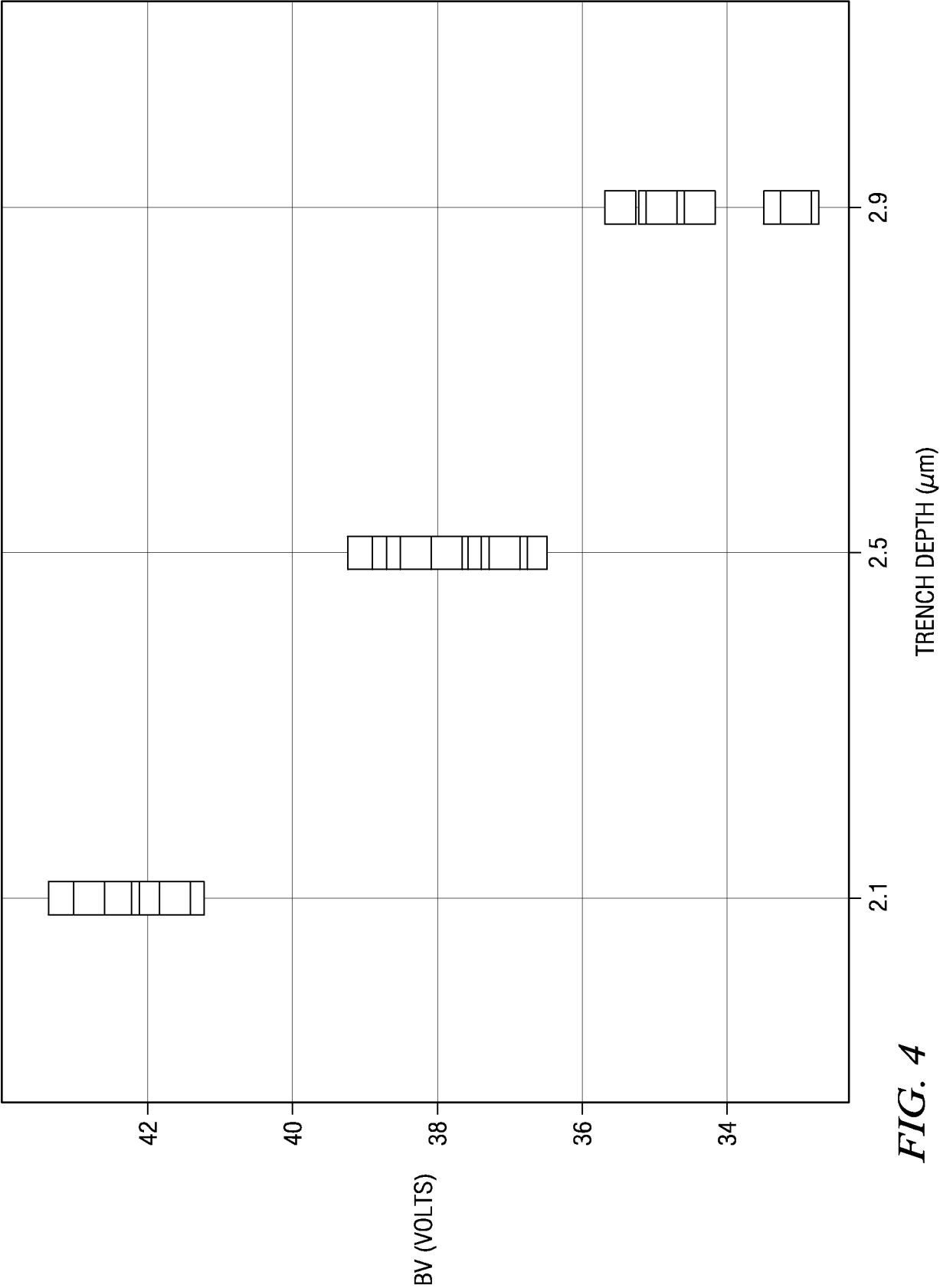


FIG. 1B

*FIG. 2**FIG. 3*



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/057317**A. CLASSIFICATION OF SUBJECT MATTER****H01L 29/737(2006.01)i, H01L 21/336(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 29/737; H01L 29/778; H01L 29/00; H01L 29/80; H01L 21/337; H01L 21/336

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: JFET (junction field effect transistor), deep trench isolation, sinker, top gate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A		11–15
A	US 2010-0032731 A1 (JEFFREY A. BABCOCK et al.) 11 February 2010 See paragraph [0037]–[0039]; claims 1–9; and figures 1–3B.	1–15
A	US 2008-0272395 A1 (SRINIVASA R. BANNA) 06 November 2008 See paragraph [0058]–[0069]; and figures 3–4B.	1–15
A	US 2006-0071247 A1 (KALYUAN CHEN et al.) 06 April 2006 See paragraphs [0023]–[0032]; and figures 2A–2B.	1–15
A	US 2008-0237656 A1 (RICHARD K. WILLIAMS et al.) 02 October 2008 See paragraphs [0171]–[0176]; and figures 7A–7B	1–15



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

11 December 2013 (11.12.2013)

Date of mailing of the international search report

11 December 2013 (11.12.2013)

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2013/057317

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