



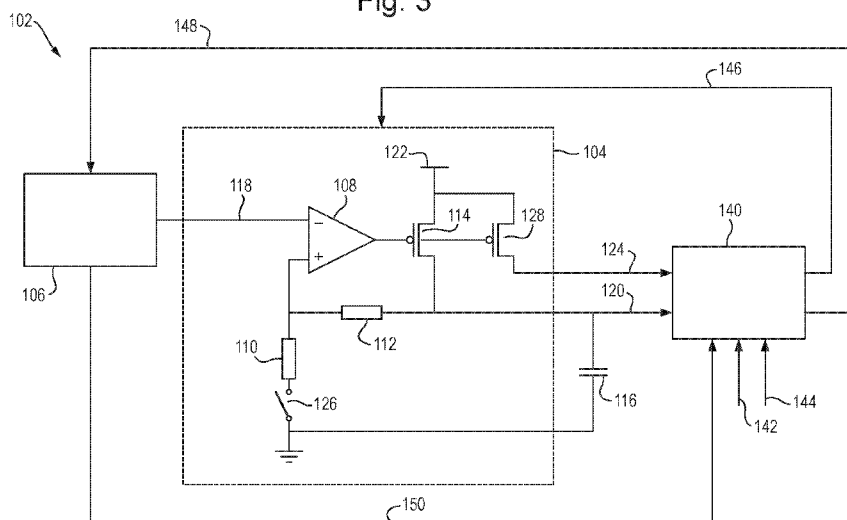
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(54) **Title:** VOLTAGE REGULATORS**Fig. 3**

(57) **Abstract:** A voltage regulator (102) includes a first portion comprising a low-dropout (LDO) regulator (104); and a second portion comprising an energy storage device (116). The voltage regulator is arranged to: a) power up the LDO regulator at least until an output voltage (120) thereof reaches a predetermined value; b) charge the energy storage device while the LDO regulator is powered up; c) power down the LDO regulator; d) provide a current to a load by discharging the energy storage device while the LDO regulator is powered down; e) detect when the output voltage has dropped by a predetermined amount; and f) power up the LDO regulator again.

Voltage Regulators

5 The present invention relates to voltage regulators, particularly low-dropout voltage regulators.

Low-dropout (or LDO) voltage regulators are linear DC voltage regulators that are capable of operating with very low input-output differential voltages. The advantages of such regulators with respect to other types of voltage regulators include having a lower minimum operating voltage, higher power efficiency and lower heat dissipation.

15 In typical LDO voltage regulators, it is often the case that the power efficiency is significantly lower when the regulator is providing very small load currents. This renders such devices sub-optimal for applications in which current consumption is highly important, such as in battery powered devices wherein high current consumption could potentially lead to dramatic shortening of battery life.

20 The present invention seeks to provide an improved approach to designing and implementing low-dropout voltage regulators in terms of power efficiency at low load currents.

When viewed from a first aspect, the present invention provides a method of operating a voltage regulator including a first portion comprising a low-dropout (LDO) regulator; and a second portion comprising an energy storage device comprising:

- a) powering up the LDO regulator at least until an output voltage thereof reaches a predetermined value;
- b) charging the energy storage device while the LDO regulator is powered up;
- c) powering down the LDO regulator;
- d) providing a current to a load by discharging the energy storage device while the LDO regulator is powered down;
- e) detecting when the output voltage has dropped by a predetermined amount; and

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f) powering up the LDO regulator again.

When viewed from a second aspect, the present invention provides a voltage regulator including a first portion comprising a low-dropout (LDO) regulator; and a
5 second portion comprising an energy storage device, wherein said voltage regulator is arranged to:

a) power up the LDO regulator at least until an output voltage thereof reaches a predetermined value;

b) charge the energy storage device while the LDO regulator is powered up;

10 c) power down the LDO regulator;

d) provide a current to a load by discharging the energy storage device while the LDO regulator is powered down;

e) detect when the output voltage has dropped by a predetermined amount; and

15 f) power up the LDO regulator again.

Thus it will be seen that in accordance with the invention, the LDO regulator can operate in a pulsed mode of operation, in which the LDO regulator is only powered for pulsed time intervals rather than being powered continuously. Preferably steps
20 b) to f) of the sequence set out above are carried out repeatedly. This has been found to provide significant improvements in power efficiency for low load currents over LDO regulators known in the art.

In a set of embodiments, the LDO regulator comprises one or more selected from
25 the group comprising: an error amplifier, an output driver transistor, a feedback divider and a decoupling capacitor.

There are a number of possible ways of checking whether the output voltage of the LDO regulator has reached the predetermined value, however, in a set of
30 embodiments, the predetermined value is provided by an output voltage of a third portion comprising a voltage reference circuit. In a particular set of embodiments, the voltage reference circuit comprises a bandgap circuit. The Applicant has appreciated that in some such embodiments it is advantageous also to operate the voltage reference circuit in a pulsed mode of operation, such that the voltage

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reference circuit is selectively powered depending on the output voltage of the LDO regulator.

5 The LDO regulator and voltage reference circuit could be powered on simultaneously, but in a set of embodiments, the voltage reference circuit is powered on first. The delay between the voltage reference circuit and LDO regulator being powered on could be predetermined, but in a further set of
10 embodiments, the LDO regulator is only powered on when the output voltage of the reference voltage circuit has been determined to be stable – for example by having a variation below a threshold amount. This ensures that the output of the voltage reference circuit is relatively constant and is not in a transient state.

While it is possible to start the LDO regulator at any voltage, it may be difficult to get it to reach the desired amplitude if not properly initialised. In a set of embodiments,
15 the output voltage of the LDO regulator is initialised to the output voltage that would be obtained if the LDO regulator were operated in continuous mode. This ensures that the output voltage falls and rises to the correct value.

In order to provide an output voltage from the regulator continuously even when the
20 LDO regulator and voltage reference circuits are powered down, current is provided to the load by discharging an energy storage device. In a set of embodiments, the energy storage device comprises a capacitor.

Operating an LDO regulator in a pulsed mode will inevitably lead to a ripple on the
25 output voltage. However, the present invention may, at least in some embodiments, advantageously provide a pulse period (time between 'on' pulses) that is responsive to load current, thus reducing the level of ripple on the output voltage over a wide range of load currents. Advantageously, the level of ripple may be substantially the same over a wide range of load currents.

30 When the voltage supplied by the energy storage device has dropped by a pre-determined amount, the LDO regulator and optionally the voltage reference circuit are powered on again and recharge the energy storage device. It or they could be powered on for a fixed time but in a set of embodiments the LDO regulator is
35 powered on again until the output voltage has reached an operating value which

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may be the predetermined level. The pulse length may therefore be responsive to variations in load since the LDO regulator is only powered up for as long as it takes to recharge the energy storage device. The pulse length will, in general, also depend on the actual capacitance value, operating temperature, and silicon process parameters such as transistor threshold voltage.

In a set of embodiments, the level of charge on the energy storage device is determined by sensing an output current flowing through the first portion in order to charge said energy storage device. Thus it will be appreciated by a person skilled in the art that the LDO regulator may be switched off when the energy storage device reaches a certain level of charge without needing to measure the voltage across the energy storage device directly.

In some embodiments a mirror transistor arranged to generate a sensing current that is smaller than and related to the output current through an output transistor. In a set of embodiments a sensing current is measured, the sensing current is a fixed fraction of the output current. This may be achieved by using transistors of different physical sizes (e.g. different transistor widths and/or lengths) and thus in a set of embodiments, the sensing current may be determined by a ratio of transistor sizes.

When the voltage supplied by the energy storage device has dropped by a predetermined amount, the LDO regulator and optionally the voltage regulator are powered on again. In a set of embodiments, the voltage regulator arrangement comprises a fourth portion comprising a control circuit that determines powering up and powering down operations of the LDO regulator and/or the voltage reference circuit. In a set of embodiments, the control circuit is arranged to: monitor the output voltage of the LDO regulator; monitor the current flowing through the LDO regulator (which corresponds to the sum of the currents through the energy storage device and the load); determine whether to power up the LDO regulator; and produce an LDO power up signal. Additionally or alternatively, the control circuit may be further arranged to determine whether to power down the LDO regulator; and produce an LDO power down signal.

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In a set of embodiments, the control circuit comprises a voltage monitor circuit for determining when a monitored voltage has fallen below a threshold, the voltage monitor circuit comprising:

- a monitored voltage input;
- 5 a reference capacitor arranged to be able to store a value of the monitored voltage as a reference capacitor voltage;
- a timeout capacitor arranged to be able to store a value of the monitored voltage as a timeout capacitor voltage, said timeout capacitor undergoing a higher leakage than said reference capacitor; and
- 10 a comparator arranged to:
 - compare the monitored voltage to the reference capacitor voltage;
 - compare the timeout capacitor voltage to the reference capacitor voltage; and
 - produce a logic signal on an output of the comparator based on said
- 15 comparisons, said logic signal having a first logic value at least if the reference capacitor voltage is lower than or equal to both the monitored voltage and the timeout capacitor voltage.

It will be appreciated by those skilled in the art that, by storing a value of the LDO regulator output voltage at a particular time as the reference capacitor voltage and subsequently comparing the value of the LDO regulator output voltage to the reference capacitor voltage, the voltage monitor can detect changes in the level of the regulator output. By giving the timeout capacitor a higher leakage rate than the reference capacitor, a time limit is set, such that if the LDO regulator output voltage has not dropped below the reference capacitor voltage in an appropriate amount of time, the timeout capacitor voltage will have, thus causing the comparator to give the predetermined output by some point in time, which may obviate the effects of drift if the output of the LDO regulator is only falling slowly.

30 In some embodiments, the output logic signal could have a second logic value as soon as the monitored voltage or the timeout capacitor voltage drops below the reference capacitor voltage. However, in a set of embodiments, the comparator is arranged such that the logic signal has a second logic value once the monitored voltage or the timeout capacitor voltage drops below the reference capacitor

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voltage by an offset voltage. This allows the voltage monitor circuit to allow for a ripple on the LDO regulator output voltage.

There are a number of comparators that could provide the functionality outlined above. However, in an advantageous set of embodiments, the comparator comprises:

a first portion including a first transistor with a gate terminal connected to the reference capacitor;

a second portion in parallel with the first portion including a second transistor with a gate terminal connected to the monitored voltage and a third transistor with a gate terminal connected to the timeout capacitor, wherein said second and third transistors are in series; and

a bistable portion connected to said first and second portions and arranged to produce said logic signal.

Such a comparator can advantageously compare the reference capacitor voltage to both the LDO regulator output and timeout capacitor voltages simultaneously. Current will typically flow asymmetrically through the first and second portions. More current will flow through the portion which is connected to the highest voltage at any given time. The bistable portion then causes the output of the comparator to saturate to either logic high or logic low. By "stacking" transistor pairs, multiple comparisons may be made within the same comparator. This advantageous arrangement can provide a significant reduction in power consumption compared to conventional arrangements using multiple comparators and Boolean logic gates. In some circumstances a reduction of 50% could be achieved.

The control circuit described hereinabove can be used to provide power selectively to the LDO regulator. However, the principle can also apply to operating the voltage reference circuit. Thus, in some sets of embodiments, the control circuit is further arranged to determine whether to power up the voltage reference circuit; and produce a voltage reference power up signal. Additionally or alternatively, the control circuit may be arranged to determine whether to power down the voltage reference circuit; and produce a voltage reference power down signal.

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In some embodiments, the voltage regulator has a selectable mode of operation in which the voltage reference circuit is powered continuously. Additionally or alternatively the voltage regulator has a selectable mode of operation in which the LDO regulator is powered continuously.

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Thus it will be appreciated by a person skilled in the art that the present invention provides a method, and a low-dropout voltage regulator and voltage reference circuit that provide a target power efficiency at a given load current, particularly relatively low load currents, by using a pulse mode of operation.

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An embodiment of the invention will now be described, by way of example only, with reference to the accompanying drawings in which:

Fig. 1 is a schematic diagram of a typical known LDO regulator circuit shown for reference purposes only;

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Fig. 2 is a graph of the load current dependent power efficiency of a typical LDO regulator circuit;

Fig. 3 is a schematic diagram of an LDO regulator circuit in accordance with an embodiment of the invention;

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Fig. 4 is a schematic diagram of a control circuit in accordance with the embodiment of Fig. 3;

Fig. 5 is a timing diagram illustrating the operation of the same embodiment of the invention;

Fig. 6 is a graph demonstrating a typical output voltage ripple associated with the use of embodiments of the invention;

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Fig. 7 is a graph of the current-dependent power efficiency of an embodiment of the invention compared to that of a typical LDO regulator circuit;

Fig. 8 is a circuit diagram of a voltage monitor suitable for use with the LDO regulator embodiment of Fig. 3;

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Fig. 9 is a circuit diagram of a three-input comparator suitable for use in the voltage monitor of Fig. 8;

Fig. 10 is a timing diagram showing the relationship between the inputs and the output of the three-input comparator of Fig. 9; and

Fig. 11 is a timing diagram showing the advantage of the timeout capacitor of the voltage monitor of Fig. 8.

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A conventional LDO regulator circuit and associated bandgap circuit are shown in Fig. 1. The LDO regulator and associated bandgap circuit 2 are composed of two sections, the LDO regulator 4 itself, and a bandgap circuit 6 arranged to provide a stable reference voltage 18. The bandgap reference circuit operates by using a voltage difference between two p-n junctions operated at different current densities to produce an output voltage with low temperature dependence. A person skilled in the art will appreciate that a number of such bandgap reference circuits are known in the art, but an exemplary circuit is a Brokaw reference circuit.

The LDO regulator 4 comprises an error amplifier 8, a p-type metal-oxide semiconductor (PMOS) output driver 14, a feedback divider 10 and 12, and a decoupling capacitor 16. The error amplifier 8 monitors the difference between the reference voltage 18 from the bandgap circuit 6 and a voltage proportional (based on the ratio of feedback resistors 10 and 12) to the output voltage 20 and causes the PMOS output driver 14 to drive the output voltage 20 toward a constant output voltage (V_{OUT}) that can be approximated as shown in Equation 1, wherein R_1 and R_2 are the resistances of feedback divider resistors 10, 12 respectively.

$$V_{OUT} = V_{BG} \cdot \left(1 + \frac{R_2}{R_1}\right)$$

Equation 1

The reference voltage (V_{BG}) 18 is provided by the bandgap circuit 2. The supply current 24 that is drawn from the input supply (VDD) 22 can be expressed as per Equation 2, wherein I_1 and I_2 correspond to currents 26 and 28 respectively, I_{DDQ} is a quiescent current and I_{OUT} is the output current 30.

$$I_{DD} = I_{OUT} + \frac{V_{OUT}}{R_1 + R_2} + I_1 + I_2 = I_{OUT} + I_{DDQ}$$

Equation 2

The power efficiency of the circuit is then defined by Equation 3.

$$\eta = \frac{P_{OUT}}{P_{DD}} = \frac{V_{OUT} I_{OUT}}{V_{DD} I_{DD}} = \frac{V_{OUT} I_{OUT}}{V_{DD} (I_{OUT} + I_{DDQ})}$$

Equation 3

A graph showing the relationship between power efficiency and load current is shown in Fig. 2. It is clearly seen that for smaller load currents, the power efficiency rapidly declines. When the power efficiency is low, more power is being drawn by the circuit than is being delivered to the load, with the difference being dissipated as heat.

An embodiment of the present invention is shown in Fig. 3. The circuit 102 comprises three sections: an LDO regulator 104, a bandgap circuit 106, and a control circuit 140. The LDO regulator 104 comprises an error amplifier 108, PMOS output drivers 114 and 128, a feedback divider 110 and 112, a decoupling capacitor 116, and a power up switch 126. The error amplifier 108 monitors the difference between a reference voltage 118 from the bandgap circuit 106 and a voltage proportional to the output voltage 120, the proportion being determined by the ratio of feedback resistors 110 and 112. The error amplifier 108 causes a PMOS output driver 114 to drive the output voltage 120 toward a constant output voltage (V_{OUT}) that can be approximated by the expression of Equation 1 above. The output voltage 120 is a first input to the control circuit 140.

Rather than monitoring the output current through the PMOS output driver 114, the control circuit 140 is arranged to monitor the current through a second PMOS output driver 128 that is physically N times smaller (in this example 1000 times smaller) than the first. This second PMOS output driver generates a small current I_{SENSE} 124 that is approximately N times smaller than the current through the first PMOS output driver 114 (in this case 1000 times smaller). As it is proportional to the current through the first PMOS output driver 114, I_{SENSE} provides an indication of the level of charge on the decoupling capacitor 116 while minimising the input current provided to the control circuit 140.

The circuit 102 improves power efficiency by operating the LDO regulator 104 and bandgap circuit 106 in a pulsed mode, rather than having them powered up continuously as will now be explained. A decoupling capacitor 116 serves as an energy storage device when the LDO regulator 104 is powered down, supplying current to the load. The output voltage V_{OUT} 120 drops gradually as the charge on the decoupling capacitor 116 is being depleted. When V_{OUT} has dropped by a predefined amount, the LDO regulator 104 and bandgap circuit 106 are powered up

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to replenish charge on the decoupling capacitor 116, and then powered down again as soon as the charging of the decoupling capacitor 116 has been completed. As the current I_{SENSE} 124 drops to a minimal value once the capacitor 116 is fully charged, this provides an indication of the level of charge on the capacitor without measuring it directly.

In an exemplary implementation, the pulse length (duration of power-up) is around $3\ \mu\text{s}$, and does not depend on load current. The pulse period scales inversely with load current since a higher load current means that the capacitor 116 will be depleted more quickly, ranging from around 100 ms at zero load, to around $100\ \mu\text{s}$ at 1mA load. At higher load currents the system may switch to a continuous mode of operation.

The quiescent current is around 0.1 mA when LDO regulator 104 and bandgap circuit 106 are powered up, but drops to around $0.1\ \mu\text{A}$ when they are powered down. In effect, I_{DDQ} in Equation 3 can be replaced with a time-averaged current that scales with I_{LOAD} . This results in much improved power efficiency at low load currents.

The control circuit 140 has inputs for three more signals:

PWRUP_MBIAS_IN 142, a logic signal for enforcing a continuous mode of operation for the bandgap circuit 106;

PWRUP_VREG_IN 144, a logic signal for enforcing a continuous mode of operation for the LDO regulator 104; and

MBIAS_READY 150, a logic signal that indicates if the V_{BG} voltage 118 is valid.

The control circuit 140 also has two outputs:

PWRUP_MBIAS 148, a logic signal for powering up the bandgap circuit 106; and

PWRUP_VREG 146, a logic signal for powering up the LDO regulator 104.

An example embodiment of a control circuit 140 is shown in greater detail in Fig. 4. The control circuit 140 comprises a V_{OUT} monitor 160, an I_{SENSE} monitor 162, an S-R latch 164, logic OR gates 166 and 168, and a logic AND gate 170.

In this particular embodiment it is assumed in the following that both PWRUP_VREG_IN 144 and PWRUP_MBIAS_IN 142 are 'low', i.e. that both LDO regulator 104 and bandgap circuit 106 are operated in pulsed mode.

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Initially, V_{OUT} 120 is initialised to the voltage level given by Equation 1, and the S-R latch 164 is "reset" so that the intermediate logic signal REFRESH 172 is set to '0'. PWRUP_MBIAS 148 and PWRUP_VREG 146 will then be '0' due to the OR logic gates 168 and 166 and the AND logic gate 170, and thus both LDO regulator 104 and bandgap circuit 106 are then powered down.

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V_{OUT} 120 is high impedance when the LDO regulator 104 is powered down. Load current I_{OUT} will then gradually deplete the charge that is held on decoupling capacitor 116, causing V_{OUT} 120 to drop at a rate as per Equation 4.

15

$$\frac{dV_{OUT}}{dt} = \frac{I_{OUT}}{C}$$

Equation 4

In this example, the capacitance of the decoupling capacitor 116 is $C=1\ \mu\text{F}$. The drop rate is then $1\ \text{mV}/\mu\text{s}$ per mA of load current. The V_{OUT} monitor circuit 160 detects when V_{OUT} 120 has dropped by a predetermined amount relative to the level in Equation 1. When this drop in V_{OUT} 120 is detected by V_{OUT} monitor circuit 160, the SET line 174 is pulsed 'high', which "sets" the S-R latch 164 so that REFRESH='1'. Subsequently, PWRUP_MBIAS 148 goes 'high', powering up the bandgap circuit 106. The structure and operation of V_{OUT} monitor circuit 160 is described in greater detail with reference to Figs. 8 to 11.

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The bandgap circuit 106 will set MBIAS_READY 150 'high' after a short delay, once the V_{BG} voltage 118 has stabilized. After stabilization, PWRUP_VREG 146 goes 'high', powering up the LDO regulator 104.

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PMOS output driver 114 conducts a relatively large current while the LDO regulator 104 is charging decoupling capacitor 116. When V_{OUT} reaches the voltage level in

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Equation 1 the current drops rapidly. The I_{SENSE} monitor circuit 162 detects this drop by comparing the I_{SENSE} current 124 against a predetermined threshold level.

When I_{SENSE} 124 drops below the threshold, the RESET line 176 is pulsed 'high',
 5 resetting the S-R latch 164 so that REFRESH='0'. This subsequently causes PWRUP_MBIAS 148 and PWRUP_VREG 146 to change back to '0', powering down LDO regulator 104 and bandgap circuit 106.

This sequence repeats with a period dependent on I_{OUT} and the capacitance C of
 10 decoupling capacitor 116. With this implementation, the control circuit 140 consumes around $0.1 \mu\text{A}$ when REFRESH='0' and around $10 \mu\text{A}$ when REFRESH='1'.

Fig. 5 shows a timing diagram of the periodic signals associated with the pulsed
 15 mode of operation of a typical embodiment of the invention. The time between the start of the SET pulse 174 that powers on the LDO regulator 104 and bandgap circuit 106 begins the charging of decoupling capacitor 116 and the start of the RESET pulse 176 that powers down the LDO regulator 104 and bandgap circuit 106 once the capacitor is recharged is the charge time, T_{charge} , and in this
 20 implementation is typically around $3 \mu\text{s}$. The time between the start of adjacent SET pulses is the cycle time or period, T_{cycle} , and depends on load current and the capacitance of decoupling capacitor 116. The waveforms associated with logic signals REFRESH 172, PWRUP_MBIAS 148, MBIAS_READY 150, PWRUP_VREG 146, V_{OUT} 120, and I_{SENSE} 124 are shown and correspond to the
 25 periodic sequence as described previously.

The V_{OUT} waveform shown in Fig. 5 can be seen in greater detail in Fig. 6. The difference between the maximal and minimal output voltages, V_{max} and V_{min} respectively, is defined as the ripple voltage V_{ripple} . This ripple voltage in this
 30 implementation is typically around 75 mV.

Fig. 7 shows a comparison of the load current dependent power efficiencies of an LDO regulator circuit operated in continuous mode and pulsed mode. It can be clearly seen that the pulsed mode of operation provides a great improvement in

power efficiency for low load currents when compared to the continuous mode of operation.

Fig. 8 is a circuit diagram of a circuit 160 suitable for use in monitoring the V_{OUT} signal 120 in the LDO regulator embodiment of Fig. 3. The V_{OUT} monitor circuit 160 is based on a comparator 202, described in more detail with reference to Fig. 9. The circuit also includes a reference capacitor 232 and a timeout capacitor 234. The voltage across the reference capacitor 232 provides a reference input 206 to the comparator 202; the voltage across the timeout capacitor 234 provides a timeout input 208 to the comparator 202; and the LDO regulator output 120 which provides a monitor input 204 to the comparator 202.

A 'leakage' transistor 236 is diode-connected across the timeout capacitor 234 with its drain connected to one side of the capacitor 234 and its source and gate connected to the other side (ground). This causes a controlled leakage of charge from the timeout capacitor 234 as will be described below.

A first switch 238 and a second switch 240 selectively connect the LDO regulator output 120 to the timeout capacitor 234 and the reference capacitor 232 respectively.

In use the REFRESH signal 172 (see Figs. 4 and 5) operates to close the first and second switches 238, 240 for a fixed time such that the reference and timeout capacitors 232, 234 are connected to the LDO regulator output 120 for long enough to charge the capacitors 232, 234 to the instantaneous voltage of the LDO regulator output 120. The refresh signal 244 then goes low again, opening the switches 238, 240. At this point the output 209 is at logic low.

The leakage transistor 236 permits a small leakage current to flow therethrough. This causes the voltage across the timeout capacitor 234 to decrease slowly over time. As explained further below with reference to Fig. 11, this prevents issues with voltage drift that could potentially occur should it take a long time for the LDO regulator output 120 to drop below the voltage on the reference input 206.

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If the voltage at either the LDO regulator output 120 or across the timeout capacitor 234 drops below the voltage across the reference capacitor 232 by more than a built-in offset, which will be explained further below, the output 209 is set to logic high as explained below with reference to Fig. 9. When the output 209 is set to logic high, the refresh signal 244 is also set to logic high, thereby restarting the operation described above.

Fig. 9 is a circuit diagram of a three-input comparator 202 suitable for use in the voltage monitor of Fig. 8. The comparator 202 has the monitor input 204, the reference input 206, the timeout input 208 and the output 209 as mentioned previously with reference to Fig. 8.

The monitor input 204 is connected to the gate terminal of a monitor NMOS transistor 210. The timeout input 208 is connected to the gate terminal of a timeout NMOS transistor 212. The monitor and timeout transistors 210, 212 are connected in series with one another, such that the source terminal of the monitor transistor 210 is connected to the drain terminal of the timeout transistor 212.

The reference input 206 is connected to the gate terminals of both upper and lower reference NMOS transistors 214, 216, which are connected in series with one another, such that the source terminal of the upper reference transistor 214 is connected to the drain terminal of the lower reference transistor 216. It will be appreciated that the designations 'upper' and 'lower' are merely used as labels and do not carry any other connotation.

The transistors 210, 212, 214, 216 are fabricated such that the monitor and timeout transistors 210, 212 on one side of the circuit have a physical width N times larger than that of the reference transistors 214, 216 on the other side of the circuit (where N is not necessarily an integer). In one specific example, N is chosen to be 2.75 (corresponding to an 11:4 ratio), providing the comparator with a built-in offset of 75 mV.

The source terminals of the timeout transistor 212 and the lower reference transistor 216 are connected to one another and to a current source 228.

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A first bistable portion PMOS transistor 220 is arranged such that its source terminal is connected to the power supply rail 218, its drain terminal connected to the drain terminal of the monitor transistor 210 and its gate terminal is connected to the drain terminal of the upper reference transistor 214.

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A second bistable portion PMOS transistor 222 is arranged such that its source terminal is connected to the power supply rail 218, its drain terminal connected to the drain terminal of the upper reference transistor 214, and its gate terminal is connected to the drain terminal of the monitor transistor 210.

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A third bistable portion PMOS transistor 224 is connected such that its source terminal is connected to the power supply rail 218 and its gate and drain terminals are connected to both the drain terminal of the monitor transistor 210 and the gate terminal of the second bistable portion transistor 222.

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A fourth bistable portion PMOS transistor 226 is connected such that its source terminal is connected to the power supply rail 218 and its gate and drain terminals are connected to both the drain terminal of the upper reference transistor 214 and the gate terminal of the first bistable portion transistor 220.

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While this particular implementation utilises a single-ended output from node 215, in practice the output has to be amplified further to obtain a rail-to-rail logic signal at the output 209. This can be achieved using an inverting amplifier, since the voltage at node 215 becomes more negative as the voltage at the monitor input 204 and/or the timeout input 208 drop below the voltage at the reference input 206. For ease of illustration, this is simply shown as an inverter 213 that takes the voltage at node 215 and turns it into a logic signal of the correct polarity at the output 209. In an alternative implementation, the output from the comparator 202 is differential and is taken across node 215 (inverting output) and the drain terminal of the monitor transistor 210 (non-inverting output). This differential signal is then fed into a second amplifier stage which converts it into a rail-to-rail logic signal.

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As will now be explained, in use the comparator 202 operates such that the output 209 is set to logic high whenever the voltage at either the monitor input 204 or the timeout input 208 drops below the voltage at the reference input 206 by more than

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the built-in offset, which in this example is 75 mV as mentioned above. When this occurs, current will flow asymmetrically through each side of the comparator.

Specifically, more current will flow through the upper and lower reference NMOS transistors 214, 216 than through the monitor and timeout transistors 210, 212

5 despite the difference in physical size. As a consequence, the bistable portion PMOS transistors 220, 222, 224, 226 cause the output 209 of the comparator 202 to saturate to logic high.

Similarly, if the voltages at both the monitor input 204 and the timeout input 208 are
10 the same as that at the reference input 206, or differ from it by less than the offset voltage, more current will flow through the monitor and timeout transistors 210, 212 than through the upper and lower reference NMOS transistors 214, 216. As a consequence, the bistable portion PMOS transistors 220, 222, 224, 226 cause the output 209 of the comparator 202 to saturate to logic low.

15 Fig. 10 is a timing diagram showing the relationship between the inputs 204, 206, 208 and the output 209 of the three-input comparator 202 of Fig. 9. At an initial time 300, the monitor input 204, reference input 206 and the timeout input 208 are all charged to the value of the LDO regulator output 120 and thus are substantially
20 equal.

At a subsequent time 302, the voltage on the monitor input 204 has dropped below the threshold 211, which is 75 mV less than the voltage on the reference input 206 as described above. In accordance with the operation of the comparator circuit
25 202, the signal on the output 209 transitions from logic low to logic high at this time.

The voltage on the monitor input 204 then increases above the threshold 211 at time 304, causing the signal on the output 209 to revert to logic low.

30 Later, at time 306, the voltage on the timeout input 208 has decreased below the threshold 211. Again, the comparator 202 operates as previously described, and the output signal 209 transitions to logic high once more.

Fig. 11 is a timing diagram showing the advantage of the timeout capacitor 234 of
35 the V_{OUT} monitor circuit 160 of Fig. 8. In this instance, the monitor input 204 is

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decreasing at such a slow rate e.g. because the load on the LDO regulator is very low, that the voltage on the reference input 206 begins to drift. This is due to leakage on the reference capacitor 232. Thus, even if the voltage on the monitor input 204 were to drop to a value more than 75 mV below its original value (i.e. the value which was stored across the reference capacitor 232 at an initial time 400),
5 despite having crossed the intended threshold 211, the comparator 202 would not create a transition to logic high on the output 209.

However, due to the leakage transistor 236, the timeout capacitor 234 leaks current
10 at a greater rate than the reference capacitor 232. This causes the voltage on the timeout input 208 to decrease in a known way, such that at time 402, the output 209 will undergo a transition to logic high even if the voltage on the monitor input 204 has not decreased below the voltage on the reference input 206 by more than 75 mV yet. As previously mentioned, this will cause a refresh of the monitoring circuit
15 (storing new values on the capacitors 232, 234).

Thus it will be seen that a method of operating a low-dropout voltage regulator and a low-dropout voltage regulator arrangement with improved power efficiency at low load currents has been described herein. Although a particular embodiment has
20 been described in detail, it will be appreciated by those skilled in the art that many variations and modifications are possible using the principles of the invention set out herein.

Claims

1. A voltage regulator including a first portion comprising a low-dropout (LDO) regulator; and a second portion comprising an energy storage device, wherein said
5 voltage regulator is arranged to:
- a) power up the LDO regulator at least until an output voltage thereof reaches a predetermined value;
 - b) charge the energy storage device while the LDO regulator is powered up;
 - c) power down the LDO regulator;
 - 10 d) provide a current to a load by discharging the energy storage device while the LDO regulator is powered down;
 - e) detect when the output voltage has dropped by a predetermined amount; and
 - f) power up the LDO regulator again.
- 15
2. The voltage regulator as claimed in claim 1, arranged to carry out steps b) to f) repeatedly.
3. The voltage regulator as claimed in claim 1 or 2, comprising one or more
20 selected from the group comprising: an error amplifier, an output driver transistor, a feedback divider and a decoupling capacitor.
4. The voltage regulator as claimed in any preceding claim, wherein the
25 predetermined value is provided by an output voltage of a third portion comprising a voltage reference circuit.
5. The voltage regulator as claimed in claim 4, wherein the voltage reference circuit comprises a bandgap circuit.
- 30
6. The voltage regulator as claimed in claim 4 or 5, arranged to power the voltage reference circuit selectively depending on the output voltage of the LDO regulator.

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7. The voltage regulator as claimed in claim 6, arranged to power on the voltage reference circuit before the LDO regulator.
8. The voltage regulator as claimed in claim 7, arranged to power on the LDO regulator only after the output voltage of the reference voltage circuit has been determined to be stable.
9. The voltage regulator as claimed in claim 8, arranged to determine that the output voltage of the reference voltage circuit is stable once a variation in the output voltage is below a threshold amount.
10. The voltage regulator as claimed in any preceding claim, wherein the regulator is arranged to power up the LDO regulator in step f) until the output voltage thereof has reached an operating value.
11. The voltage regulator as claimed in any preceding claim, wherein the energy storage device comprises a capacitor.
12. The voltage regulator as claimed in any preceding claim, arranged to carry out step e) by determining an output current flowing through the first portion in order to charge the energy storage device.
13. The voltage regulator as claimed in claim 12, comprising a mirror transistor arranged to generate a sensing current that is smaller than and related to the output current.
14. The voltage regulator as claimed in claim 13, wherein the sensing current is a fixed fraction of the output current.
15. The voltage regulator as claimed in claim 14, wherein the fraction is determined by a ratio of transistor sizes.

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16. The voltage regulator as claimed in any preceding claim, comprising a fourth portion including a control circuit arranged to determine powering up and powering down of the LDO regulator and/or the voltage reference circuit.
- 5 17. The voltage regulator as claimed in any preceding claim, wherein the control circuit is arranged to:
- monitor the output voltage of the LDO regulator;
 - monitor the current flowing through the LDO regulator;
 - determine whether to power up the LDO regulator; and
 - 10 produce an LDO power up signal.
18. The voltage regulator as claimed in claim 16 or 17, wherein the control circuit comprises a voltage monitor circuit comprising:
- a monitored voltage input;
 - 15 a reference capacitor arranged to be able to store a value of the monitored voltage as a reference capacitor voltage;
 - a timeout capacitor arranged to be able to store a value of the monitored voltage as a timeout capacitor voltage, said timeout capacitor undergoing a higher leakage than said reference capacitor; and
 - 20 a comparator arranged to:
 - compare the monitored voltage to the reference capacitor voltage;
 - compare the timeout capacitor voltage to the reference capacitor voltage; and
 - produce a logic signal on an output of the comparator based on said
 - 25 comparisons, said logic signal having a first logic value at least if the reference capacitor voltage is lower than or equal to both the monitored voltage and the timeout capacitor voltage.
19. The voltage regulator as claimed in claim 18, wherein the comparator is
- 30 arranged such that said logic signal has a second logic value once the monitored voltage or the timeout capacitor voltage drops below the reference capacitor voltage by an offset voltage.

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20. The voltage regulator as claimed in claim 18 or 19, wherein the comparator comprises:

a first portion including a first transistor with a gate terminal connected to the reference capacitor;

5 a second portion in parallel with the first portion including a second transistor with a gate terminal connected to the monitored voltage and a third transistor with a gate terminal connected to the timeout capacitor, wherein said second and third transistors are in series; and

10 a bistable portion connected to said first and second portions and arranged to produce said logic signal.

21. The voltage regulator as claimed in any of claims 16 to 20, wherein the control circuit is arranged to:

15 determine whether to power up the voltage reference circuit; and produce a voltage reference power up signal.

22. The voltage regulator as claimed in any of claims 16 to 21, wherein the control circuit is arranged to:

20 determine whether to power down the voltage reference circuit; and produce a voltage reference power down signal.

23. The voltage regulator as claimed in any preceding claim, having a selectable mode of operation in which the voltage reference circuit is powered continuously.

25

24. The voltage regulator as claimed in any preceding claim, having a selectable mode of operation in which the LDO regulator is powered continuously.

25. A method of operating a voltage regulator including a first portion comprising a low-dropout (LDO) regulator; and a second portion comprising an energy storage device comprising:

30

a) powering up the LDO regulator at least until an output voltage thereof reaches a predetermined value;

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b) charging the energy storage device while the LDO regulator is powered up;

c) powering down the LDO regulator;

d) providing a current to a load by discharging the energy storage device
5 while the LDO regulator is powered down;

e) detecting when the output voltage has dropped by a predetermined amount; and

f) powering up the LDO regulator again.

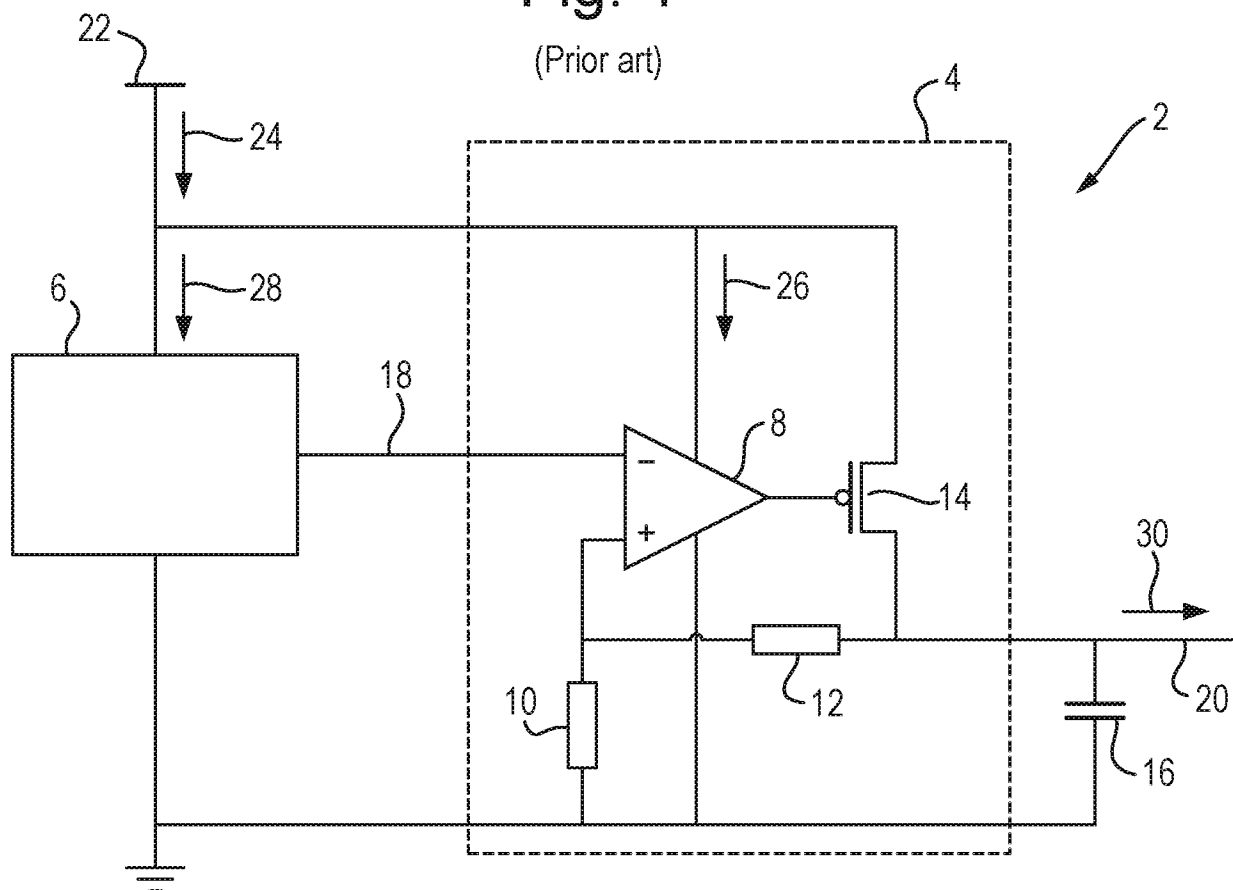
10 26. The method as claimed in claim 25, comprising carrying out steps b) to f) repeatedly.

27. The method as claimed in claim 25 or 26, wherein the voltage regulator is the voltage regulator of any of claims 3 to 24.

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Fig. 1

(Prior art)

**Fig. 2**

(Prior art)

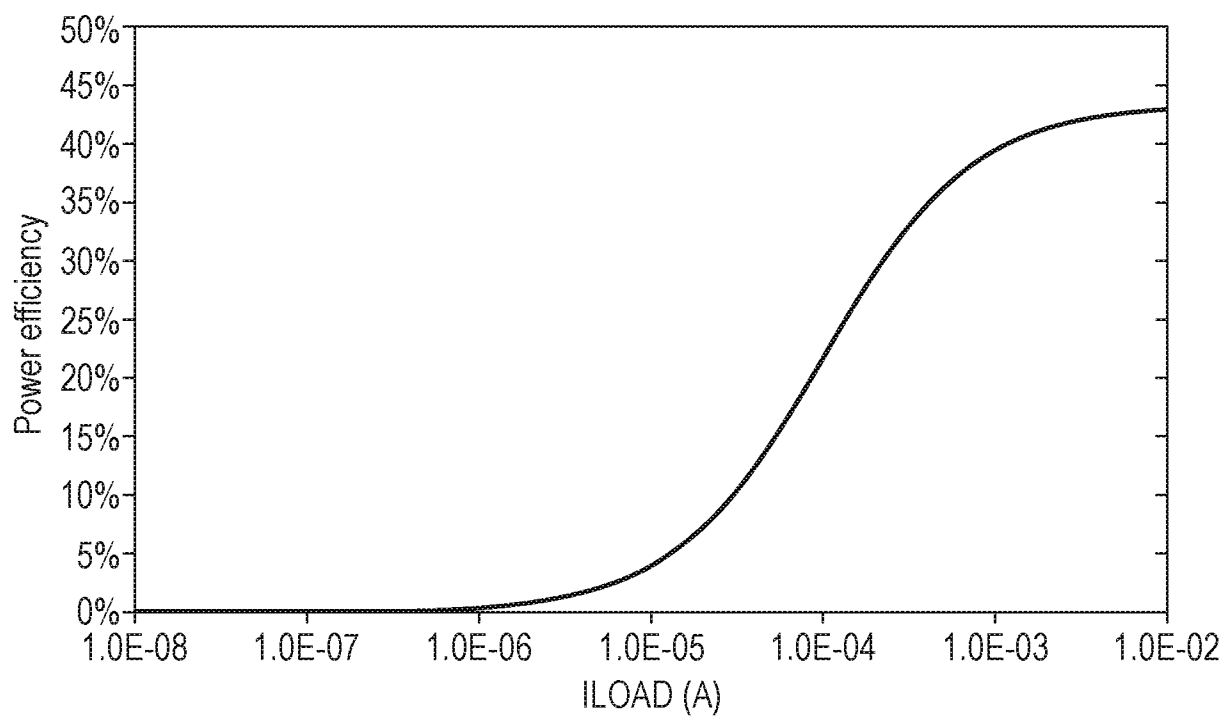


Fig. 3

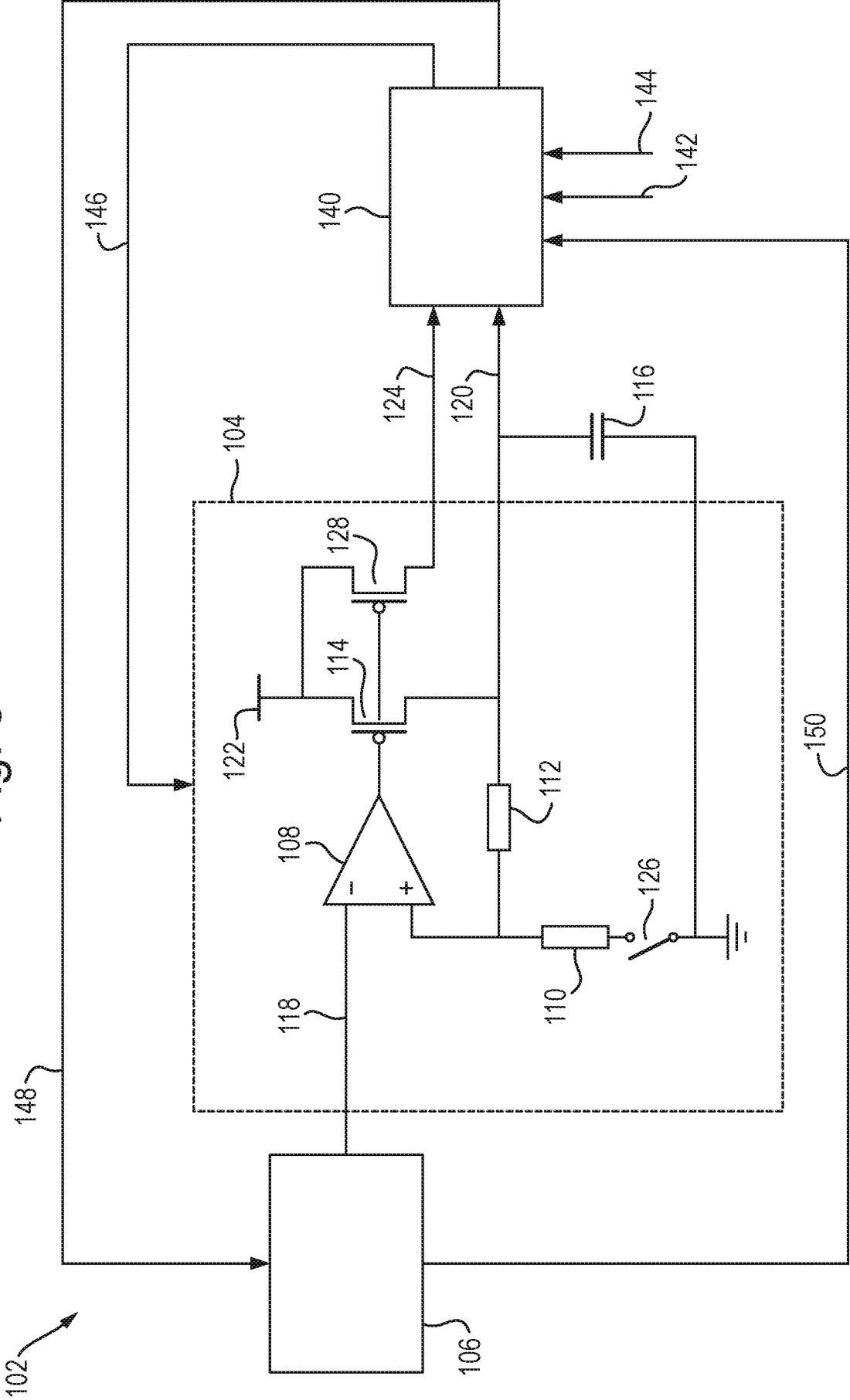


Fig. 4

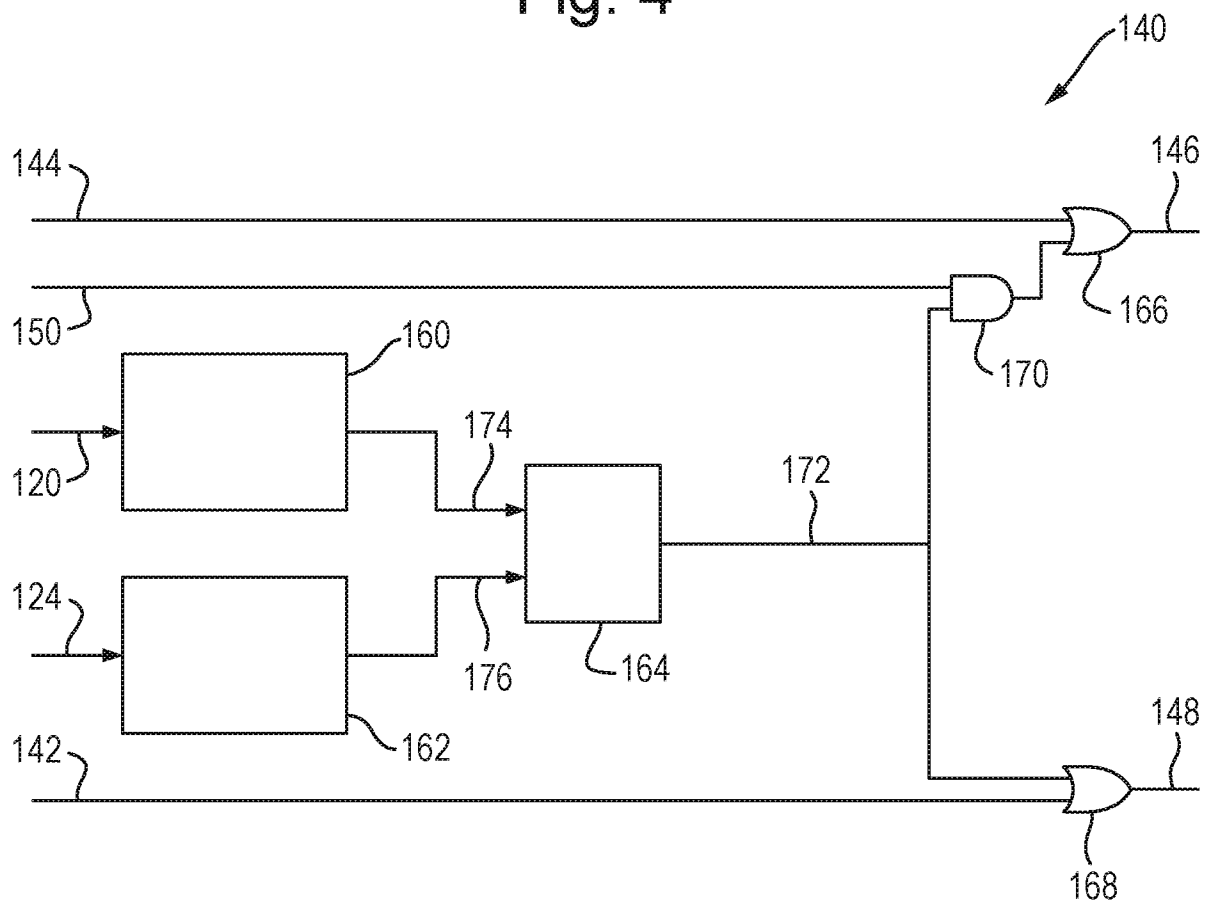


Fig. 5

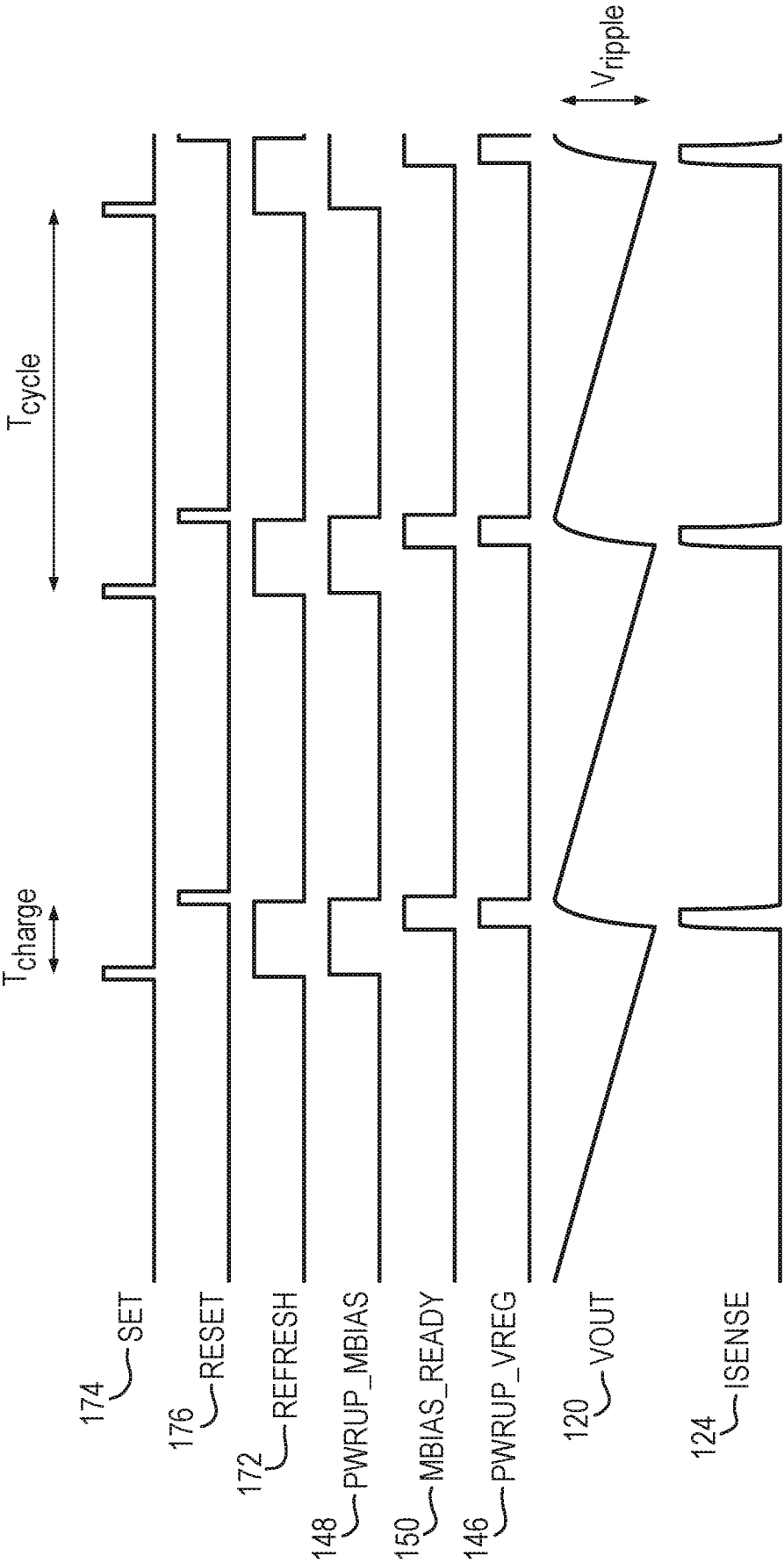


Fig. 6

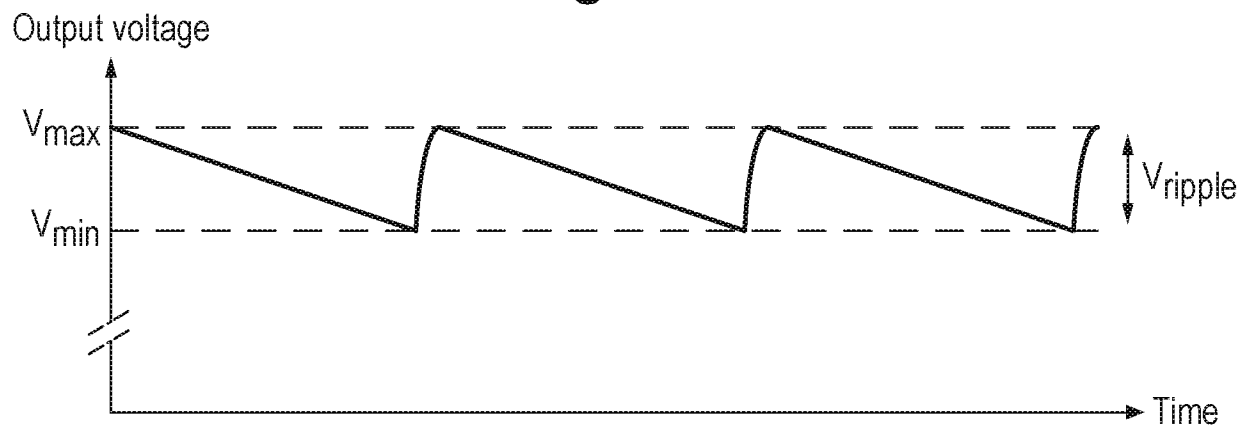


Fig. 7

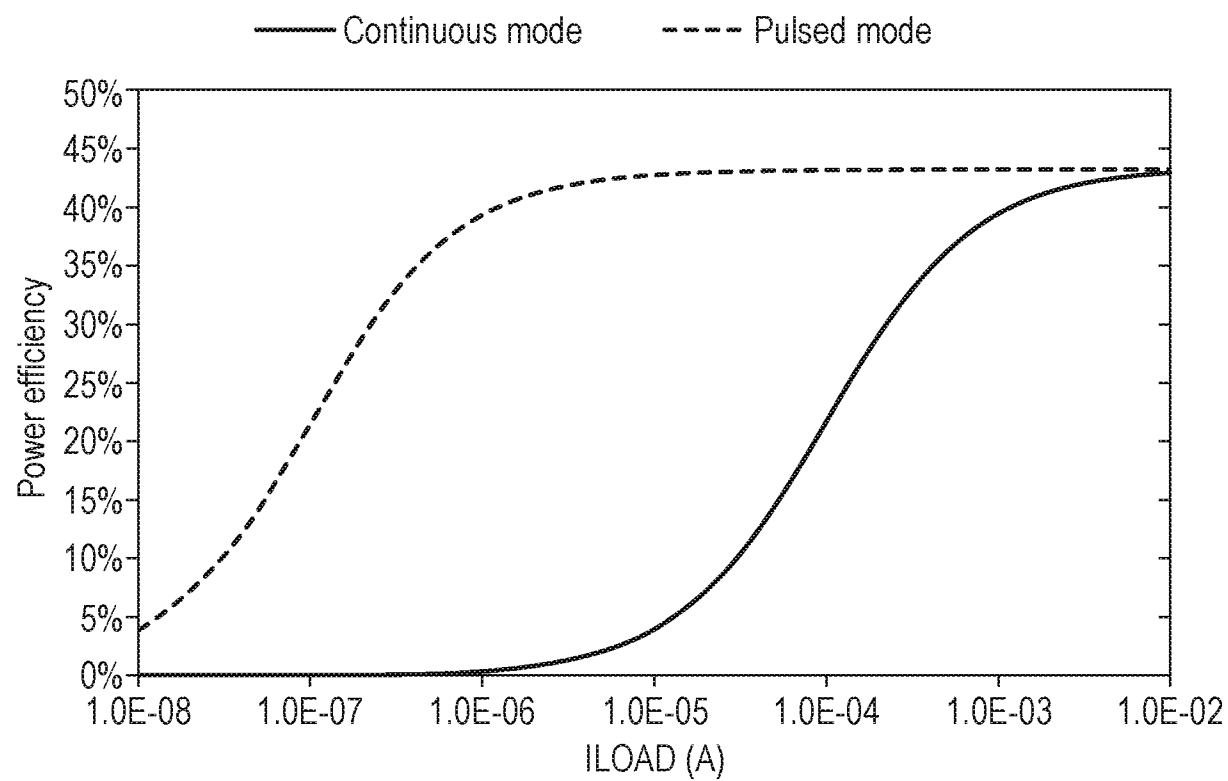


Fig. 8

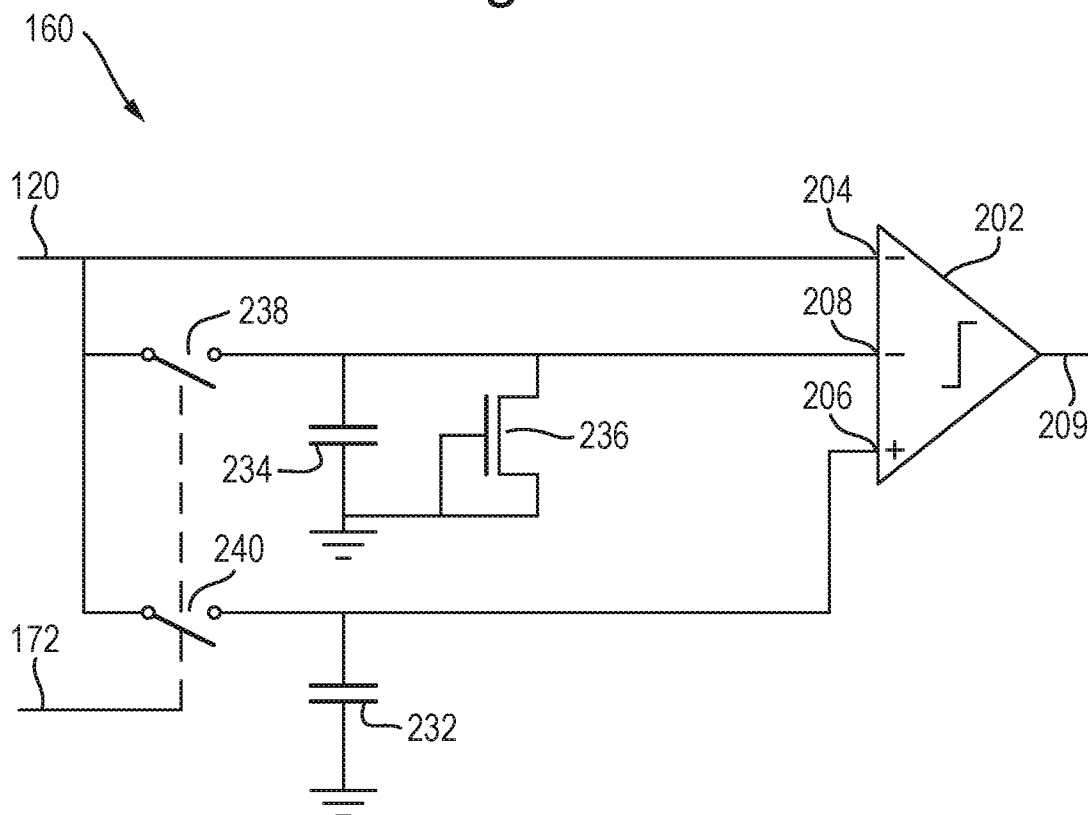


Fig. 9

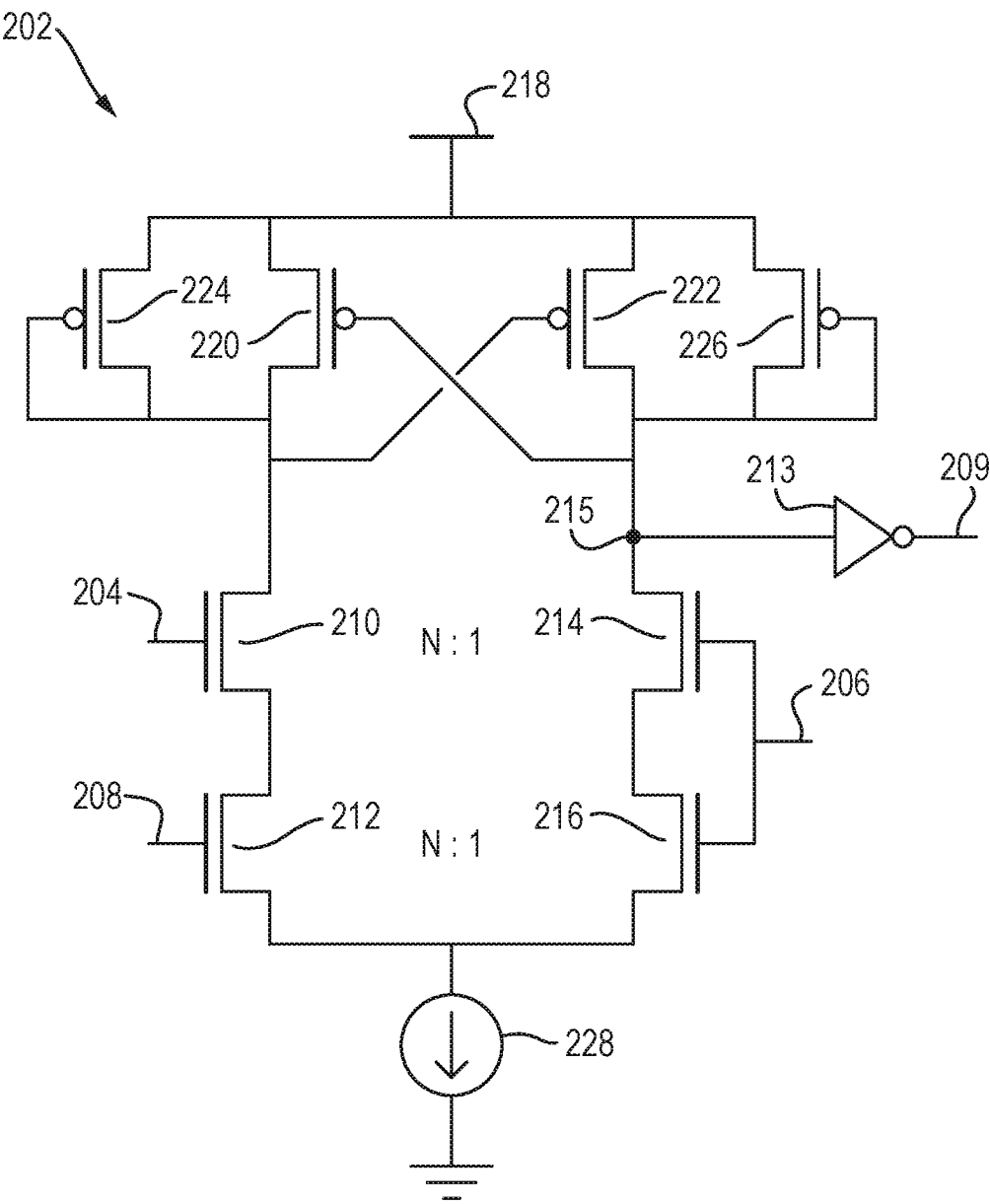


Fig. 10

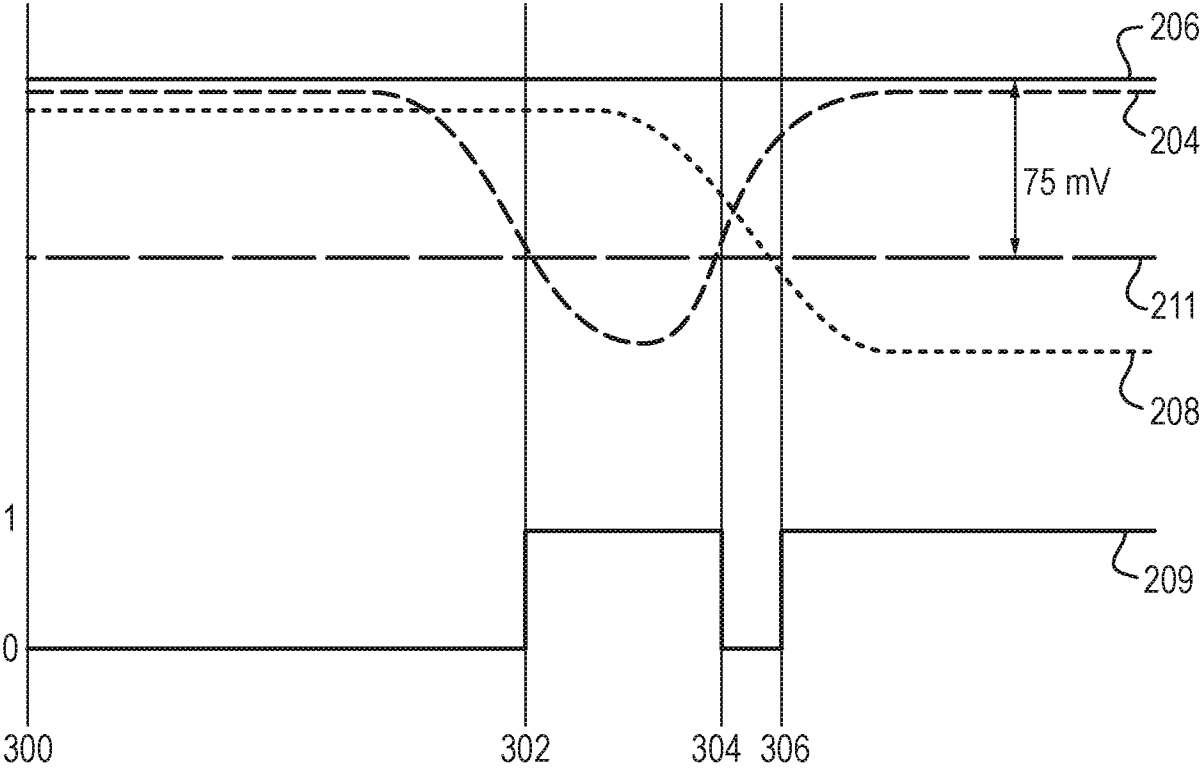
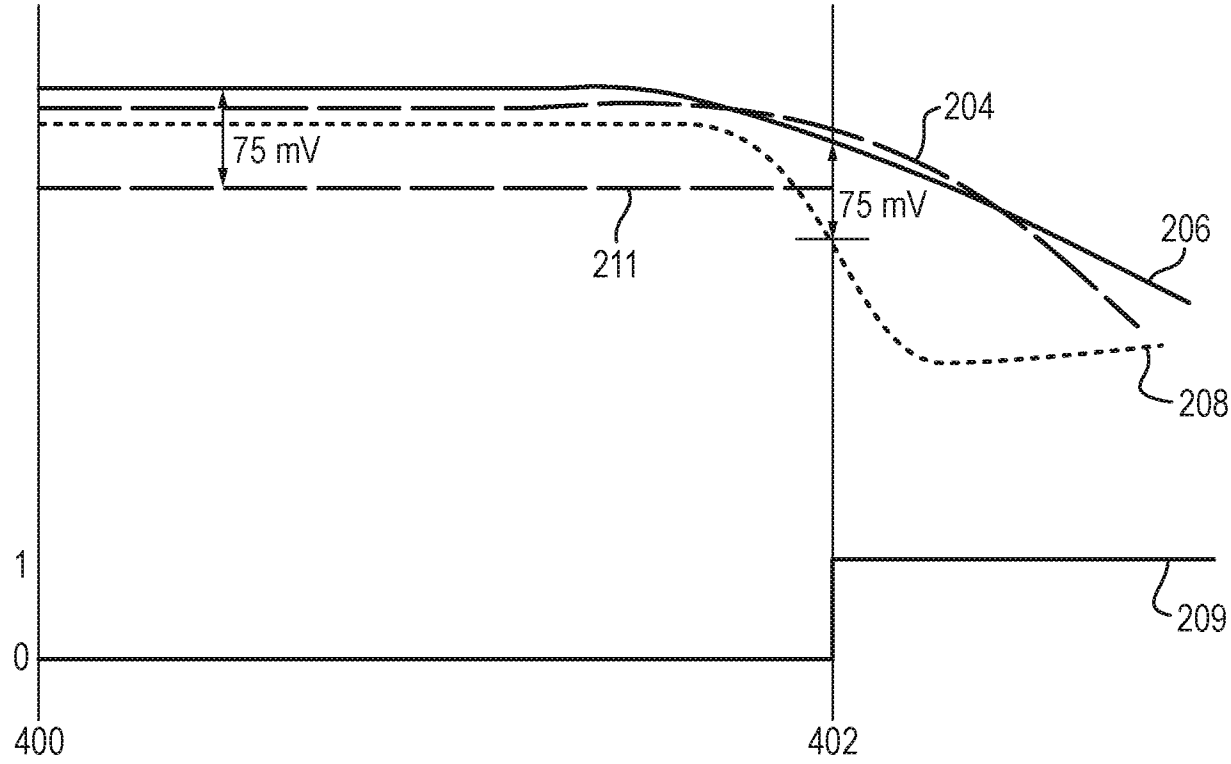


Fig. 11



INTERNATIONAL SEARCH REPORT

International application No

PCT/GB2016/051787

A. CLASSIFICATION OF SUBJECT MATTER
 INV. G05F1/46 G05F1/56
 ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
 G05F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2013/008225 A1 (DSP GROUP LTD [IL]; AMIR ERAN [IL]) 17 January 2013 (2013-01-17) abstract; figures 1,3,5 -----	1-27
X	US 2009/224741 A1 (MARHOLEV BOJKO [US] ET AL) 10 September 2009 (2009-09-10) paragraph [0018] - paragraph [0026]; figure 2 -----	1-6,10, 11,16, 21,22, 24-27
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A	US 2006/108993 A1 (CHIEN HUNG J [TW] ET AL) 25 May 2006 (2006-05-25) abstract; figures 4,5 -----	1-27



Further documents are listed in the continuation of Box C.



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Date of the actual completion of the international search

19 August 2016

Date of mailing of the international search report

30/08/2016

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/GB2016/051787

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