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(54) Title: FORMATION OF THROUGH WAFER ELECTRICAL INTERCONNECTIONS AND OTHER STRUCTURES US ING AN ETCH STOP LAYER

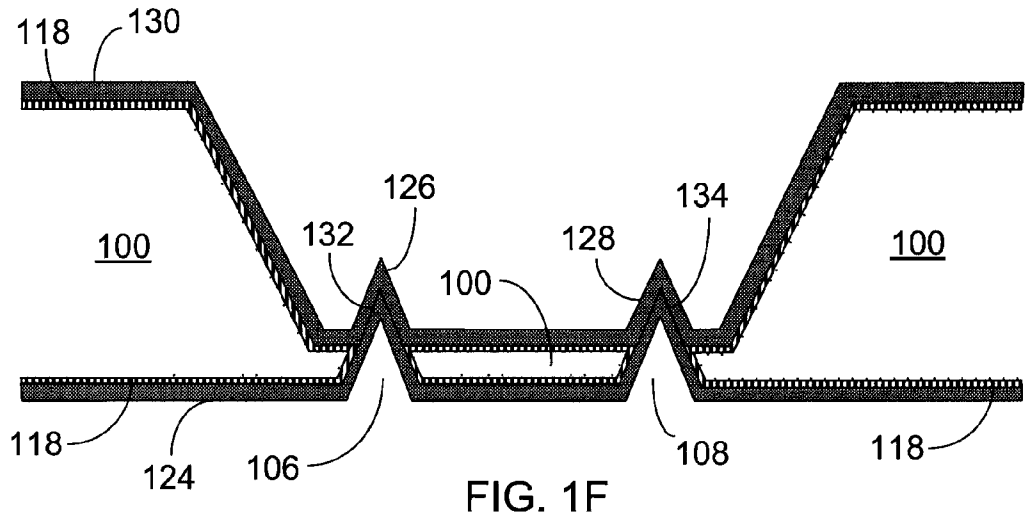

FIG. 1F

(57) Abstract: Providing through wafer interconnections in a semiconductor wafer includes forming a sacrificial membrane (110) in a possibly recessed portion of a semiconductor wafer, depositing metallization (124) over one side of the wafer so as to cover exposed portions of the sacrificial membrane facing the one side of the wafer, removing possibly after etching for exposing exposed portions of the sacrificial membrane facing the other side of the wafer, and depositing metallization (130) over the other side of the wafer so as to contact the previously deposited metallization Techniques also are disclosed for' providing capacitive and other structures using thin metal membranes

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AMENDED CLAIMS

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1. Λ method of providing through-wafer interconnections is a semiconductor wafer having first and second sides, the method comprising:

etching one or more micro-vias in the second side of the wafer;

providing an etch stop layer over the second aide, wherein the etch stop layer covers surfaces in the one or more micro-vias;

etching a oavity in the first side of the wafer to a depth such that portions of the etch stop layer, in areas where the one or more micro-vias were etched, are exposed in the cavity, wherein the cavity is etched to a depth such that a sum of the depth of tike cavity and an average depth of the one or more micro-vias exceeds the total thickness of the wafer;

depositing metallization over one side of the wafer,

subsequently removing regions of the etch stop layer f om. areas corresponding to where the one or more micro-vias were etched; and

depositing metallization over the other side of the wafer so that the metallization deposited over the first side is in contact with the metallization deposited over the second side to form the through-wafer interconnections in areas corresponding to whexe the one or more micro-vias were etched.

2. The method of claim 1 whereir. the semiconductor wafer comprises silicon, and the etch stop layer comprises at least one of silicon dioxide or silicon nitride.

3. The method of claim 1 wherein the semiconductor wafer comprises silicon, and wherein providing an etch stop layer includes thermally growing a silicon dioxide layer.

4. The method of claim 1 wherein a dimension of the cavity is larger than a corresponding dimension of each of the one or more micro-vias.

5. The method of claim 1 wherein the cavity in the first side of the wafer is etched to a depth so as to expose thin membranes of the etoh stop layer in the cavity.

6. The method of claim 1 including providing an isolation layer over surfaces of the semiconductor wafer prior to depositing metallization over the one side of the wafer.

7. The method of claim 1 including:

selectively growing an oxide layer over the first and second sides of the wafer after etching the oavity in the first side, such that portions of the etch stop layer remain exposed in the cavity, and wherein the thickness of the oxide layer is greater than the thickness of the etch stop layer, and

wherein removing regions of the etch stop layer includes using an etchant that etches both the etch stop layer and the oxide layer.

8. The method of claim 7 including thermally growing the oxide layer.

AMENDED SHEET (ARTICLE 19)

9. The method of claim 7 wherein the oxide layer is at least three times as thick as the etch stop layer.

10. A method of providing through-wafer structures in a semiconductor wafer having first and second sides, the method comprising:

forming a sacrificial dielectric membrane in or on a pre-existing semiconductor wafer;

depositing metallization over one side of the wafer so as to cover exposed portions of the sacrificial membrane facing the one side of the wafer,

removing exposed portions of the sacrificial membrane facing the other side of the wafer, and

depositing metallization over said other side of the wafer so as to contact the previously deposited metallization.

11. The method of claim 10 wherein the sacrificial membrane comprises at least one of silicon dioxide or silicon nitride.

12. The method of claim 10 wherein removing exposed portions of the sacrificial membrane includes etching the exposed portions.

13. The method of claim 10 including patterning the metallization to form an inductor.

14. The method of claim 10 including patterning the metal membrane to form a movable cantilever structure,

5S. The method of claim 10 wherein only some of the exposed portions of the sacrificial membrane that face the other side of the wafer are removed, the method further including patterning the metallization to form a plurality of electrical interconnections through a single hermetic via in the semiconductor wafer.

16. A method of providing a capacitive structure in a semiconductor wafer having first and second sides, the method comprising:

etching one or more micro-vias in the second side of the wafer;

providing an etch stop layer over the second side, wherein the etch stop layer covers surfaces in the one or more micro-vias;

etching a cavity in the first side of the wafer to a depth such that portions of the etch stop layer, in areas where the one or more micro-vias were etched, are exposed in the cavity; and

depositing metallization over both sides of the wafer to form a capacitive structure comprising a portion of the etoh stop layer sandwiched between layers of the metallization.

17. A method of providing a oapacitive structure in a semiconductor wafer having first and second sides, the method comprising;

etching a cavity in the first side of the wafer;

providing an etch stop layer over the first side of the wafer, wherein the etch stop layer covers surfaces in the cavity;

etching one or more micro-vias in the second side of the wafer to a depth such that the one or more micro-vias reach the etch stop layer; and

depositing metallization over both sides of the wafer to form a capactive structure comprising a portion of the etch stop layer sandwiched between layers of the metallization.

18. A method comprising:

forming a sacrificial membrane in a pre-existing semiconductor wafer,

depositing metallization over one side of the wafer so as to cover exposed portions of the sacrificial membrane facing the one side of the wafer;

removing exposed portions of the sacrificial membrane facing the other side of the wafer so that at least a portion of the metallization foims a metal membrane.

19. The method of claim 18 including patterning the metal membrane to form an inductor.

20. The method of claim 18 including patterning the metal membrane to form a movable cantilever structure.

21. A method of fabricating a package that houses a micro component, the method comprising:

forming a sacrificial membrane in a pre-existing semiconductor wafer;

depositing metallization over one side of the wafer so as to cover exposed portions of the sacrificial membrane facing the one side of the wafer,

removing exposed portions of the sacrificial membrane facing the other side of the wafer so that at least a portion of the metallization forms a metal membrane;

using the semiconductor wafer with the metal membrane as part of the package to house the micro component; and

using the metal membrane to evaluate the hermeticity of the package.

22. The method of claim 21 wherein evaluating the hermeticity of the package includes sensing changes in the shape of the metal membrane.

23, The method of claim 22 including using the changes to determine a relative pressure or leak rale.