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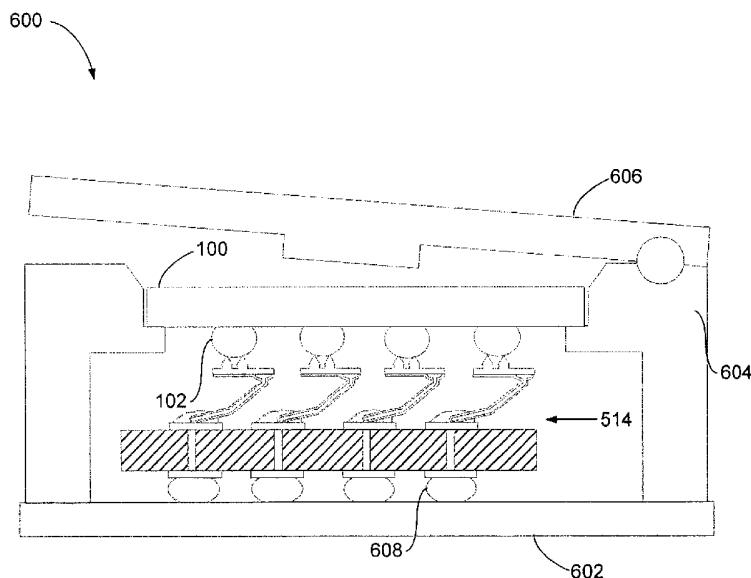
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(54) Title: METHOD FOR MAKING A SOCKET TO PERFORM TESTING ON INTEGRATED CIRCUITS AND SOCKET MADE



(57) Abstract: A interconnect structure is inexpensively manufactured and easily insertable into a socket. The interconnect structure is manufactured by forming a sacrificial substrate with cavities that is covered by a masking material having openings corresponding to the cavities. A first plating process is performed by depositing conductive material, followed by coupling wires within the openings and performing another plating process by depositing more conductive material. The interconnect structure is completed by first removing the masking material and sacrificial substrate. Ends of the wires are coupled opposite now-formed contact structures to a board. To complete the socket, a support device is coupled to the board to hold a tested integrated circuit.

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METHOD FOR MAKING A SOCKET TO PERFORM TESTING ON
INTEGRATED CIRCUITS AND SOCKET MADE

BACKGROUND OF THE INVENTION

Field of the Invention

This invention is directed to a socket for an integrated circuit. More particularly, the socket is a test or burn-in socket for connecting an integrated circuit to a tester for final
5 testing or a burn-in board for burn-in.

Background Art

Testing of semiconductor chips is an important operation in semiconductor manufacturing. Different types of tests are performed at different stages of a semiconductor chip manufacturing process. For example, initial tests can be performed on a wafer scale
10 when semiconductor chips have been fabricated on a wafer, but have not yet been diced and packaged. These initial tests may help to identify defective chips prior to performing more expensive and time consuming packaging steps. After the initial testing, a wafer is diced and individual semiconductor chips are packaged. More exacting tests and burn-in operations are then performed on a chip scale to evaluate individual semiconductor chips or groups of
15 multiple chips.

One technique for performing testing and burn-in operation is to cast individual chips in sockets. Unfortunately, limitations exists in conventional sockets. Conventional sockets may be expensive to manufacture and somewhat unreliable. Some conventional sockets have also used pogo pins as contact elements. Such pogo pins are unreliable and non-wiping.
20 Pogo pins also limit the pitch of an interconnect structure in a socket. For example, a pitch of less than 40 mils with pogo pins becomes mechanically difficult and prohibitively expensive.

Therefore, what is needed is a burn-in socket testing device with an easily insertable interconnect structure that is coupled via drop-in, plug-in, or the like connections. The interconnect structure also needs to be manufactured through an inexpensive manufacturing
25 process.

BRIEF SUMMARY OF THE INVENTION

Embodiments of the present invention provide a method including the steps of fabricating elements (e.g., cavities) in a sacrificial substrate, fabricating a contact structure utilizing the elements in the sacrificial substrate, fabricating an interconnect structure
30 utilizing the contact structure, and fabricating a testing board utilizing the interconnect

structure. Other embodiments of the present invention provide a burn-in socket manufactured by this method.

5 Still other embodiments of the present invention provide a system for testing an integrated circuit board. The system includes a socket. The socket includes a board, an interconnect structure manufactured to be insertable into the socket, the interconnect structure being coupled to the board. The interconnect structure includes a substrate and first and second pads coupled to the substrate and coupled to each other through vias running through the substrate, the second pads coupling the interconnect structure to the board. The interconnect structure also includes resilient contacts coupled to the first pads, the resilient contacts interacting with the integrated circuit during the testing. The socket also includes a support structure coupled to the board that secures contact between the integrated circuit board and the resilient contacts during the testing.

10 Further embodiments, features, and advantages of the present inventions, as well as the structure and operation of the various embodiments of the present invention, are described in detail below with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE FIGURES

The accompanying drawings, which are incorporated herein and form a part of the specification, illustrate exemplary embodiments of the present invention and, together with the description, further serve to explain the principles of the invention and to enable a person skilled in the pertinent art to make and use the invention.

20 FIGS. 1A and 1B illustrate a side view and a bottom view, respectively, of a tested flip-chip semiconductor according to embodiments of the present invention.

FIGS. 2A and 2B illustrate a cross-sectional and bottom view, respectively, of a sacrificial substrate according to embodiments of the present invention.

25 FIG. 3A and 3B illustrate a cross-sectional and bottom view, respectively, of the sacrificial substrate of FIGS. 2A and 2B with a masking material.

FIGS. 4A, 4B, 4C, and 4D show processing steps for forming a testing socket according to embodiments of the present invention.

30 FIGS. 5A and 5B show further processing steps for forming the testing socket according to embodiments of the present invention.

FIG. 6 shows a still further processing step for forming the testing socket according to embodiments of the present invention.

FIG. 7 shows a plurality of sockets used to test a plurality of devices on a wafer according to embodiments of the present invention.

FIG. 8 shows a flowchart depicting an overall method for making a socket according to embodiments of the present invention.

FIG. 9 shows a flowchart depicting more detailed method steps for the method of FIG. 8.

5 Exemplary embodiments of the present invention will now be described with reference to the accompanying drawings. In the drawings, like reference numbers indicate identical or functionally similar elements. Additionally, the left-most digit(s) of a reference number identifies the drawing in which the reference number first appears.

DETAILED DESCRIPTION OF EMBODIMENTS THE INVENTION

10 Embodiments of the invention provide an interconnect structure that is inexpensively manufactured and easily insertable into a socket. The interconnect structure is manufactured by forming a sacrificial substrate with cavities that is covered by a masking material having openings corresponding to the cavities. A first plating process is performed by depositing
15 conductive material, followed by coupling wires within the openings and performing another plating process by depositing more conductive material. The interconnect structure is completed by first removing the masking material and sacrificial substrate. Ends of the wires are coupled opposite now-formed contact structures to a board. To complete the socket, a support device is coupled to the board to hold a tested integrated circuit.

Integrated Circuit Semiconductor

20 FIGS. 1A-1B show side and bottom views, respectively, of a semiconductor chip 100 (e.g., an integrated circuit (IC)) that is to be tested according to embodiments of the present invention. Semiconductor chip 100 can be packaged or unpackaged. Semiconductor chip 100 can be, but is not limited to, a flip-chip semiconductor with solder ball contacts 102 (e.g., "controlled collapse chip connection" (also known as "C4")). In general, any type of
25 semiconductor chip and contacts can be used.

Interconnect structure Manufacturing Process

FIGS. 2-6 illustrate a process of making an interconnect structure (e.g., a tile) 514 (FIG. 5) for a socket 600 (FIG. 6) according to embodiments of the present invention.

30 FIGS. 2A-2B show cross-sectional and bottom views, respectively, of a sacrificial substrate 200 according to embodiments of the present invention. Sacrificial substrate 200 can be any material into which elements (e.g., cavities) 202 can be formed. As its name implies, sacrificial substrate 200 can be dissolved, etched away, or otherwise removed from a

final structure. In some embodiments, a copper or aluminum sheet or foil can be used for sacrificial substrate 200. In other embodiments, silicon, ceramic, titanium-tungsten, and the like can be used for the sacrificial substrate 200. As shown, cavities 202 are formed in the sacrificial substrate 200. In various embodiments, cavities 200 can be formed by embossing, etching, or the like. As will be seen, cavities 200 correspond to contacts 102 on semiconductor chip 100.

FIGs. 3A-3B show cross-sectional and bottom views, respectively, of sacrificial substrate 200 with a masking material 300 applied, according to embodiments of the present invention. In some embodiments, masking material 300 can be a photoresist material. As shown, openings 302 are formed in masking material 300. These openings 302 expose cavities 202 that were formed in FIG. 2.

FIGs. 4A-4D show additional processing steps according to embodiments of the present invention. In FIG. 4A, a conductive material 400 is deposited or plated in openings 302. In some embodiments, conductive material 400 can be a hard, metallic, and/or electrically conductive material. For example, conductive material 400 can be a rhodium material and a palladium cobalt alloy. As will be seen, conductive material 400 forms a contact tip 402 that is used to contact semiconductor chip 100 during testing. Although shown with two extensions, contact tip 402 can have one or more extensions as required by different specifications and embodiments. In other embodiments, contact tip 402 can be made of a plurality of layered materials, for example a soft gold layer, a nickel layer, and a hard gold layer. In other embodiments an non-exhaustive list of other materials can include: silver, palladium, platinum, rhodium, conductive nitrides, conductive carbides, tungsten, titanium, molybdenum, rhenium, indium, osmium, refractory metals, or the like. Throughout the rest of the specification the term conductive material 400 will be used, and this term is meant to include one or more materials, and if more than one material, layered materials. Conductive material 400 can be deposited in openings 302 using any suitable method. In various embodiments, the deposition method can be electroplating, physical or chemical vapor deposition, sputtering, or the like. The layers that form the contact tip 402 may be deposited in a like manner.

Although not shown, in various embodiments a release material can be deposited in openings 302 before depositing conductive material 400. Use of a release material facilitates eventual removal of a contact structure 506 (FIG. 5B) formed by conductive material 400 from sacrificial substrate 200. In some embodiments, a release layer can be a layer of aluminum. In still other embodiments, although also not shown, a seed layer consisting of a

conductive material can also be deposited in openings 302 before depositing conductive material 400. In still other embodiments, the seed layer can be deposited as a blanket layer over the entire sacrificial substrate 200 prior to depositing masking material 300. The seed layer can facilitate electroplating, if electroplating is used to deposit conductive material 400.

5 FIG. 4B shows a wire 404 being bonded in each opening 302 to conductive material 400 according to embodiments of the present invention. Wire 404 can be bonded using well known wire bonding techniques. One example of a wire bonding technique is found in U.S. Patent No. 5,601,740 to Eldridge et al., which is incorporated by reference herein in its entirety. In some embodiments, wire 404 can be made of a relatively soft, readily shapeable
10 material, while in other embodiments other types of materials can be used. Examples of materials that can be used for wire 404 include gold, aluminum, copper, platinum, lead, tin, indium, their alloys, or the like. In some embodiments, the diameter of wire 404 can be in the range 0.25 to 10 mils. It is to be appreciated, wire 404 can have other shaped cross-sections, such as rectangular or any other shape.

15 FIG. 4C shows wires 404 and conductive material 400 being plated with a second conductive material 406. In some embodiments, conductive material 406 is harder than a material making up wire 404 to strengthen the contact structure 506 (FIG. 5B). Some examples of suitable materials include, nickel, copper, solder, iron, cobalt, tin, boron, phosphorous, chromium, tungsten, molybdenum, bismuth, indium, cesium, antimony, gold,
20 lead, tin, silver, rhodium, palladium, platinum, ruthenium, their alloys, or the like. In some embodiments, conductive material 406 can be 0.2 to 10 mils thick. Conductive material 406 can be deposited on wire 404 using any suitable method. In various embodiments, deposition methods include electroplating, physical or chemical vapor deposition, sputtering, or the like. Example methods for wire bonding a wire and then over plating the wire are described in
25 U.S. Patent No. 5,476,211 to Khandros, U.S. Patent No. 5,917,707 to Khandros et al., and U.S. Patent No. 6,336,269 to Eldridge et al., which are all incorporated by reference herein in their entirety.

FIG. 4D illustrates the process after masking material 300 has been removed.

30 FIGS. 5A-5B show additional processing steps according to embodiments of the present invention. FIG. 5A shows free ends 500 of wires 404 having conductive coating 406 being coupled to a wiring substrate 502 through use of coupling material 504. In various embodiments, the coupling can be done by wiring, soldering, brazing, or the like. In embodiments that the step of coupling free end 500 of wires 404 having conductive coating 406 includes heating, wires 404 and contact structure 506 (FIG. 5B) can also be heat treated.

One example of this is found in U.S. Patent No. 6,150,186 to Chen et al., which is incorporated herein by reference in its entirety, and which discloses methods for heat treating spring contact structures.

FIG. 5B shows a configuration for wiring substrate 502 according to embodiments of the present invention. Wiring substrate 502 can be a ceramic substrate with pads 508 and 510 on opposite sides of wiring substrate 502. The pads 508 and 510 can be coupled through the use of vias 512 that run through wiring substrate 502. In other embodiments, wiring substrate 502 can be a printed circuit board or a printed wiring board. As also shown in FIG. 5B, sacrificial substrate 200 is removed, which can be done by etching, dissolving, or the like, the material forming sacrificial substrate 200. Another term for the wiring substrate 502 having contact elements 506, the pads 508, 510 and vias 512 is an interconnect structure 514. In some embodiments, interconnect structure 514 can be used to make a test or burn-in socket 600 (FIG. 6). In various embodiments interconnect structure 514 can be a modular interconnect structure, a drop-in interconnect structure, a plug-in interconnect structure, or the like, that is easily inserted into the socket 600, or any other socket.

Further advantages of the process of making interconnect structure 514 according to the present invention are that the process can be inexpensive and can be performed separately on a interconnect structure. In this way, defective interconnect structures can be identified and removed prior to formation of the socket. This process has further advantages in that a interconnect structure with contact elements arranged at a fine pitch of less than 40 mils, including about 10 mils or less, can be made inexpensively and mass produced. Accordingly, this process is a reliable and inexpensive technique for producing a fine pitch socket.

Socket Forming Process

FIG. 6 shows a socket 600 in which interconnect structure 514 is coupled and electrically wired to a board 602 (e.g., a test board or socket board) according to embodiments of the present invention. In some embodiments, board 602 can include a support structure 604 with a hinged closing device 606 for holding integrated circuit (IC) 100 during testing. In various embodiments, board 602 can be a test board or burn-in board. Interconnect structure 514 can electrically connected to board 602 in any suitable manner, such as by soldering 608, pins (not shown), or any other type of contact. For example, the pins can form a friction fit with corresponding holes (not shown). In alternative embodiments, board 602 can be a socket board that is itself plugged into or otherwise attached to a larger test system (not shown).

FIG. 7 shows an embodiment with multiple interconnect structures 700 coupled to board 702 according to the present invention. Although shown with multiple IC's 100, in other embodiments one IC 100 with many ball contacts 102 can be tested. In this embodiment, an array of spring contacts 704 for contacting IC 100 is built by coupling a plurality of interconnect structures 700 to board 702 in various configurations depending on the configuration of ball contacts 102. As discussed above, in various embodiments board 702 can be a test board or burn in board, and a plurality of support structures similar to 604 (not shown in FIG. 7 for convenience) can be secured to board 702 around interconnect structures 700.

10 Methodology to Manufacture the Interconnect Structure and Socket

FIG. 8 shows a method 800 for making sockets according to embodiments of the present invention. At step 802, a sacrificial substrate is formed with any type or amount of elements formed in the substrate as desired. For example, cavities can be formed as depicted in FIG. 2. At step 804, plated wires are formed based on the sacrificial substrate. This can be done through the various methods as described with respect to FIGs. 3-4. At step 806, an interconnect structure is formed based on the plated wires. This can be done through the various methods described with respect to FIG. 5. At step 808, a socket is formed based on the interconnect structure. Thus can be done through the various methods described with respect to FIGs. 6 and 7.

20 FIG. 9 shows a flowchart depicting a more detailed method 900 for making sockets according to embodiments of the present invention. At step 902, cavities (e.g. elements or cavities 202) are formed in a sacrificial substrate (e.g., substrate 200). At step 904, a masking material (e.g., masking material 300) is deposited on the sacrificial substrate. At step 906, openings (e.g., openings 302) are formed in the masking material corresponding to the cavities. At step 908, conductive material (e.g., conductive material 400) is deposited or plated in the openings. At step 910, wires (e.g., wires 404) are coupled to the conductive material. At step 912, a second conductive material (e.g., conducting material 406) is deposited or plated on the wires and the first conductive material. At step 914, the masking material is removed. At step 916, a coupling material (e.g., coupling material 504) is used to couple tips (e.g., tips 500) of the wires having the conductive material to a wiring substrate (e.g., wiring substrate 502). At step 918, the sacrificial substrate is removed to form an interconnect structure (e.g., interconnect structure 514 or 700). At step 920, the interconnect structure is coupled to a board (e.g., board 602 or 702) to form a socket (e.g., socket 600).

Conclusion

While various embodiments of the present invention have been described above, it should be understood that they have been presented by way of example only, and not limitation. It will be apparent to persons skilled in the relevant art that various changes in
5 form and detail can be made therein without departing from the spirit and scope of the invention. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

WHAT IS CLAIMED IS:

1. A method comprising the steps of:
fabricating elements in a sacrificial substrate;
fabricating a contact structure utilizing said elements in said sacrificial substrate;
5 fabricating a interconnect structure utilizing said contact structure; and
fabricating a testing board utilizing said interconnect structure.
2. The method of claim 1, wherein said fabricating elements step comprises the
step of fabricating cavities in said sacrificial substrate.
3. The method of claim 2, further comprising the step of embossing said
10 sacrificial substrate to perform said fabricating cavities step.
4. The method of claim 2, further comprising the step of etching said sacrificial
substrate to perform said fabricating cavities step.
5. The method of claim 1, further comprising the step of forming said sacrificial
substrate from copper.
- 15 6. The method of claim 1, further comprising the step of forming said sacrificial
substrate from aluminum.
7. The method of claim 1, further comprising the step of forming said sacrificial
substrate from silicon.
8. The method of claim 1, further comprising the step of forming said sacrificial
20 substrate from ceramic.
9. The method of claim 1, further comprising the step of forming said sacrificial
substrate from titanium-tungsten.

10. The method of claim 1, wherein said fabricating a contact structure step comprises the steps of:
- depositing masking material on said sacrificial substrate;
 - forming openings in said masking material corresponding to said elements;
 - 5 depositing first conductive material in said openings;
 - bonding a wire to said conductive material in each of said openings;
 - depositing second conductive material over said wires; and
 - removing said masking material.
11. The method of claim 10, further comprising the step of utilizing photoresist
10 material as said masking material.
12. The method of claim 10, further comprising the step of using hard metallic material as said first conductive material.
13. The method of claim 10, further comprising the step of using rhodium material as said first conductive material.
14. The method of claim 10, wherein said depositing first conductive material step
15 comprises the steps of:
- depositing a soft gold layer;
 - depositing a nickel layer, and
 - depositing a hard gold layer.
15. The method of claim 10, wherein said depositing first conductive material step
20 comprises the step of using electroplating to perform said depositing.
16. The method of claim 10, wherein said depositing first conductive material step comprises the step of using vapor deposition to perform said depositing.
17. The method of claim 10, wherein said depositing first conductive material step
25 comprises the step of sputtering to perform said depositing.
18. The method of claim 10, further comprising the step of depositing a release material in said openings before performing said depositing first conductive material step.
19. The method of claim 18, wherein said depositing a release material step comprises the step of using aluminum as said release material.

20. The method of claim 10, further comprising the step of depositing a seed layer in said opening before performing said depositing first conductive material step.
21. The method of claim 10, further comprising the step of depositing a seed layer over said sacrificial substrate before performing said depositing masking material step.
- 5 22. The method of claim 10, wherein said bonding a wire step comprises the step of using soft, shapeable material as said wire.
23. The method of claim 10, wherein said bonding a wire step comprises the step of using gold as said wire.
24. The method of claim 10, wherein said bonding a wire step comprises the step
10 of using aluminum as said wire.
25. The method of claim 10, wherein said bonding a wire step comprises the step of using copper as said wire.
26. The method of claim 10, wherein said bonding a wire step comprises the step of using platinum as said wire.
- 15 27. The method of claim 10, wherein said bonding a wire step comprises the step of using lead as said wire.
28. The method of claim 10, wherein said bonding a wire step comprises the step of using tin as said wire.
29. The method of claim 10, wherein said bonding a wire step comprises the step
20 of using indium as said wire.
30. The method of claim 10, wherein said bonding a wire step comprises the step of using alloy as said wire.
31. The method of claim 10, further comprising the step of using a harder material for said second conductive material than material used for said wire to strengthen a contact
25 structure.

32. The method of claim 1, wherein said fabricating a interconnect structure step comprises the steps of:
- coupling free ends of said wires to a wiring substrate; and
 - removing said sacrificial substrate.
- 5 33. The method of claim 32, wherein said coupling step comprises the step of using wiring to couple said free ends of said wires to said wiring substrate.
34. The method of claim 32, wherein said coupling step comprises the step of using brazing to couple said free ends of said wires to said wiring substrate.
35. The method of claim 32, wherein said coupling step comprises the step of
10 using heating techniques to couple said free ends of said wires to said wiring substrate.
36. The method of claim 32, further comprising the steps of forming said wiring substrate by:
- coupling first and second pads to opposite sides of a substrate; and
 - interconnecting said first and second pads with a vias running through said substrate.
- 15 37. The method of claim 36, wherein said forming step comprises the step of using a ceramic material to form said substrate.
38. The method of claim 1, wherein said fabricating testing board step further comprises the step of coupling said interconnect structure to a board.
39. The method of claim 38, further comprising the step of coupling a support
20 structure to said board to hold a tested system.
40. The method of claim 1, wherein said fabricating a interconnect structure step comprises fabricating a plurality of interconnect structures and wherein said fabricating a testing board step further comprises utilizing said plurality of interconnect structures.
41. A burn-in socket for testing an integrated circuit board manufactured by the
25 method of claim 1.

42. A system for exercising an integrated circuit board comprising:
a socket including,
a board;
an interconnect structure manufactured to be insertable into said socket, said
5 interconnect structure being coupled to said board, said interconnect structure including,
a substrate,
first and second pads coupled to said substrate and coupled to each
other through vias running through said substrate, said second pads coupling said
interconnect structure to said board, and
10 resilient contacts coupled to said first pads, said resilient contacts
interacting with the integrated circuit during the testing, and
a support structure coupled to said board that secures contact between the
integrated circuit board and said resilient contacts during the testing.
43. A system according to claim 42, wherein said interconnect structure is a
15 modular interconnect structure that is inserted into said socket.
44. A system according to claim 42, wherein said interconnect structure is a drop-
in interconnect structure that is dropped into said socket.
45. A system according to claim 42, wherein said interconnect structure is a plug-
in interconnect structure that is plugged into said socket.
- 20 46. A system according to claim 42, wherein said socket includes a plurality of
said interconnect structures.

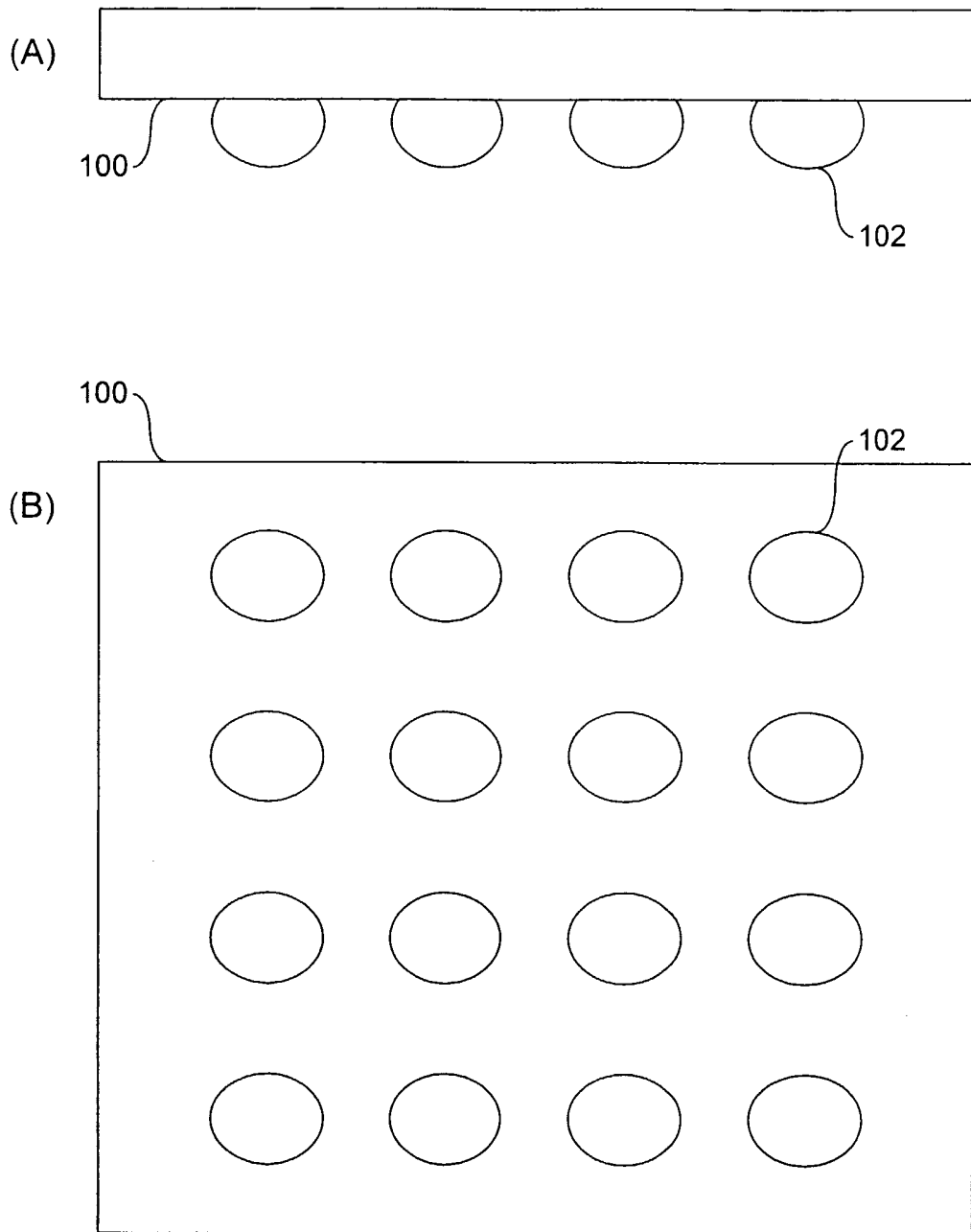


FIG. 1

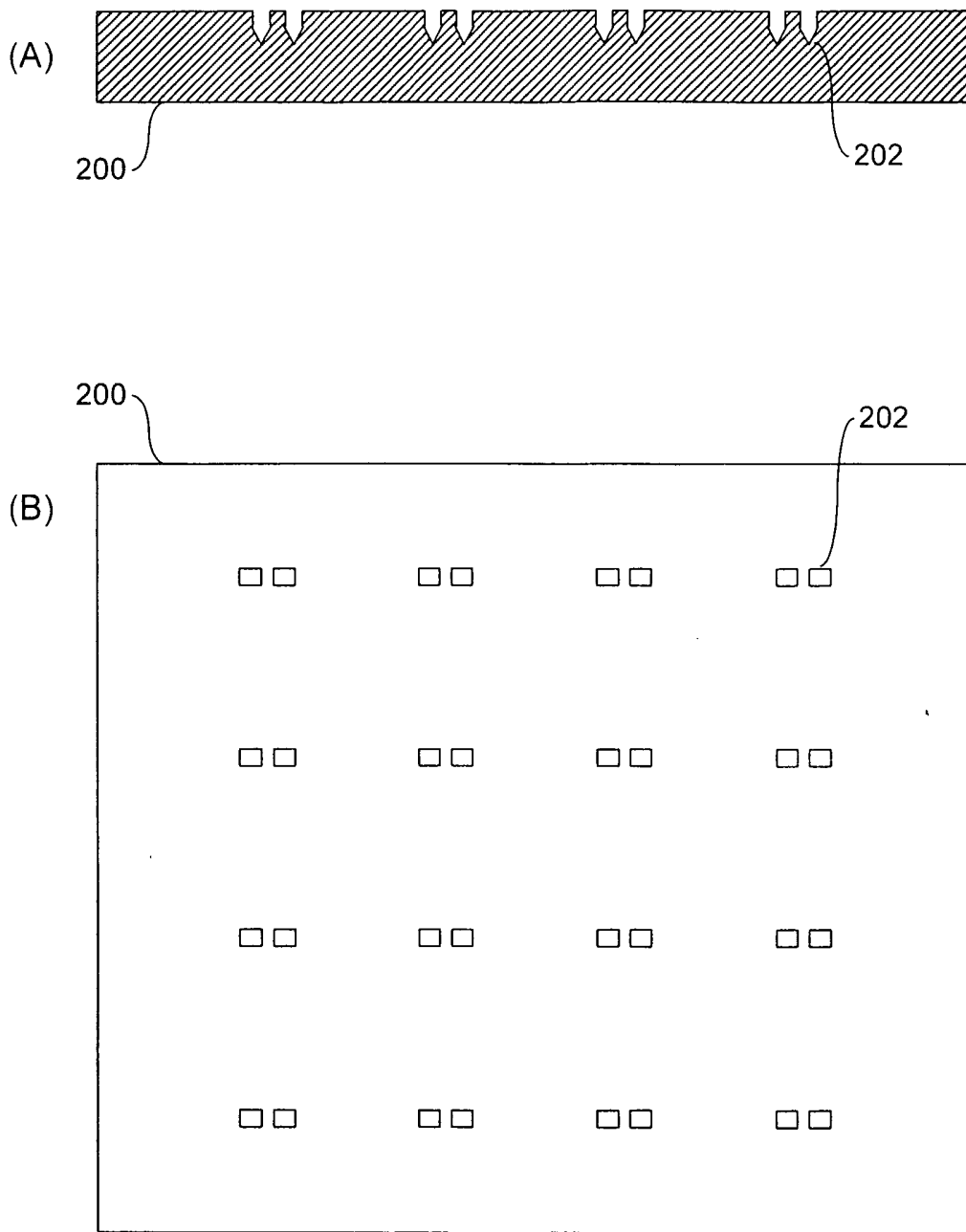


FIG. 2

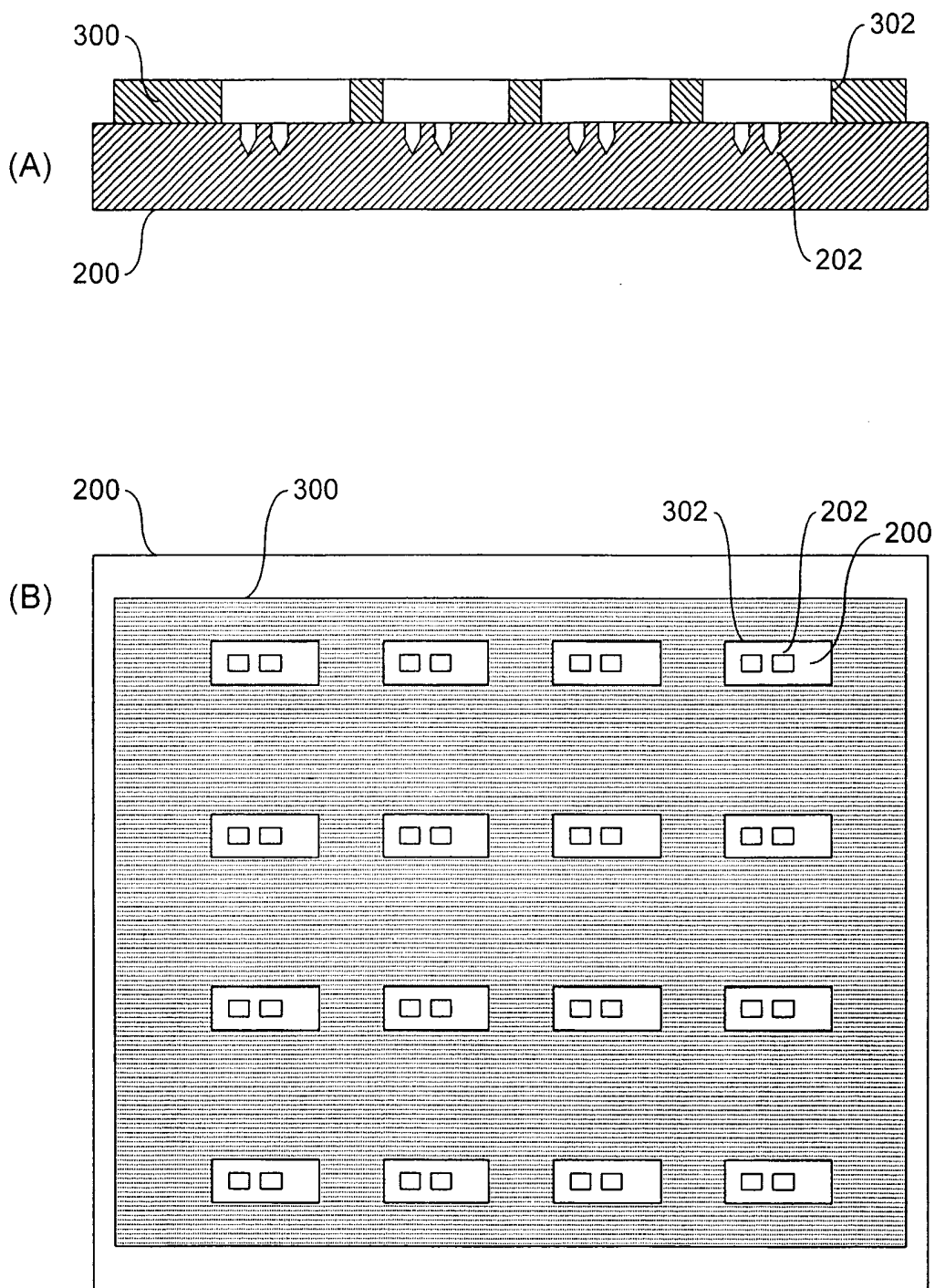


FIG. 3

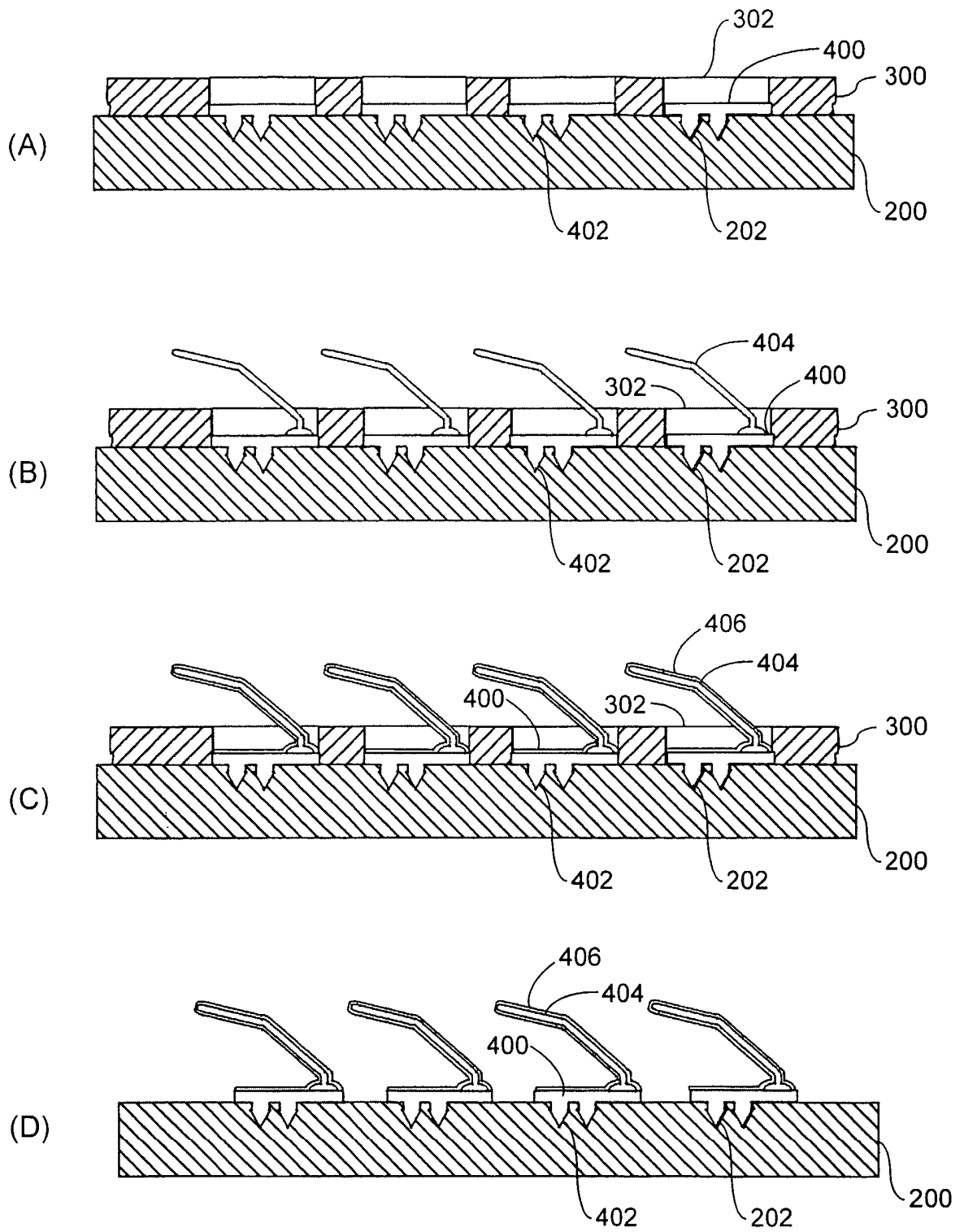


FIG. 4

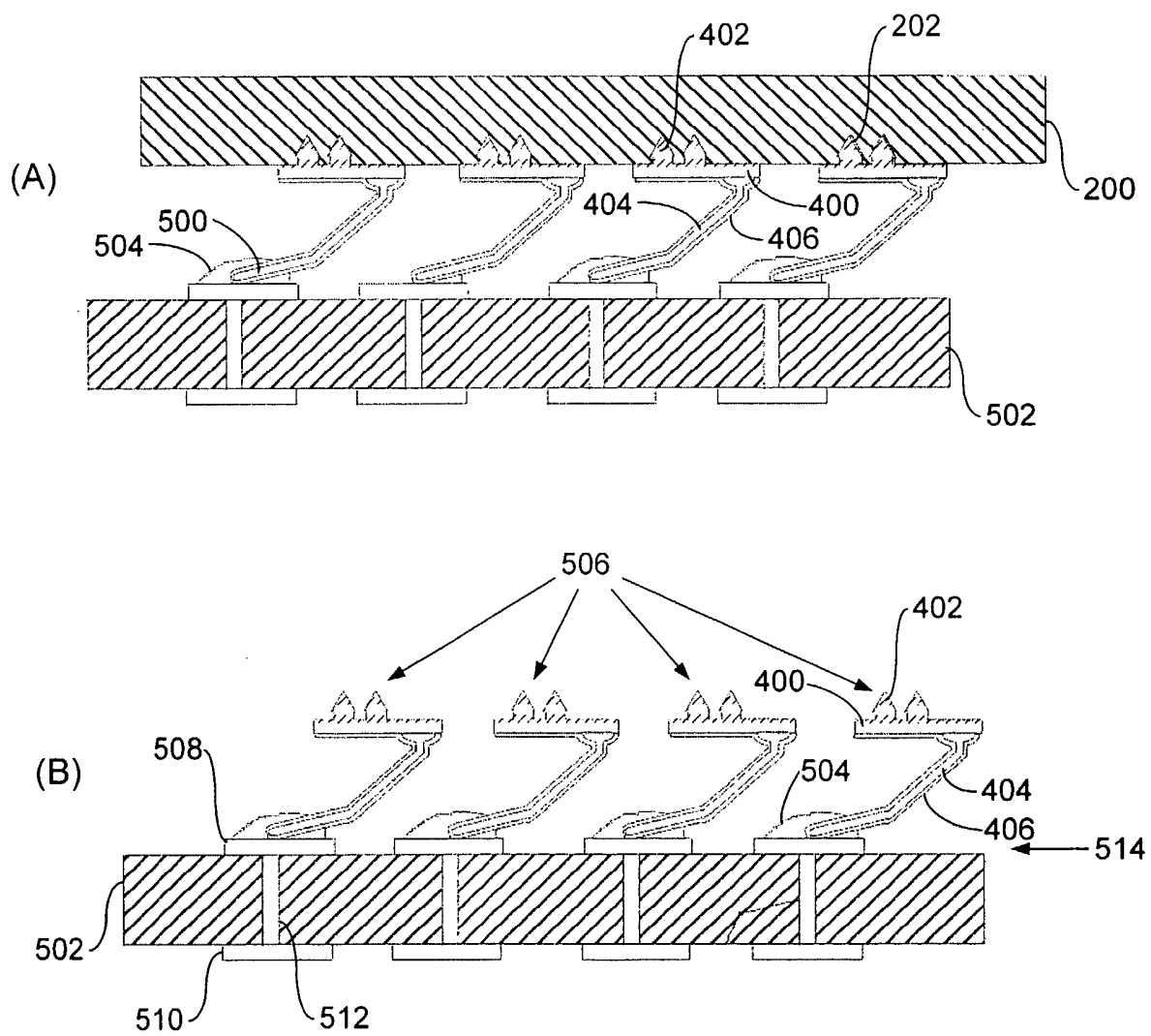


FIG. 5

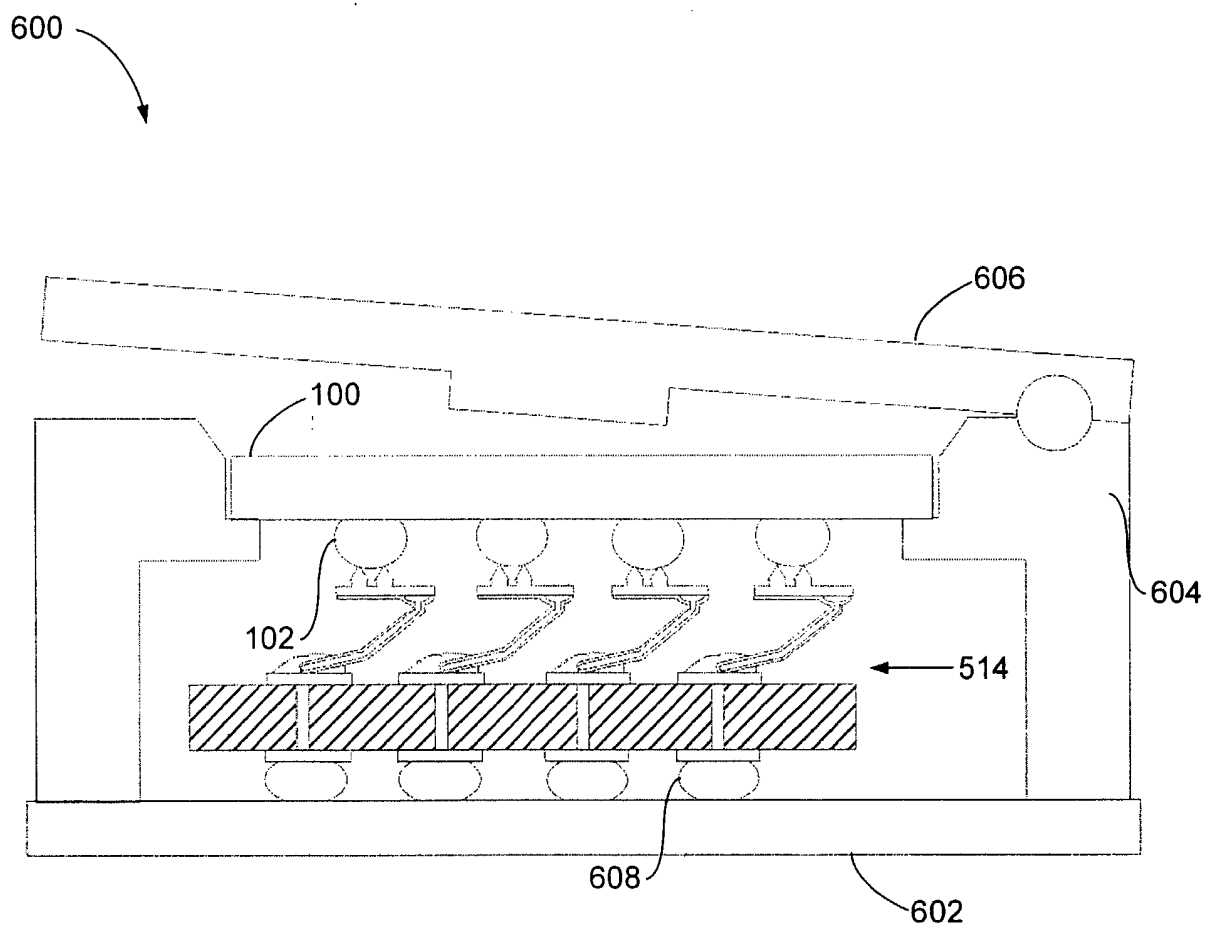


FIG. 6

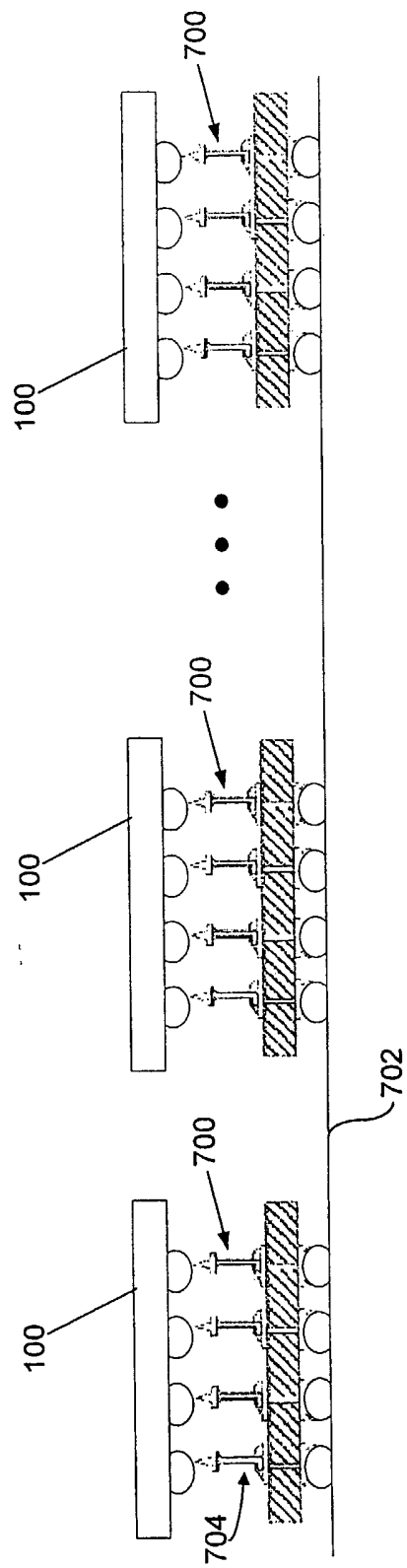


FIG. 7

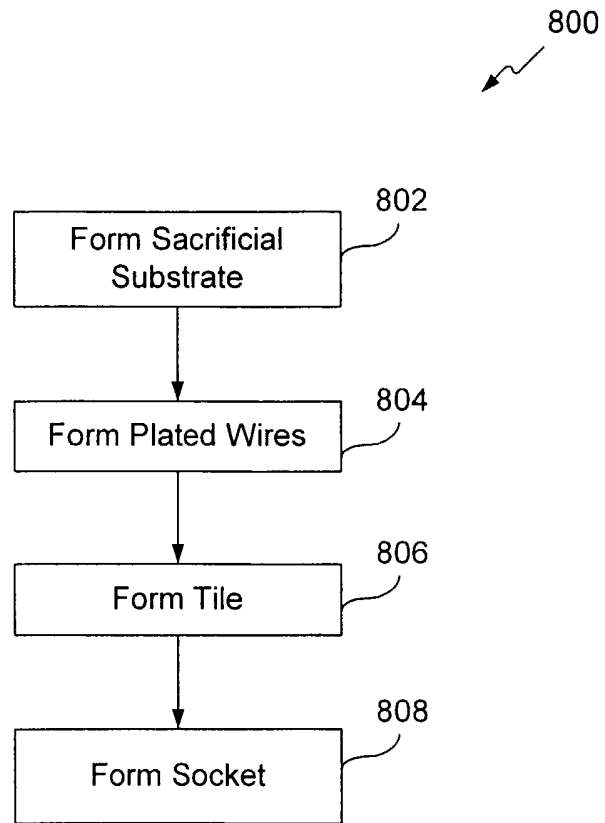


FIG. 8

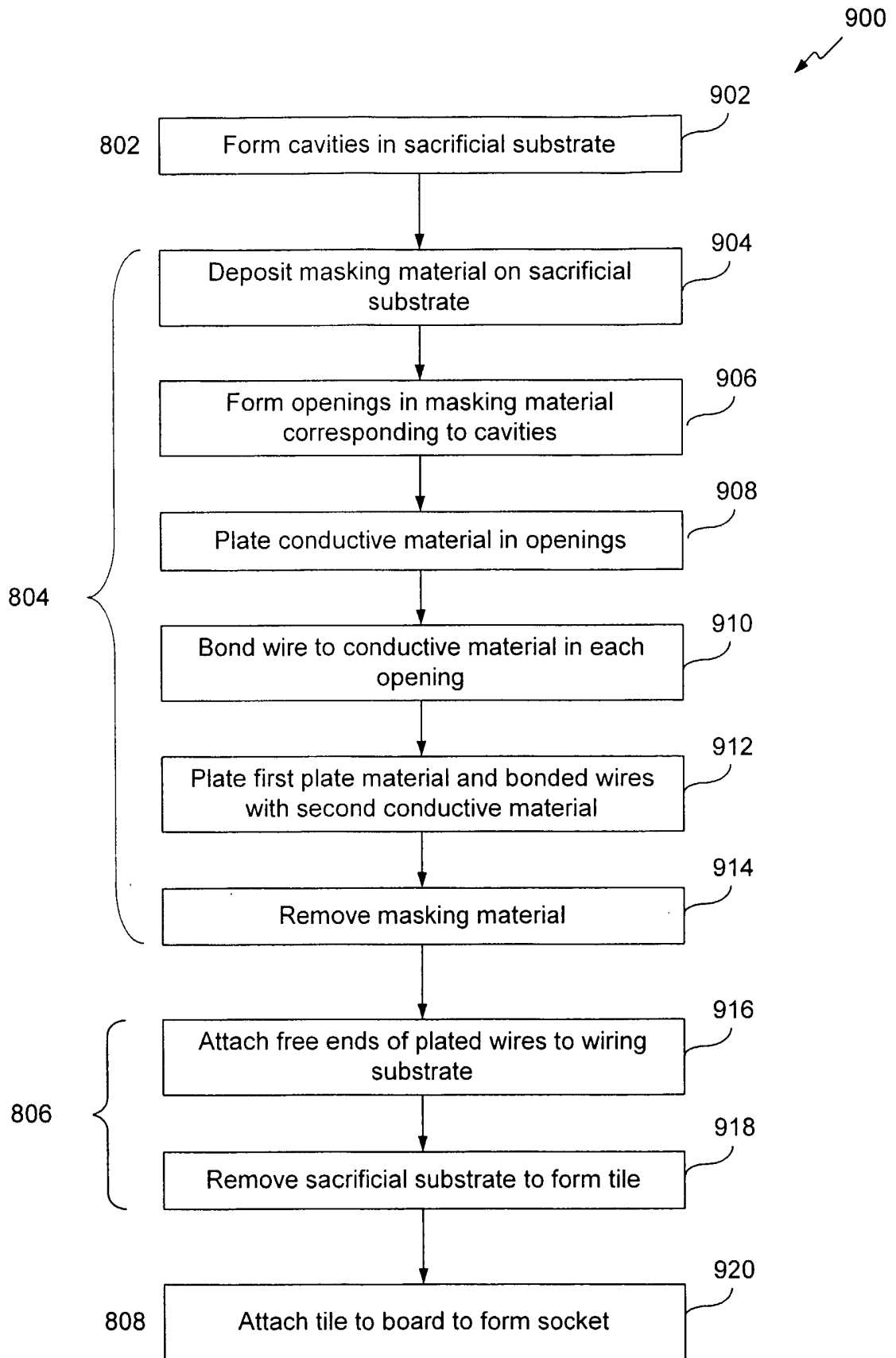


FIG. 9