(12) STANDARD PATENT (11) Application No. **AU 2005267809 B2**
(19) AUSTRALIAN PATENT OFFICE

(54) Title
System and method for interleaving

(51) International Patent Classification(s)
H04L 1/00 (2006.01)

(21) Application No: **2005267809** (22) Date of Filing: **2005.07.29**

(87) WIPO No: **WO06/015270**

(30) Priority Data

(31) Number	(32) Date	(33) Country
60/592,999	**2004.07.29**	**US**

(43) Publication Date: **2006.02.09**
(44) Accepted Journal Date: **2010.02.11**

(71) Applicant(s)
Qualcomm Incorporated

(72) Inventor(s)
Wang, Michael Mao;Ling, Fuyun;Murali, Ramaswamy;Vijayan, Rajiv

(74) Agent / Attorney
Madderns, First Floor 64 Hindmarsh Square, Adelaide, SA, 5000

(56) Related Art
US 6747948
US 6304581
US 6463556

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

CORRECTED VERSION

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
9 February 2006 (09.02.2006)

PCT

(10) International Publication Number
WO 2006/015270 A1

(51) International Patent Classification:
H04L 1/00 (2006.01)

(21) International Application Number:
PCT/US2005/027106

(22) International Filing Date: 29 July 2005 (29.07.2005)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/592,999 29 July 2004 (29.07.2004) US

(71) Applicant *(for all designated States except US)*: **QUALCOMM INCORPORATED** [US/US]; 5775 Morehouse Drive, San Diego, CA 92121 (US).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **WANG, Michael, Mao** [US/US]; 8514 Rumex Lane, San Diego, CA 92129 (US). **LING, Fuyun** [US/US]; 17264 Sangallo Lane, San Diego, CA 92127 (US). **MURALI, Ramaswamy** [IN/US]; 11723 Springside Road, San Diego, CA 92128 (US). **VIJAYAN, Rajiv** [US/US]; 9604 Babauta Road, San Diego, CA 92129 (US).

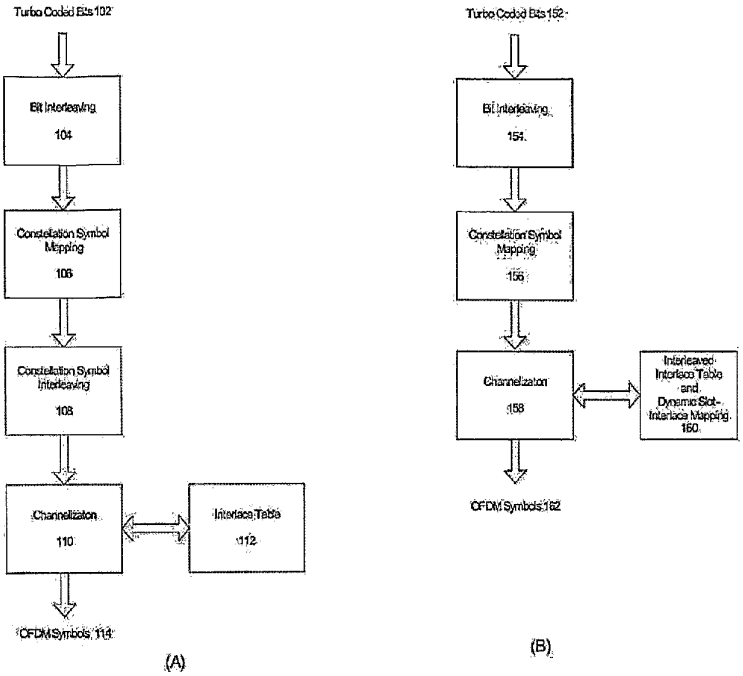
(74) Agents: **WADSWORTH, Philip R.,** et al.; QUALCOMM Incorporated, 5775 Morehouse Drive, San Diego, CA 92121-1714 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI,

[Continued on next page]

(54) Title: SYSTEM AND METHOD FOR INTERLEAVING



(57) Abstract: A system and method for frequency diversity uses interleaving. Subcarriers of an interlace are interleaved in a bit reversal fashion and the interlaces are interleaved in the bit reversal fashion.

WO 2006/015270 A1

FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *with international search report*

(48) Date of publication of this corrected version:
10 August 2006

(15) Information about Correction:
see PCT Gazette No. 32/2006 of 10 August 2006

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

SYSTEM AND METHOD FOR INTERLEAVING

Claim of Priority under 35 U.S.C. §119

[0001] The present Application for Patent claims priority to Provisional Application No. 60/592,999 entitled "METHOD OF CHANNEL INTERLEAVING IN A OFDM WIRELESS COMMUNICATIONS SYSTEM" filed July 29, 2004, and assigned to the assignee hereof and hereby expressly incorporated by reference herein.

BACKGROUND

Field

[0002] The present disclosed embodiments relates generally to wireless communications, and more specifically to channel interleaving in a wireless communications system.

Background

[0003] Orthogonal frequency division multiplexing (OFDM) is a technique for broadcasting high rate digital signals. In OFDM systems, a single high rate data stream is divided into several parallel low rate substreams, with each substream being used to modulate a respective subcarrier frequency. It should be noted that although the present invention is described in terms of quadrature amplitude modulation, it is equally applicable to phase shift keyed modulation systems.

[0004] The modulation technique used in OFDM systems is referred to as quadrature amplitude modulation (QAM), in which both the phase and the amplitude of the carrier frequency are modulated. In QAM modulation, complex QAM symbols are generated from plural data bits, with each symbol including a real number term and an imaginary number term and with each symbol representing the plural data bits from which it was generated. A plurality of QAM bits are transmitted together in a pattern that can be graphically represented by a complex plane. Typically, the pattern is referred to as a "constellation". By using QAM modulation, an OFDM system can improve its efficiency.

[0005] It happens that when a signal is broadcast, it can propagate to a receiver by more than one path. For example, a signal from a single transmitter can propagate along a straight line to a receiver, and it can also be reflected off of physical objects to

propagate along a different path to the receiver. Moreover, it happens that when a system uses a so-called "cellular" broadcasting technique to increase spectral efficiency, a signal intended for a received might be broadcast by more than one transmitter. Hence, the same signal will be transmitted to the receiver along more than one path. Such parallel propagation of signals, whether man-made (i.e., caused by broadcasting the same signal from more than one transmitter) or natural (i.e., caused by echoes) is referred to as "multipath". It can be readily appreciated that while cellular digital broadcasting is spectrally efficient, provisions must be made to effectively address multipath considerations.

[0006] Fortunately, OFDM systems that use QAM modulation are more effective in the presence of multipath conditions (which, as stated above, must arise when cellular broadcasting techniques are used) than are QAM modulation techniques in which only a single carrier frequency is used. More particularly, in single carrier QAM systems, a complex equalizer must be used to equalize channels that have echoes as strong as the primary path, and such equalization is difficult to execute. In contrast, in OFDM systems the need for complex equalizers can be eliminated altogether simply by inserting a guard interval of appropriate length at the beginning of each symbol. Accordingly, OFDM systems that use QAM modulation are preferred when multipath conditions are expected.

[0007] In a typical trellis coding scheme, the data stream is encoded with a convolutional encoder and then successive bits are combined in a bit group that will become a QAM symbol. Several bits are in a group, with the number of bits per group being defined by an integer "m" (hence, each group is referred to as having an "m-ary" dimension). Typically, the value of "m" is four, five, six, or seven, although it can be more or less.

[0008] After grouping the bits into multi-bit symbols, the symbols are interleaved. By "interleaving" is meant that the symbol stream is rearranged in sequence, to thereby randomize potential errors caused by channel degradation. To illustrate, suppose five words are to be transmitted. If, during transmission of a non-interleaved signal, a temporary channel disturbance occurs. Under these circumstances, an entire word can be lost before the channel disturbance abates, and it can be difficult if not impossible to know what information had been conveyed by the lost word.

[0009] In contrast, if the letters of the five words are sequentially rearranged (i.e., "interleaved") prior to transmission and a channel disturbance occurs, several letters

might be lost, perhaps one letter per word. Upon decoding the rearranged letters, however, all five words would appear, albeit with several of the words missing letters. It will be readily appreciated that under these circumstances, it would be relatively easy for a digital decoder to recover the data substantially in its entirety. After interleaving the m-ary symbols, the symbols are mapped to complex symbols using QAM principles noted above, multiplexed into their respective sub-carrier channels, and transmitted.

SUMMARY

According to a first aspect of the present invention, there is provided a method for interleaving, including:

interleaving subcarriers of an interlace in a bit reversal fashion, involving mapping symbols of a constellation symbol sequence into corresponding subcarriers in a sequential linear fashion according to an assigned slot index; and

interleaving the interlaces in the bit reversal fashion, wherein the bit reversal fashion is a reduce-set bit reversal operation if the number of subcarriers is not a power of two.

According to a second aspect of the present invention, there is provided a processor configured to:

interleave subcarriers of an interlace in a bit reversal fashion, involving mapping symbols of a constellation symbol sequence into corresponding subcarriers in a sequential linear fashion according to an assigned slot index; and

interleave the interlaces in the bit reversal fashion, wherein the bit reversal fashion is a reduce-set bit reversal operation if the number of subcarriers is not a power of two.

According to a third aspect of the present invention, there is provided a processor, including:

means for interleaving subcarriers of an interlace in a bit reversal fashion, involving mapping symbols of a constellation symbol sequence into corresponding subcarriers in a sequential linear fashion according to an assigned slot index; and

means for interleaving the interlaces in the bit reversal fashion,

wherein the bit reversal fashion is a reduce-set bit reversal operation if the number of subcarriers is not a power of two.

According to a fourth aspect of the present invention, there is provided a computer readable storage medium encoded with a computer program, the computer program including instructions that when executed by data processing apparatus cause the data processing apparatus to perform operations, the operations including:

interleaving subcarriers of an interlace in a bit reversal fashion, involving mapping symbols of a constellation symbol sequence into corresponding subcarriers in a sequential linear fashion according to an assigned slot index; and

interleaving the interlaces in the bit reversal fashion, wherein the bit reversal fashion is a reduce-set bit reversal operation if the number of subcarriers is not a power of two.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A shows a channel interleaver in accordance with an embodiment;

FIG. 1B shows a channel interleaver in accordance with another embodiment;

FIG. 2A shows code bits of a turbo packet placed into an interleaving buffer in accordance with an embodiment;

FIG. 2B shows an interleaver buffer arranged into an N/m rows by m columns matrix in accordance with an embodiment;

FIG. 3 illustrates an interleaved interlace table in accordance with an embodiment;

FIG. 4 shows a channelization diagram in accordance with an embodiment;

FIG. 5 shows a channelization diagram with all one's shifting sequence resulting in long runs of good and poor channel estimates for a particular slot, in accordance with an embodiment; and

FIG. 6 shows a Channelization diagram with all two's shifting sequence resulting in evenly spread good and poor channel estimate interlaces; and

FIG. 7 shows a wireless device configured to implement interleaving in accordance with an embodiment.

DETAILED DESCRIPTION

In an embodiment, a channel interleaver comprises a bit interleaver and a symbol interleaver. Figure 1 shows two types of channel interleaving schemes. Both schemes use bit interleaving and interlacing to achieve maximum channel diversity.

Figure 1A shows a channel interleaver in accordance with an embodiment. Figure 1B shows a channel interleaver in accordance with another embodiment. The interleaver of figure 1B uses bit-interleaver solely to achieve m-ary modulation diversity and uses a two-dimension interleaved interlace table and run-time slot-to-interlace mapping to achieve frequency diversity which provides better interleaving performance without the need for explicit symbol interleaving.

Figure 1A shows Turbo coded bits 102 input into bit interleaving block 104. Bit interleaving block 104 outputs interleaved bits, which are input into constellation symbol mapping block 106. Constellation symbol mapping block 106 outputs constellation symbol mapped bits, which are input into constellation symbol interleaving block 108. Constellation symbol interleaving block 108 outputs constellation symbol interleaved bits into channelization block 110. Channelization block 110 interlaces the constellation symbol interleaved bits using an interlace table 112 and outputs OFDM symbols 114.

Figure 1B shows Turbo coded bits 152 input into bit interleaving block 154. Bit interleaving block 154 outputs interleaved bits, which are input into constellation symbol mapping block 156.

Constellation symbol mapping block 15 outputs constellation symbol mapped bits, which are input into channelization block 158. Channelization block 158 channelizes the constellation symbol interleaved bits using an interleaved interlace table and dynamic slot-interlace mapping 160 and outputs OFDM symbols 162.

Bit Interleaving for modulation diversity

The interleaver of figure 1B uses bit interleaving 154 to achieve modulation diversity. The code bits 152 of a turbo packet are interleaved in such a pattern that adjacent code bits are mapped into different constellation symbols. For example, for 2m-Ary modulation, the N bit interleaver buffer are divided into N/m blocks. Adjacent code bits are written into adjacent blocks sequentially and then are read out one by one from the beginning of the buffer to the end in the sequential order, as shown in Figure 2A (Top). This guarantees that adjacent code bits be mapped to different constellation symbols. Equivalently, as is illustrated in Figure 2B (Bottom), the interleaver buffer is arranged into an N/m rows by m columns matrix. Code bits are written into the buffer column by column and are read out row by row. To avoid the adjacent code bit to be mapped to the same bit position of the constellation symbol due to the fact that certain bits of a constellation symbol are more reliable than the others for 16QAM depending on the mapping, for example, the first and third bits are more reliable than the second and fourth bits, rows shall be read out from left to right and right to left alternatively.

Figure 2A shows code bits of a turbo packet 202 placed into an interleaving buffer 204 in accordance with an embodiment. Figure 2B is an illustration of bit interleaving operation in accordance with an embodiment. Code bits of a Turbo packet 250 are placed into an interleaving buffer 252 as shown in figure 2B. The interleaving buffer 252 is transformed by swapping the second and third columns, thereby creating interleaving buffer 254, wherein m=4, in accordance with an embodiment. Interleaved code bits of a Turbo packet 256 are read from the interleaving buffer 254.

For simplicity, a fixed m=4 may be used, if the highest modulation level is 16 and if code bit length is always divisible by 4. In this case, to improve the separation for QPSK, the middle two columns are swapped before being read out. This procedure is depicted in Figure 2B (Bottom). It would be apparent to those skilled in the art that any two columns may be swapped. It would also be apparent to those skilled in the art that the columns may be placed in any order. It would also be apparent to those skilled in the art that the rows may be placed in any order.

In another embodiment, as a first step, the code bits of a turbo packet 202 are distributed into groups. Note that the embodiments of both figure 2A and figure 2B also distribute the code bits into groups. However, rather than simply swapping rows or columns, the code bits within each group are shuffled according to a group bit order for

each given group. Thus, the order of four groups of 16 code bits after being distributed into groups may be {1, 5, 9, 13} {2, 6, 10, 14} {3, 7, 11, 15} {4, 8, 12, 16} using a simple linear ordering of the groups and the order of the four groups of 16 code bits after shuffling may be {13, 9, 5, 1} {2, 10, 6, 14} {11, 7, 15, 3} {12, 8, 4, 16}. Note that swapping rows or columns would be a regressive case of this intra-group shuffling.

[0028] Interleaved Interlace for frequency diversity

[0029] In accordance with an embodiment, the channel interleaver uses interleaved interlace for constellation symbol interleaving to achieve frequency diversity. This eliminates the need for explicit constellation symbol interleaving. The interleaving is performed at two levels:

[0030] · Within or Intra Interlace Interleaving: In an embodiment, 500 subcarriers of an interlace are interleaved in a bit-reversal fashion.

[0031] · Between or Inter Interlace Interleaving: In an embodiment, eight interlaces are interleaved in a bit-reversal fashion.

[0032] It would be apparent to those skilled in the art that the number of subcarriers can be other than 500. It would also be apparent to those skilled in the art that the number of interlaces can be other than eight.

[0033] Note that since 500 is not power of 2, a reduced-set bit reversal operation shall be used in accordance with an embodiment. The following code shows the operation:

```
[0034]  vector<int> reducedSetBitRev(int n)
[0035]  {
[0036]      int m=exponent(n);
[0037]      vector<int> y(n);
[0038]      for (int i=0, j=0; i<n; i++,j++)
[0039]      {
[0040]          int k;
[0041]          for (; (k=bitRev(j,m))>=n; j++);
[0042]          y[i]=k;
[0043]      }
[0044]      return y;
```

[0045] }

[0046] where n=500, m is the smallest integer such that $2^m > n$ which is 8, and bitRev is the regular bit reversal operation.

[0047] The symbols of the constellation symbol sequence of a data channel is mapped into the corresponding subcarriers in a sequential linear fashion according to the assigned slot index, determined by a Channelizer, using the interlace table as is depicted in Figure 3, in accordance with an embodiment.

[0048] Figure 3 illustrates an interleaved interlace table in accordance with an embodiment. Turbo packet 302, constellation symbols 304, and interleaved interlace table 306 are shown. Also shown are interlace 3 (308), interlace 4 (310), interlace 2 (312), interlace 6 (314), interlace 1 (316), interlace 5 (318), interlace 3 (320), and interlace 7 (322).

[0049] In an embodiment, one out of the eight interlaces is used for pilot, i.e., Interlace 2 and Interlace 6 is used alternatively for pilot. As a result, the Channelizer can use seven interlaces for scheduling. For convenience, the Channelizer uses *Slot* as a scheduling unit. A slot is defined as one interlace of an OFDM symbol. An *Interlace Table* is used to map a slot to a particular interlace. Since eight interlaces are used, there are then eight slots. Seven slots will be set aside for use for Channelization and one slot for Pilot. Without loss of generality, Slot 0 is used for the Pilot and Slots 1 to 7 are used for Channelization, as is shown in Figure 4 where the vertical axis is the slot index 402, the horizontal axis is the OFDM symbol index 404 and the bold-faced entry is the interlace index assigned to the corresponding slot at an OFDM symbol time.

[0050] Figure 4 shows a channelization diagram in accordance with an embodiment. Figure 4 shows the slot indices reserved for the scheduler 406 and the slot index reserved for the Pilot 408. The bold faced entries are interlace index numbers. The number with square is the interlace adjacent to pilot and consequently with good channel estimate.

[0051] The number surrounded with a square is the interlace adjacent to the pilot and consequently with good channel estimate. Since the Scheduler always assigns a chunk of contiguous slots and OFDM symbols to a data channel, it is clear that due to the inter-interlace interleaving, the contiguous slots that are assigned to a data channel will

be mapped to discontinuous interlaces. More frequency diversity gain can then be achieved.

[0052] However, this static assignment (i.e., the slot to physical interlace mapping table1 does not change over time) does suffer one problem. That is, if a data channel assignment block (assuming rectangular) occupies multiple OFDM symbols, the interlaces assigned to the data channel does not change over the time, resulting in loss of frequency diversity. The remedy is simply cyclically shifting the Scheduler interlace table (i.e., excluding the Pilot interlace) from OFDM symbol to OFDM symbol.

[0053] Figure 5 depicts the operation of shifting the Scheduler interlace table once per OFDM symbol. This scheme successfully destroys the static interlace assignment problem, i.e., a particular slot is mapped to different interlaces at different OFDM symbol time.

[0054] Figure 5 shows a channelization diagram with all one's shifting sequence resulting in long runs of good and poor channel estimates for a particular slot 502, in accordance with an embodiment. Figure 5 shows the slot indices reserved for the scheduler 506 and the slot index reserved for the Pilot 508. Slot symbol index 504 is shown on the horizontal axis.

[0055] However, it is noticed that slots are assigned four continuous interlaces with good channel estimates followed by long runs of interlaces with poor channel estimates in contrast to the preferred patterns of short runs of good channel estimate interlaces and short runs of interlaces with poor channel estimates. In the figure, the interlace that is adjacent to the pilot interlace is marked with a square. A solution to the long runs of good and poor channel estimates problem is to use a shifting sequence other than the all one's sequence. There are many sequences can be used to fulfill this task. The simplest sequence is the all two's sequence, i.e., the Scheduler interlace table is shifted twice instead of once per OFDM symbol. The result is shown in Figure 6 which significantly improves the Channelizer interlace pattern. Note that this pattern repeats every $2 \times 7 = 14$ OFDM symbols, where 2 is the Pilot interlace staggering period and 7 is the Channelizer interlace shifting period.

[0056] To simplify the operation at both transmitters and receivers, a simple formula can be used to determine the mapping from slot to interlace at a given OFDM symbol time

---

[1] The Scheduler slot table does not include the Pilot slot.

[0057] $i = \Re'\{(N - ((R \times t)\%N) + s - 1)\%N\}$

where

[0058] · $N = I - 1$ is the number of interlaces used for traffic data scheduling, where I is the total number of interlaces;

[0059] · $i \in \{0,1,\cdots,I-1\}$, excluding the pilot interlace, is the interlace index that Slot s at OFDM symbol t maps to;

[0060] · $t = 0,1,\cdots,T-1$ is the OFDM symbol index in a super frame, where T is the total number of OFDM symbols in a frame2;

[0061] · $s = 1,2,\cdots,S-1$ s is the slot index where S is the total number of slots;

[0062] · R is the number of shifts per OFDM symbol;

[0063] · $\Re'$ is the reduced-set bit-reversal operator. That is, the interlace used by the Pilot shall be excluded from the bit-reversal operation.

[0064] Example: In an embodiment, I=8, R=2. The corresponding Slot-Interlace mapping formula becomes

[0065] $i = \Re'\{(7 - ((2 \times t)\%7) + s - 1)\%7\}$

[0066] where $\Re'$ corresponds to the following table:

$x \Rightarrow \Re'\{x\}$
$0 \Rightarrow 0$
$1 \Rightarrow 4$
$2 \Rightarrow 2$ or 6
$3 \Rightarrow 1$
$4 \Rightarrow 5$
$5 \Rightarrow 3$
[0067] $6 \Rightarrow 7$

[0068] This table can be generated by the following code:

```
[0069] int reducedSetBitRev(int x, int exclude, int n)
[0070] {
[0071]         int m=exponent(n);
```

---

[2] OFDM symbol index in a superframe instead of in a frame gives additional diversity to frames since the number of OFDM symbols in a frame in the current design is not divisible by 14.

```
[0072]      int y;
[0073]      for (int i=0; j=0; i<=x; i++, j++)
[0074]      {
[0075]          for (; (y=bitRev(j, m))==exclude; j++);
[0076]      }
[0077]      return y;
[0078]  }
```

[0079] where m=3 and bitRev is the regular bit reversal operation.

[0080] For OFDM symbol t=11, Pilot uses Interlace 6. The mapping between Slot and Interlace becomes:

[0081] · Slot 1 maps to interlace of $\Re'\{(7-(2\times 11)\%7+1-1)\%7\}=\Re\{6\}=7$;

[0082] ·Slot 2 maps to interlace of $\Re'\{(7-(2\times 11)\%7+2-1)\%7\}=\Re\{0\}=0$;

[0083] ·Slot 3 maps to interlace of $\Re'\{(7-(2\times 11)\%7+3-1)\%7\}=\Re\{1\}=4$;

[0084] ·Slot 4 maps to interlace of $\Re'\{(7-(2\times 11)\%7+4-1)\%7\}=\Re\{2\}=2$;

[0085] ·Slot 5 maps to interlace of $\Re'\{(7-(2\times 11)\%7+5-1)\%7\}=\Re\{3\}=1$;

[0086] ·Slot 6 maps to interlace of $\Re'\{(7-(2\times 11)\%7+6-1)\%7\}=\Re\{4\}=5$;

[0087] ·Slot 7 maps to interlace of $\Re'\{(7-(2\times 11)\%7+7-1)\%7\}=\Re\{5\}=3$.

[0088] The resulting mapping agrees with the mapping in Figure 6. Figure 6 shows a Channelization diagram with all two's shifting sequence resulting in evenly spread good and poor channel estimate interlaces.

[0089] In accordance with an embodiment, an interleaver has the following features:

[0090] The bit interleaver is designed to taking advantage of m-Ary modulation diversity by interleaving the code bits into different modulation symbols;

[0091] The "symbol interleaving" designed to achieve frequency diversity by INTRA-interlace interleaving and INTER-interlace interleaving;

[0092] Additional frequency diversity gain and channel estimation gain are achieved by changing the slot-interlace mapping table from OFDM symbol to OFDM symbol. A simple rotation sequence is proposed to achieve this goal.

[0093] Figure 7 shows a wireless device configured to implement interleaving in accordance with an embodiment. Wireless device 702 comprises an antenna 704, duplexer 706, a receiver 708, a transmitter 710, processor 712, and memory 714. Processor 712 is capable of performing interleaving in accordance with an embodiment. The processor 712 uses memory 714 for buffers or data structures to perform its operations.

[0094] Those of skill in the art would understand that information and signals may be represented using any of a variety of different technologies and techniques. For example, data, instructions, commands, information, signals, bits, symbols, and chips that may be referenced throughout the above description may be represented by voltages, currents, electromagnetic waves, magnetic fields or particles, optical fields or particles, or any combination thereof.

[0095] Those of skill would further appreciate that the various illustrative logical blocks, modules, circuits, and algorithm steps described in connection with the embodiments disclosed herein may be implemented as electronic hardware, computer software, or combinations of both. To clearly illustrate this interchangeability of hardware and software, various illustrative components, blocks, modules, circuits, and steps have been described above generally in terms of their functionality. Whether such functionality is implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system. Skilled artisans may implement the described functionality in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the present invention.

[0096] The various illustrative logical blocks, modules, and circuits described in connection with the embodiments disclosed herein may be implemented or performed with a general purpose processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general purpose processor may be a microprocessor, but in the alternative, the processor may be any conventional processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, a plurality of

2005267809 11 Jan 2010

microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

The steps of a method or algorithm described in connection with the embodiments disclosed herein may be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module may reside in RAM memory, flash memory, ROM memory, EPROM memory, EEPROM memory, registers, hard disk, a removable disk, a CD-ROM, or any other form of storage medium known in the art. An exemplary storage medium is coupled to the processor such the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium may be integral to the processor. The processor and the storage medium may reside in an ASIC. The ASIC may reside in a user terminal, hi the alternative, the processor and the storage medium may reside as discrete components in a user terminal.

The previous description of the disclosed embodiments is provided to enable any person skilled in the art to make or use the present invention. Various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without departing from the spirit or scope of the invention. Thus, the present invention is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

It will be understood that the term "comprise" and any of its derivatives (eg comprises, comprising) as used in this specification is to be taken to be inclusive of features to which it refers, and is not meant to exclude the presence of any additional features unless otherwise stated or implied.

The reference to any prior art in this specification is not, and should not be taken as, an acknowledgement of any form of suggestion that such prior art forms part of the common general knowledge.

2005267809 11 Jan 2010

THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:

1. A method for interleaving, including:

interleaving subcarriers of an interlace in a bit reversal fashion, involving mapping symbols of a constellation symbol sequence into corresponding subcarriers in a sequential linear fashion according to an assigned slot index; and

interleaving the interlaces in the bit reversal fashion, wherein the bit reversal fashion is a reduce-set bit reversal operation if the number of subcarriers is not a power of two.

2. The method of claim 1 wherein the number of subcarriers is 500.

3. The method of any one of claims 1 or 2 wherein the number of interlaces is eight.

4. A processor configured to:

interleave subcarriers of an interlace in a bit reversal fashion, involving mapping symbols of a constellation symbol sequence into corresponding subcarriers in a sequential linear fashion according to an assigned slot index; and

interleave the interlaces in the bit reversal fashion, wherein the bit reversal fashion is a reduce-set bit reversal operation if the number of subcarriers is not a power of two.

5. The processor of claim 4 wherein the number of subcarriers is 500.

6. The processor of any one of claims 4 or 5 wherein the number of interlaces is eight.

7. A processor, including:

means for interleaving subcarriers of an interlace in a bit reversal fashion, involving mapping symbols of a constellation symbol sequence into corresponding subcarriers in a sequential linear fashion according to an assigned slot index; and

means for interleaving the interlaces in the bit reversal fashion,

wherein the bit reversal fashion is a reduce-set bit reversal operation if the number of subcarriers is not a power of two.

8. The processor of claim 7 wherein the number of subcarriers is 500.

9. The processor of any one of claims 7 or 8 wherein the number of interlaces is 8.

2005267809 11 Jan 2010

10. A computer readable storage medium encoded with a computer program, the computer program including instructions that when executed by data processing apparatus cause the data processing apparatus to perform operations, the operations including:

interleaving subcarriers of an interlace in a bit reversal fashion, involving mapping symbols of a constellation symbol sequence into corresponding subcarriers in a sequential linear fashion according to an assigned slot index; and

interleaving the interlaces in the bit reversal fashion, wherein the bit reversal fashion is a reduce-set bit reversal operation if the number of subcarriers is not a power of two.

11. The computer readable storage medium of claim 10 wherein the number of subcarriers is 500.

12. The computer readable storage medium of any one of claims 10 or 11 wherein the number of interlaces is 8.

13. A method as claimed in claim 1, substantially as herein described with reference to the accompanying drawings.

14. A processor as claimed in claim 4, substantially as herein described with reference to the accompanying drawings.

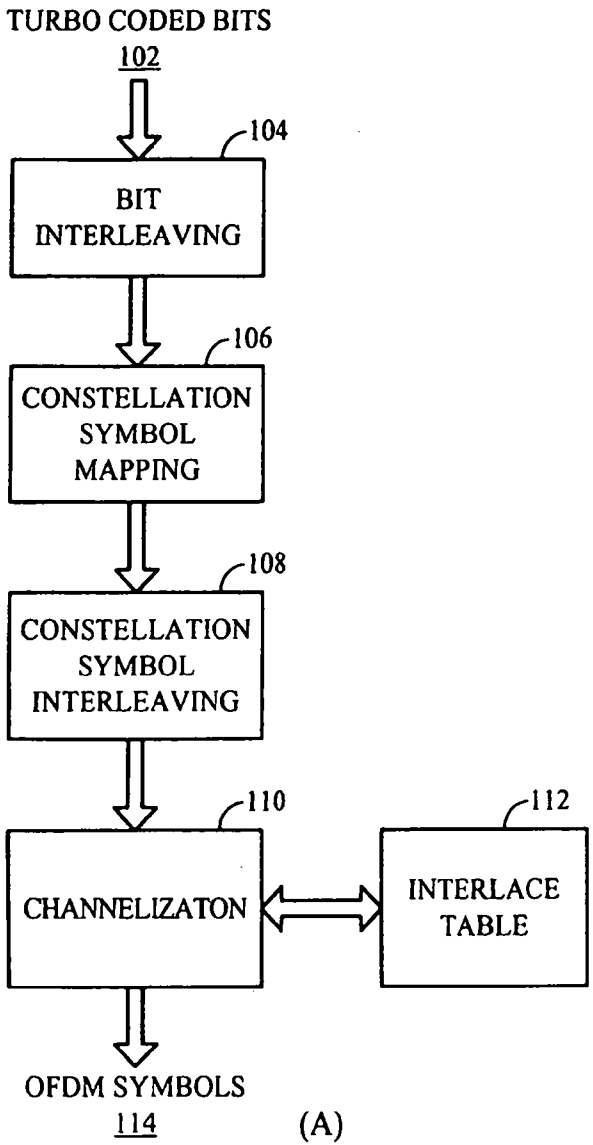
15. A processor as claimed in claim 7, substantially as herein described with reference to the accompanying drawings.

16. A computer readable storage medium as claimed in claim 10, substantially as herein described with reference to the accompanying drawings.

17. A method substantially as herein described with reference to any one of the embodiments of the invention illustrated in the accompanying drawings.

18. A processor substantially as herein described with reference to any one of the embodiments of the invention illustrated in the accompanying drawings.

19. A computer readable storage medium substantially as herein described with reference to any one of the embodiments of the invention illustrated in the accompanying drawings.


TURBO CODED BITS
102
104
BIT INTERLEAVING
106
CONSTELLATION SYMBOL MAPPING
108
CONSTELLATION SYMBOL INTERLEAVING
110
CHANNELIZATON
112
INTERLACE TABLE
OFDM SYMBOLS
114
(A)

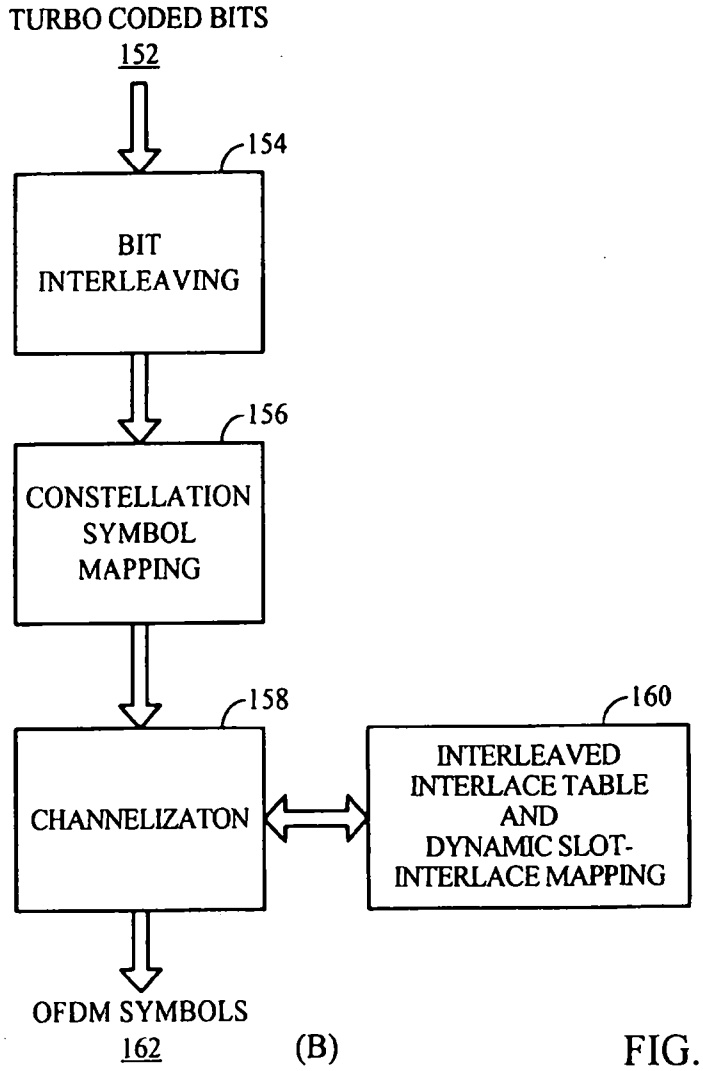

TURBO CODED BITS
152
154
BIT INTERLEAVING
156
CONSTELLATION SYMBOL MAPPING
158
CHANNELIZATON
160
INTERLEAVED INTERLACE TABLE AND DYNAMIC SLOT-INTERLACE MAPPING
OFDM SYMBOLS
162
(B)

FIG. 1

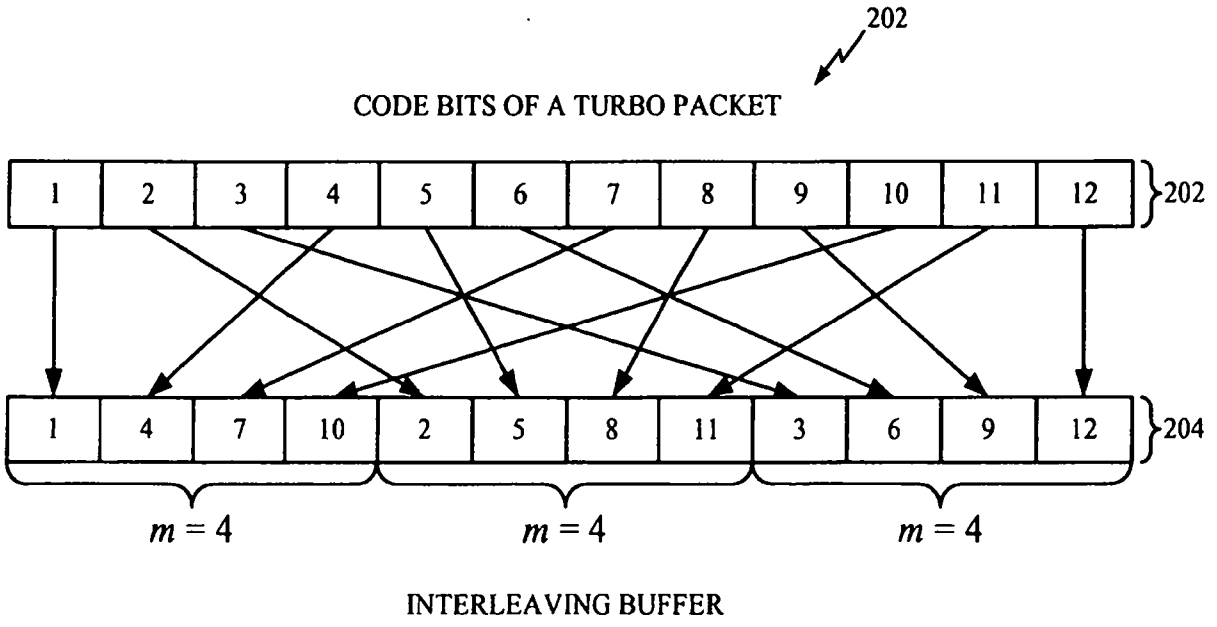

202
CODE BITS OF A TURBO PACKET
1 2 3 4 5 6 7 8 9 10 11 12
202
1 4 7 10 2 5 8 11 3 6 9 12
204
m = 4
m = 4
m = 4
INTERLEAVING BUFFER

FIG. 2A

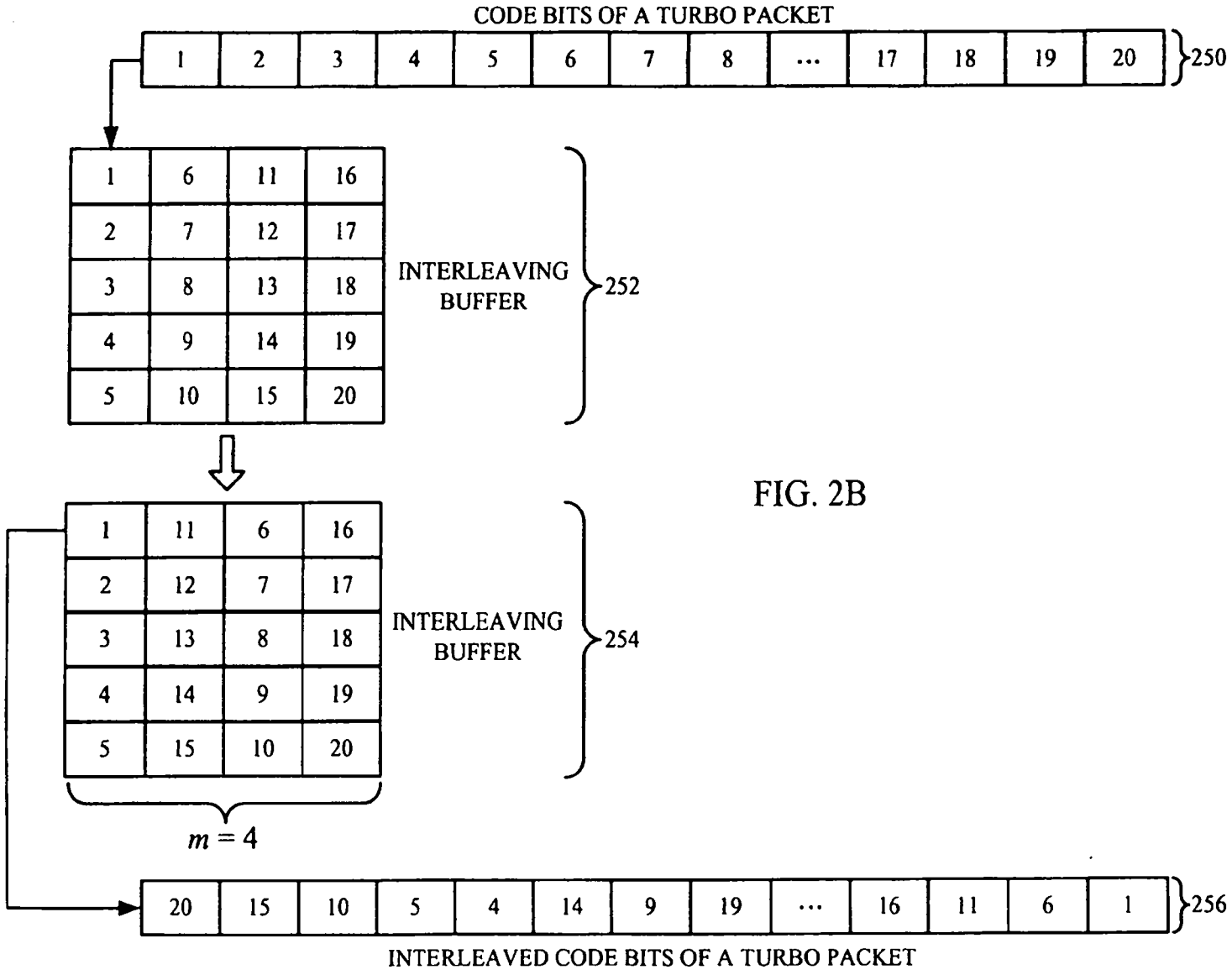

CODE BITS OF A TURBO PACKET
1 2 3 4 5 6 7 8 ... 17 18 19 20
250
1 6 11 16
2 7 12 17
3 8 13 18
4 9 14 19
5 10 15 20
INTERLEAVING BUFFER
252
1 11 6 16
2 12 7 17
3 13 8 18
4 14 9 19
5 15 10 20
INTERLEAVING BUFFER
254
m = 4
20 15 10 5 4 14 9 19 ... 16 11 6 1
256
INTERLEAVED CODE BITS OF A TURBO PACKET

FIG. 2B

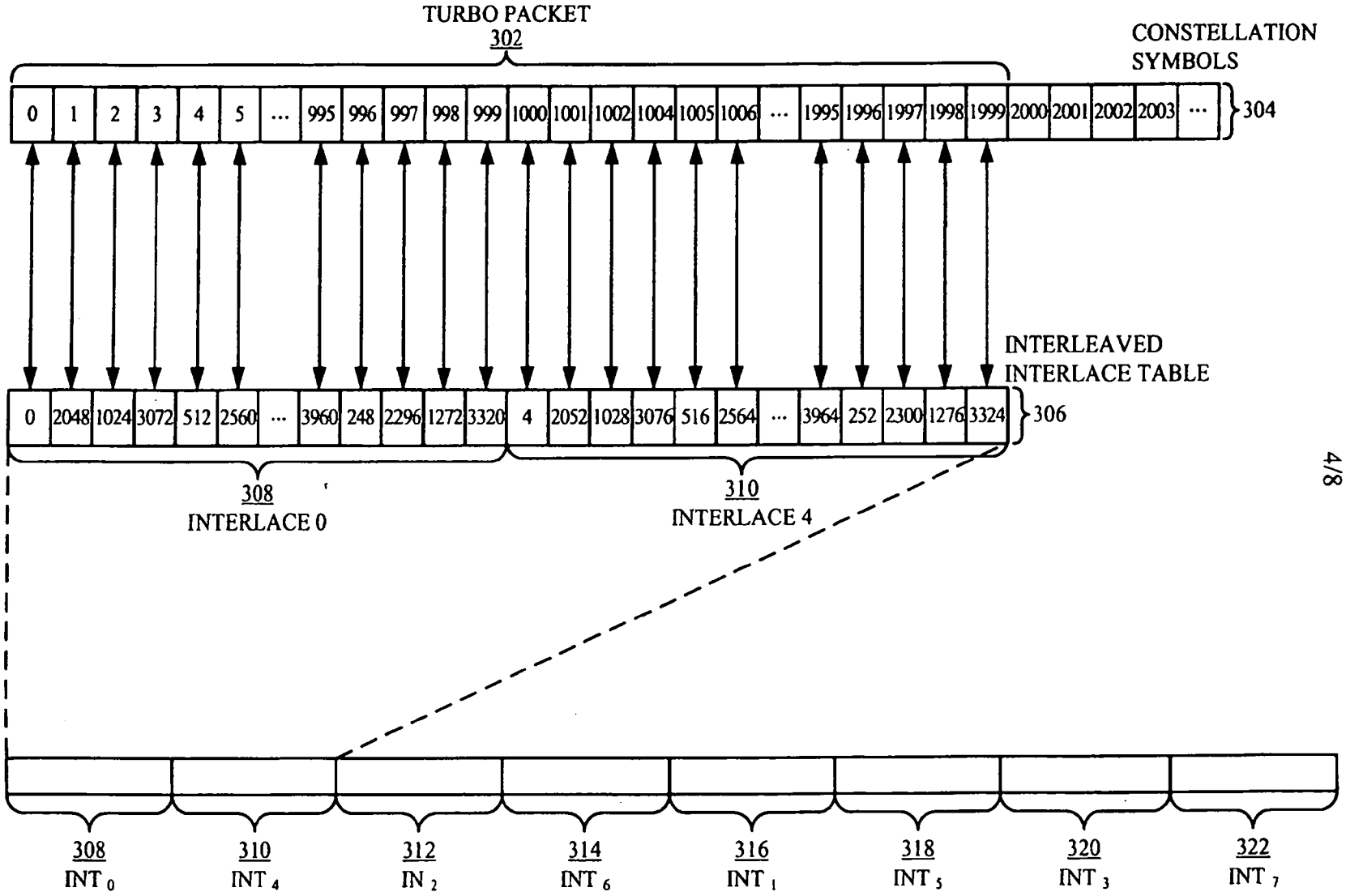

TURBO PACKET
302
CONSTELLATION
SYMBOLS
0 1 2 3 4 5 ... 995 996 997 998 999 1000 1001 1002 1004 1005 1006 ... 1995 1996 1997 1998 1999 2000 2001 2002 2003 ...
304
INTERLEAVED
INTERLACE TABLE
0 2048 1024 3072 512 2560 ... 3960 248 2296 1272 3320 4 2052 1028 3076 516 2564 ... 3964 252 2300 1276 3324
306
308
INTERLACE 0
310
INTERLACE 4
308 INT 0
310 INT 4
312 IN 2
314 INT 6
316 INT 1
318 INT 5
320 INT 3
322 INT 7

FIG. 3

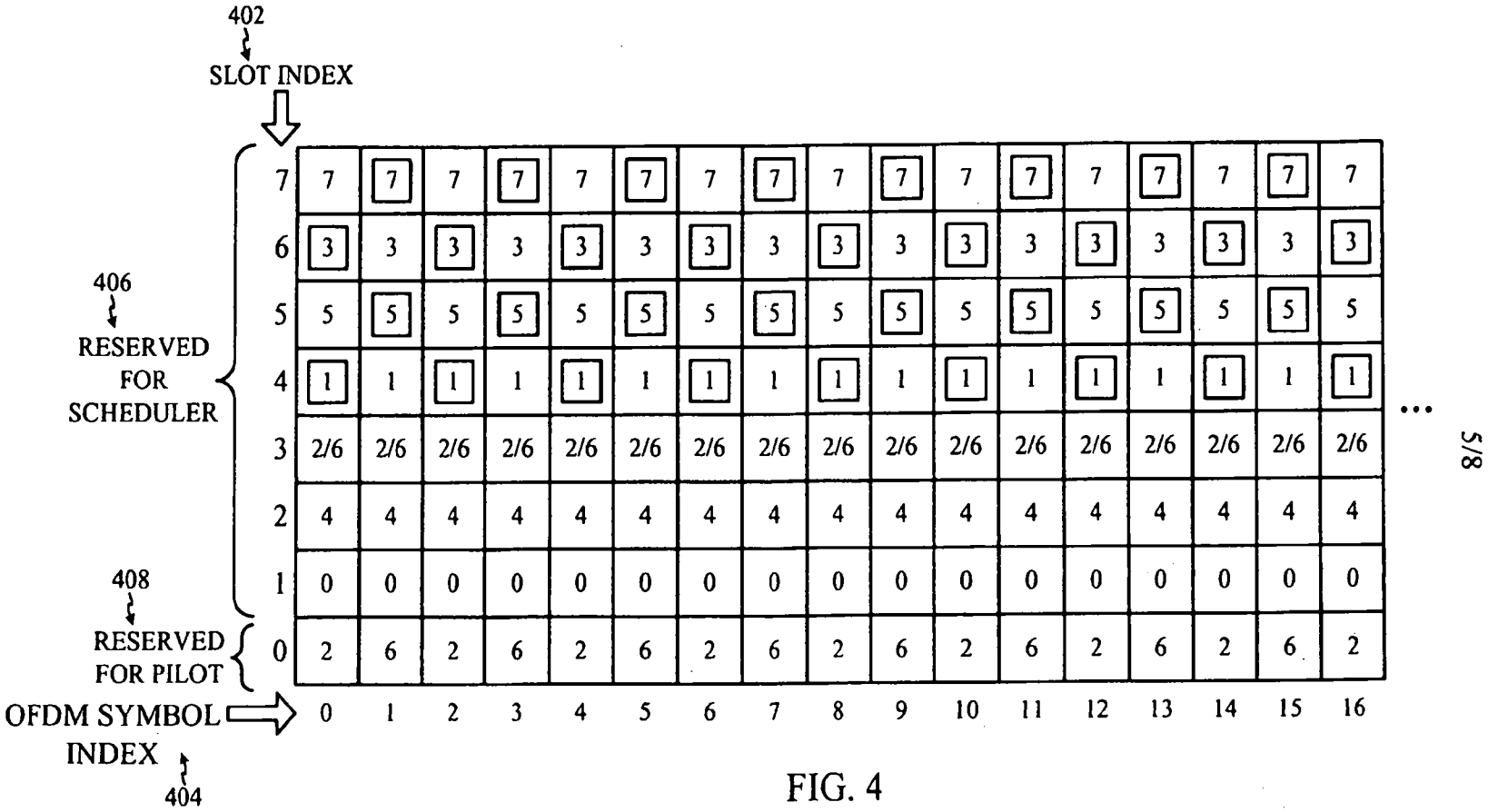

402
SLOT INDEX
406
RESERVED FOR SCHEDULER
408
RESERVED FOR PILOT
OFDM SYMBOL INDEX
404
7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7
6 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3
5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5
4 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
3 2/6 2/6 2/6 2/6 2/6 2/6 2/6 2/6 2/6 2/6 2/6 2/6 2/6 2/6 2/6 2/6 2/6
2 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 2 6 2 6 2 6 2 6 2 6 2 6 2 6 2 6 2
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
...

FIG. 4

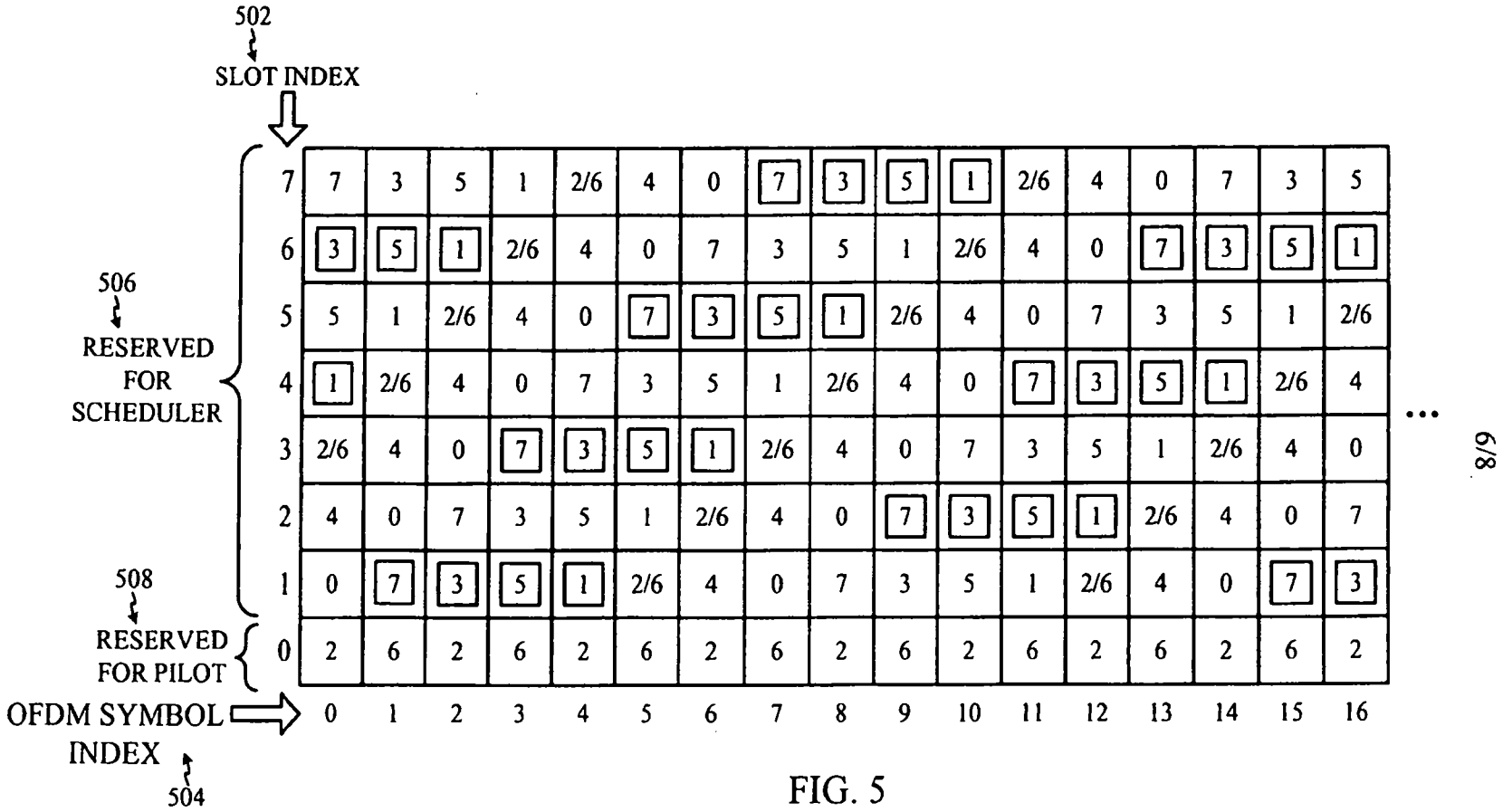

502
SLOT INDEX
506
RESERVED FOR SCHEDULER
508
RESERVED FOR PILOT
OFDM SYMBOL INDEX
504
7 7 3 5 1 2/6 4 0 7 3 5 1 2/6 4 0 7 3 5
6 3 5 1 2/6 4 0 7 3 5 1 2/6 4 0 7 3 5 1
5 5 1 2/6 4 0 7 3 5 1 2/6 4 0 7 3 5 1 2/6
4 1 2/6 4 0 7 3 5 1 2/6 4 0 7 3 5 1 2/6 4
3 2/6 4 0 7 3 5 1 2/6 4 0 7 3 5 1 2/6 4 0
2 4 0 7 3 5 1 2/6 4 0 7 3 5 1 2/6 4 0 7
1 0 7 3 5 1 2/6 4 0 7 3 5 1 2/6 4 0 7 3
0 2 6 2 6 2 6 2 6 2 6 2 6 2 6 2 6 2
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

FIG. 5

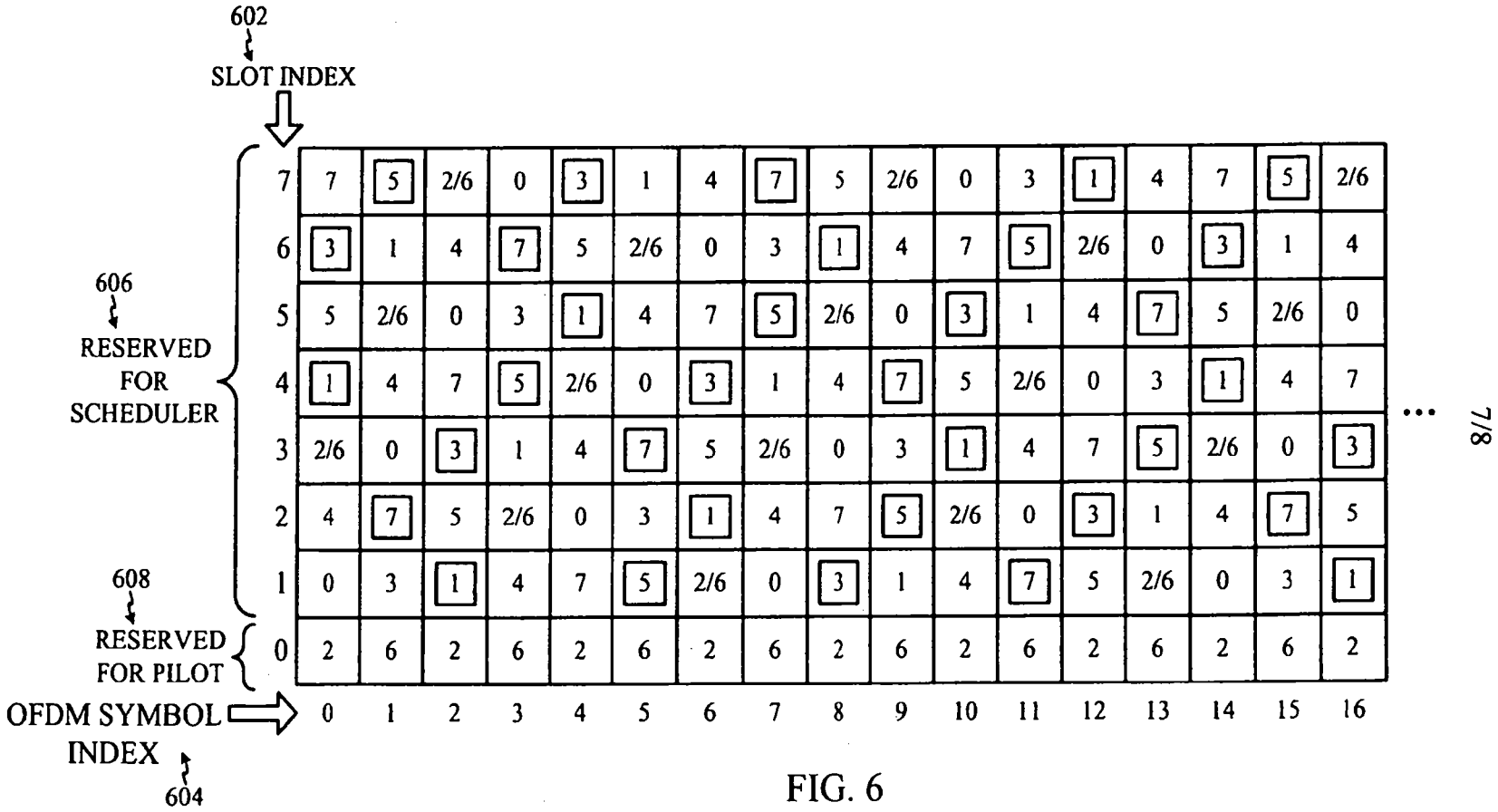

602
SLOT INDEX
606
RESERVED FOR SCHEDULER
608
RESERVED FOR PILOT
OFDM SYMBOL INDEX
604
7 7 5 2/6 0 3 1 4 7 5 2/6 0 3 1 4 7 5 2/6
6 3 1 4 7 5 2/6 0 3 1 4 7 5 2/6 0 3 1 4
5 5 2/6 0 3 1 4 7 5 2/6 0 3 1 4 7 5 2/6 0
4 1 4 7 5 2/6 0 3 1 4 7 5 2/6 0 3 1 4 7
3 2/6 0 3 1 4 7 5 2/6 0 3 1 4 7 5 2/6 0 3
2 4 7 5 2/6 0 3 1 4 7 5 2/6 0 3 1 4 7 5
1 0 3 1 4 7 5 2/6 0 3 1 4 7 5 2/6 0 3 1
0 2 6 2 6 2 6 2 6 2 6 2 6 2 6 2 6 2 6 2
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
...
7/8

FIG. 6

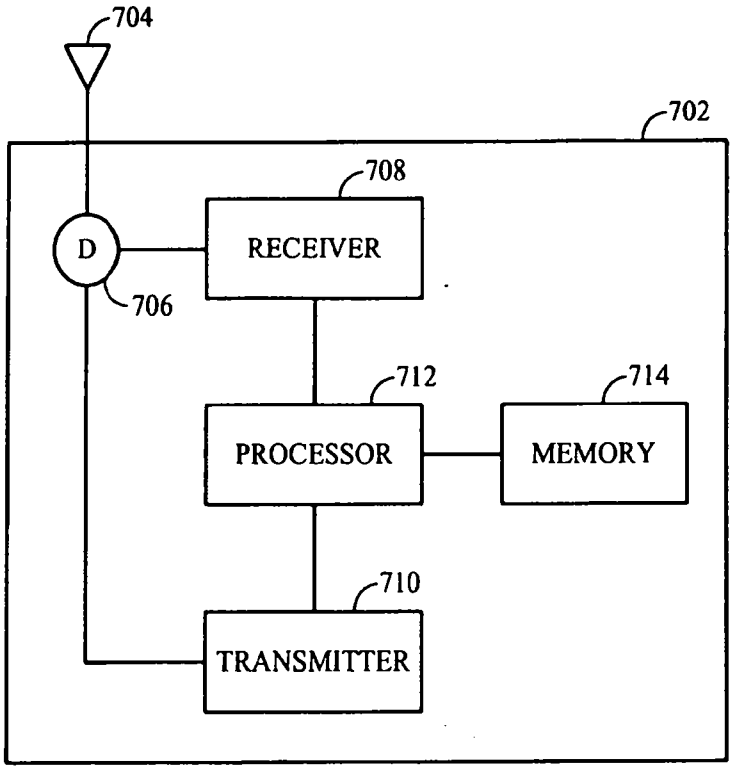

704
702
708
D
RECEIVER
706
712
714
PROCESSOR
MEMORY
710
TRANSMITTER

FIG. 7