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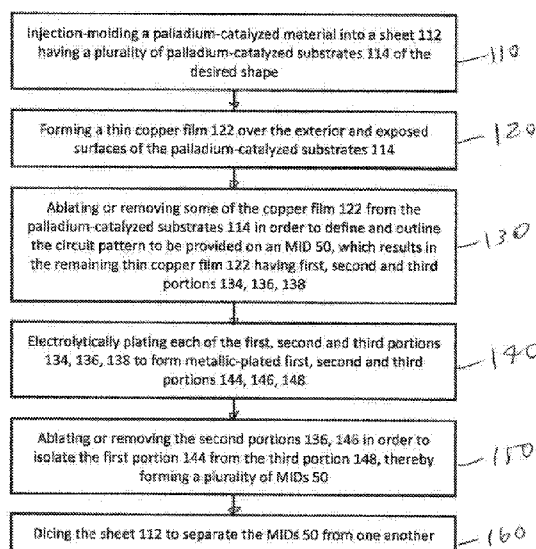
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(54) Title: MOLDED INTERCONNECT DEVICE AND METHOD OF MAKING SAME

FIG. 1



(57) Abstract: In some embodiments, a manufacturing process includes injection molding a palladium-catalyzed material into a substrate, forming a thin copper film over exterior and exposed surfaces of the substrate; ablating or removing copper film from the substrate to provide first, second and optional third portions of the copper film and ablated sections; electrolytically plating each portion to form metallic-plated portions; and ablating or removing the second portion in order to isolate the first portion. The metallic-plated first portion comprises a circuit portion of a molded interconnect device (MID), and where the metallic-plated third portion comprises a Faraday cage portion of a MID. A soft etching step may be included. A solder resist application step can be added, along with an associated solder resist removal step.

SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN,
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MOLDED INTERCONNECT DEVICE AND METHOD OF MAKING SAME

RELATED APPLICATIONS

[0001] This application claims priority to United States provisional application Serial No. 62/359,365, filed on July 7, 2016 and United States provisional application Serial No. 62/435,305, filed on December 16, 2016, the contents of which are incorporated herein in their entireties.

BACKGROUND OF THE DISCLOSURE

[0002] Molded interconnect devices (“MIDs”) are three-dimensional manufactured parts that typically include plastic components and electronic circuit traces. A plastic substrate or housing is created and electrical circuits and devices are plated, layered, or implanted upon the plastic substrate. MIDs typically have fewer parts than conventionally manufactured devices, which results in space and weight savings. Applications for MIDs include mobile telephones, automated teller machines, steering wheel components for automobiles, RFID components, lighting, medical devices and many other consumer and/or commercial products.

[0003] Current processes for manufacturing MIDs include two-shot molding, laser direct structuring technology (LDS), microscopic integrated processing technology (MIPTEC), and a laser developed additive technology. Each of these manufacturing processes have been known in the art for some time, yet each has its own drawbacks such that many individuals believe that further improvements to manufacturing MIDs would be beneficial.

[0004] Two-shot molding involves the use of two separate plastic parts, typically one platable and one non-platable. The platable part forms the circuitry, and the non-platable part fulfills mechanical functions and completes the molding. The two parts are fused together and circuits are created through use of electroless plating. The platable plastic is metallized, while the non-platable plastic remains non-conductive.

[0005] LDS technology involves the steps of injection molding (using any of a variety of dielectric thermoplastic materials, including polyamide, polycarbonate, and liquid crystal polymer), laser activation of the thermoplastic material, and then metallization (electroless plating). The laser etches a wiring pattern onto the part and prepares it for metallization. With LDS, only a single thermoplastic material is required thereby making the molding step a one-shot process, and generally preferable as compared to the two-shot molding process.

[0006] MIPTEC technology, which is offered by Panasonic Corporation, involves a molding stage, a circuit forming stage, a plating stage, and a cutting stage.

[0007] The molding stage includes injection-molding the intended shape using a thermoplastic resin, such as polyphthalamide (PPA).

[0008] The circuit forming stage includes two steps, namely: (1) metallization; and (2) patterning. Thin copper film is formed in the base metallization process (copper-strike). A laser is then used to remove the copper and outline the circuit pattern, with the wavelength and exposure time of the laser optimized to achieve copper removal without damaging the substrate.

[0009] The plating stage includes two or three steps, namely: (1) electrolytic copper plating; (2) optional soft etching; and (3) electrolytic nickel and gold plating. First, copper is electrically plated to form the circuit pattern. Then, if desired, soft etching is applied to remove unnecessary copper-strike that was not removed by the laser in the circuit forming stage. Finally, nickel and gold are plated on the electrolytically-plated copper, forming the circuit pattern to help prevent oxidation and corrosion.

[0010] An optional cutting stage then includes dicing the sheet form into individual MIDs.

[0011] Thus, MIPTEC technology, like LDS technology, has only a one-shot molding process, but also provides MIDs which can be fine patterned and bare chip mounted.

[0012] The laser developed additive technology is similar to the MIPTEC technology, but allows for other thermoplastic materials, such as polyamide (PA), polycarbonate (PC) and acrylonitrile butadiene styrene (ABS) or liquid crystal polymer (LCP), to be used in the process. Like polyphthalamide (PPA), however, these thermoplastic materials are all dielectric materials and require the separate and extra step of surface activation treatment prior to the circuit forming stage. This extra step adds both time and expense to these technologies.

[0013] MIPTEC and LDS technology processes have limitations, and in some circumstances even impossibilities, in connection with plating features that are not within a line-of-sight. For instance, as illustrated in FIGS. 25 and 26, a through-hole type via 60 is illustrated. Plating of the through-hole type via 60, as illustrated in FIG. 25, could not be achieved with a MIPTEC technology process because the chemical applied to the surface of the plastic would also need to be applied to the vertical walls of the via 60. Plating of the through-hole type via 60, as illustrated in FIG. 26, could not be achieved with a LDS technology process because vertical walls could not be achieved due to laser activation required angle of incidence. FIG.

27 illustrates a different line-of-sight feature 70, referred to herein as an overhang or an undercut, which likely is not possible with a MIPTEC and/or LDS technology process.

BRIEF SUMMARY OF THE DISCLOSURE

[0014] A first preferred embodiment of a manufacturing process includes the steps of: injection molding a palladium-catalyzed material, such as, for example, resins or epoxy molding compounds into a palladium-catalyzed substrate of a desired shape; forming a thin copper film over exterior and exposed surfaces of the palladium-catalyzed substrate; ablating or removing some of the copper film from the palladium-catalyzed substrate to provide first, second and optional third portions of the copper film; electrolytically plating each of the first, second and third portions of the copper film to form metallic-plated first, second and third portions; and ablating or removing the second portion in order to isolate the metallic-plated first portion from the metallic-plated third portion, where the metallic-plated first portion comprises a circuit portion of a molded interconnect device (MID), and where the metallic-plated third portion comprises a Faraday cage portion of the MID.

[0015] A second preferred embodiment of a manufacturing process includes the steps of: injection molding a palladium-catalyzed material, such as, for example, resins or epoxy molding compounds into a palladium-catalyzed substrate of a desired shape; forming a thin copper film over exterior and exposed surfaces of the palladium-catalyzed substrate; ablating or removing some of the copper film from the palladium-catalyzed substrate to provide first, second and optional third portions of the copper film; electrolytic copper plating; soft etching to remove any unnecessary copper; electrolytic nickel plating; electrolytic gold plating; and ablating or removing the second portion in order to isolate the metallic-plated first portion from the metallic-plated third portion, where the metallic-plated first portion comprises a circuit portion of the MID, and where the metallic-plated third portion comprises a Faraday cage portion of the MID.

[0016] A third preferred embodiment of a manufacturing process includes the steps of: injection molding a palladium-catalyzed material, such as, for example, resins or epoxy molding compounds into a palladium-catalyzed substrate of a desired shape; forming a thin copper film over exterior and exposed surfaces of the palladium-catalyzed substrate; ablating or removing some of the copper film from the palladium-catalyzed substrate to provide ablated sections and first, second and optional third portions of the copper film; electrolytically plating each of the first, second and third portions of the copper film with copper plating; non-selectively adding solder resist; selectively removing the solder resist

from parts of the first portion which will form contact points for connection of the MID to an associated device or assembly, such as a printed circuit board, and from the ablated sections; electrolytically plating the contact points with nickel plating and gold plating to form metallic-plated first, second and third portions; and ablating or removing the second portion in order to isolate the metallic-plated first portion from the metallic-plated third portion, where the metallic-plated first portion comprises a circuit portion of the MID, and where the metallic-plated third portion comprises a Faraday cage portion of the MID.

[0017] A fourth preferred embodiment of a manufacturing process includes the steps of: injection molding a palladium-catalyzed material, such as, for example, resins or epoxy molding compounds into a palladium-catalyzed substrate of a desired shape; forming a thin copper film over exterior and exposed surfaces of the palladium-catalyzed substrate; ablating or removing some of the copper film from the palladium-catalyzed substrate to provide ablated sections and first, second and optional third portions of the copper film; electrolytically plating each of the first, second and third portions of the copper film with copper plating, nickel plating and gold plating; non-selectively adding solder resist; selectively removing the solder resist from parts of the first portion which will form contact points for connection of the MID to an associated device or assembly, such as a printed circuit board, and from the ablated sections; and ablating or removing the second portion in order to isolate the metallic-plated first portion from the metallic-plated third portion, where the metallic-plated first portion comprises a circuit portion of the MID, and where the metallic-plated third portion comprises a Faraday cage portion of the MID.

[0018] Each manufacturing process results in an MID having a palladium-catalyzed substrate, a circuit portion, and an optional Faraday cage portion, where the Faraday cage portion and the circuit portion may be isolated from one another.

[0019] These and other aspects and features of the invention are described in further detail below.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0020] FIG. 1 is a flow chart showing the steps of a first embodiment of a process of manufacturing a molded interconnect device (MID);

[0021] FIG. 2 is a flow chart showing the sub-steps of an electrolytic plating step of the first embodiment of the manufacturing process;

[0022] FIG. 3 is a perspective view of a sheet;

[0023] FIG. 4 is a perspective view of one of the substrates separated from the sheet;

[0024] FIG. 5 is a top plan view of the substrate of FIG. 4;

[0025] FIG. 6 is a bottom plan view of the substrate of FIG. 4;

[0026] FIG. 7 is a cross-sectional view of a first assembly;

[0027] FIG. 8 is a perspective view of a second assembly;

[0028] FIG. 9 is a top plan view of the second assembly of FIG. 8;

[0029] FIG. 10 is a bottom plan view of the second assembly of FIG. 8;

[0030] FIG. 11 is a perspective view of a third assembly;

[0031] FIG. 12 is a top plan view of the third assembly of FIG. 11;

[0032] FIG. 13 is a bottom plan view of the third assembly of FIG. 11;

[0033] FIG. 14 is a cross-sectional view, shown in perspective, of the third assembly of FIG. 11, in accordance with an embodiment;

[0034] FIG. 15 is an enlarged view of a portion of FIG. 14;

[0035] FIG. 16 is a perspective view of a fourth assembly;

[0036] FIG. 17 is a flow chart showing the steps of a second embodiment of a process of manufacturing a molded interconnect device (MID);

[0037] FIG. 18 is a flow chart showing the steps of a third embodiment of a process of manufacturing a molded interconnect device (MID);

[0038] FIG. 19 is a partial perspective, cross-sectional view of the MID during formation in accordance with the third embodiment;

[0039] FIG. 20 is a perspective view of the MID during formation in accordance with the third embodiment;

[0040] FIG. 21 is a perspective view of the MID during formation in accordance with the third embodiment;

[0041] FIG. 22 is a flow chart showing the steps of a fourth embodiment of a process of manufacturing a molded interconnect device (MID);

[0042] FIG. 23 is a partial perspective, cross-sectional view of the MID during formation in accordance with the fourth embodiment;

[0043] FIG. 24 is a perspective view of the MID during formation in accordance with the fourth embodiment;

[0044] FIGS. 25-27 illustrate cross-sectional views of prior art line-of-sight features, such as through-hole type vias and overhangs or undercuts which can be plated by any of the embodiments of the process.

DETAILED DESCRIPTION OF THE INVENTION

[0045] The present disclosure is directed to novel manufacturing processes 100, 200, 300, 400 for forming a molded interconnect device (MID) 50. The manufacturing processes 100, 200, 300, 400 are useful for the creation of MIDs, such as printed circuit boards, flex circuits, connectors, thermal management features, electromagnetic interference (EMI) shielding, high current conductors, radio frequency identification (RFID) apparatuses, antennas, wireless power, sensors, MEMS apparatuses, LEDs, microprocessors and memory, ASICs, passives, and other electrical and electro-mechanical apparatuses.

[0046] Attention is directed to FIGS. 1-16 relating to a first embodiment of the manufacturing process 100 used to form the MID 50. FIG. 1 illustrates a flow chart depicting the steps of the manufacturing process 100. FIG. 2 illustrates a flow chart depicting the steps of a sub-process of the manufacturing process 100. The manufacturing process 100 includes a molding stage, a circuit forming stage, a plating stage, and a cutting stage.

[0047] The molding stage of the manufacturing process 100 advantageously includes only a single step, which step will be referenced by reference numeral 110. Step 110 is an injection-molding step where a palladium-catalyzed material (sometimes called palladium-doped in the art), such as, for example, resins or epoxy molding compounds, is injection-molded in the form of a sheet 112 containing a plurality of connected substrates 114 (each formed in the intended shape) for production purposes. Each substrate 114 may be formed in a desired three-dimensional shape. In some embodiments, each substrate 114 is formed of the same three-dimensional shape. FIG. 3 illustrates the formation of the MID 50 after the completion of step 110, where the sheet 112 contains the plurality of substrates 114. FIGS. 4-6 illustrate a singulated substrate 114. The material which is injection-molded is a palladium-catalyzed resin, but is intended to be inclusive of materials where the palladium (or any comparable material that does not need to be surface treated to accept metallization) is provided within, or infused within, the material itself.

[0048] The circuit forming stage of the manufacturing process 100 includes two steps, which steps will be referred to as steps 120 and 130.

[0049] Step 120 is a metallization step where a thin copper film 122 is formed over the exterior and exposed surfaces of the palladium-catalyzed substrates 114 to form a first assembly 123. Metallization step 120 is commonly referred to as copper-striking. FIG. 7 illustrates the formation of the MID 50 after the completion of step 120, where the substrate 114 has the copper film 122 formed thereon (the first assembly 123 is shown in cross-section

for clarity to show the substrate 114). Sections 124 (shown with shading for clarity) which do not have the copper film 122 formed thereon are where the substrate 114 is connected to the adjacent substrate 114 in the sheet 112. Sections 124 are illustrative only and do not denote required locations for the connection points.

[0050] Step 130 is a circuit patterning step where a laser (not shown) ablates or removes portions of the copper film 122 from the first assembly 123 to expose portions 131, 132 of the substrate 114 and form a second assembly 133. This action defines and outlines a circuit pattern within the remaining copper film 122 to be provided for the MID 50. FIGS. 8-10 illustrate the formation of the MID 50 after the completion of step 130, where the non-ablated/removed copper film 122 preferably includes first, second and optional and selectively sized/shaped third portions 134, 136, 138 which are to be subject to the plating stage, as will be described further below. The first portion 134 forms the circuit pattern, the second portion(s) 136 forms a bus portion(s) which connects the first portion 134 to the third portion(s) 138, if provided, and the third portion(s) 138, if provided, is/are generally a Faraday cage portion (hereinafter, the second portion(s) 136 is referred to in the singular, but more than one second portion 136 may be provided; hereinafter, the third portion(s) 138 is referred to in the singular, but more than one third portion 138 may be provided). The remaining steps will be described and illustrated showing the third portion(s) 138 with the understanding that the size/shape of the third portion(s) 138 could be changed as desired, and also with the understanding that the third portion(s) 138 could not be provided at all.

[0051] The plating stage of the manufacturing process 100 includes two steps, which steps will be referred to as steps 140 and 150.

[0052] Step 140 is an electrolytic plating step where a probe (not shown) is attached/connected to one of the first, second and third portions 134, 136, 138 and electricity is run through the first, second and third portions 134, 136, 138 and desired metallic molecules from a desired metallic bath are drawn to and secured to the first, second and third portions 134, 136, 138, until the desired metallic plating of the first, second and third portions 134, 136, 138 is built up to the desired thickness, thus forming metallic-plated first, second and third portions 144, 146, 148 (it is to be understood that metallic-plated third portion 148 will only be formed if third portion 138 is provided), thereby forming a third assembly 143. FIGS. 11-13 illustrate the formation of the MID 50 after the completion of step 140.

[0053] It is to be understood that the electrolytic plating step 140 can include the electrolytic plating of any metal(s) as desired. In a preferred embodiment, the electrolytic plating step 140 begins with a step 141 wherein a copper material is electrolytic plated onto the first,

second and third portions 144, 146, 148 to form a copper plating 173, followed by a step 171 wherein a nickel material is electrolytic plated onto the copper material 173 to form a nickel plating 174, followed by a step 172 wherein a gold material is electrolytic plated onto the nickel material 147 to form a gold plating 175, as illustrated in FIGS. 14 and 15.

[0054] Step 150 is a circuit isolation step where a laser (not shown) ablates or removes the formed second (bus) portion(s) 136/146, beginning with second portion 146, and finishing with second portion 136, until the surface of the substrate 114 is provided between the first and third portions 144, 148, thereby providing portions 152 of the substrate 114 which are visible, and thereby forming a fourth assembly 153. The ablated sections 152 are connected to or continuous with the ablated sections 132 such that the first portion 144 (namely the circuit pattern) is isolated from the third portion 148 (namely the Faraday cage portion). FIG. 16 illustrates the MID 50 that is formed after the completion of step 150.

[0055] Step 160 is a cutting step where the sheet 112 is diced in order to separate each of the MIDs 50. The sheet 112 can be diced along saw streets 162 (the saw streets 162 are not shown in FIGS. 4-16), thereby exposing the sections 124.

[0056] Either before or after step 160 of the manufacturing process 100 is performed, one or more of the MIDs 50 can then be inspected, as desired and in any of a number of known manners, to ensure that the MIDs 50 are suitable for their intended use. The MIDs 50 may then be packaged and shipped. If desired, further electronic components may be electrically connected and secured to the first portion 144, namely the circuit portions, before the MIDs 50 are packaged and shipped. It is to be understood that the sheet 112 of MIDs 50 could be packaged and shipped prior to the cutting step 160 being performed.

[0057] Attention is directed to FIG. 17 relating to a second embodiment of the manufacturing process 200 used to form the MID 50. FIG. 17 illustrates a flow chart depicting the steps of the manufacturing process 200. Like manufacturing process 100, manufacturing process 200 includes a molding stage, a circuit forming stage, a plating stage, and a cutting stage.

Manufacturing process 200 includes each of the same steps 110, 120, 130, 140 (including steps 141, 142, 143), 150, 160 from manufacturing process 100, but also includes a further step 245 that would preferably be a part of the plating stage. Step 245 is a soft etching step which would preferably be performed after step 141, but before step 142. As a part of the soft etching step 245, soft etching would be applied in order to remove any unnecessary copper from areas that are not part of the first, second or third portions 144, 146, 148 of the MID 50 and to prevent any unnecessary nickel and/or gold plating.

[0058] Attention is directed to FIGS. 18-21 relating to a third embodiment of the manufacturing process 300 used to form the MID 50. FIG. 18 illustrates a flow chart depicting the steps of the manufacturing process 300. Like manufacturing process 100, manufacturing process 300 includes a molding stage, a circuit forming stage, a plating stage, and a cutting stage. Manufacturing process 300 includes each of the same steps 110, 120, 130, 141, 142, 143, 150, 160 from manufacturing process 100, also includes steps 380, 381 after step 141 and before step 142. The soft etching step 245 may be included after step 141.

[0059] Step 380 is a solder resist addition step where solder resist 337 is added non-selectively onto the entire assembly, including the copper plating 173 and the ablated sections 131, 132 as shown in FIG. 19. Step 380 is a solder resist removal step where a laser (not shown) ablates or removes the solder resist 337 from one or more sections 339 of the copper plating 173 overlaying the first portion 134 which will form contact point(s) for connection of the MID 50 to an associated device or assembly, such as a printed circuit board, as shown in FIG. 20. In some embodiments, the solder resist 337 on the ablated section 131, 132 and on the second portion 136 is also removed in step 380. In some embodiments, all of the solder resist 337 overlaying the ablated sections 131, 132 is removed. In some embodiments, only a portion of the solder resist 337 overlaying the ablated sections 131, 132 is removed. Alternatively, or additionally, during step 150, the solder resist 337 on the second portion 136 and the solder resist 337 that remains on the ablated sections 131, 132 that prevents the isolation of the first portion 144 is removed. Thereafter, in steps 142 and 143, the nickel plating 174 and the gold plating 175 are only electrolytic plated onto the sections 339 as shown in FIG. 21. This manufacturing process 300 reduces the amount of precious metal used and provides for limiting solder flow once the resulting MID 50 is soldered to another component.

[0060] Attention is directed to FIGS. 22-24 relating to a fourth embodiment of the manufacturing process 400 used to form the MID 50. FIG. 22 illustrates a flow chart depicting the steps of the manufacturing process 400. Like manufacturing process 100, manufacturing process 400 includes a molding stage, a circuit forming stage, a plating stage, and a cutting stage. Manufacturing process 300 includes each of the same steps 110, 120, 130, 141, 142, 143, 150, 160 from manufacturing process 100, also includes steps 490, 491 after step 143 and before step 150. The soft etching step 245 may be included after step 141.

[0061] Step 490 is a solder resist addition step where solder resist 337 is added non-selectively onto the entire assembly, including the gold plating 175 and the ablated sections

131, 132 as shown in FIG. 23. Step 491 is a solder resist removal step where a laser (not shown) ablates or removes the solder resist 337 from one or more sections 439 of the gold plating 175 overlaying the first portion 134 which will form contact point(s) for connection of the MID 50 to an associated device or assembly, such as a printed circuit board, as shown in FIG. 24. In some embodiments, the solder resist 337 on the ablated section 131, 132 and on the second portion 136 is also removed in step 491. In some embodiments, all of the solder resist 337 overlaying the ablated sections 131, 132 is removed. In some embodiments, only a portion of the solder resist 337 overlaying the ablated sections 131, 132 is removed.

Alternatively, or additionally, during step 150, the solder resist 337 on the second portion 136 and the solder resist 337 that remains on the ablated sections 131, 132 that prevents the isolation of the first portion 144 is removed. This manufacturing process 400 provides for limiting solder flow once the resulting MID 50 is soldered to another component.

[0062] The manufacturing processes 100, 200, 300, 400 of forming the MIDs 50 are advantageous as compared to the prior-known MID manufacturing processes, especially as compared to the MIPTEC and laser developed additive technology processes. More specifically, as the injection-molded material is infused with palladium, it is then unnecessary to perform any type of surface activation treatment to the substrate 114 of the type which is required in all prior-known MID manufacturing processes. Thus, the manufacturing processes 100, 200, 300, 400 removes a step which is needed in all prior-known MID manufacturing processes, thereby saving both manufacturing costs and manufacturing time.

[0063] MIPTEC and LDS technology processes also have limitations, and in some circumstances even impossibilities, in connection with plating features that are not within a line-of-sight. For instance, as illustrated in FIGS. 25 and 26, a through-hole type via 60 is illustrated. Plating of the through-hole type via 60, as illustrated in FIG. 25, could not be achieved with a MIPTEC technology process because the chemical applied to the surface of the plastic would also need to be applied to the vertical walls of the via 60. Plating of the through-hole type via 60, as illustrated in FIG. 26, could not be achieved with a LDS technology process because vertical walls could not be achieved due to laser activation required angle of incidence. FIG. 27 illustrates a different line-of-sight feature 70, referred to herein as an overhang or an undercut, which likely is not possible with a MIPTEC and/or LDS technology process. The through-hole type vias 60 and overhang/undercut 70 of FIGS. 25-27, however, can be easily plated with the manufacturing processes 100, 200, 300, 400 described and illustrated herein.

[0064] Furthermore, it has been determined that the manufacturing processes 100, 200, 300, 400 provide for improved plating adhesion as compared to the prior-known MID manufacturing processes, thereby making the MIDs 50 formed from the manufacturing processes 100, 200, 300, 400 more robust and reliable than the MIDs formed from the prior-known MID manufacturing processes.

[0065] Advantageously, each of the manufacturing processes 100, 200, 300, 400 may provide an MID 50 having a Faraday cage configuration, where the third portions 148 provide the Faraday cage configuration which is useful in providing better EMI shielding for any packaged integrated circuit application. To aid in the provision of the Faraday cage configuration, each substrate 114 provided in the sheet 112 may have one or more vias (not shown) formed along saw street, namely where the sheet 112 is diced during step 160 to provide the individual MIDs 50. These vias allow for the metallization and electrolytic plating, of steps 120 and 140/140a, respectively, of all sides of the MIDs 50. It is to be understood that the size/shape of the Faraday cage configuration, if provided, may vary as desired.

[0066] All references, including publications, patent applications, and patents, cited herein are hereby incorporated by reference to the same extent as if each reference were individually and specifically indicated to be incorporated by reference and were set forth in its entirety herein.

[0067] The use of the terms “a” and “an” and “the” and “at least one” and similar referents in the context of describing the invention (especially in the context of the following claims) are to be construed to cover both the singular and the plural, unless otherwise indicated herein or clearly contradicted by context. The use of the term “at least one” followed by a list of one or more items (for example, “at least one of A and B”) is to be construed to mean one item selected from the listed items (A or B) or any combination of two or more of the listed items (A and B), unless otherwise indicated herein or clearly contradicted by context. The terms “comprising,” “having,” “including,” and “containing” are to be construed as open-ended terms (i.e., meaning “including, but not limited to,”) unless otherwise noted. Recitation of ranges of values herein are merely intended to serve as a shorthand method of referring individually to each separate value falling within the range, unless otherwise indicated herein, and each separate value is incorporated into the specification as if it were individually recited herein. All processes described herein can be performed in any suitable order unless otherwise indicated herein or otherwise clearly contradicted by context. The use of any and all examples, or exemplary language (e.g., “such as”) provided herein, is intended merely to

better illuminate the invention, and does not pose a limitation on the scope of the invention unless otherwise claimed. No language in the specification should be construed as indicating any non-claimed element as essential to the practice of the invention.

[0068] Preferred embodiments of this invention are described herein, including the best mode known to the inventors for carrying out the invention. Variations of those preferred embodiments may become apparent to those of ordinary skill in the art upon reading the foregoing description. The inventors expect skilled artisans to employ such variations as appropriate, and the inventors intend for the invention to be practiced otherwise than as specifically described herein. Accordingly, this invention includes all modifications and equivalents of the subject matter recited in the claims appended hereto as permitted by applicable law. Moreover, any combination of the above-described elements in all possible variations thereof is encompassed by the invention unless otherwise indicated herein or otherwise clearly contradicted by context.

CLAIMS:

1. A method of forming a molded interconnect device (MID), the method comprising the steps of:
 - a) injection molding a palladium-catalyzed material into a palladium-catalyzed substrate of a desired shape;
 - b) forming a thin copper film over exterior and exposed surfaces of the palladium-catalyzed substrate;
 - c) ablating or removing some of the copper film from the palladium-catalyzed substrate to provide at least first and second portions of the copper film and one or more ablated sections;
 - d) electrolytically plating each of the first and second portions of the copper film to form at least metallic-plated first and second portions; and
 - e) ablating or removing the second portion in order to isolate the metallic-plated first portion, where the metallic-plated first portion comprises a circuit portion of the MID.
2. The method as defined in claim 1, wherein in step c) a third portion of the copper film is provided, wherein in step d) the third portion of the copper film is electrolytically plated to form a metallic-plated third portion, and wherein step e) results in the metallic-plated third portion comprising a Faraday cage portion of the MID.
3. The method as defined in claim 1, wherein step (d) further comprises electrolytic copper plating, electrolytic nickel plating, and electrolytic gold plating.
4. The method as defined in claim 3, further comprising the step of soft etching to remove any unnecessary copper, wherein the soft etching step is performed after the electrolytic copper plating step and before the electrolytic nickel plating step.
5. The method as defined in claim 1, wherein in step a) the injection-molding step provides a sheet having a plurality of palladium-catalyzed substrates.
6. The method as defined in claim 5, further comprising step f) dicing the sheet to separate the MIDs from one another.

7. A method of forming a molded interconnect device (MID), the method comprising the steps of:

- a) injection molding a palladium-catalyzed material into a palladium-catalyzed substrate of a desired shape;
- b) forming a thin copper film over exterior and exposed surfaces of the palladium-catalyzed substrate;
- c) ablating or removing some of the copper film from the palladium-catalyzed substrate to provide first and second portions of the copper film and one or more ablated sections;
- d) electrolytically plating the first portion of the copper film with a first plating and to form an assembly;
- e) non-selectively adding solder resist onto the assembly;
- f) ablating or removing the solder resist from one or more parts of the first portion;
- g) electrolytically plating the one or more parts of the first portion to form a metallic-plated first portion; and
- h) ablating or removing the solder resist on the second portion, the second portion, and the solder resist from the one or more ablated sections in order to isolate the metallic-plated first portion, where the metallic-plated first portion comprises a circuit portion of the MID.

8. The method as defined in claim 7, wherein step c) provides a third portion of the copper film, wherein step d) electrolytically plates the third portion of the copper film to form a metallic-plated third portion, and wherein step h) results in the metallic-plated third portion comprising a Faraday cage portion of the MID.

9. The method as defined in claim 7, wherein the step of ablating or removing solder resist from the one or more ablated sections is performed during step f).

10. The method as defined in claim 7, wherein in step d) the plating is copper plating, and wherein step g) includes the steps of electrolytic nickel plating and electrolytic gold plating.

11. The method as defined in claim 10, further comprising the step of soft etching to remove any unnecessary copper, wherein the soft etching step is performed after step d).

12. The method as defined in claim 7, wherein step a) provides a sheet having a plurality of palladium-catalyzed substrates.

13. The method as defined in claim 12, further comprising step i) dicing the sheet to separate the MIDs from one another.

14. A method of forming a molded interconnect device (MID), the method comprising the steps of:

- a) injection molding a palladium-catalyzed material into a palladium-catalyzed substrate of a desired shape;
- b) forming a thin copper film over exterior and exposed surfaces of the palladium-catalyzed substrate;
- c) ablating or removing some of the copper film from the palladium-catalyzed substrate to provide first and second portions of the copper film and one or more ablated sections;
- d) electrolytically plating the first portion of the copper film with a plating and to form an assembly;
- e) non-selectively adding solder resist onto the assembly;
- f) ablating or removing the solder resist on the second portion, the second portion, the solder resist from one or more sections of the first portion, and the solder resist from the one or more ablated sections in order to isolate the metallic-plated first portion, where the metallic-plated first portion comprises a circuit portion of the MID.

15. The method as defined in claim 14, wherein step c) provides a third portion of the copper film, wherein step d) electrolytically plates the third portion of the copper film to form a metallic-plated third portion, and wherein step g) results in the metallic-plated third portion comprising a Faraday cage portion of the MID.

16. The method as defined in claim 14, wherein the step of ablating or removing solder resist from the one or more ablated sections is performed during step f).

17. The method as defined in claim 14, wherein step d) includes the steps of electrolytic copper plating, electrolytic nickel plating and electrolytic gold plating.

18. The method as defined in claim 17, further comprising the step of soft etching to remove any unnecessary copper, wherein the soft etching step is performed after the electrolytic copper plating step.

19. The method as defined in claim 14, wherein step a) provides a sheet having a plurality of palladium-catalyzed substrates.

20. The method as defined in claim 14, further comprising step h) dicing the sheet to separate the MIDs from one another.

21. A molded interconnect device (MID) comprising:
a palladium-catalyzed substrate;
a circuit portion; and
a Faraday cage portion, the Faraday cage portion being isolated from the circuit portion.

22. The MID as defined in claim 21, wherein each of the circuit portion and the Faraday cage portion has a metallized layer secured to the palladium-catalyzed substrate and an electrolytic metallic plated layer secured to the metallized layer.

23. The MID as defined in claim 21, wherein the metallized layer is formed of copper.

24. The MID as defined in claim 21, wherein the electrolytic metallic plated layer is formed of an electrolytic copper plated layer, an electrolytic nickel plated layer, and an electrolytic gold plated layer.

FIG. 1

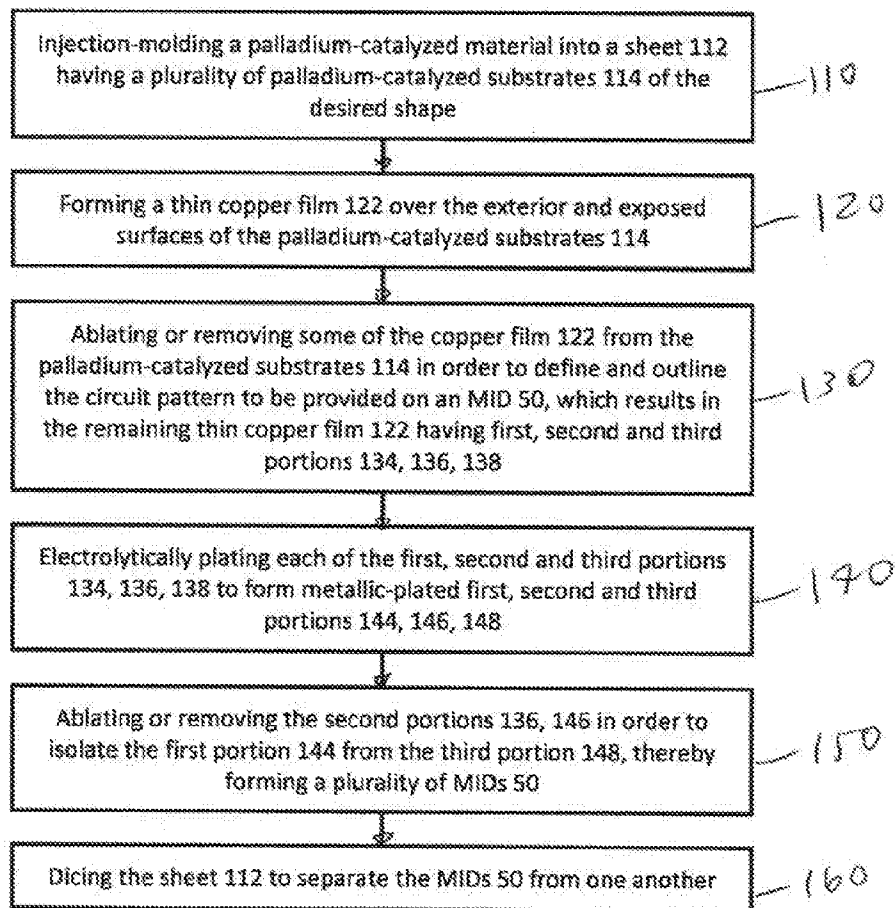
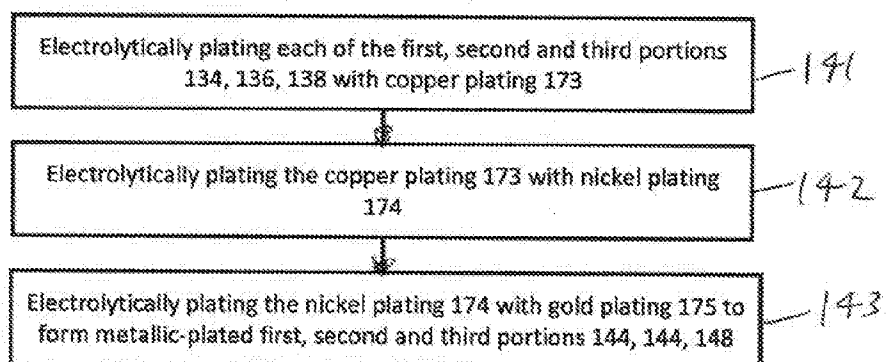


FIG. 2



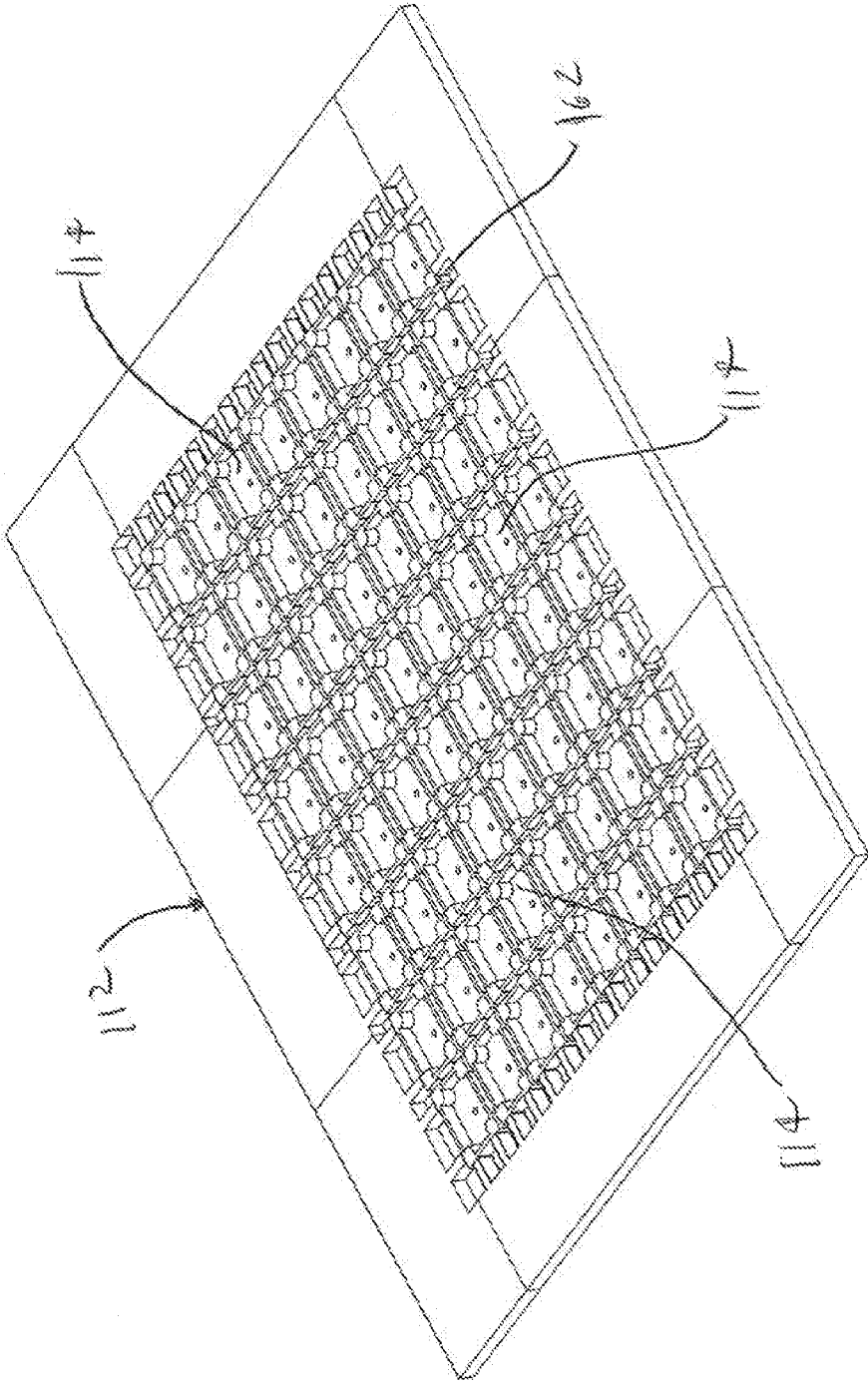
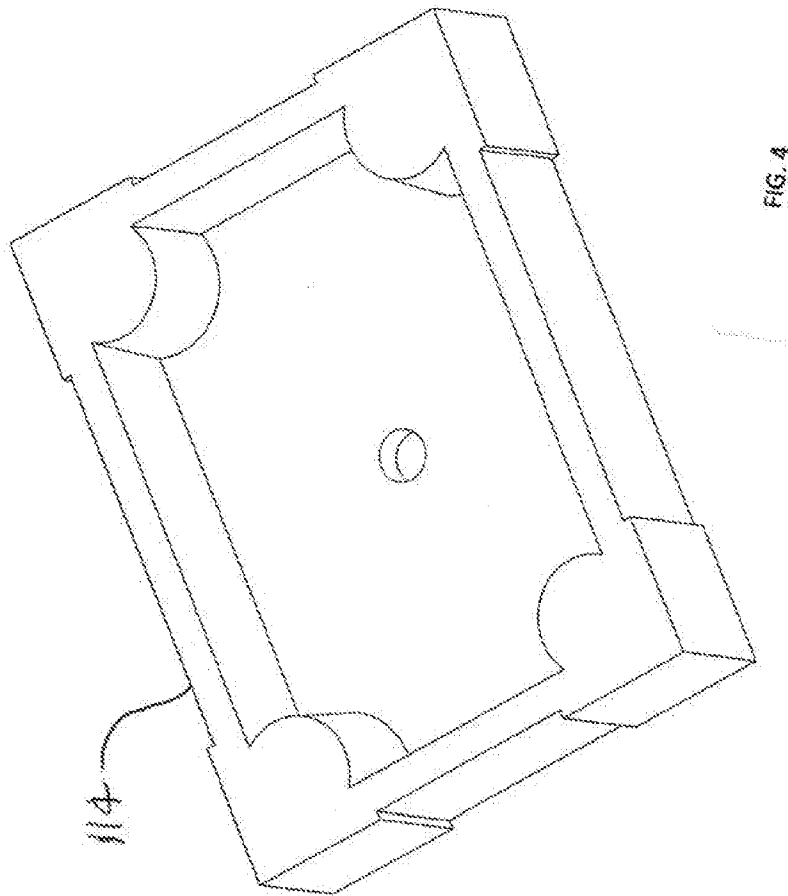


FIG. 3



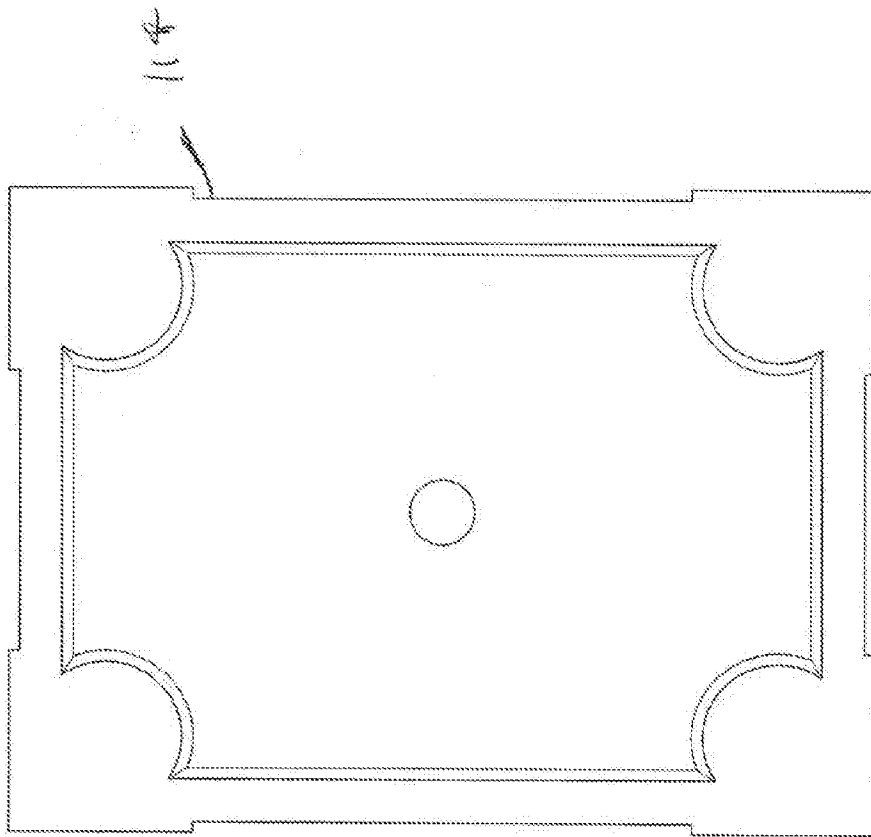


FIG. 5

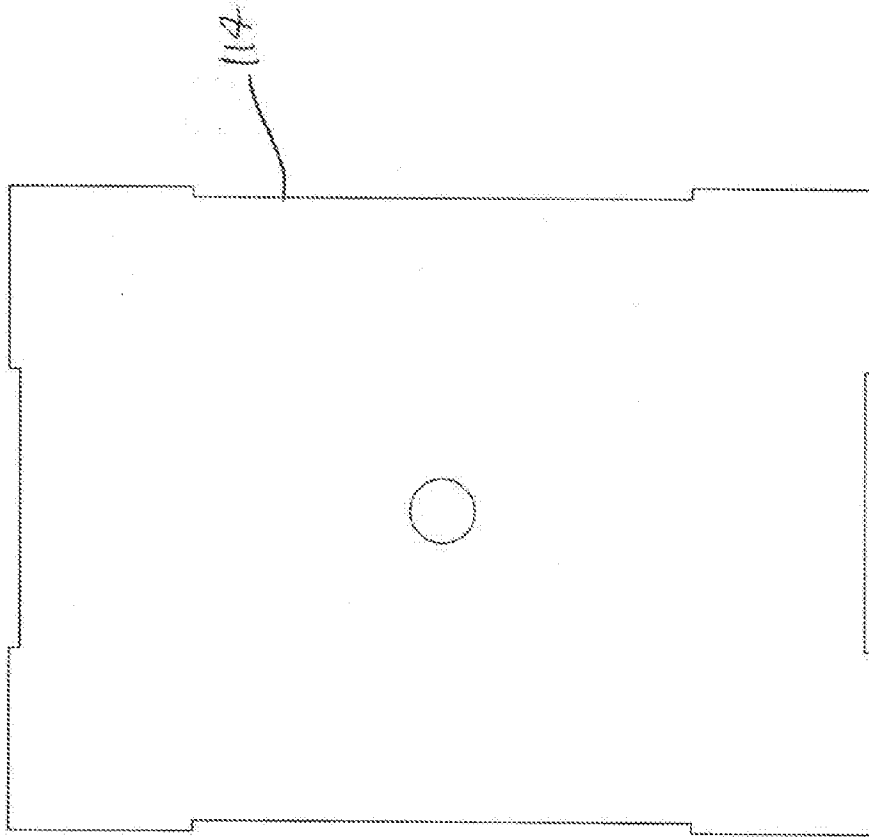


FIG. 6

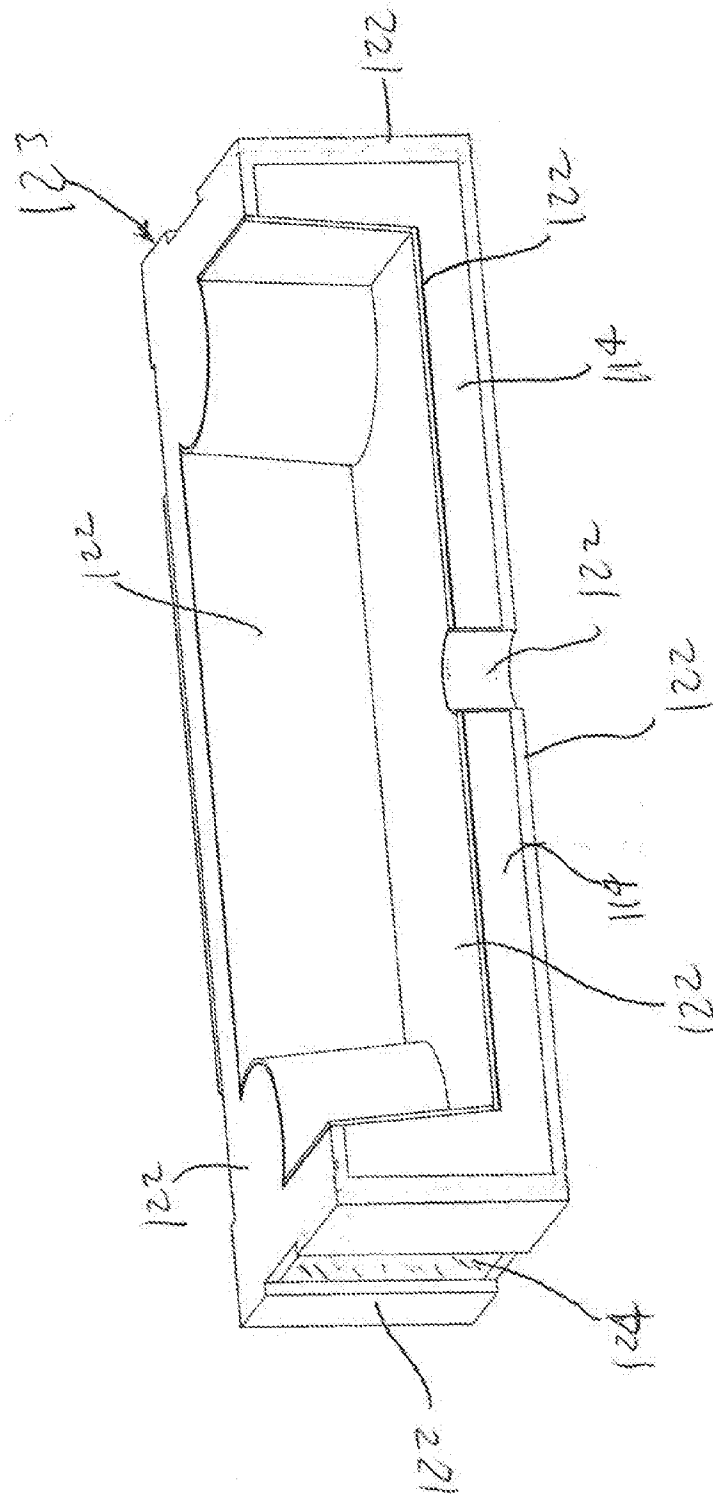


Fig. 1

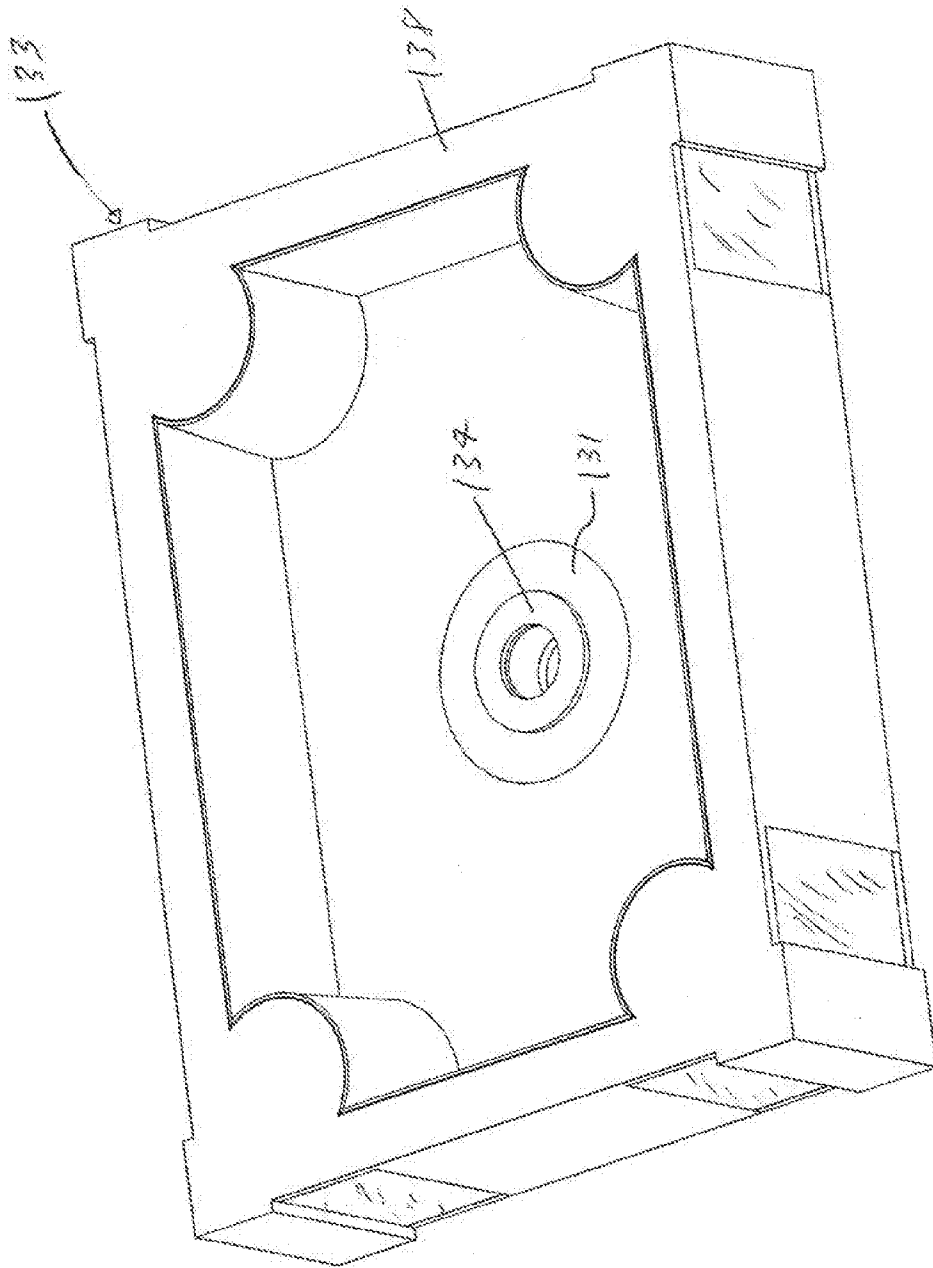


FIG. 8

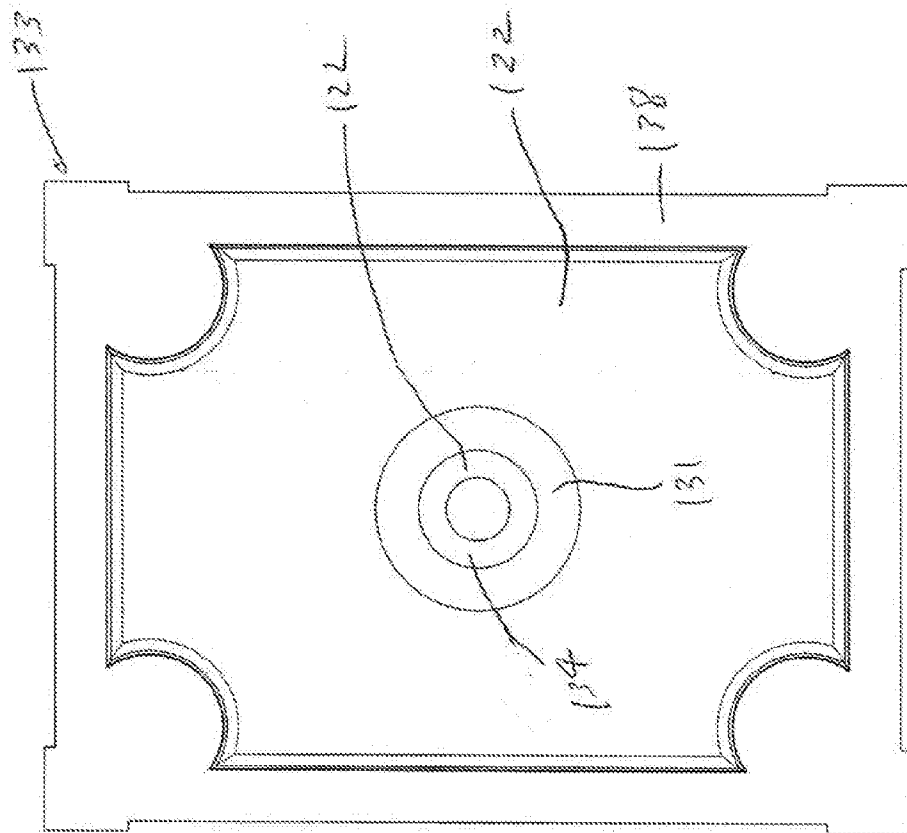


FIG. 9

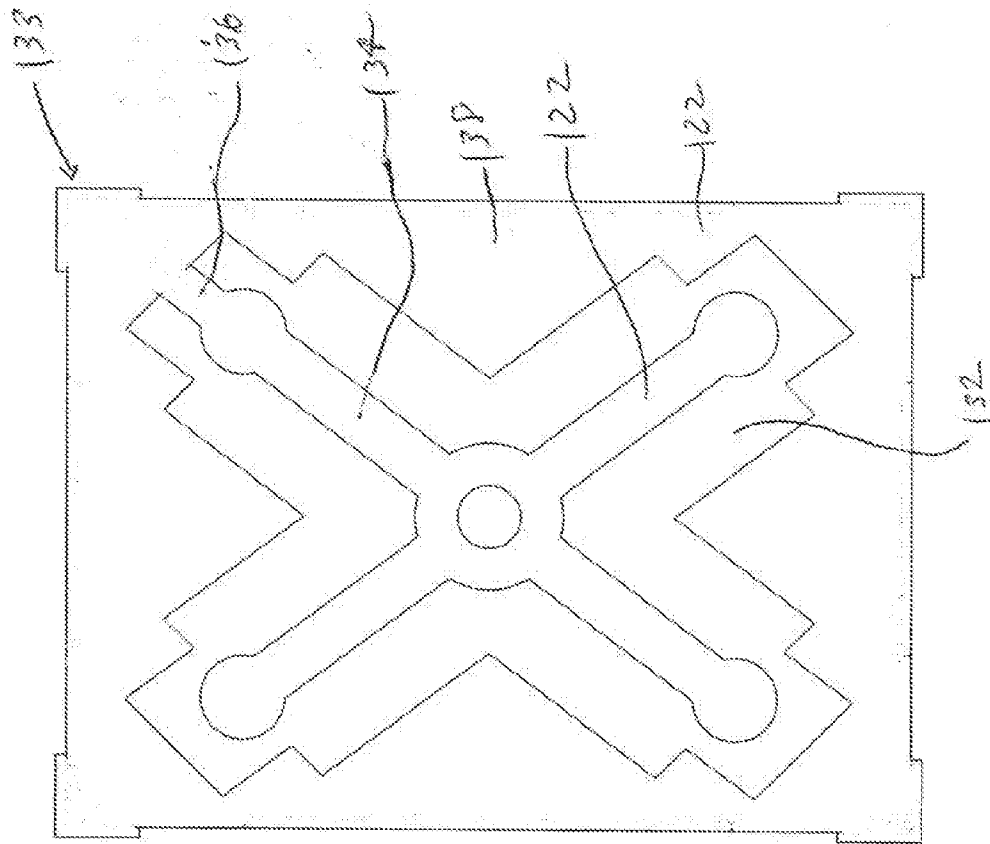


FIG. 10

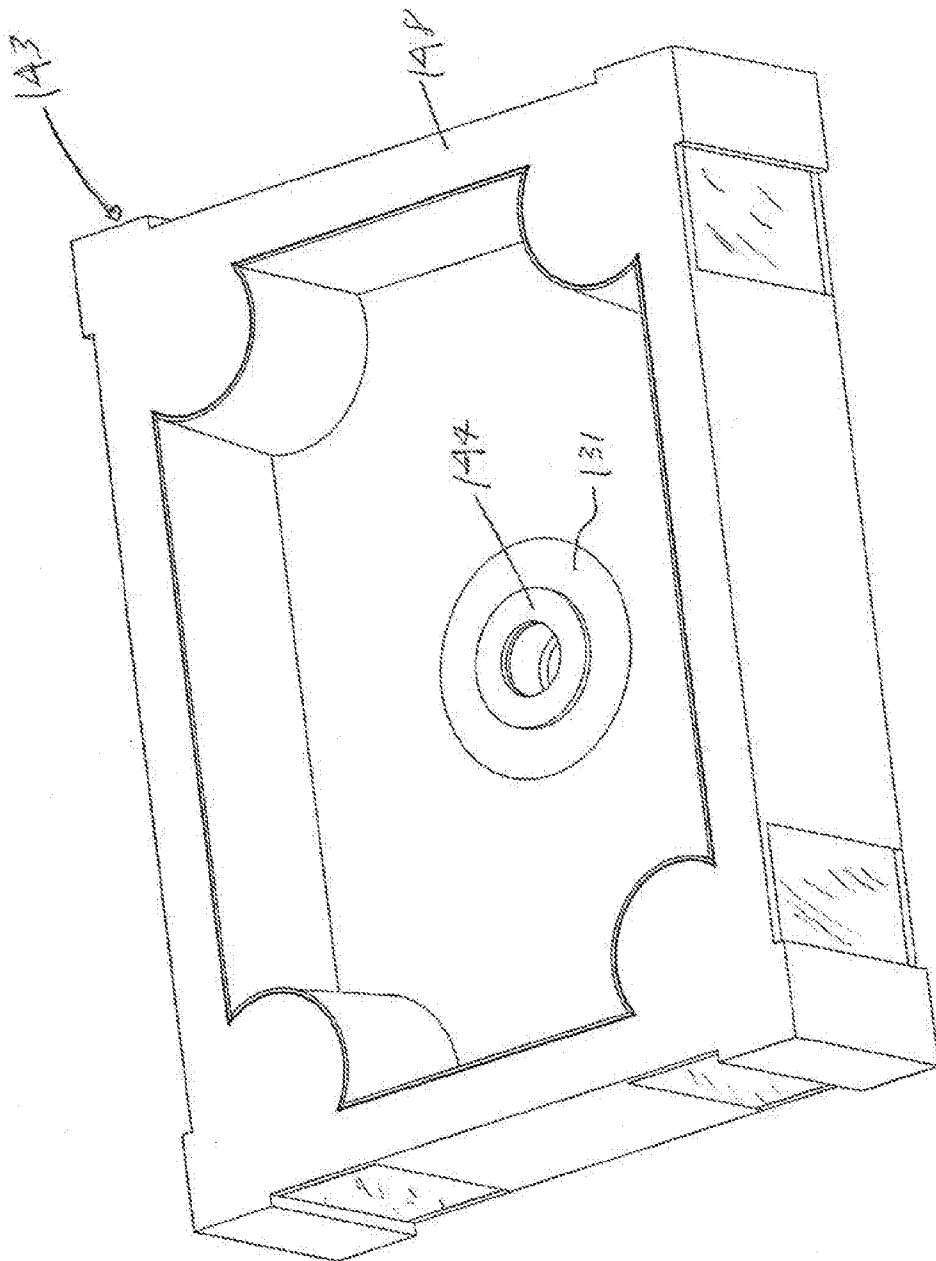


FIG. 11

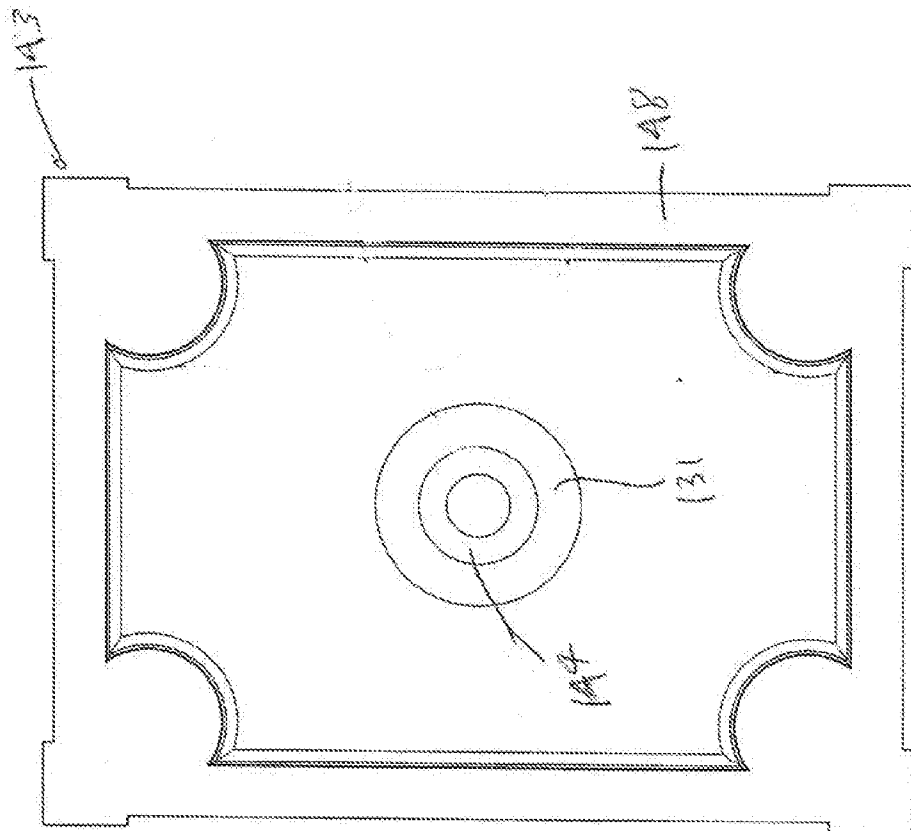


FIG. 12

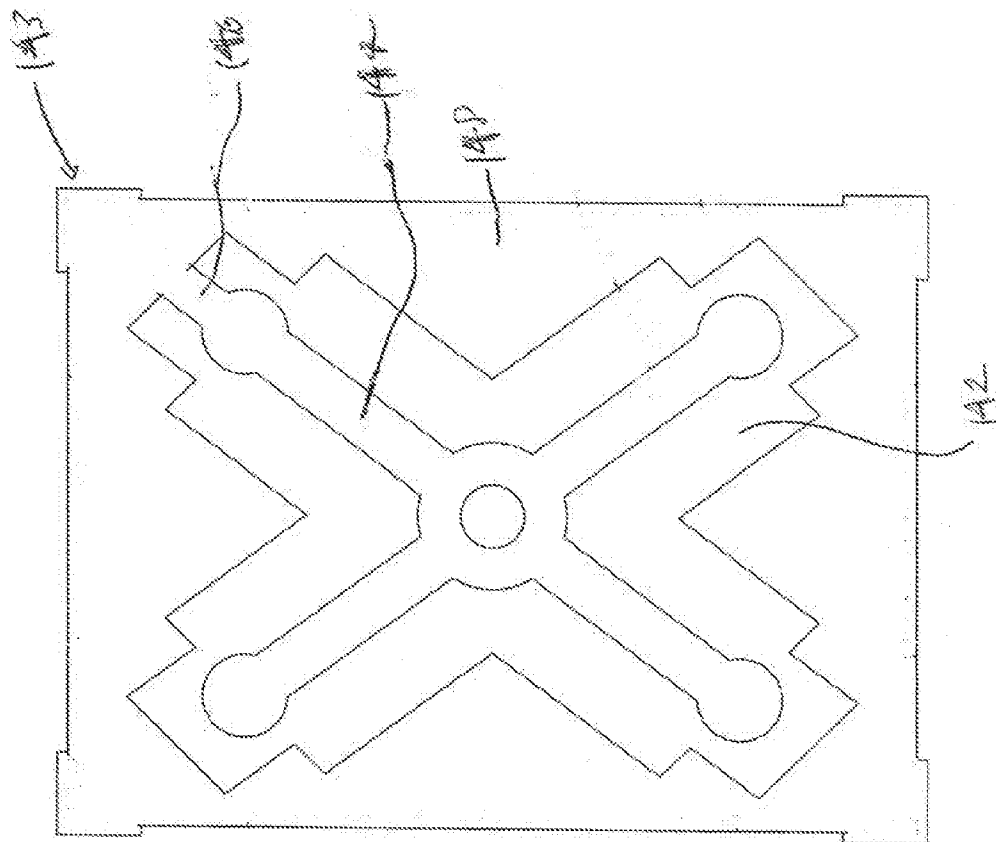


FIG. 13

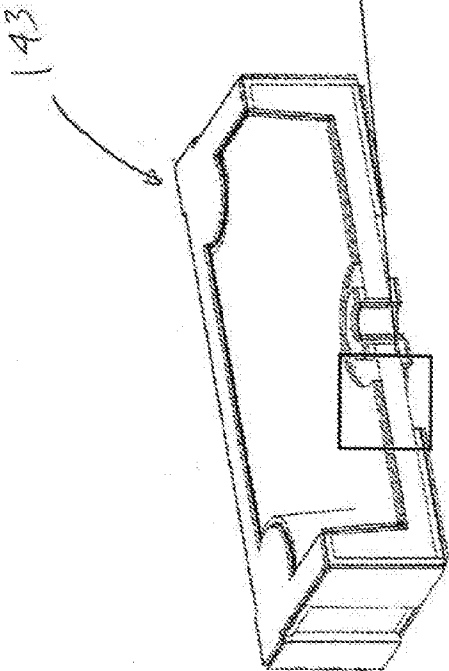


FIG. 14

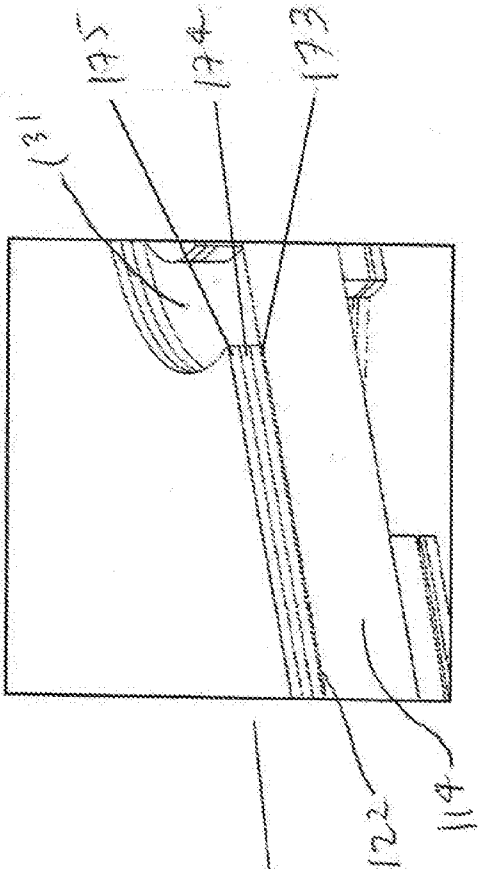


FIG. 15

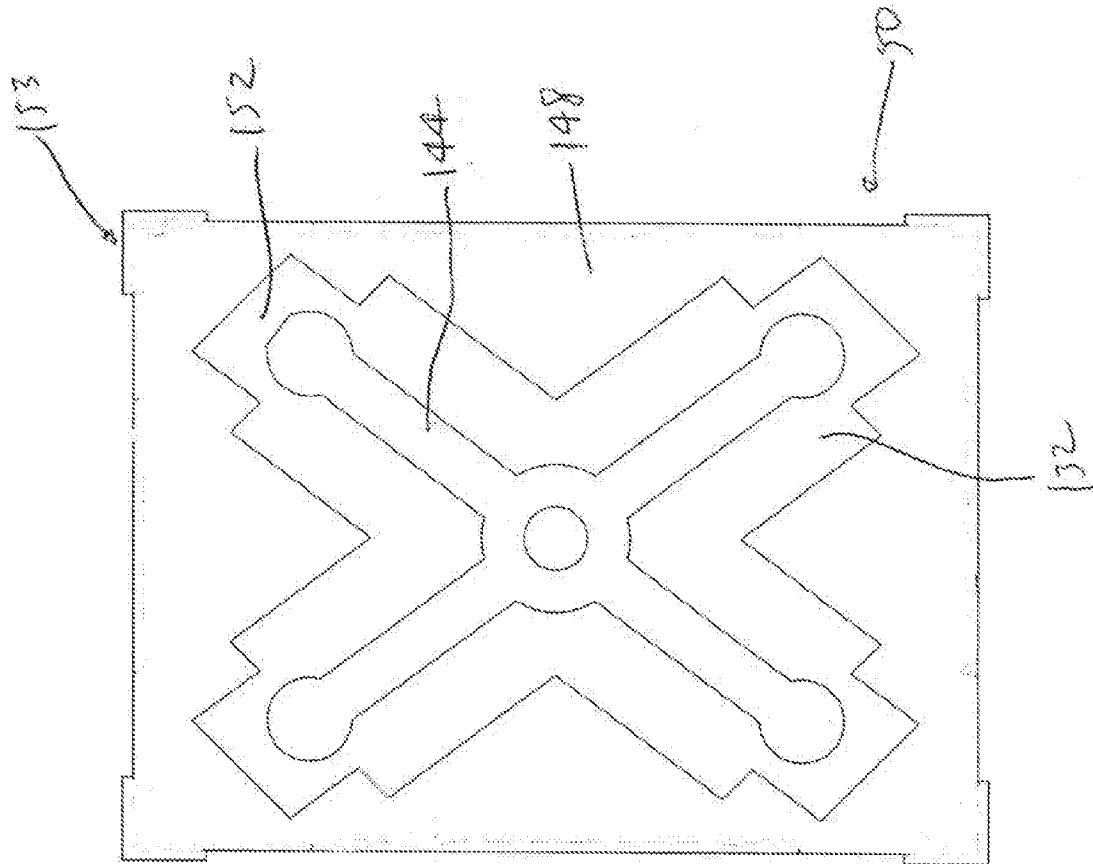


FIG. 16

FIG. 17

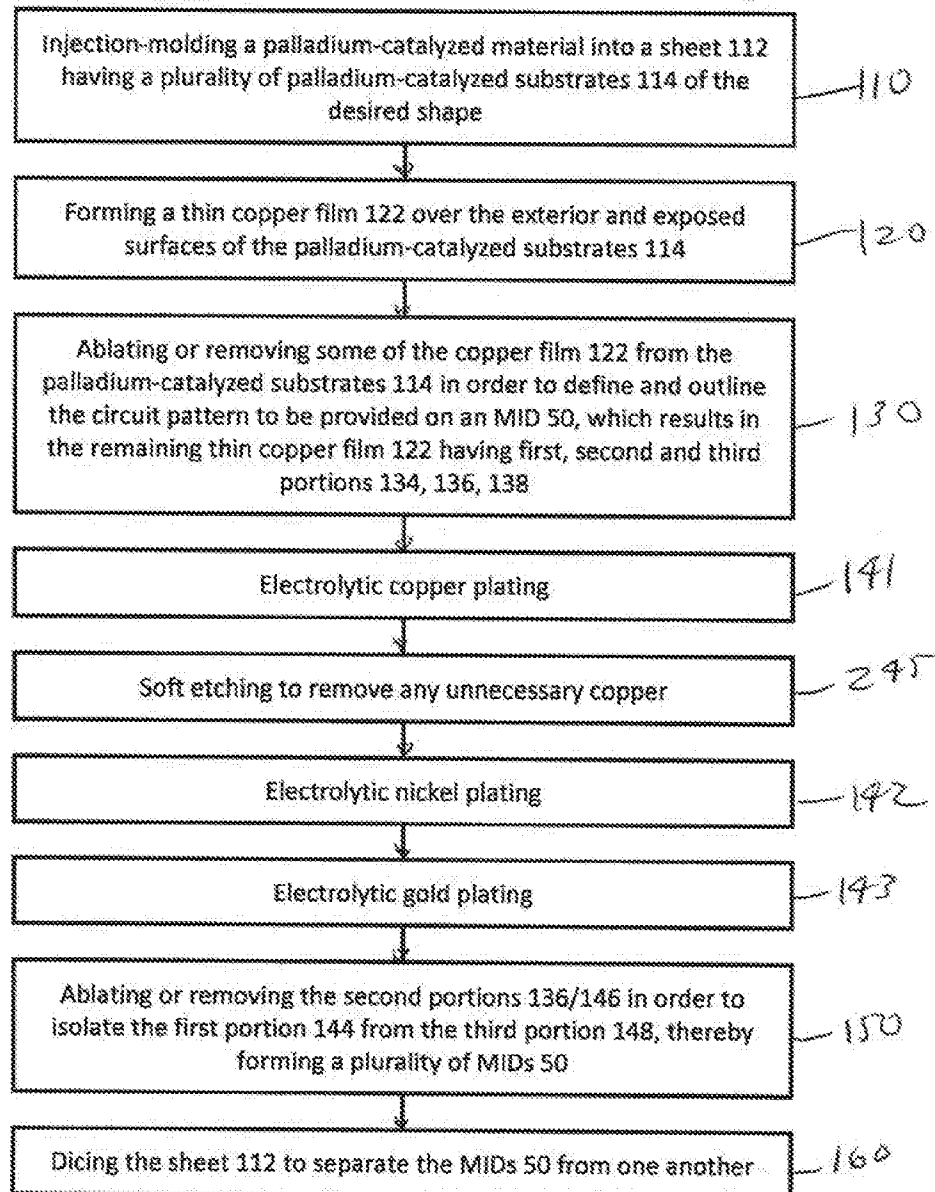
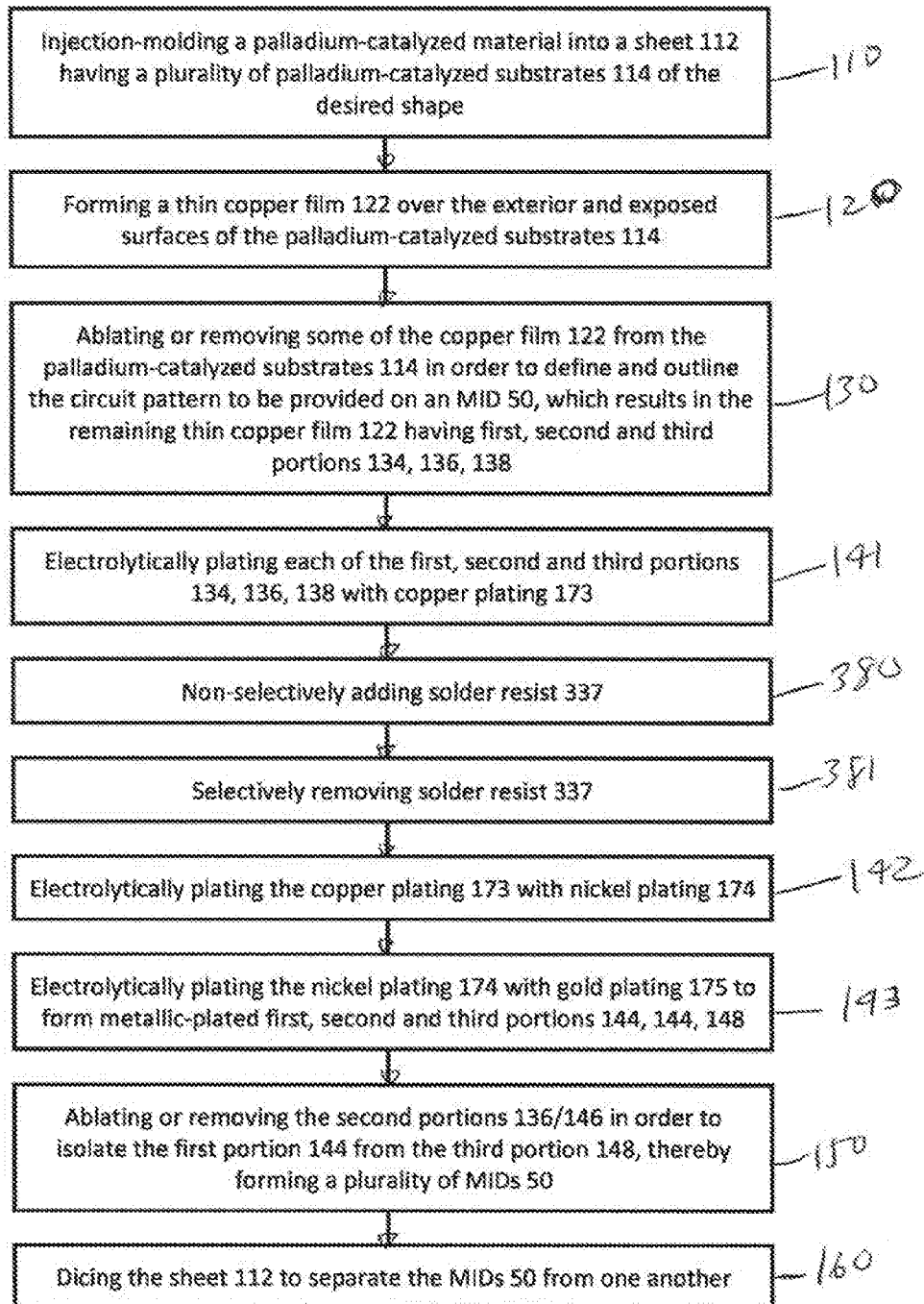


FIG. 18



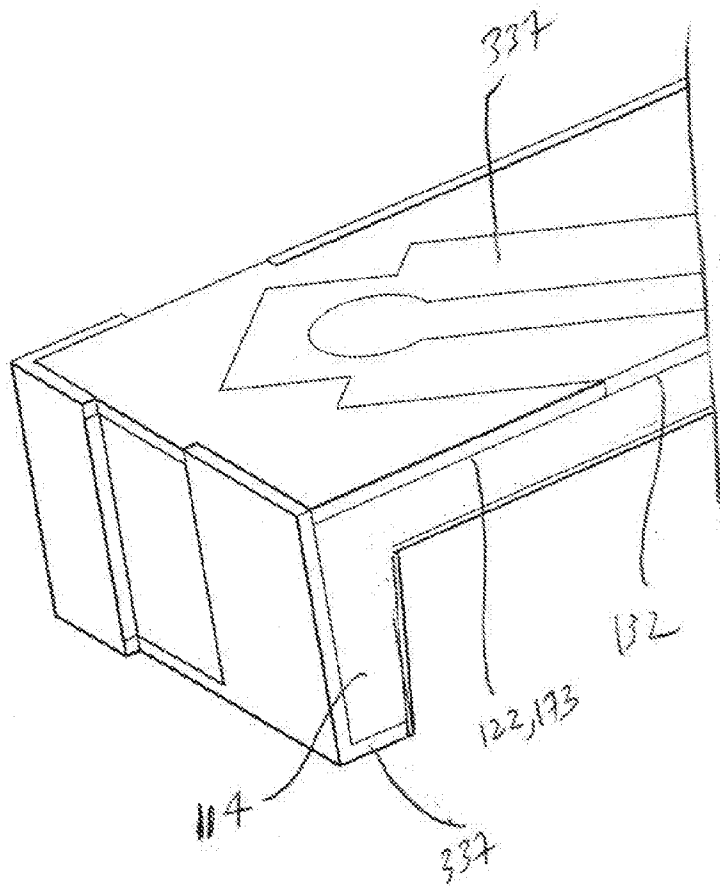


FIG. 19

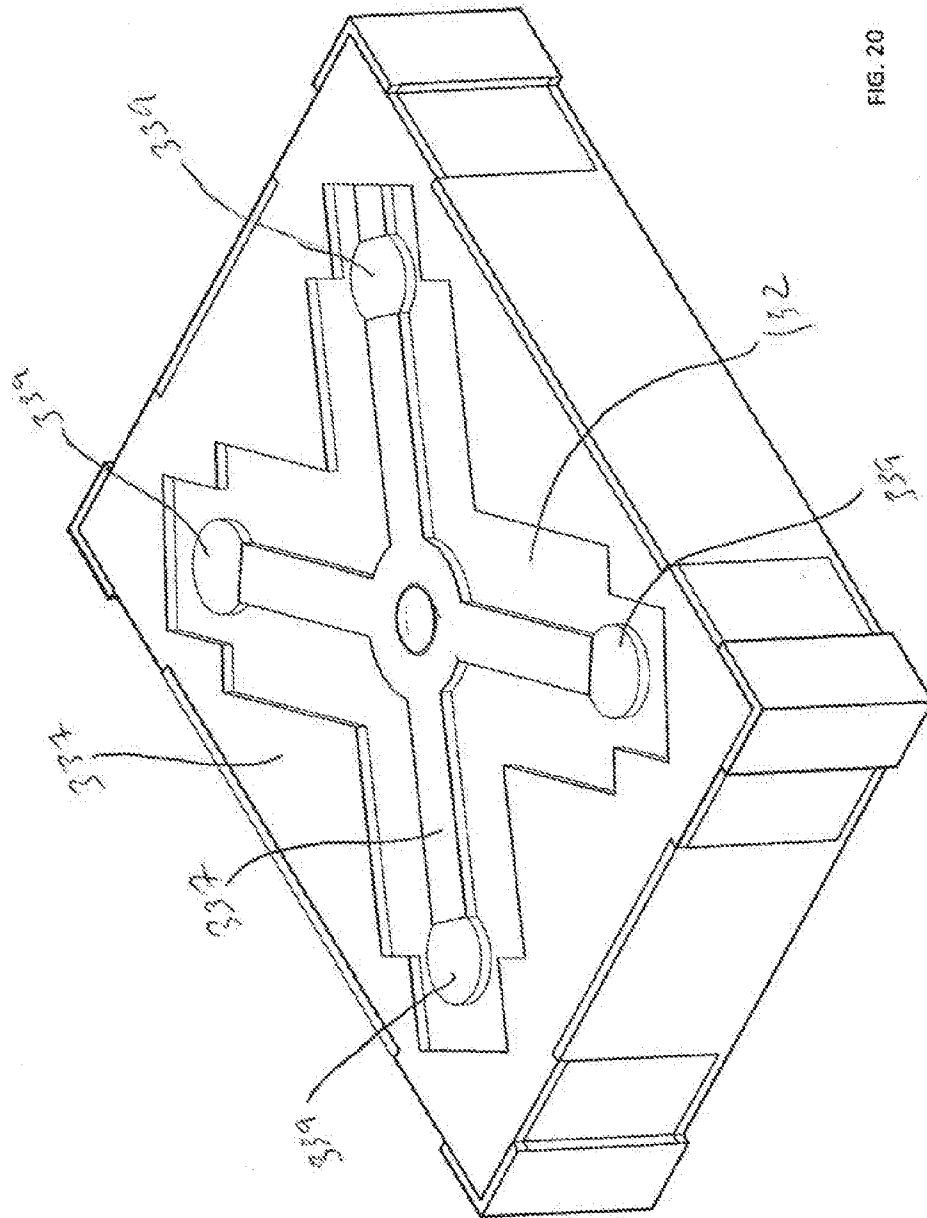


FIG. 20

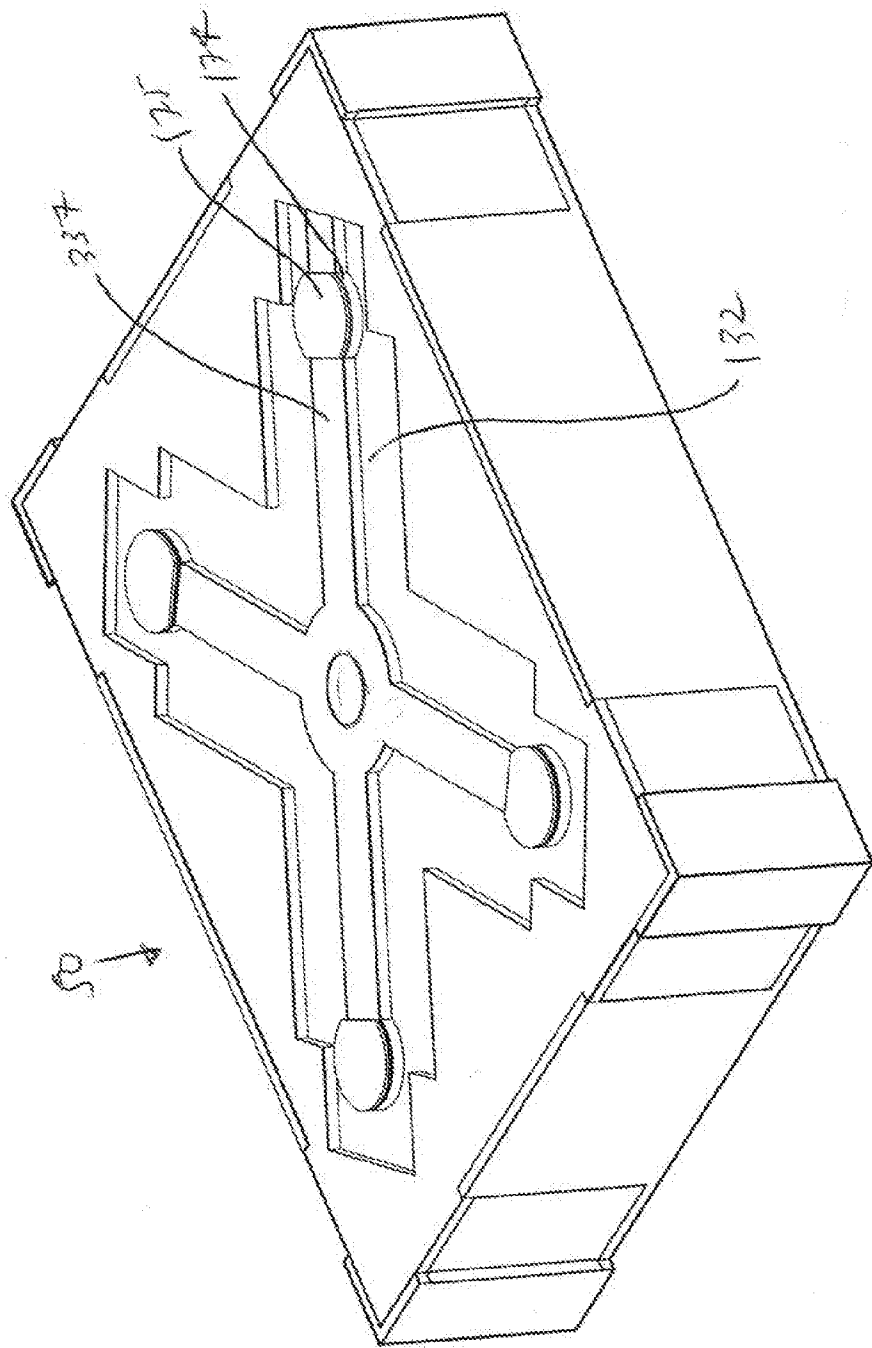
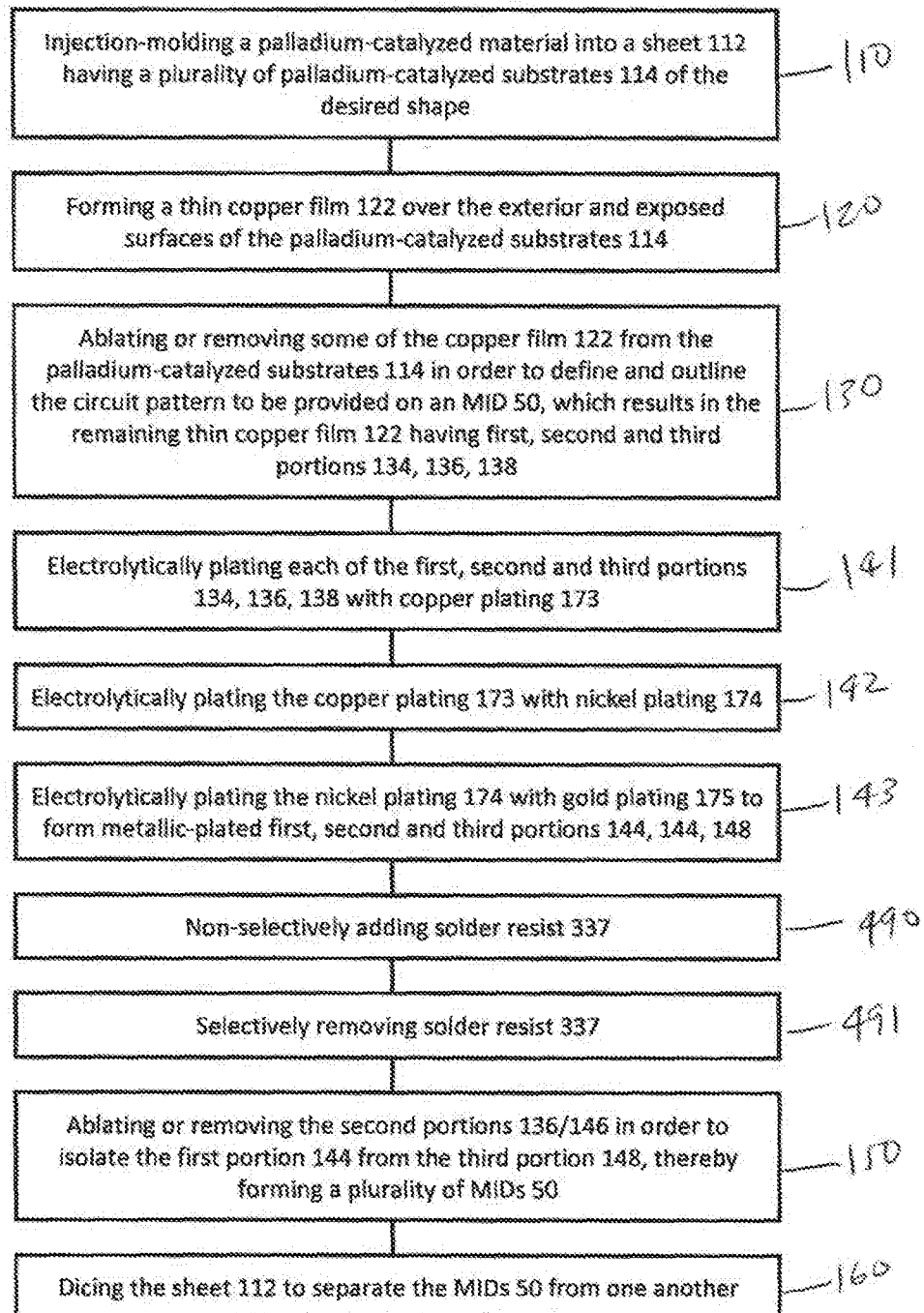


FIG. 21

FIG. 22



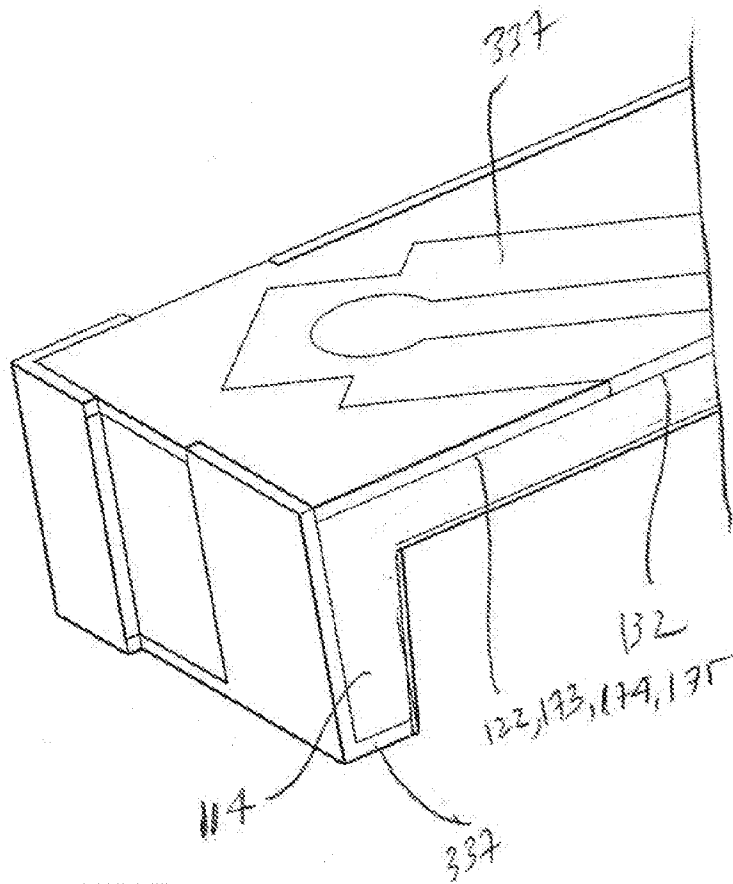
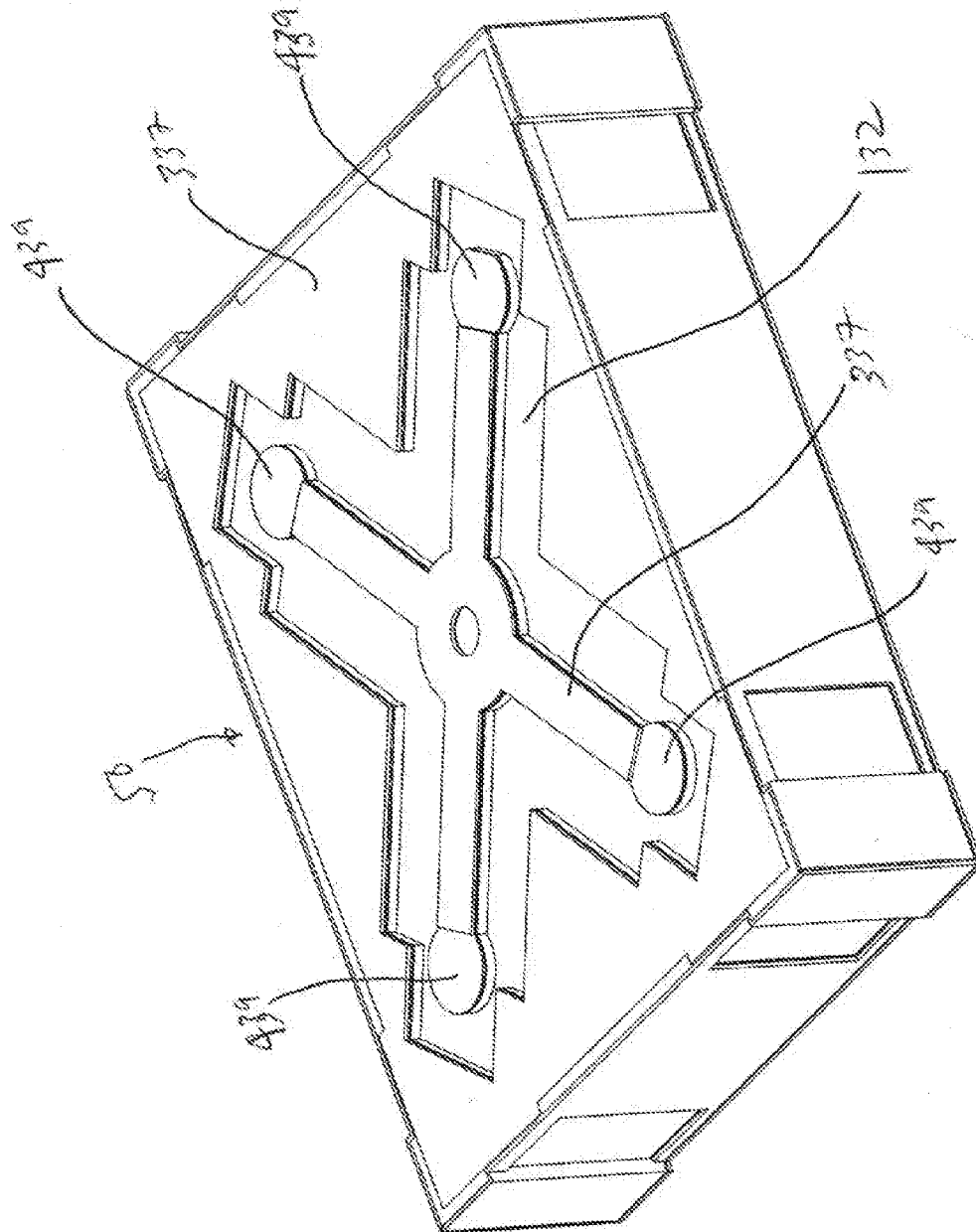


FIG. 23



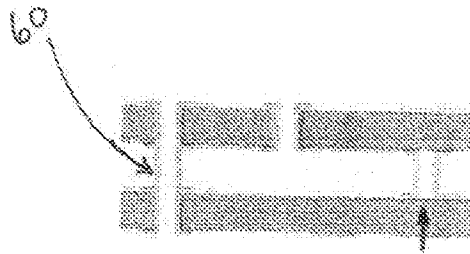


FIG. 25

PRIOR ART



FIG. 26

PRIOR ART

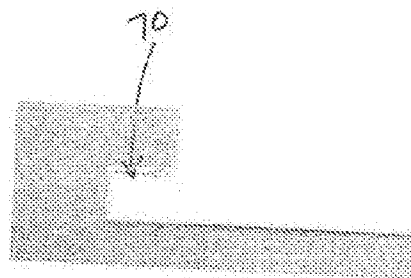


FIG. 27

PRIOR ART

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/040721**A. CLASSIFICATION OF SUBJECT MATTER****H05K 3/10(2006.01)i, H05K 3/04(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H05K 3/10; H05K 3/46; B32B 15/04; B29C 45/14; G01N 33/48; H04B 10/00; G01N 35/00; C23C 14/14; G02B 6/36; H05K 3/04

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: mold, interconnect, catalyst, substrate, palladium, laser, faraday

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2008-0212972 A1 (STEPHEN T. NELSON et al.) 04 September 2008 See paragraphs [0033]–[0065] and figure 2.	21–24
A		1–20
A	US 2008-0113205 A1 (THOMAS LICHTENEGGER et al.) 15 May 2008 See paragraphs [0035]–[0054] and figures 1–3.	1–24
A	US 2012-0134631 A1 (CHENG-FENG CHIANG et al.) 31 May 2012 See paragraphs [0051]–[0058] and figures 1–8.	1–24
A	US 2011-0303644 A1 (RICHARD MACARY) 15 December 2011 See paragraphs [0025]–[0032] and figures 1–3.	1–24
A	KR 10-1363157 B1 (CERAGEM MEDISYS INC.) 26 February 2014 See paragraphs [0087]–[0109] and figure 23.	1–24



Further documents are listed in the continuation of Box C.



See patent family annex.

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"E" earlier application or patent but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

20 September 2017 (20.09.2017)

Date of mailing of the international search report

21 September 2017 (21.09.2017)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

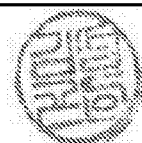


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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/040721

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