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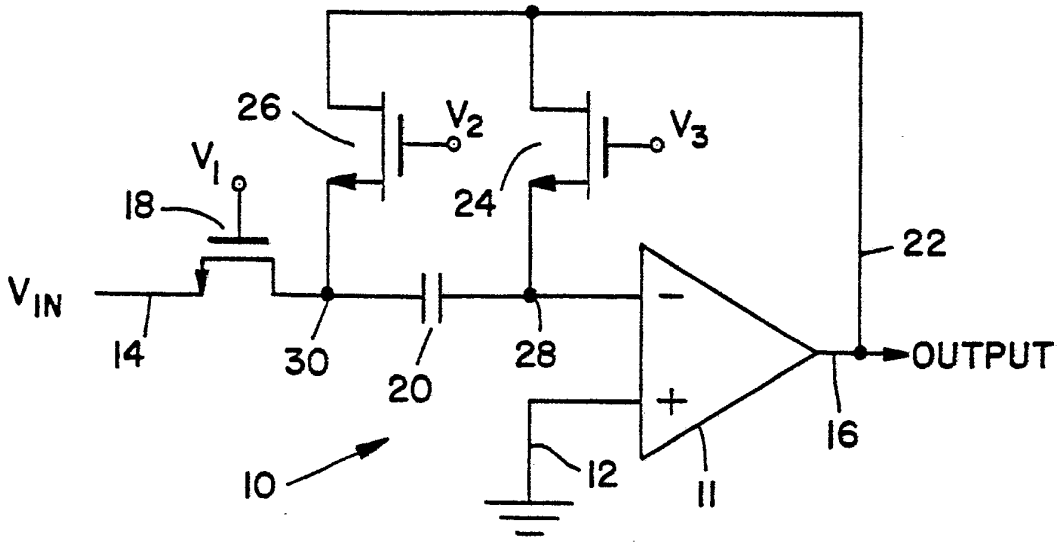

(57) Abstract

An operational amplifier based sample and hold circuit adapted for implementation as an integrated circuit is comprised of MOS transistor elements. The operational amplifier (11) has a positive terminal (+) connected to ground and a negative input lead connected to one side of a capacitor (20), the other side of which is connected to a first MOS transistor (18) whose gate is controlled by clock signals (V1). A feedback lead (22) from the operational amplifier output (16) is connected to second (24) and third (26) transistors in parallel. The second transistor (24) is connected to the input lead between the capacitor and the operational amplifier and the third transistor (26) is connected to the input lead between the capacitor and the first transistor. The gates of the second and third transistors are connected to separate clock signal sources (V3, V2). The timing of the clock signals to the three transistors is such that the Vin signal is sampled and held and the operational amplifier's offset is cancelled.

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SAMPLE AND HOLD CIRCUIT WITH OFFSET CANCELLATION

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and Roger Mao

Background of the Invention

This invention relates to operational amplifiers, and more particularly, to an improved operational amplifier voltage driven sample and hold circuit that can be implemented as an integrated monolithic circuit with no external components.

Sample and hold type operational amplifier circuits are used in data acquisition and data conversion (digital to analog or analog to digital conversion) systems where there is a need to sample a signal voltage and hold that voltage for a certain period of time. A problem which arose with such circuits, concerned the inherent offset voltage of the conventional sample and hold circuit and the variation of that offset voltage with temperature. Offset voltage may be defined as the value of the output voltage when sampling zero input voltage at a stated temperature.

In sample and hold operational amplifier circuits, it is desirable to eliminate offset voltage because it introduces errors in the signal being sampled. Further, change in the offset voltage with temperature causes this error to be temperature dependent and, therefore, not absolutely determinable at time of manufacture.

In sample and hold circuits previously devised, offset voltage cancellation was accomplished with external trimming using external resistors. However, such offset voltage trim devices were only good for the temperature at

which the trim was performed and therefore temperature variations of the offset voltage were not correctable.

It is a general object of the present invention to provide an improved operational amplifier based sample and hold circuit.

Another object of the present invention is to provide an operational amplifier sample and hold circuit that:

(1) cancels offset voltage normally associated with such circuits without requiring external circuitry;

(2) cancels the effects of temperature variations on the offset voltage; and

(3) cancels the effects of long term offset drift.

Another object of the present invention is to provide an operational amplifier sample and hold circuit that is made to work with zero common mode input voltage, thereby simplifying its design requirements.

Yet another object of the present invention is to provide an operational amplifier sample and hold circuit that is particularly adaptable for implementation as an MOS type integrated circuit semiconductor with no external components.

Summary of the Invention

In brief, the present invention provides an operational amplifier sample and hold circuit that is comprised of an amplifier having a bias section, a constant current source for a differential amplifier section and an output stage, all connected between common power leads supplying V_{DD} and V_{SS} power levels.

The input lead to the negative terminal of the operational amplifier is first connected through a first tran-

sistor whose gate is connected to a "sample" clock source. Connected between this switching transistor and the negative input terminal is a capacitor. A feedback lead from the output of the operational amplifier is connected in parallel to second and third transistors. This second transistor is connected to the input lead between the capacitor and the negative input terminal for the operational amplifier, and its gate is also connected to the "sample" clock source. The third transistor is connected to the input lead between the first transistor and the capacitor and its gate is connected to the "hold" clock source. When the "sample" clock is supplied to turn on the first and second transistors, the offset voltage through the output feedback of the operational amplifier is stored on the node between the capacitor and its negative input terminal. Simultaneously, the input signal Vin is present on the outer node between the capacitor and the first transistor. Subsequently, when the sample signal terminates and transistors one and two go off, the hold signal is applied to the gate of the third transistor and at the outer node the output voltage is forced to the value of Vin. Thus, Vin is sampled and held and the operational amplifier's offset has been cancelled. When the second transistor is provided with relatively small geometry and the capacitor has a relatively large value, the offset caused by switch feed through (i.e., when the second transistor goes off) can be kept suitably small. Such an amplifier, forced to work with zero common mode voltage, provides important advantages when implemented as an MOS integrated operational amplifier by easing the design requirements on the operational amplifier. The first, second and third transistors can be replaced with complementary devices, i.e., each transistor being replaced by a P-channel and an N-channel transistor tied in parallel to each other. This provides the device with a large signal handling capability because the complementary devices are capable of handling bipolar signals.

Other objects, advantages and features of the invention will become apparent from the following detailed description of a preferred embodiment presented in conjunction with the accompanying drawing.

Brief Description of the Drawing

Fig. 1 is a schematic block diagram of an operational amplifier based sample and hold device according to the present invention;

Fig. 2 is a voltage-timing diagram showing wave forms for the three control transistors for the circuit of Fig. 1A; and

Fig. 3 is a detailed circuit diagram for the device of Fig. 1.

Detailed Description of Embodiment

With reference to the drawing, Fig. 1 shows an operational amplifier based sample and hold circuit 10 embodying principles of the present invention. Generally, it comprises an operational amplifier 11 having a positive input terminal connected by a lead 12 to ground potential, a negative input terminal connected to a lead 14 and an output lead 16. An input lead 15 providing a signal voltage from a voltage driven signal source Vin is connected to the source of a first transistor 18 whose drain is connected to one side of a capacitor 20. The other side of this capacitor is connected to the negative input terminal of the operational amplifier.

A feedback lead 22 extends from the output lead 16 and is connected to the drain terminal of a second transistor 24 and also to the drain terminal of a third transistor 26 in parallel. The other source terminal of the

transistor 24 is connected to a node 28 in the lead 14, between the capacitor and the negative input terminal, and the source terminal of the third transistor 26 is connected to a node 30 between the first transistor and the capacitor.

The general operation of the circuit 10 may be explained with reference to the wave diagrams of Fig. 2. As shown in the "sample" phase, voltages V_3 and V_1 are first applied to the gates of transistors 24 and 18 to turn these transistors "on". Note that the voltage V_3 is slightly ahead of voltage V_1 in time. This is because transistor 26 must be "off" before transistor 24 turns "on" so that the offset voltage is stored and held on node 28 before transistor 24 turns "off". With transistor 24 turned on, the offset voltage of the operational amplifier 10 is stored on node 28 between the capacitor 20 and the negative input lead. The signal Vin is stored on the node 30 between the capacitor and the first transistor 18. Now, voltage V_3 goes off, followed by voltage V_1. A voltage V_2, supplied to the third transistor 26, turns on when V_1 is turned off and this connects the output to node 30, thereby forcing the output voltage to the value of Vin at node 30 (before V_1 went off). Thus, Vin is sampled and held and the operational amplifier's offset has been cancelled. Some residual offset does remain, due to capacitive feed through from V_3 through the parasitic gate overlap capacitance of transistor 24. However, this value is minimized by using a P-channel and an N-channel transistor with complementary clock drives, and by using a relatively large value capacitor 20.

In Fig. 3, a full circuit diagram for the sample and hold type circuit 10 is shown in greater detail, including all of the elements of a particular operational amplifier 10 comprised of complementary MOS elements.

In general, the operational amplifier 10 is comprised of a differential amplifier 32, connected to a biasing network 34, and an intermediate level shift stage 36, connected to an output stage 38. The differential amplifier typically includes an input stage 40 and a constant current source 42.

All but one of the transistor elements of the various components of the operational amplifier 10 are MOSFET devices and most of them operate in the saturation mode as opposed to the linear mode. The bias network 34 which assures that the appropriate MOSFET devices of the circuit operate in the proper saturation region, comprises two MOSFET devices 44 and 46, each having source, drain and gate electrodes. The source electrode of transistor 44 is connected to a positive voltage supply V_{DD} via a power lead 48 and the source of transistor 46 is connected by a lead 50 to a negative power supply V_{SS}. The drain and gate electrodes of transistor 44 are connected to a junction 52 and the drain and gate electrodes of transistor 46 are connected to a junction 54. These junctions 52 and 54 are interconnected by a lead 56, and a lead 58, from the junction 54 provides the biasing voltage for the circuit.

The constant current source 42 comprises a MOSFET device 60, whose gate is connected to the biasing voltage lead 58. The source of transistor 60 is connected to the negative power lead 50 and its drain is connected to the input stage 40 of the differential amplifier.

This input stage comprises a pair of MOSFET devices 62 and 64, whose respective source electrodes are connected to a common lead 66, which is also connected to the drain of transistor 60. A drain electrode of the device 62 is connected to a junction 68 of the differential amplifier and the drain electrode of device 64 is connected to a junction 70 of the differential amplifier.

The gate of input device 62 is connected to a negative input terminal of the operational amplifier and the gate of device 64 is connected to ground.

The load section of the differential amplifier 32 comprises a pair of MOSFET devices 72 and 74, whose source terminals are both connected to the positive power lead 48. The gates of these devices are interconnected by a lead 76 which is also connected by a lead 78 to the junction 68.

The intermediate level shift stage 36 of the operational amplifier 11 comprises a pair of MOSFET devices 80 and 82, connected in series between the positive and negative power leads. The drain of device 80 is connected to the positive power lead 48 and the source of device 82 is connected to the negative power lead 50.

The source of device 80 is connected by a lead 84 to the drain of device 82. The gate of device 80 is connected by a lead 86 from the junction 70. A first junction 88 in the lead 86 is connected by a lead 90 to the gate of a MOSFET device 92 in the ouput stage 38 of the operational amplifier 11. A second junction 94 in the lead 86 is connected by a lead 96 to one side of a capacitor 98, whose other side is connected to the lead 84.

The output stage 38 comprises the MOSFET device 92, whose source is connected to the positive power lead 48 and a second MOSFET device 100 whose source is connected to the negative power lead 50. The drain electrodes of these two transistors are interconnected by a common lead 102. The gate of MOSFET 100 is connected by a lead 104 to a junction 106 in the lead 84 between the devices 80 and 82. A second portion of the output stage is preferably provided in the form of an NPN transistor 108 whose emitter terminal is connected by a lead 110 to an N-channel MOS

transistor 112. The collector of device 108 is connected to V_{DD} line 48 and the source of transistor 112 is connected to V_{SS} line 50. The base of transistor 108 is connected by a lead 114 to the interconnecting lead 102 and the gate of device 112 is connected to the lead 104 from the level shift section.

A frequency compensation means for the operational amplifier is preferably provided between the differential amplifier section 32 and the output stage 38. It comprises a capacitor 116 (C_2) having one side connected to a junction 118 in the output side of the differential amplifier 32. The other side of this capacitor is connected by a lead 120 to an interconnection lead 122 between the drain electrodes of two MOSFET devices 124 and 126, whose sources are both connected to one end of a lead 128, whose other end terminates at an output junction 130 for the operational amplifier 11 in the lead 110. The gate of MOSFET 124 is connected to power lead 48 and the gate of MOSFET 126 is connected to lead 50. In a lead 127 between the leads 102 and 104, is a capacitor 129 which is used to frequency compensate the output stage.

The operational amplifier 11 functions in the conventional manner but has a Class A-B drive, which provides for unusually low power dissipation. A more detailed description of this operational amplifier 11 may be found in my co-pending application, Serial No._____, filed _____. However, other operational amplifier circuits may be used with the sample and hold circuit of the present invention. The example shown in Fig. 3 illustrates how the entire circuit 10 may be conveniently and efficiently formed with CMOS transistor elements (and compatible NPN type transistors) to provide the necessary offset cancellation function. Thus, the circuit 10 may be readily included as one of several building blocks of much larger integrated circuits re-

quiring voltage driven sample and hold functions.

Although the embodiment shown utilizes single gate MOS transistor devices 18, 24 and 26, it should be readily apparent that the invention also contemplates the use of complementary dual-gate devices in lieu of the devices 18, 24 and 26, in order to accommodate bipolar signal inputs.

To those skilled in the art to which this invention relates, many changes in construction and widely differing embodiments and applications of the invention will suggest themselves without departing from the spirit and scope of the invention. The disclosures and the description herein are purely illustrative and are not intended to be in any sense limiting.

I claim:

IN THE CLAIMS:

1. A sample and hold circuit comprising an operational amplifier having a positive input terminal connected to ground, a negative input terminal connected to an input conductor and to an output with a feedback conductor connected to said output, a capacitor, a first transistor means having one terminal adapted for connection to a data source and a second terminal connected to one side of said capacitor, with a gate means connected to a first clock signal source, means for connecting the other side of said capacitor to said negative input terminal of said operational amplifier, further characterized by containing:

a second and a third transistor means, each having one terminal connected to said feedback conductor, the other terminal of said second transistor being connected to a first node in said input conductor between said negative input terminal and said capacitor, the other terminal of said third transistor means being connected to a second node in said input conductor between said first transistor means and said capacitor; and gate means for said second and third transistor means connected to second and third clock signal sources.

2. The sample and hold circuit as described in claim 1 further characterized in that said clock signal to said first transistor means is timed to be slightly ahead of the clock signals to the gate of said second transistor.

3. The sample and hold circuit as described in claim 1 further characterized in that said transistor means are each N-channel MOS single gate transistors.

4. The sample and hold circuit as described in claim 1 further characterized in that all three of said transistor means are complementary MOS transistors controllable by bipolar clock signals.

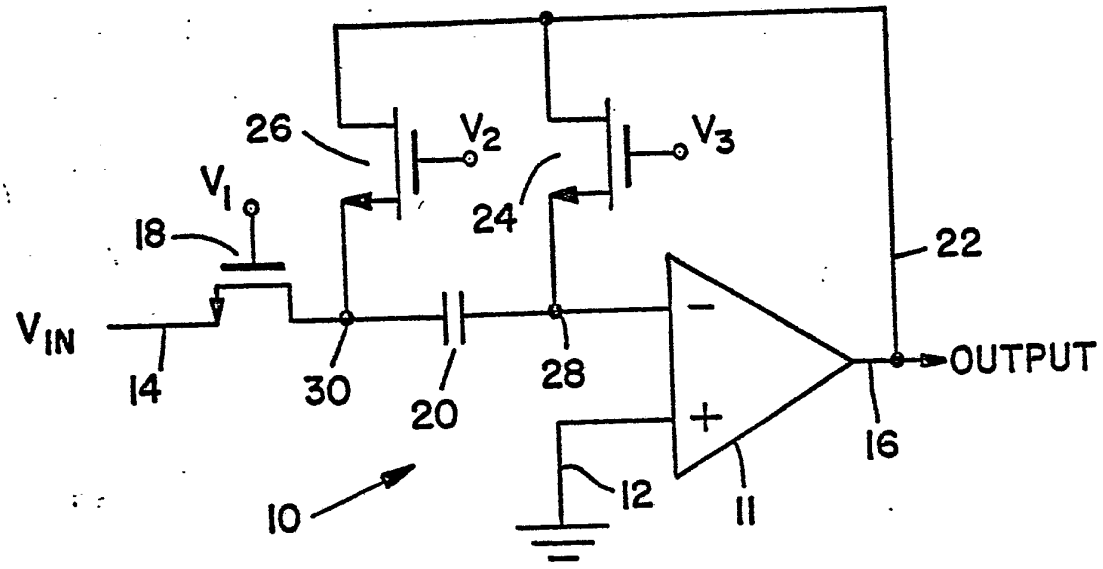

FIG_1

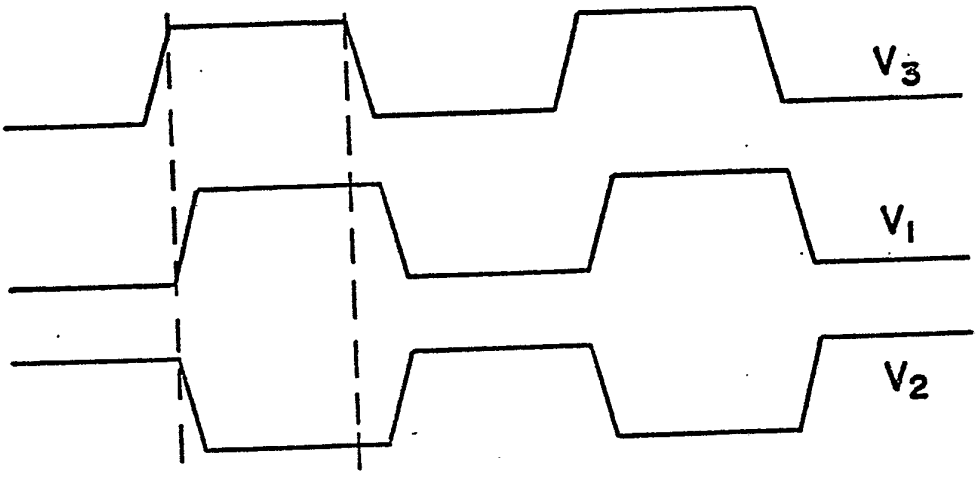

FIG_2

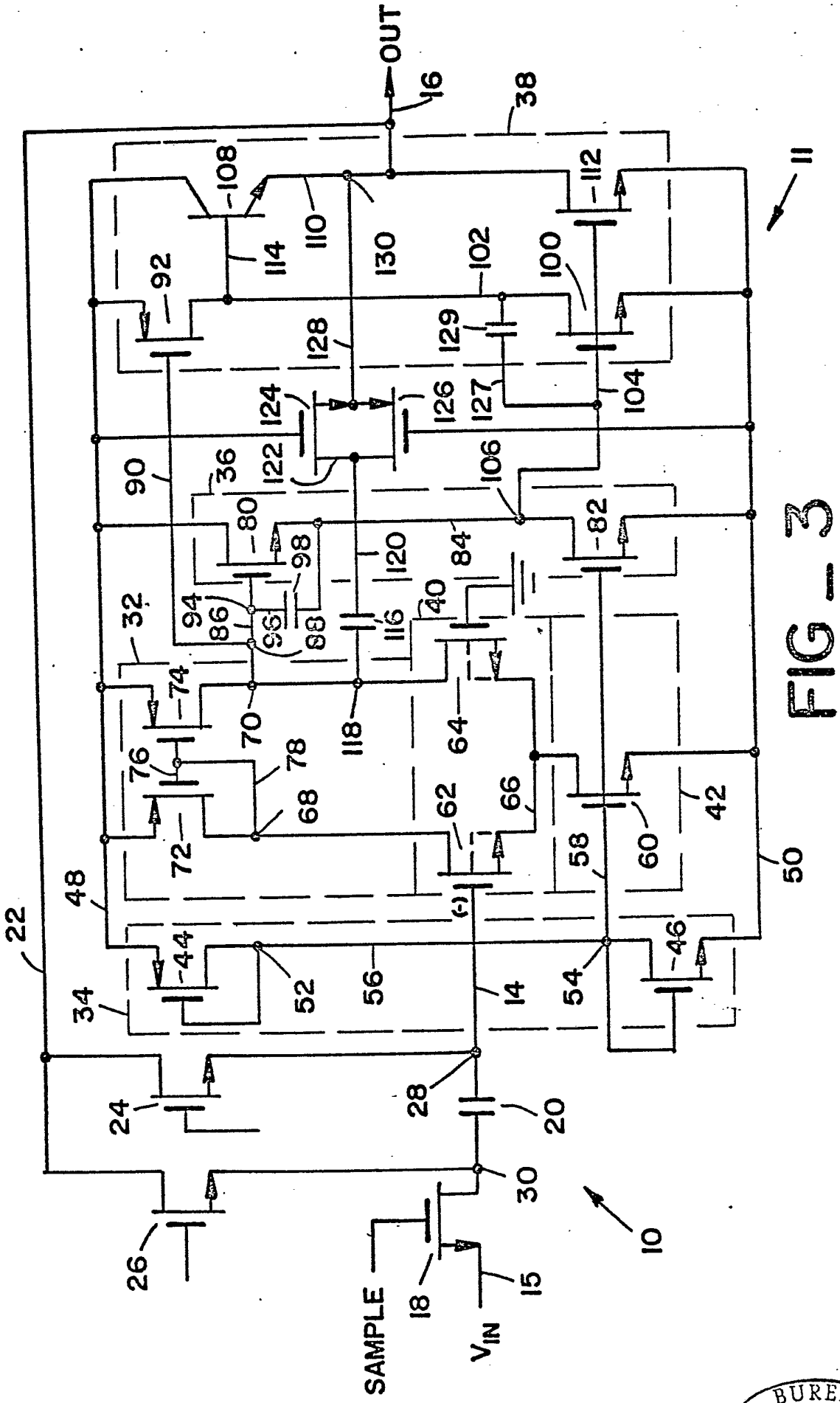

FIG - 3

INTERNATIONAL SEARCH REPORT

International Application No PCT/US80/01130

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

INT. CL.[3] G11C 27/02
US. Cl. 307/353

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
U.S.	307/251, 352, 353 328/128, 151, 162

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
X	US, A, 4,066,919, Published 02 January 1978 Huntington	1-4

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IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
11 December 1980	31 DEC 1980
International Searching Authority [1]	**Signature of Authorized Officer** [20]
ISA/US	John Zazworsky