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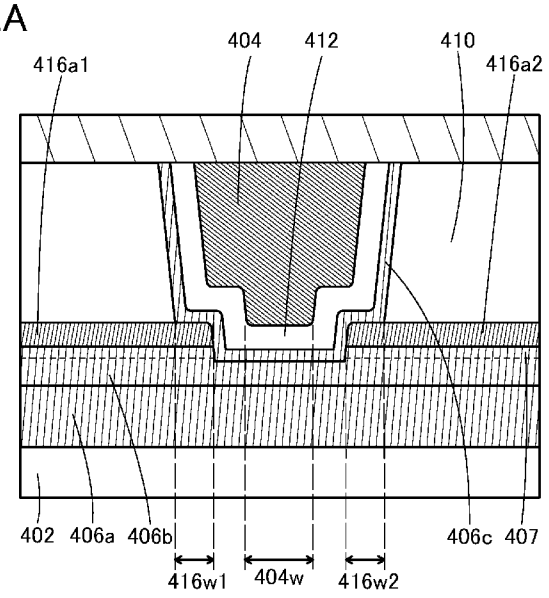
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(54) Title: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

FIG. 2A



(57) Abstract: A minute transistor is provided. A transistor with low parasitic capacitance is provided. A transistor having high frequency characteristics is provided. A semiconductor device including the transistor is provided. A semiconductor device includes an oxide semiconductor, a first conductor, a second conductor, a third conductor, a first insulator, and a second insulator. The first conductor overlaps with the oxide semiconductor with the first insulator positioned therebetween. The second insulator has an opening and a side surface of the second insulator overlaps with a side surface of the first conductor in the opening with the first insulator positioned therebetween. Part of a surface of the second conductor and part of a surface of the third conductor are in contact with the first insulator in the opening. The oxide semiconductor overlaps with the second conductor and the third conductor.

DESCRIPTION

SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

TECHNICAL FIELD

[0001]

The present invention relates to, for example, a transistor, a semiconductor device, and manufacturing methods thereof. The present invention relates to, for example, a display device, a light-emitting device, a lighting device, a power storage device, a memory device, a processor, and an electronic device. The present invention relates to a method for manufacturing a display device, a liquid crystal display device, a light-emitting device, a memory device, and an electronic device. The present invention relates to a driving method of a semiconductor device, a display device, a liquid crystal display device, a light-emitting device, a memory device, and an electronic device.

[0002]

Note that one embodiment of the present invention is not limited to the above technical field. The technical field of one embodiment of the invention disclosed in this specification and the like relates to an object, a method, or a manufacturing method. In addition, one embodiment of the present invention relates to a process, a machine, manufacture, or a composition of matter.

[0003]

In this specification and the like, a semiconductor device generally means a device that can function by utilizing semiconductor characteristics. A display device, a light-emitting device, a lighting device, an electro-optical device, a semiconductor circuit, and an electronic device include a semiconductor device in some cases.

BACKGROUND ART

[0004]

In recent years, a transistor including an oxide semiconductor has attracted attention. An oxide semiconductor can be formed by a sputtering method or the like, and thus can be used for a semiconductor of a transistor in a large display device. In addition, the transistor including an oxide semiconductor is advantageous in reducing capital investment because part of production equipment for a transistor including amorphous silicon can be retrofitted and utilized.

[0005]

It is known that a transistor including an oxide semiconductor has an extremely low

leakage current in an off state. For example, a low-power-consumption CPU utilizing a characteristic of low leakage current of the transistor including an oxide semiconductor is disclosed (see Patent Document 1).

[0006]

Furthermore, a method for manufacturing a transistor including an oxide semiconductor in which a gate electrode is embedded in an opening is disclosed (see Patent Documents 2 and 3).

[Reference]

[Patent Document]

[0007]

[Patent Document 1] Japanese Published Patent Application No. 2012-257187

[Patent Document 2] Japanese Published Patent Application No. 2014-241407

[Patent Document 3] Japanese Published Patent Application No. 2014-240833

DISCLOSURE OF INVENTION

[0008]

An object is to provide a minute transistor. Another object is to provide a transistor with low parasitic capacitance. Another object is to provide a transistor having high frequency characteristics. Another object is to provide a transistor with favorable electric characteristics. Another object is to provide a transistor having stable electric characteristics. Another object is to provide a transistor having low off-state current. Another object is to provide a novel transistor. Another object is to provide a semiconductor device including the transistor. Another object is to provide a semiconductor device that operates at high speed. Another object is to provide a novel semiconductor device. Another object is to provide a module including any of the above semiconductor devices. Another object is to provide an electronic device including any of the above semiconductor devices or the module.

[0009]

Note that the descriptions of these objects do not disturb the existence of other objects. In one embodiment of the present invention, there is no need to achieve all the objects. Other objects will be apparent from and can be derived from the description of the specification, the drawings, the claims, and the like.

[0010]

(1) One embodiment of the present invention is a semiconductor device including an oxide semiconductor, a first conductor, a second conductor, a third conductor, a first insulator, and a second insulator. The first conductor overlaps with the oxide semiconductor with the first

insulator positioned therebetween. The second insulator has an opening and a side surface of the second insulator overlaps with a side surface of the first conductor in the opening with the first insulator positioned therebetween. Part of a surface of the second conductor and part of a surface of the third conductor are in contact with the first insulator in the opening. The oxide semiconductor overlaps with the second conductor and the third conductor.

[0011]

(2) One embodiment of the present invention is the semiconductor device described in (1) where the first conductor is a multi-layer film including a conductor that is less likely to allow passage of oxygen.

[0012]

(3) One embodiment of the present invention is the semiconductor device described in (1) or (2) where each of the second conductor and the third conductor is a multi-layer film including a conductor that is less likely to allow passage of oxygen.

[0013]

(4) One embodiment of the present invention is the semiconductor device described in any one of (1) to (3) where a third insulator overlaps with the oxide semiconductor, and the third insulator contains at least one of main component elements of the oxide semiconductor other than oxygen.

[0014]

(5) One embodiment of the present invention is the semiconductor device described in any one of (1) to (4) where the first conductor has a region serving a gate electrode of a transistor, and the transistor has a gate line width of greater than or equal to 5 nm and less than or equal to 60 nm.

[0015]

(6) One embodiment of the present invention is a method for manufacturing a semiconductor device, including the following steps: forming a second insulator over a first insulator; forming an oxide semiconductor over the second insulator; forming a first conductor over the oxide semiconductor; etching part of the first conductor, part of the oxide semiconductor, and part of the second insulator to form a multi-layer film including the first conductor, the oxide semiconductor, and the second insulator; forming a third insulator over the first insulator and the multi-layer film; forming an opening exposing the oxide semiconductor in the third insulator and the first conductor to separate the first conductor into a first conductor layer and a second conductor layer; etching part of the third insulator to expand the opening and to expose a top surface of the first conductor layer and a top surface of the second conductor layer; forming a fourth insulator over the third insulator, the first conductor layer, the second conductor layer, and

the oxide semiconductor; forming a fifth insulator over the fourth insulator; forming a third conductor over the fifth insulator; and performing chemical mechanical polishing on the third conductor, the fifth insulator, and the fourth insulator to expose the third insulator. The second insulator and the fourth insulator contain at least one of main component elements of the oxide semiconductor other than oxygen.

[0016]

(7) One embodiment of the present invention is a method for manufacturing a semiconductor device, including the following steps: forming a second insulator over a first insulator; forming an oxide semiconductor over the second insulator; forming a first conductor over the oxide semiconductor; etching part of the first conductor, part of the oxide semiconductor, and part of the second insulator to form a multi-layer film including the first conductor, the oxide semiconductor, and the second insulator; forming a third insulator over the first insulator and the multi-layer film; forming an opening exposing the oxide semiconductor in the third insulator and the first conductor to separate the first conductor into a first conductor layer and a second conductor layer; etching part of the third insulator to expand the opening and to expose a top surface of the first conductor layer and a top surface of the second conductor layer; forming a fourth insulator over the third insulator, the first conductor layer, the second conductor layer, and the oxide semiconductor; forming a fifth insulator over the fourth insulator; forming a third conductor over the fifth insulator; performing chemical mechanical polishing on the third conductor, the fifth insulator, and the fourth insulator to expose the third insulator; forming a sixth insulator over the third insulator and the third conductor using plasma including oxygen to add the oxygen in the plasma to the third insulator as excess oxygen; and performing heat treatment to move the excess oxygen to the oxide semiconductor. The second insulator and the fourth insulator contain at least one of main component elements of the oxide semiconductor other than oxygen.

[0017]

(8) One embodiment of the present invention is a method for manufacturing a semiconductor device, including the following steps: forming a second insulator over a first insulator; forming an oxide semiconductor over the second insulator; forming a first conductor over the oxide semiconductor; etching part of the first conductor, part of the oxide semiconductor, and part of the second insulator to form a multi-layer film including the first conductor, the oxide semiconductor, and the second insulator; forming a third insulator over the first insulator and the multi-layer film; forming, in the third insulator, an opening exposing the multi-layer film and an opening exposing the first insulator; forming an organic film over the first insulator, the third insulator, a side surface of the third insulator, the multi-layer film, and the side surface of the

multi-layer film; etching part of the organic film with the organic film over the side surface of the third insulator and the side surface of the multi-layer film left; etching the first conductor using the organic film left over at least the side surface of the third insulator as a mask to separate the first conductor into a first conductor layer and a second conductor layer; removing the organic film over the side surface of the third insulator and the side surface of the multi-layer film to form an opening reaching a surface of the first conductor layer and a surface of the second conductor layer; forming a fourth insulator over the third insulator, the first conductor layer, the second conductor layer, and the oxide semiconductor; forming a fifth insulator over the fourth insulator; forming a third conductor over the fifth insulator; performing chemical mechanical polishing on the third conductor, the fifth insulator, and the fourth insulator to expose the third insulator; and forming a sixth insulator over the third insulator and the third conductor. The second insulator and the fourth insulator contain at least one of main component elements of the oxide semiconductor other than oxygen.

[0018]

(9) One embodiment of the present invention is a method for manufacturing a semiconductor device, including the following steps: forming a second insulator over a first insulator; forming an oxide semiconductor over the second insulator; forming a first conductor over the oxide semiconductor; etching part of the first conductor, part of the oxide semiconductor, and part of the second insulator to form a multi-layer film including the first conductor, the oxide semiconductor, and the second insulator; forming a third insulator over the first insulator and the multi-layer film; forming, in the third insulator, an opening exposing the multi-layer film and an opening exposing the first insulator; forming an organic film over the first insulator, the third insulator, a side surface of the third insulator, the multi-layer film, and the side surface of the multi-layer film; etching part of the organic film with the organic film over the side surface of the third insulator and the side surface of the multi-layer film left; etching the first conductor using the organic film left over at least the side surface of the third insulator as a mask to separate the first conductor into a first conductor layer and a second conductor layer; removing the organic film over the side surface of the third insulator and the side surface of the multi-layer film to form an opening reaching a surface of the first conductor layer and a surface of the second conductor layer; forming a fourth insulator over the third insulator, the first conductor layer, the second conductor layer, and the oxide semiconductor; forming a fifth insulator over the fourth insulator; forming a third conductor over the fifth insulator; performing chemical mechanical polishing on the third conductor, the fifth insulator, and the fourth insulator to expose the third insulator; forming a sixth insulator over the third insulator and the third conductor using plasma including oxygen to add the oxygen in the plasma to the third insulator as excess oxygen;

and performing heat treatment to transfer the excess oxygen to the oxide semiconductor. The second insulator and the fourth insulator contain at least one of main component elements of the oxide semiconductor other than oxygen.

[0019]

(10) One embodiment of the present invention is the method for manufacturing the semiconductor device described in any one of (6) to (9), further including a step of forming a fourth conductor that is less likely to allow passage of oxygen than the first conductor, over the first conductor.

[0020]

(11) One embodiment of the present invention is the method for manufacturing the semiconductor device described in any one of (6) to (10), further including a step of forming a fifth conductor that is less likely to allow passage of oxygen than the third conductor, below the third conductor.

[0021]

(12) One embodiment of the present invention is the method for manufacturing a semiconductor device described in any one of (8) to (11) where the organic film is formed by plasma using a gas containing carbon and halogen.

[0022]

(13) One embodiment of the present invention is the method for manufacturing the semiconductor device described in any one of (6) to (12) where the sixth insulator is an insulator that is less likely to allow passage of oxygen than the first insulator, the third insulator, and the fifth insulator.

[0023]

Note that in the semiconductor device of one embodiment of the present invention, the oxide semiconductor may be replaced with another semiconductor.

[0024]

A minute transistor can be provided. Alternatively, a transistor with low parasitic capacitance can be provided. Alternatively, a transistor having high frequency characteristics can be provided. Alternatively, a transistor with favorable electric characteristics can be provided. Alternatively, a transistor with stable electric characteristics can be provided. Alternatively, a transistor with low off-state current can be provided. Alternatively, a novel transistor can be provided. Alternatively, a semiconductor device including the transistor can be provided. Alternatively, a semiconductor device which can operate at high speed can be provided. Alternatively, a novel semiconductor device can be provided. A module including any of the above semiconductor devices can be provided. An electronic device including any

of the above semiconductor devices or the module can be provided.

[0025]

Note that the description of these effects does not disturb the existence of other effects. One embodiment of the present invention does not necessarily achieve all the effects listed above. Other effects will be apparent from and can be derived from the description of the specification, the drawings, the claims, and the like.

BRIEF DESCRIPTION OF DRAWINGS

[0026]

In the accompanying drawings:

FIGS. 1A to 1C are a top view and cross-sectional views of a transistor of one embodiment of the present invention;

FIGS. 2A and 2B are cross-sectional views each illustrating part of a transistor of one embodiment of the present invention;

FIG. 3 is a cross-sectional view illustrating part of a transistor of one embodiment of the present invention;

FIGS. 4A to 4C are a top view and cross-sectional views of a transistor of one embodiment of the present invention;

FIGS. 5A to 5C are a top view and cross-sectional views of a transistor of one embodiment of the present invention;

FIGS. 6A to 6C are a top view and cross-sectional views of a transistor of one embodiment of the present invention;

FIGS. 7A to 7C are a top view and cross-sectional views of a transistor of one embodiment of the present invention;

FIGS. 8A to 8C are a top view and cross-sectional views of a transistor of one embodiment of the present invention;

FIG. 9 is a cross-sectional view of a transistor of one embodiment of the present invention;

FIGS. 10A to 10D are Cs-corrected high-resolution TEM images of a cross section of a CAAC-OS and a cross-sectional schematic view of a CAAC-OS;

FIGS. 11A to 11D are Cs-corrected high-resolution TEM images of a plane of a CAAC-OS;

FIGS. 12A to 12C show structural analysis of a CAAC-OS and a single crystal oxide semiconductor by XRD;

FIGS. 13A and 13B show electron diffraction patterns of a CAAC-OS;

FIG. 14 shows a change in crystal part of an In-Ga-Zn oxide induced by electron irradiation;

FIGS. 15A to 15C are a top view and cross-sectional views illustrating a method for manufacturing a transistor of one embodiment of the present invention;

FIGS. 16A to 16C are a top view and cross-sectional views illustrating a method for manufacturing a transistor of one embodiment of the present invention;

FIGS. 17A to 17C are a top view and cross-sectional views illustrating a method for manufacturing a transistor of one embodiment of the present invention;

FIGS. 18A to 18C are a top view and cross-sectional views illustrating a method for manufacturing a transistor of one embodiment of the present invention;

FIGS. 19A to 19C are a top view and cross-sectional views illustrating a method for manufacturing a transistor of one embodiment of the present invention;

FIGS. 20A to 20C are a top view and cross-sectional views illustrating a method for manufacturing a transistor of one embodiment of the present invention;

FIGS. 21A to 21C are a top view and cross-sectional views illustrating a method for manufacturing a transistor of one embodiment of the present invention;

FIGS. 22A to 22C are a top view and cross-sectional views illustrating a method for manufacturing a transistor of one embodiment of the present invention;

FIGS. 23A to 23C are a top view and cross-sectional views illustrating a method for manufacturing a transistor of one embodiment of the present invention;

FIGS. 24A to 24C are a top view and cross-sectional views illustrating a method for manufacturing a transistor of one embodiment of the present invention;

FIGS. 25A to 25C are a top view and cross-sectional views illustrating a method for manufacturing a transistor of one embodiment of the present invention;

FIGS. 26A to 26C are a top view and cross-sectional views illustrating a method for manufacturing a transistor of one embodiment of the present invention;

FIGS. 27A to 27C are a top view and cross-sectional views illustrating a method for manufacturing a transistor of one embodiment of the present invention;

FIGS. 28A to 28C are a top view and cross-sectional views illustrating a method for manufacturing a transistor of one embodiment of the present invention;

FIGS. 29A to 29C are a top view and cross-sectional views illustrating a method for manufacturing a transistor of one embodiment of the present invention;

FIGS. 30A to 30C are a top view and cross-sectional views illustrating a method for manufacturing a transistor of one embodiment of the present invention;

FIGS. 31A to 31C are a top view and cross-sectional views illustrating a method for

manufacturing a transistor of one embodiment of the present invention;

FIGS. 32A to 32C are a top view and cross-sectional views illustrating a method for manufacturing a transistor of one embodiment of the present invention;

FIGS. 33A to 33C are a top view and cross-sectional views illustrating a method for manufacturing a transistor of one embodiment of the present invention;

FIGS. 34A to 34C are a top view and cross-sectional views illustrating a method for manufacturing a transistor of one embodiment of the present invention;

FIGS. 35A to 35C are a top view and cross-sectional views illustrating a method for manufacturing a transistor of one embodiment of the present invention;

FIGS. 36A to 36C are a top view and cross-sectional views illustrating a method for manufacturing a transistor of one embodiment of the present invention;

FIGS. 37A to 37C are a top view and cross-sectional views illustrating a method for manufacturing a transistor of one embodiment of the present invention;

FIGS. 38A and 38B are each a circuit diagram of a memory device of one embodiment of the present invention;

FIG. 39 is a cross-sectional view of a semiconductor device of one embodiment of the present invention;

FIG. 40 is a cross-sectional view of a semiconductor device of one embodiment of the present invention;

FIGS. 41A to 41F are cross sectional views and circuit diagrams of a semiconductor device of one embodiment of the present invention;

FIG. 42 is a block diagram of a CPU of one embodiment of the present invention;

FIG. 43 is a circuit diagram of a memory element of one embodiment of the present invention;

FIGS. 44A and 44B are plan views of imaging devices;

FIGS. 45A and 45B are plan views of pixels of an imaging device;

FIGS. 46A and 46B are cross-sectional views of an imaging device;

FIGS. 47A and 47B are cross-sectional views of imaging devices;

FIG. 48 illustrates a configuration example of an RF tag;

FIGS. 49A to 49C are a circuit diagram, a top view, and a cross-sectional view of a semiconductor device of one embodiment of the present invention;

FIGS. 50A and 50B are a circuit diagram and a cross-sectional view of a semiconductor device of one embodiment of the present invention;

FIG. 51 illustrates a display module;

FIGS. 52A and 52B are perspective views illustrating a cross-sectional structure of a

package using a lead frame interposer;

FIGS. 53A to 53E each illustrate an electronic device of one embodiment of the present invention;

FIGS. 54A to 54D each illustrate an electronic device of one embodiment of the present invention;

FIGS. 55A to 55C each illustrate an electronic device of one embodiment of the present invention; and

FIGS. 56A to 56F illustrate application examples of an RF tag of one embodiment of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

[0027]

Hereinafter, embodiment of the present invention will be described in detail with the reference to the drawings. However, the present invention is not limited to the description below, and it is easily understood by those skilled in the art that modes and details disclosed herein can be modified in various ways. Further, the present invention is not construed as being limited to description of the embodiments and the examples. In describing structures of the present invention with reference to the drawings, common reference numerals are used for the same portions in different drawings. Note that the same hatched pattern is applied to similar parts, and the similar parts are not especially denoted by reference numerals in some cases.

[0028]

Note that the size, the thickness of films (layers), or regions in drawings is sometimes exaggerated for simplicity.

[0029]

In this specification, for example, when the shape of an object is described with the use of a term such as "diameter", "grain size (diameter)", "dimension", "size", or "width", the term can be regarded as the length of one side of a minimal cube where the object fits, or an equivalent circle diameter of a cross section of the object. The term "equivalent circle diameter of a cross section of the object" refers to the diameter of a perfect circle having the same area as that of the cross section of the object.

[0030]

A voltage usually refers to a potential difference between a given potential and a reference potential (e.g., a ground potential (GND) or a source potential). A voltage can be referred to as a potential and vice versa.

[0031]

Note that the ordinal numbers such as “first” and “second” in this specification are used for convenience and do not denote the order of steps or the stacking order of layers. Therefore, for example, description can be made even when "first" is replaced with "second" or "third", as appropriate. In addition, the ordinal numbers in this specification and the like are not necessarily the same as those which specify one embodiment of the present invention.

[0032]

Note that an impurity in a semiconductor refers to, for example, elements other than the main components of the semiconductor. For example, an element with a concentration of lower than 0.1 atomic% is an impurity. When an impurity is contained, the density of states (DOS) may be formed in a semiconductor, the carrier mobility may be decreased, or the crystallinity may be decreased, for example. In the case where the semiconductor is an oxide semiconductor, examples of an impurity which changes characteristics of the semiconductor include Group 1 elements, Group 2 elements, Group 14 elements, Group 15 elements, and transition metals other than the main components; specifically, there are hydrogen (included in water), lithium, sodium, silicon, boron, phosphorus, carbon, and nitrogen, for example. In the case of an oxide semiconductor, oxygen vacancy may be formed by entry of impurities such as hydrogen. Further, in the case where the semiconductor is a silicon film, examples of an impurity which changes characteristics of the semiconductor include oxygen, Group 1 elements except hydrogen, Group 2 elements, Group 13 elements, and Group 15 elements.

[0033]

Note that the channel length refers to, for example, a distance between a source (source region or source electrode) and a drain (drain region or drain electrode) in a region where a semiconductor (or a portion where a current flows in a semiconductor when a transistor is on) and a gate electrode overlap with each other or a region where a channel is formed in a top view of the transistor. In one transistor, channel lengths in all regions are not necessarily the same. In other words, the channel length of one transistor is not limited to one value in some cases. Therefore, in this specification, the channel length is any one of values, the maximum value, the minimum value, or the average value in a region where a channel is formed.

[0034]

The channel width refers to, for example, the length of a portion where a source and a drain face each other in a region where a semiconductor (or a portion where a current flows in a semiconductor when a transistor is on) and a gate electrode overlap with each other, or a region where a channel is formed. In one transistor, channel widths in all regions are not necessarily the same. In other words, the channel width of one transistor is not limited to one value in some cases. Therefore, in this specification, the channel width is any one of values, the

maximum value, the minimum value, or the average value in a region where a channel is formed.

[0035]

Note that depending on transistor structures, a channel width in a region where a channel is actually formed (hereinafter referred to as an effective channel width) is different from a channel width shown in a top view of a transistor (hereinafter referred to as an apparent channel width) in some cases. For example, in a transistor having a three-dimensional structure, an effective channel width is greater than an apparent channel width shown in a top view of the transistor, and its influence cannot be ignored in some cases. For example, in a miniaturized transistor having a three-dimensional structure, the proportion of a channel formation region formed in a side surface of a semiconductor is increased in some cases. In that case, an effective channel width obtained when a channel is actually formed is greater than an apparent channel width shown in the top view.

[0036]

In a transistor having a three-dimensional structure, an effective channel width is difficult to measure in some cases. For example, estimation of an effective channel width from a design value requires an assumption that the shape of a semiconductor is known. Therefore, in the case where the shape of a semiconductor is not known accurately, it is difficult to measure an effective channel width accurately.

[0037]

Therefore, in this specification, in a top view of a transistor, an apparent channel width that is a length of a portion where a source and a drain face each other in a region where a semiconductor and a gate electrode overlap with each other is referred to as a surrounded channel width (SCW) in some cases. Furthermore, in this specification, in the case where the term "channel width" is simply used, it may denote a surrounded channel width and an apparent channel width. Alternatively, in this specification, in the case where the term "channel width" is simply used, it may denote an effective channel width in some cases. Note that the values of a channel length, a channel width, an effective channel width, an apparent channel width, a surrounded channel width, and the like can be determined by obtaining and analyzing a cross-sectional TEM image and the like.

[0038]

Note that in the case where field-effect mobility, a current value per channel width, and the like of a transistor are obtained by calculation, a surrounded channel width may be used for the calculation. In that case, the values may be different from those calculated using an effective channel width in some cases.

[0039]

Note that in this specification, the description "A has a shape such that an end portion extends beyond an end portion of B" may indicate, for example, the case where at least one of end portions of A is positioned on an outer side of at least one of end portions of B in a top view or a cross-sectional view. Thus, the description "A has a shape such that an end portion extends beyond an end portion of B" can be read as the description "one end portion of A is positioned on an outer side of one end portion of B in a top view," for example.

[0040]

In this specification, the term "parallel" indicates that the angle formed between two straight lines is greater than or equal to −10° and less than or equal to 10°, and accordingly also includes the case where the angle is greater than or equal to −5° and less than or equal to 5°. The term "perpendicular" indicates that the angle formed between two straight lines is greater than or equal to 80° and less than or equal to 100°, and accordingly also includes the case where the angle is greater than or equal to 85° and less than or equal to 95°.

[0041]

In this specification, the trigonal and rhombohedral crystal systems are included in the hexagonal crystal system.

[0042]

(Embodiment 1)

<Transistor Structure 1>

A structure of a transistor included in a semiconductor device of one embodiment of the present invention will be described below.

[0043]

FIGS. 1A to 1C are a top view and cross-sectional views of a semiconductor device of one embodiment of the present invention. FIG. 1A is the top view, and FIGS. 1B and 1C are the cross-sectional views taken along dashed-dotted lines A1-A2 and A3-A4 in FIG. 1A, respectively. Note that for simplification of the drawing, some components are not illustrated in the top view in FIG. 1A. In FIGS. 1B and 1C, paths through which excess oxygen passes are indicated by arrows.

[0044]

In FIGS. 1B and 1C, the transistor includes an insulator 402 over a substrate 400; an insulator 406a over the insulator 402; a semiconductor 406b over the insulator 406a; conductors 416a1 and 416a2 each including a region in contact with a top surface of the semiconductor 406b; an insulator 410 in contact with top surfaces of the conductors 416a1 and 416a2; an insulator 406c in contact with the top surface of the semiconductor 406b; an insulator 412 over the insulator 406c; a conductor 404 over the semiconductor 406b with the insulator 412 and the

insulator 406c positioned therebetween; an insulator 408 over the insulator 410, the conductor 404, the insulator 412, and the conductor 404c; an opening reaching the conductor 404 through the insulator 408; an opening reaching the conductor 416a1 through the insulator 408 and the insulator 410; an opening reaching the conductor 416a2 through the insulator 408 and the insulator 410; a conductor 437, a conductor 431, and a conductor 429 that are embedded in the openings; a conductor 438 over the insulator 408, which includes a region in contact with the conductor 437; a conductor 432 over the insulator 408, which includes a region in contact with the conductor 431; and a conductor 430 over the insulator 408, which includes a region in contact with the conductor 429.

[0045]

Note that the semiconductor 406b includes a region 407 in which the top surface of the semiconductor 406b is in contact with the conductors 416a1 and 416a2.

[0046]

In the transistor, the conductor 404 serves as a gate electrode. Furthermore, the conductor 404 can have a stacked structure including a conductor that hardly allows oxygen to pass therethrough. For example, when the conductor that hardly allows oxygen to pass therethrough is formed as a lower layer, an increase in the electric resistance value due to oxidation of the conductor 404 can be prevented. The insulator 412 serves as a gate insulator.

[0047]

The conductors 416a1 and 416a2 function as a source electrode and a drain electrode of the transistor. The conductors 416a1 and 416a2 each can have a stacked structure including a conductor that hardly allows oxygen to pass therethrough. For example, when the conductor that hardly allows oxygen to pass therethrough is formed as an upper layer, an increase in the electric resistance value due to oxidation of the conductors 416a1 and 416a2 can be prevented. Note that the electric resistance values of the conductors can be measured by a two-terminal method or the like.

[0048]

Therefore, the resistance of the semiconductor 406b can be controlled by a potential applied to the conductor 404. That is, conduction or non-conduction between the conductors 416a1 and 416a2 can be controlled by the potential applied to the conductor 404.

[0049]

As illustrated in FIGS. 1B and 1C, the top surface of the semiconductor 406b is in contact with the conductors 416a1 and 416a2. In addition, the insulator 406a and the semiconductor 406b can be electrically surrounded by an electric field of the conductor 404 serving as the gate electrode. A structure in which a semiconductor is electrically surrounded

by an electric field of a gate electrode is referred to as a surrounded channel (s-channel) structure. Therefore, a channel is formed in the entire semiconductor 406b (bulk) in some cases. In the s-channel structure, a large amount of current can flow between a source and a drain of the transistor, so that an on-state current can be increased. In addition, since the insulator 406a and the semiconductor 406b are surrounded by the electric field of the conductor 404, an off-state current can be decreased.

[0050]

The transistor can also be referred to as a trench-gate self-aligned s-channel FET (TGSA s-channel FET) because the region serving as a gate electrode is formed in a self-aligned manner to fill the opening formed in the insulator 410 and the like.

[0051]

FIGS. 2A and 2B are each an enlarged view of a central portion of the transistor. In FIG. 2A, the length of a region where a bottom surface of the conductor 404 serving as a gate electrode and the top surface of the semiconductor 406b are parallel to each other with the insulator 412 and the insulator 406c positioned therebetween, is referred to as a gate line width 404w. In the opening in the insulator 410, the length of a region which is in contact with the insulator 406c and the top surface of the conductor 416a1 and is parallel to a bottom surface of the conductor 416a1 is a first opening width 416w1. Furthermore, in the opening in the insulator 410, the length of a region which is in contact with the insulator 406c and the top surface of the conductor 416a2 and is parallel to a bottom surface of the conductor 416a2 is a second opening width 416w2. In the transistor of one embodiment of the present invention, the length of the opening reaching the semiconductor 406b is not changed regardless of the first opening width 416w1 and the second opening width 416w2. Furthermore, the gate line width 404w can be smaller than the opening reaching the semiconductor 406b. That is, the gate line width 404w can be smaller than the minimum feature size. Specifically, the gate line width 404w can be greater than or equal to 5 nm and less than or equal to 60 nm, preferably greater than or equal to 5 nm and less than or equal to 30 nm.

[0052]

When an electric field from the gate electrode is blocked by other conductors, switching characteristics of the transistor may be degraded. In the transistor, the positional relationship between the conductor 404 and the conductors 416a1 and 416a2 is changed by the thicknesses of the insulator 406c and the insulator 412. That is, the relationship between the thicknesses of the conductors 416a1 and 416a2 serving as the source electrode and the drain electrode and the thickness of the insulator 412 serving as the gate insulator affects electric characteristics of the transistor.

[0053]

In FIG. 2B, the thickness of the insulator 412 in a region between the conductor 416a1 and the conductor 416a2 is denoted by 412h. The thickness of the conductor 416a1 or the conductor 416a2 is denoted by 416h. It is preferable that the thickness 412h be less than or equal to the thickness 416h because the electric field from the gate electrode is applied to the entire channel formation region, making the operation of the transistor favorable. The thickness 412h is set to less than or equal to 30 nm, preferably less than or equal to 10 nm.

[0054]

The transistor can have a structure in which the thickness416h has a small value. An end portion of the conductor 416a1 has a region facing the conductor 404 with the insulator 406c and the insulator 412 positioned therebetween. An end portion of the conductor 416a2 has a region facing the conductor 404 with the insulator 406c and the insulator 412 positioned therebetween. The vicinities of these regions are denoted by portions surrounded by dotted circles in FIG. 2B; however, the area of these regions can be further reduced. Thus, parasitic capacitance of these regions in the transistor is reduced.

[0055]

Note that the transistor is surrounded by an insulator which has a function of blocking oxygen and impurities such as hydrogen, whereby stable electric characteristics can be obtained. For example, as the insulator 408, an insulator which has a function of blocking oxygen and impurities such as hydrogen may be used.

[0056]

An insulator which has a function of blocking oxygen and impurities such as hydrogen may be formed to have a single-layer structure or a stacked-layer structure including an insulator containing, for example, boron, carbon, nitrogen, oxygen, fluorine, magnesium, aluminum, silicon, phosphorus, chlorine, argon, gallium, germanium, yttrium, zirconium, lanthanum, neodymium, hafnium, or tantalum.

[0057]

Furthermore, for example, the insulator 408 may be formed using aluminum oxide, magnesium oxide, silicon nitride oxide, silicon nitride, gallium oxide, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, or tantalum oxide. Note that the insulator 408 preferably contains aluminum oxide. For example, when the insulator 408 is formed using plasma including oxygen, oxygen can be added to the insulator 410 serving as a base layer of the insulator 408. Alternatively, oxygen can be added to side surfaces of the insulator 412. The added oxygen becomes excess oxygen in the insulator 410 or the insulator 412. When the insulator 408 contains aluminum oxide, entry of impurities such as

hydrogen into the semiconductor 406b can be inhibited. Furthermore, when the insulator 408 contains aluminum oxide, for example, outward diffusion of excess oxygen added to the insulator 410 and the insulator 412 can be reduced.

[0058]

The insulator 402 may be formed to have, for example, a single-layer structure or a stacked-layer structure including an insulator containing boron, carbon, nitrogen, oxygen, fluorine, magnesium, aluminum, silicon, phosphorus, chlorine, argon, gallium, germanium, yttrium, zirconium, lanthanum, neodymium, hafnium, or tantalum. For example, the insulator 402 preferably includes silicon oxide or silicon oxynitride.

[0059]

Note that the insulator 410 preferably includes an insulator with low dielectric constant. For example, the insulator 410 preferably includes silicon oxide, silicon oxynitride, silicon nitride oxide, silicon nitride, silicon oxide to which fluorine is added, silicon oxide to which carbon is added, silicon oxide to which carbon and nitrogen are added, porous silicon oxide, a resin, or the like. Alternatively, the insulator 410 preferably has a stacked structure of a resin and silicon oxide, silicon oxynitride, silicon nitride oxide, silicon nitride, silicon oxide to which fluorine is added, silicon oxide to which carbon is added, silicon oxide to which carbon and nitrogen are added, or porous silicon oxide. When silicon oxide or silicon oxynitride, which is thermally stable, is combined with a resin, the stacked-layer structure can have thermal stability and low dielectric constant. Examples of the resin include polyester, polyolefin, polyamide (e.g., nylon or aramid), polyimide, polycarbonate, and acrylic.

[0060]

The insulator 412 may be formed to have, for example, a single-layer structure or a stacked-layer structure including an insulator containing boron, carbon, nitrogen, oxygen, fluorine, magnesium, aluminum, silicon, phosphorus, chlorine, argon, gallium, germanium, yttrium, zirconium, lanthanum, neodymium, hafnium, or tantalum. For example, the insulator 412 preferably includes silicon oxide or silicon oxynitride.

[0061]

Note that the insulator 412 preferably contains an insulator with a high dielectric constant. For example, the insulator 412 preferably includes gallium oxide, hafnium oxide, oxide including aluminum and hafnium, oxynitride including aluminum and hafnium, oxide including silicon and hafnium, oxynitride including silicon and hafnium, or the like. The insulator 412 preferably has a stacked-layer structure including silicon oxide or silicon oxynitride and an insulator with a high dielectric constant. Because silicon oxide and silicon oxynitride have thermal stability, combination of silicon oxide or silicon oxynitride with an

insulator with a high dielectric constant allows the stacked-layer structure to be thermally stable and have a high dielectric constant. For example, when an aluminum oxide, a gallium oxide, or a hafnium oxide of the insulator 412 is on the insulator 406c side, entry of silicon included in the silicon oxide or the silicon oxynitride into the semiconductor 406b can be suppressed. When silicon oxide or silicon oxynitride is on the insulator 406c side, for example, trap centers might be formed at the interface between aluminum oxide, gallium oxide, or hafnium oxide and silicon oxide or silicon oxynitride. The trap centers can shift the threshold voltage of the transistor in the positive direction by trapping electrons in some cases.

[0062]

Each of the conductors 416a1 and 416a2 may be formed to have a single-layer structure or a stacked-layer structure including a conductor containing, for example, one or more kinds of boron, nitrogen, oxygen, fluorine, silicon, phosphorus, aluminum, titanium, chromium, manganese, cobalt, nickel, copper, zinc, gallium, yttrium, zirconium, molybdenum, ruthenium, platinum, silver, indium, tin, tantalum, and tungsten. Alternatively, a film of an alloy or compound containing the above element may be used: a conductor containing aluminum, a conductor containing copper and titanium, a conductor containing copper and manganese, a conductor containing indium, tin, and oxygen, a conductor containing titanium and nitrogen, or the like may be used. Alternatively, each of the conductors 416a1 and 416a2 is preferably a stacked-layer film of a conductor containing nitrogen and tantalum containing nitrogen that is less likely to transmit oxygen.

[0063]

The conductor 404 may be formed to have, for example, a single-layer structure or a stacked-layer structure including a conductor containing one or more kinds of boron, nitrogen, oxygen, fluorine, silicon, phosphorus, aluminum, titanium, chromium, manganese, cobalt, nickel, copper, zinc, gallium, yttrium, zirconium, molybdenum, ruthenium, silver, indium, tin, tantalum, and tungsten. Alternatively, a film of an alloy or compound containing the above element may be used: a conductor containing aluminum, a conductor containing copper and titanium, a conductor containing copper and manganese, a conductor containing indium, tin, and oxygen, a conductor containing titanium and nitrogen, or the like may be used. Alternatively, each of the conductors 416a1 and 416a2 is preferably a stacked-layer film of a conductor containing nitrogen and tantalum containing nitrogen that is less likely to transmit oxygen.

[0064]

Each of the conductors 429, 430, 431, 432, 437, and 438 may be formed to have a single-layer structure or a stacked-layer structure including a conductor containing, for example, one or more kinds of boron, nitrogen, oxygen, fluorine, silicon, phosphorus, aluminum, titanium,

chromium, manganese, cobalt, nickel, copper, zinc, gallium, yttrium, zirconium, molybdenum, ruthenium, silver, indium, tin, tantalum, and tungsten. Alternatively, a film of an alloy or compound containing the above element may be used: a conductor containing aluminum, a conductor containing copper and titanium, a conductor containing copper and manganese, a conductor containing indium, tin, and oxygen, a conductor containing titanium and nitrogen, or the like may be used. Alternatively, each of the conductors 416a1 and 416a2 is preferably a stacked-layer film of a conductor containing nitrogen and tantalum containing nitrogen that is less likely to transmit oxygen.

[0065]

As the semiconductor 406b, an oxide semiconductor is preferably used. However, silicon (including strained silicon), germanium, silicon germanium, silicon carbide, gallium arsenide, aluminum gallium arsenide, indium phosphide, gallium nitride, an organic semiconductor, or the like can be used in some cases.

[0066]

The insulator 406a and the insulator 406c are desirably oxides including one or more, or two or more elements other than oxygen included in the semiconductor 406b. However, silicon (including strained silicon), germanium, silicon germanium, silicon carbide, gallium arsenide, aluminum gallium arsenide, indium phosphide, gallium nitride, an organic semiconductor, or the like can be used in some cases.

[0067]

<Transistor structure 2>

A transistor having a structure different from that in FIGS. 1A to 1C will be described with reference to FIGS. 4A to 4C. FIGS. 4A to 4C are a top view and cross-sectional views of a semiconductor device of one embodiment of the present invention. FIG. 4A is the top view, and FIGS. 4B and 4C are the cross-sectional views taken along dashed-dotted lines A1-A2 and A3-A4 in FIG. 4A, respectively. Note that for simplification of the drawing, some components are not illustrated in the top view in FIG. 4A.

[0068]

In FIGS. 4B and 4C, the transistor includes an insulator 401 over the substrate 400; a conductor 310 over the insulator 401; an insulator 301 in contact with top surfaces of the insulator 401 and the conductor 310 and side surfaces of the conductor 310; an insulator 303 over the insulator 301; the insulator 402 over the insulator 303; the insulator 406a over the insulator 402; the semiconductor 406b over the insulator 406a; the conductors 416a1 and 416a2 each including the region in contact with the top surface of the semiconductor 406b; the insulator 410 in contact with the top surfaces of the conductors 416a1 and 416a2; the insulator 406c in

contact with the top surface of the semiconductor 406b; the insulator 412 over the insulator 406c; the conductor 404 placed over the semiconductor 406b with the insulator 412 and the insulator 406c positioned therebetween; the insulator 408 over the insulator 410, the conductor 404, the insulator 412, and the insulator 406c; the opening reaching the conductor 404 through the insulator 408; the opening reaching the conductor 416a1 through the insulator 408 and the insulator 410; the opening reaching the conductor 416a2 through the insulator 408 and the insulator 410; the conductor 437, the conductor 431, and the conductor 429 that are embedded in the openings; the conductor 438 over the insulator 408, which includes the region in contact with the conductor 437; the conductor 432 over the insulator 408, which includes the region in contact with the conductor 431; and the conductor 430 over the insulator 408, which includes the region in contact with the conductor 429.

[0069]

Note that the semiconductor 406b includes the region 407 in which the top surface of the semiconductor 406b is in contact with the conductor 416a1 and the conductor 416a2.

[0070]

In the transistor, the conductor 404 serves as a first gate electrode. Furthermore, the conductor 404 can have a stacked structure including a conductor that hardly allows oxygen to pass therethrough. For example, when the conductor that hardly allows oxygen to pass therethrough is formed as a lower layer, an increase in the electric resistance value due to oxidation of the conductor 404 can be prevented. The insulator 412 serves as the gate insulator.

[0071]

The conductors 416a1 and 416a2 function as a source electrode and a drain electrode of the transistor. The conductors 416a1 and 416a2 can each have a stacked structure including a conductor that hardly allows oxygen to pass therethrough. For example, when the conductor that hardly allows oxygen to pass therethrough is formed as an upper layer, an increase in the electric resistance value due to oxidation of the conductors 416a1 and 416a2 can be prevented.

[0072]

Therefore, the resistance of the semiconductor 406b can be controlled by a potential applied to the conductor 404. That is, conduction or non-conduction between the conductors 416a1 and 416a2 can be controlled by the potential applied to the conductor 404.

[0073]

The conductor 310 functions as a second gate electrode. The conductor 310 can be a multilayer film including a conductive film that hardly allows oxygen to pass therethrough. The use of a multilayer film including a conductive film that hardly allows oxygen to pass therethrough can prevent a decrease in conductivity due to oxidation of the conductor 310. The

insulators 301, 303, and 402 serve as a second gate insulator. The threshold voltage of the transistor can be controlled by a potential applied to the conductor 310. Furthermore, by the potential applied to the conductor 310, electrons are injected to the insulator 303 and thus the threshold voltage of the transistor can be controlled. The first gate electrode and the second gate electrode are electrically connected to each other, whereby a high on-state current can be obtained. Note that the functions of the first gate electrode and the second gate electrode may be replaced with each other.

[0074]

FIG. 9 illustrates an example in which the first gate electrode and the second gate electrode are electrically connected. In the opening reaching the conductor 404 through the insulator 408, the conductor 440 is embedded, and a top surface of the conductor 440 is electrically connected to a conductor 444 formed over the insulator 408. In an opening reaching the conductor 310 through the insulator 408, the insulator 410, the insulator 402, the insulator 303, and the insulator 301, the conductor 442 is embedded, and a top surface of the conductor 442 and the conductor 444 are electrically connected. That is, the conductor 404 serving as the first gate electrode is electrically connected to the conductor 310 serving as the second gate electrode through the conductors 440, 444, and 442.

[0075]

For example, the insulator 401 may be formed of aluminum oxide, magnesium oxide, silicon nitride oxide, silicon nitride, gallium oxide, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, or tantalum oxide. Note that the insulator 401 preferably includes aluminum oxide or silicon nitride. The insulator 401 including aluminum oxide or silicon nitride can suppress entry of impurities such as hydrogen into the semiconductor 406b, and can reduce outward diffusion of oxygen, for example

[0076]

The insulator 301 may be formed to have, for example, a single-layer structure or a stacked-layer structure including an insulator containing boron, carbon, nitrogen, oxygen, fluorine, magnesium, aluminum, silicon, phosphorus, chlorine, argon, gallium, germanium, yttrium, zirconium, lanthanum, neodymium, hafnium, or tantalum. For example, the insulator 301 preferably includes silicon oxide or silicon oxynitride.

[0077]

The insulator 303 may serves as an electron injection layer, for example. The insulator 303 may be formed to have, for example, a single-layer structure or a stacked-layer structure including an insulator containing boron, carbon, nitrogen, oxygen, fluorine, magnesium, aluminum, silicon, phosphorus, chlorine, argon, gallium, germanium, yttrium, zirconium,

lanthanum, neodymium, hafnium, or tantalum. For example, the insulator 303 preferably includes silicon nitride, hafnium oxide, or aluminum oxide.

[0078]

Each of the conductors 310, 440, 442, and 444 may be formed to have a single-layer structure or a stacked-layer structure including a conductor containing, for example, one or more kinds of boron, nitrogen, oxygen, fluorine, silicon, phosphorus, aluminum, titanium, chromium, manganese, cobalt, nickel, copper, zinc, gallium, yttrium, zirconium, molybdenum, ruthenium, silver, indium, tin, tantalum, and tungsten. Alternatively, a film of an alloy or compound containing the above element may be used: a conductor containing aluminum, a conductor containing copper and titanium, a conductor containing copper and manganese, a conductor containing indium, tin, and oxygen, a conductor containing titanium and nitrogen, or the like may be used.

[0079]

This transistor is different from the transistor in FIGS. 1A to 1C in that the conductor 310 serving as the second gate electrode is included. For the same components as those in FIGS. 1A to 1C, refer to the above description.

[0080]

<Transistor structure 3>

A transistor having a structure different from that in FIGS. 1A to 1C will be described with reference to FIGS. 5A to 5C. FIGS. 5A to 5C are a top view and cross-sectional views of a semiconductor device of one embodiment of the present invention. FIG. 5A is the top view and FIGS. 5B and 5C are the cross-sectional views taken along dashed-dotted lines A1-A2 and A3-A4 in FIG. 5A, respectively. Note that for simplification of the drawing, some components in the top view in FIG. 5A are not illustrated.

[0081]

This transistor is different from the transistor in FIGS. 1A to 1C in the shapes of the conductors 416a1 and 416a2. Details thereof are described below with reference to FIG. 3.

[0082]

FIG. 3 is an enlarged view of a central portion of the transistor in FIGS. 5A to 5C. In the case where an angle formed by a plane which is parallel to the substrate and a side surface of the conductor 416a1 where the conductor 416a1 is in contact with the insulator 406c is a taper angle 446, the taper angle 446 is less than or equal to 90°. An angle formed by a plane which is parallel to the substrate and a side surface of the conductor 416a2 where the conductor 416a2 is in contact with the insulator 406c is a taper angle 447, the taper angle 447 is less than or equal to 90°. The taper angles 446 and 447 is less than or equal to 90°; coverage by the insulator 406c

formed on the side surfaces of the conductors 416a1 and 416a2 and the insulator 412 serving as the gate insulator is improved. When the coverage by the insulator 406c and the insulator 412 is improved, leakage current flowing through the conductor 404 serving as a gate electrode and the conductor 416a1 or 416a2 serving as a source electrode or a drain electrode can be kept low. Alternatively, leakage current flowing through the conductor 404 serving as a gate electrode and the semiconductor 406b having a channel formation region can be kept low. The taper angles 446 and 447 are each greater than or equal to 10° and less than 90°, preferably, greater than or equal to 30° and less than or equal to 80°.

[0083]

The length of the opening reaching the semiconductor 406b is not changed regardless of the first opening width 416w1 and the second opening width 416w2. Furthermore, the gate line width 404w can be smaller than the opening reaching the semiconductor 406b. That is, the gate line width 404w can be smaller than the minimum feature size. Specifically, the gate line width 404w can be greater than or equal to 5 nm and less than or equal to 60 nm, preferably greater than or equal to 5 nm and less than or equal to 30 nm. For the other components, the description of the transistor in FIGS. 1A to 1C is referred to.

[0084]

<Transistor structure 4>

A transistor having a structure different from that in FIGS. 1A to 1C will be described here with reference to FIGS. 6A to 6C. FIGS. 6A to 6C are a top view and cross-sectional views of a semiconductor device of one embodiment of the present invention. FIG. 6A is the top view, and FIGS. 6B and 6C are the cross-sectional views taken along dashed-dotted lines A1-A2 and A3-A4 in FIG. 6A, respectively. Note that for simplification of the drawing, some components are not illustrated in the top view in FIG. 6A.

[0085]

The transistor in FIGS. 6A to 6C has a structure in which the conductor 310 having a function of the second gate electrode is added to the transistor in FIGS. 5A to 5C. For the same components, refer to the above description.

[0086]

<Transistor structure 5>

A transistor having a structure different from that in FIGS. 4A to 4C will be described with reference to FIGS. 7A to 7C. FIGS. 7A to 7C are a top view and cross-sectional views of a semiconductor device of one embodiment of the present invention. FIG. 7A is the top view and FIGS. 7B and 7C are the cross-sectional views taken along dashed-dotted lines A1-A2 and A3-A4 in FIG. 7A, respectively. Note that for simplification of the drawing, some components

are not illustrated in the top view in FIG. 7A.

[0087]

This transistor is different from the transistor in FIGS. 4A to 4C in that the transistor has a plurality of channel formation regions. Although the transistor has three channel formation regions as an example in FIGS. 7A to 7C, the number of channel formation regions is not limited to this. For the other components, the description of the transistor in FIGS. 4A to 4C is referred to.

[0088]

<Transistor structure 6>

A transistor having a structure different from that in FIGS. 4A to 4C will be described with reference to FIGS. 8A to 8C. FIGS. 8A to 8C are a top view and cross-sectional views of a semiconductor device of one embodiment of the present invention. FIG. 8A is the top view, and FIGS. 8B and 8C are the cross-sectional views taken along dashed-dotted lines A1-A2 and A3-A4 in FIG. 8A, respectively. Note that for simplification of the drawing, some components are not illustrated in the top view in FIG. 8A.

[0089]

This transistor has a channel that is larger than the gate line width 404w in FIG. 2A. For the other components, the description of the transistor in FIGS. 4A to 4C is referred to.

[0090]

At least part of this embodiment can be implemented in combination with any of the embodiments described in this specification as appropriate.

[0091]

(Embodiment 2)

<Structure of oxide semiconductor>

A structure of an oxide semiconductor is described below.

[0092]

An oxide semiconductor is classified into a single crystal oxide semiconductor and a non-single-crystal oxide semiconductor. Examples of a non-single-crystal oxide semiconductor include a c-axis aligned crystalline oxide semiconductor (CAAC-OS), a polycrystalline oxide semiconductor, a nanocrystalline oxide semiconductor (nc-OS), an amorphous-like oxide semiconductor (a-like OS), and an amorphous oxide semiconductor.

[0093]

From another perspective, an oxide semiconductor is classified into an amorphous oxide semiconductor and a crystalline oxide semiconductor. Examples of a crystalline oxide semiconductor include a single crystal oxide semiconductor, a CAAC-OS, a polycrystalline

oxide semiconductor, and an nc-OS.

[0094]

It is known that an amorphous structure is generally defined as being metastable and unfixed, and being isotropic and having no non-uniform structure. In other words, an amorphous structure has a flexible bond angle and a short-range order but does not have a long-range order.

[0095]

This means that an inherently stable oxide semiconductor cannot be regarded as a completely amorphous oxide semiconductor. Moreover, an oxide semiconductor that is not isotropic (e.g., an oxide semiconductor that has a periodic structure in a microscopic region) cannot be regarded as a completely amorphous oxide semiconductor. Note that an a-like OS has a periodic structure in a microscopic region, but at the same time has a void and has an unstable structure. For this reason, an a-like OS has physical properties similar to those of an amorphous oxide semiconductor.

[0096]

<CAAC-OS>

First, a CAAC-OS is described.

[0097]

A CAAC-OS is one of oxide semiconductors having a plurality of c-axis aligned crystal parts (also referred to as pellets).

[0098]

In a combined analysis image (also referred to as a high-resolution TEM image) of a bright-field image and a diffraction pattern of a CAAC-OS, which is obtained using a transmission electron microscope (TEM), a plurality of pellets can be observed. However, in the high-resolution TEM image, a boundary between pellets, that is, a grain boundary is not clearly observed. Thus, in the CAAC-OS, a reduction in electron mobility due to the grain boundary is less likely to occur.

[0099]

A CAAC-OS observed with TEM is described below. FIG. 10A shows a high-resolution TEM image of a cross section of the CAAC-OS that is observed from a direction substantially parallel to the sample surface. The high-resolution TEM image is obtained with a spherical aberration corrector function. The high-resolution TEM image obtained with a spherical aberration corrector function is particularly referred to as a Cs-corrected high-resolution TEM image. The Cs-corrected high-resolution TEM image can be obtained with, for example, an atomic resolution analytical electron microscope JEM-ARM200F

manufactured by JEOL Ltd.

[0100]

FIG. 10B is an enlarged Cs-corrected high-resolution TEM image of a region (1) in FIG. 10A. FIG. 18B shows that metal atoms are arranged in a layered manner in a pellet. Each metal atom layer has a configuration reflecting unevenness of a surface over which the CAAC-OS is formed (hereinafter, the surface is referred to as a formation surface) or a top surface of the CAAC-OS, and is arranged parallel to the formation surface or the top surface of the CAAC-OS.

[0101]

As shown in FIG. 10B, the CAAC-OS has a characteristic atomic arrangement. The characteristic atomic arrangement is denoted by an auxiliary line in FIG. 10C. The size of a pellet is greater than or equal to 1 nm or greater than or equal to 3 nm, and the size of a space caused by tilt of the pellets is approximately 0.8 nm. Therefore, the pellet can also be referred to as a nanocrystal (nc). Furthermore, the CAAC-OS can also be referred to as an oxide semiconductor including c-axis aligned nanocrystals (CANC).

[0102]

Here, according to the Cs-corrected high-resolution TEM images, the schematic arrangement of pellets 5100 of a CAAC-OS over a substrate 5120 is illustrated by such a structure in which bricks or blocks are stacked (see FIG. 10D). The part in which the pellets are tilted as observed in FIG. 10C corresponds to a region 5161 shown in FIG. 10D.

[0103]

FIG. 11A shows a Cs-corrected high-resolution TEM image of a plane of the CAAC-OS observed from a direction substantially perpendicular to the sample surface. FIGS. 11B, 11C, and 11D are enlarged Cs-corrected high-resolution TEM images of regions (1), (2), and (3) in FIG. 11A, respectively. FIGS. 11B, 11C, and 11D indicate that metal atoms are arranged in a triangular, quadrangular, or hexagonal configuration in a pellet. However, there is no regularity of arrangement of metal atoms between different pellets.

[0104]

Next, a CAAC-OS analyzed by X-ray diffraction (XRD) is described. For example, when the structure of a CAAC-OS including an $InGaZnO_4$ crystal is analyzed by an out-of-plane method, a peak appears at a diffraction angle (2θ) of around 31° as shown in FIG. 12A. This peak is derived from the (009) plane of the $InGaZnO_4$ crystal, which indicates that crystals in the CAAC-OS have c-axis alignment, and that the c-axes are aligned in a direction substantially perpendicular to the formation surface or the top surface of the CAAC-OS.

[0105]

Note that in structural analysis of the CAAC-OS by an out-of-plane method, another peak may appear when 2θ is around 36°, in addition to the peak at 2θ of around 31°. The peak at 2θ of around 36° indicates that a crystal having no c-axis alignment is included in part of the CAAC-OS. It is preferable that in the CAAC-OS analyzed by an out-of-plane method, a peak appear when 2θ is around 31° and that a peak not appear when 2θ is around 36°.

[0106]

On the other hand, in structural analysis of the CAAC-OS by an in-plane method in which an X-ray beam is incident on a sample in a direction substantially perpendicular to the c-axis, a peak appears when 2θ is around 56°. This peak is attributed to the (110) plane of the $InGaZnO_4$ crystal. In the case of the CAAC-OS, when analysis (ϕ scan) is performed with 2θ fixed at around 56° and with the sample rotated using a normal vector of the sample surface as an axis (ϕ axis), as shown in FIG. 12B, a peak is not clearly observed. In contrast, in the case of a single crystal oxide semiconductor of $InGaZnO_4$, when ϕ scan is performed with 2θ fixed at around 56°, as shown in FIG. 12C, six peaks that are derived from crystal planes equivalent to the (110) plane are observed. Accordingly, the structural analysis using XRD shows that the directions of a-axes and b-axes are irregularly oriented in the CAAC-OS.

[0107]

Next, a CAAC-OS analyzed by electron diffraction is described. For example, when an electron beam with a probe diameter of 300 nm is incident on a CAAC-OS including an $InGaZnO_4$ crystal in a direction parallel to the sample surface, a diffraction pattern (also referred to as a selected-area transmission electron diffraction pattern) shown in FIG. 13A can be obtained. In this diffraction pattern, spots derived from the (009) plane of an $InGaZnO_4$ crystal are included. Thus, the electron diffraction also indicates that pellets included in the CAAC-OS have c-axis alignment and that the c-axes are aligned in a direction substantially perpendicular to the formation surface or the top surface of the CAAC-OS. Meanwhile, FIG. 13B shows a diffraction pattern obtained in such a manner that an electron beam with a probe diameter of 300 nm is incident on the same sample in a direction perpendicular to the sample surface. As shown in FIG. 13B, a ring-like diffraction pattern is observed. Thus, the electron diffraction also indicates that the a-axes and b-axes of the pellets included in the CAAC-OS do not have regular alignment. The first ring in FIG. 13B is considered to be derived from the (010) plane, the (100) plane, and the like of the $InGaZnO_4$ crystal. The second ring in FIG. 13B is considered to be derived from the (110) plane and the like.

[0108]

As described above, the CAAC-OS is an oxide semiconductor with high crystallinity.

Entry of impurities, formation of defects, or the like might decrease the crystallinity of an oxide semiconductor. This means that the CAAC-OS has small amounts of impurities and defects (e.g., oxygen vacancies).

[0109]

Note that the impurity means an element other than the main components of the oxide semiconductor, such as hydrogen, carbon, silicon, or a transition metal element. For example, an element (specifically, silicon or the like) having higher strength of bonding to oxygen than a metal element included in an oxide semiconductor extracts oxygen from the oxide semiconductor, which results in disorder of the atomic arrangement and reduced crystallinity of the oxide semiconductor. A heavy metal such as iron or nickel, argon, carbon dioxide, or the like has a large atomic radius (or molecular radius), and thus disturbs the atomic arrangement of the oxide semiconductor and decreases crystallinity.

[0110]

The characteristics of an oxide semiconductor having impurities or defects might be changed by light, heat, or the like. Impurities contained in the oxide semiconductor might serve as carrier traps or carrier generation sources, for example. Furthermore, oxygen vacancies in the oxide semiconductor serve as carrier traps or serve as carrier generation sources when hydrogen is captured therein.

[0111]

The CAAC-OS having small amounts of impurities and oxygen vacancies is an oxide semiconductor with low carrier density (specifically, lower than $8 \times 10^{11}/cm^3$, preferably lower than $1 \times 10^{11}/cm^3$, further preferably lower than $1 \times 10^{10}/cm^3$, and is higher than or equal to $1 \times 10^{-9}/cm^3$). Such an oxide semiconductor is referred to as a highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor. A CAAC-OS has a low impurity concentration and a low density of defect states. Thus, the CAAC-OS can be referred to as an oxide semiconductor having stable characteristics.

[0112]

<nc-OS>

Next, an nc-OS is described.

[0113]

An nc-OS has a region in which a crystal part is observed and a region in which it is difficult to observe a crystal part clearly in a high-resolution TEM image. In most cases, the size of a crystal part included in the nc-OS is greater than or equal to 1 nm and less than or equal to 10 nm, or greater than or equal to 1 nm and less than or equal to 3 nm. Note that an oxide semiconductor including a crystal part whose size is greater than 10 nm and less than or equal to

100 nm is sometimes referred to as a microcrystalline oxide semiconductor. In a high-resolution TEM image of the nc-OS, for example, it is difficult to observe a crystal grain boundary clearly in some cases. Note that there is a possibility that the origin of the nanocrystal is the same as that of a pellet in a CAAC-OS. Therefore, a crystal part of the nc-OS may be referred to as a pellet in the following description.

[0114]

In the nc-OS, a microscopic region (for example, a region with a size greater than or equal to 1 nm and less than or equal to 10 nm, in particular, a region with a size greater than or equal to 1 nm and less than or equal to 3 nm) has a periodic atomic arrangement. There is no regularity of crystal orientation between different pellets in the nc-OS. Thus, the orientation of the whole film is not ordered. Accordingly, the nc-OS cannot be distinguished from an a-like OS or an amorphous oxide semiconductor, depending on an analysis method. For example, when the nc-OS is analyzed by an out-of-plane method using an X-ray beam having a diameter larger than the size of a pellet, a peak that shows a crystal plane does not appear. Furthermore, a diffraction pattern like a halo pattern is observed when the nc-OS is subjected to electron diffraction using an electron beam with a probe diameter (e.g., 50 nm or larger) that is larger than the size of a pellet. Meanwhile, spots appear in a nanobeam electron diffraction pattern of the nc-OS when an electron beam having a probe diameter close to or smaller than the size of a pellet is applied. Moreover, in a nanobeam electron diffraction pattern of the nc-OS, regions with high luminance in a circular (ring) pattern are shown in some cases. Also in a nanobeam electron diffraction pattern of the nc-OS, a plurality of spots are shown in a ring-like region in some cases.

[0115]

Since there is no regularity of crystal orientation between the pellets (nanocrystals) as mentioned above, the nc-OS can also be referred to as an oxide semiconductor including random aligned nanocrystals (RANC) or an oxide semiconductor including non-aligned nanocrystals (NANC).

[0116]

The nc-OS is an oxide semiconductor that has high regularity as compared with an amorphous oxide semiconductor. Therefore, the nc-OS is likely to have a lower density of defect states than an a-like OS and an amorphous oxide semiconductor. Note that there is no regularity of crystal orientation between different pellets in the nc-OS. Therefore, the nc-OS has a higher density of defect states than the CAAC-OS.

[0117]

<a-like OS>

An a-like OS has a structure between those of the nc-OS and the amorphous oxide semiconductor.

[0118]

In a high-resolution TEM image of the a-like OS, a void may be observed. Furthermore, in the high-resolution TEM image, there are a region where a crystal part is clearly observed and a region in which a crystal part is not observed.

[0119]

The a-like OS has an unstable structure because it includes a void. To verify that an a-like OS has an unstable structure as compared with a CAAC-OS and an nc-OS, a change in structure caused by electron irradiation is described below.

[0120]

An a-like OS (referred to as Sample A), an nc-OS (referred to as Sample B), and a CAAC-OS (referred to as Sample C) are prepared as samples subjected to electron irradiation. Each of the samples is an In-Ga-Zn oxide.

[0121]

First, a high-resolution cross-sectional TEM image of each sample is obtained. The high-resolution cross-sectional TEM images show that all the samples have crystal parts.

[0122]

Note that which part is regarded as a crystal part is determined as follows. It is known that a unit cell of an $InGaZnO_4$ crystal has a structure in which nine layers including three In-O layers and six Ga-Zn-O layers are stacked in the c-axis direction. The distance between the adjacent layers is equivalent to the lattice spacing on the (009) plane (also referred to as d value). The value is calculated to be 0.29 nm from crystal structural analysis. Accordingly, a portion where the lattice spacing between lattice fringes is greater than or equal to 0.28 nm and less than or equal to 0.30 nm is regarded as a crystal part of $InGaZnO_4$. Each of lattice fringes corresponds to the a-b plane of the $InGaZnO_4$ crystal.

[0123]

FIG. 14 shows change in the average size of crystal parts (at 22 points to 45 points) in each sample. Note that the crystal part size corresponds to the length of a lattice fringe. FIG. 14 indicates that the crystal part size in the a-like OS increases with an increase in the cumulative electron dose. Specifically, as shown by (1) in FIG. 14, a crystal part of approximately 1.2 nm (also referred to as an initial nucleus) at the start of TEM observation grows to a size of approximately 2.6 nm at a cumulative electron dose of 4.2×10^8 e^-/nm^2. In contrast, the crystal part size in the nc-OS and the CAAC-OS shows little change from the start of electron irradiation to a cumulative electron dose of 4.2×10^8 e^-/nm^2. Specifically, as shown by (2) and

(3) in FIG. 14, the average crystal sizes in an nc-OS and a CAAC-OS are approximately 1.4 nm and approximately 2.1 nm, respectively, regardless of the cumulative electron dose.

[0124]

In this manner, growth of the crystal part in the a-like OS is induced by electron irradiation. In contrast, in the nc-OS and the CAAC-OS, growth of the crystal part is hardly induced by electron irradiation. Therefore, the a-like OS has an unstable structure as compared with the nc-OS and the CAAC-OS.

[0125]

The a-like OS has a lower density than the nc-OS and the CAAC-OS because it includes a void. Specifically, the density of the a-like OS is higher than or equal to 78.6 % and lower than 92.3 % of the density of the single crystal oxide semiconductor having the same composition. The density of each of the nc-OS and the CAAC-OS is higher than or equal to 92.3 % and lower than 100 % of the density of the single crystal oxide semiconductor having the same composition. Note that it is difficult to deposit an oxide semiconductor having a density of lower than 78 % of the density of the single crystal oxide semiconductor.

[0126]

For example, in the case of an oxide semiconductor having an atomic ratio of In:Ga:Zn = 1:1:1, the density of single crystal $InGaZnO_4$ with a rhombohedral crystal structure is 6.357 g/cm^3. Accordingly, in the case of the oxide semiconductor having an atomic ratio of In:Ga:Zn = 1:1:1, the density of the a-like OS is higher than or equal to 5.0 g/cm^3 and lower than 5.9 g/cm^3. For example, in the case of the oxide semiconductor having an atomic ratio of In:Ga:Zn = 1:1:1, the density of each of the nc-OS and the CAAC-OS is higher than or equal to 5.9 g/cm^3 and lower than 6.3 g/cm^3.

[0127]

Note that there is a possibility that an oxide semiconductor having a certain composition cannot exist in a single crystal structure. In that case, single crystal oxide semiconductors with different compositions are combined at an adequate ratio, which makes it possible to calculate density equivalent to that of a single crystal oxide semiconductor with the desired composition. The density of a single crystal oxide semiconductor having the desired composition can be calculated using a weighted average according to the combination ratio of the single crystal oxide semiconductors with different compositions. Note that it is preferable to use as few kinds of single crystal oxide semiconductors as possible to calculate the density.

[0128]

As described above, oxide semiconductors have various structures and various properties. Note that an oxide semiconductor may be a multilayer film including two or more

of an amorphous oxide semiconductor, an a-like OS, an nc-OS, and a CAAC-OS, for example.

[0129]

An oxide which can be used as the insulator 406a, the semiconductor 406b, the insulator 406c, or the like is described.

[0130]

The semiconductor 406b is an oxide semiconductor containing indium, for example. The oxide semiconductor 406b can have high carrier mobility (electron mobility) by containing indium, for example. The semiconductor 406b preferably contains an element *M*. The element *M* is preferably aluminum, gallium, yttrium, tin, or the like. Other elements which can be used as the element *M* are boron, silicon, titanium, iron, nickel, germanium, zirconium, molybdenum, lanthanum, cerium, neodymium, hafnium, tantalum, tungsten, and the like. Note that two or more of the above elements may be used in combination as the element *M*. The element *M* is an element having high bonding energy with oxygen, for example. The element *M* is an element whose bonding energy with oxygen is higher than that of indium. The element *M* is an element that can increase the energy gap of the oxide semiconductor, for example. Furthermore, the semiconductor 406b preferably contains zinc. When the oxide semiconductor contains zinc, the oxide semiconductor is easily crystallized, in some cases.

[0131]

Note that the semiconductor 406b is not limited to the oxide semiconductor containing indium. The semiconductor 406b may be, for example, an oxide semiconductor which does not contain indium and contains zinc, an oxide semiconductor which does not contain indium and contains gallium, or an oxide semiconductor which does not contain indium and contains tin, e.g., a zinc tin oxide, a gallium tin oxide, or a gallium oxide.

[0132]

For the semiconductor 406b, an oxide with a wide energy gap may be used, for example. For example, the energy gap of the semiconductor 406b is greater than or equal to 2.5 eV and less than or equal to 4.2 eV, preferably greater than or equal to 2.8 eV and less than or equal to 3.8 eV, and further preferably greater than or equal to 3 eV and less than or equal to 3.5 eV.

[0133]

For example, the insulator 406a and the insulator 406c are oxides including one or more, or two or more elements other than oxygen included in the semiconductor 406b. Since the insulator 406a and the insulator 406c each include one or more, or two or more elements other than oxygen included in the semiconductor 406b, an interface state is less likely to be formed at the interface between the insulator 406a and the semiconductor 406b and the interface between the semiconductor 406b and the insulator 406c.

[0134]

The case where the insulator 406a, the semiconductor 406b, and the insulator 406c contain indium is described. In the case of using an In-*M*-Zn oxide as the insulator 406a, when a summation of In and *M* is assumed to be 100 atomic%, the proportions of In and *M* are preferably set to be less than 50 atomic% and greater than 50 atomic%, respectively, further preferably less than 25 atomic% and greater than 75 atomic%, respectively. In the case of using an In-*M*-Zn oxide as the semiconductor 406b, when the summation of In and *M* is assumed to be 100 atomic%, the proportions of In and *M* are preferably set to be greater than 25 atomic% and less than 75 atomic%, respectively, further preferably greater than 34 atomic% and less than 66 atomic%, respectively. In the case of using an In-*M*-Zn oxide as the insulator 406c, when the summation of In and *M* is assumed to be 100 atomic%, the proportions of In and *M* are preferably set to be less than 50 atomic% and greater than 50 atomic%, respectively, further preferably less than 25 atomic% and greater than 75 atomic%, respectively. Note that the insulator 406c may be an oxide that is a type the same as that of the insulator 406a.

[0135]

As the semiconductor 406b, an oxide having an electron affinity higher than those of the insulators 406a and 406c is used. For example, as the semiconductor 406b, an oxide having an electron affinity higher than those of the insulators 406a and 406c by 0.07 eV or higher and 1.3 eV or lower, preferably 0.1 eV or higher and 0.7 eV or lower, further preferably 0.15 eV or higher and 0.4 eV or lower is used. Note that the electron affinity refers to an energy gap between the vacuum level and the bottom of the conduction band.

[0136]

An indium gallium oxide has a small electron affinity and a high oxygen-blocking property. Therefore, the insulator 406c preferably includes an indium gallium oxide. The gallium atomic ratio [Ga/(In+Ga)] is, for example, higher than or equal to 70 %, preferably higher than or equal to 80 %, further preferably higher than or equal to 90 %.

[0137]

Note that the insulator 406a and/or the insulator 406c may be gallium oxide. For example, when gallium oxide is used as the insulator 406c, leakage current between the conductor 404 and the conductor 416a1 or the conductor 416a2 can be reduced. In other words, the off-state current of the transistor can be reduced.

[0138]

At this time, when a gate voltage is applied, a channel is formed in the semiconductor 406b having the highest electron affinity in the insulator 406a, the semiconductor 406b, and the

insulator 406c.

[0139]

Here, in some cases, there is a mixed region of the insulator 406a and the semiconductor 406b between the insulator 406a and the semiconductor 406b. Furthermore, in some cases, there is a mixed region of the semiconductor 406b and the insulator 406c between the semiconductor 406b and the insulator 406c. The mixed region has a low density of interface states. For that reason, the stack of the insulator 406a, the semiconductor 406b, and the insulator 406c has a band structure where energy at each interface and in the vicinity of the interface is changed continuously (continuous junction).

[0140]

At this time, electrons move mainly in the semiconductor 406b, not in the insulator 406a and the insulator 406c. Thus, when the interface state density at the interface between the insulator 406a and the semiconductor 406b and the interface state density at the interface between the semiconductor 406b and the insulator 406c are decreased, electron movement in the semiconductor 406b is less likely to be inhibited and the on-sate current of the transistor can be increased.

[0141]

In the case where the transistor has an s-channel structure, a channel is formed in the whole of the semiconductor 406b. Therefore, as the semiconductor 406b has a larger thickness, a channel region becomes larger. In other words, the thicker the semiconductor 406b is, the larger the on-state current of the transistor is. For example, the semiconductor 406b has a region with a thickness of greater than or equal to 20 nm, preferably greater than or equal to 40 nm, more preferably greater than or equal to 60 nm, still more preferably greater than or equal to 100 nm. Note that the semiconductor 406b has a region with a thickness of, for example, less than or equal to 300 nm, preferably less than or equal to 200 nm, or more preferably less than or equal to 150 nm because the productivity of the semiconductor device including the transistor might be decreased.

[0142]

Moreover, the thickness of the insulator 406c is preferably as small as possible to increase the on-state current of the transistor. The thickness of the insulator 406c is less than 10 nm, preferably less than or equal to 5 nm, more preferably less than or equal to 3 nm, for example. Meanwhile, the insulator 406c has a function of blocking entry of elements other than oxygen (such as hydrogen and silicon) included in the adjacent insulator into the semiconductor 406b where a channel is formed. For this reason, it is preferable that the insulator 406c have a certain thickness. The thickness of the insulator 406c is greater than or equal to 0.3 nm,

preferably greater than or equal to 1 nm, further preferably greater than or equal to 2 nm, for example. The insulator 406c preferably has an oxygen blocking property to suppress outward diffusion of oxygen released from the insulator 402 and the like.

[0143]

To improve reliability, preferably, the thickness of the insulator 406a is large and the thickness of the insulator 406c is small. For example, the insulator 406a has a region with a thickness, for example, greater than or equal to 10 nm, preferably greater than or equal to 20 nm, further preferably greater than or equal to 40 nm, still further preferably greater than or equal to 60 nm. When the thickness of the insulator 406a is made large, a distance from an interface between the adjacent insulator and the insulator 406a to the semiconductor 406b in which a channel is formed can be large. Since the productivity of the semiconductor device including the transistor might be decreased, the insulator 406a has a region with a thickness, for example, less than or equal to 200 nm, preferably less than or equal to 120 nm, further preferably less than or equal to 80 nm.

[0144]

For example, silicon in the oxide semiconductor might serve as a carrier trap or a carrier generation source. Therefore, the silicon concentration of the semiconductor 406b is preferably as low as possible. For example, a region in which the concentration of silicon which is measured by secondary ion mass spectrometry (SIMS) is lower than 1×10^{19} atoms/cm^3, preferably lower than 5×10^{18} atoms/cm^3, or further preferably lower than 2×10^{18} atoms/cm^3 is provided between the semiconductor 406b and the insulator 406a. A region with a silicon concentration lower than 1×10^{19} atoms/cm^3, preferably lower than 5×10^{18} atoms/cm^3, further preferably lower than 2×10^{18} atoms/cm^3 which is measured by SIMS is provided between the semiconductor 406b and the insulator 406c.

[0145]

It is preferable to reduce the concentration of hydrogen in the insulator 406a and the insulator 406c in order to reduce the concentration of hydrogen in the semiconductor 406b. The insulator 406a and the insulator 406c each have a region in which the concentration of hydrogen measured by SIMS is lower than or equal to 2×10^{20} atoms/cm^3, preferably lower than or equal to 5×10^{19} atoms/cm^3, further preferably lower than or equal to 1×10^{19} atoms/cm^3, still further preferably lower than or equal to 5×10^{18} atoms/cm^3. It is preferable to reduce the concentration of nitrogen in the insulator 406a and the insulator 406c in order to reduce the concentration of nitrogen in the semiconductor 406b. The insulator 406a and the insulator 406c each have a region in which the concentration of nitrogen measured by SIMS is lower than $5 \times$

10^{19} atoms/cm^3, preferably lower than or equal to 5×10^{18} atoms/cm^3, further preferably lower than or equal to 1×10^{18} atoms/cm^3, still further preferably lower than or equal to 5×10^{17} atoms/cm^3.

[0146]

Note that when copper enters the oxide semiconductor, an electron trap might be generated. The electron trap might shift the threshold voltage of the transistor in the positive direction. Therefore, the concentration of copper on the surface of or in the semiconductor 406b is preferably as low as possible. For example, the semiconductor 406b preferably has a region in which the copper concentration is lower than or equal to 1×10^{19} atoms/cm^3, lower than or equal to 5×10^{18} atoms/cm^3, or lower than or equal to 1×10^{18} atoms/cm^3.

[0147]

The above three-layer structure is an example. For example, a two-layer structure without the insulator 406a or the insulator 406c may be employed. Alternatively, a four-layer structure in which any one of the insulators or the semiconductors described as examples of the insulator 406a, the semiconductor 406b, and the insulator 406c is provided below or over the insulator 406a or below or over the insulator 406c may be employed. Alternatively, an *n*-layer structure (*n* is an integer of 5 or more) in which any one of the insulators or the semiconductors described as examples of the insulator 406a, the semiconductor 406b, and the insulator 406c is provided at two or more of the following positions: over the insulator 406a, below the insulator 406a, over the insulator 406c, and below the insulator 406c.

[0148]

As the substrate 400, an insulator substrate, a semiconductor substrate, or a conductor substrate may be used, for example. As the insulator substrate, a glass substrate, a quartz substrate, a sapphire substrate, a stabilized zirconia substrate (e.g., an yttria-stabilized zirconia substrate), or a resin substrate is used, for example. As the semiconductor substrate, a single material semiconductor substrate of silicon, germanium, or the like or a compound semiconductor substrate containing silicon carbide, silicon germanium, gallium arsenide, indium phosphide, zinc oxide, or gallium oxide as a material is used, for example. A semiconductor substrate in which an insulator region is provided in the above semiconductor substrate, e.g., a silicon on insulator (SOI) substrate or the like is used. As the conductor substrate, a graphite substrate, a metal substrate, an alloy substrate, a conductive resin substrate, or the like is used. A substrate including a metal nitride, a substrate including a metal oxide, or the like is used. An insulator substrate provided with a conductor or a semiconductor, a semiconductor substrate provided with a conductor or an insulator, a conductor substrate provided with a semiconductor or an insulator, or the like is used. Alternatively, any of these substrates over which an element

is provided may be used. As the element provided over the substrate, a capacitor, a resistor, a switching element, a light-emitting element, a memory element, or the like is used.

[0149]

Alternatively, a flexible substrate may be used as the substrate 400. As a method for providing the transistor over a flexible substrate, there is a method in which the transistor is formed over a non-flexible substrate and then the transistor is separated and transferred to the substrate 400 which is a flexible substrate. In that case, a separation layer is preferably provided between the non-flexible substrate and the transistor. As the substrate 400, a sheet, a film, or a foil containing a fiber may be used. The substrate 400 may have elasticity. The substrate 400 may have a property of returning to its original shape when bending or pulling is stopped. Alternatively, the substrate 400 may have a property of not returning to its original shape. The substrate 400 has a region with a thickness of, for example, greater than or equal to 5 μm and less than or equal to 700 μm, preferably greater than or equal to 10 μm and less than or equal to 500 μm, more preferably greater than or equal to 15 μm and less than or equal to 300 μm. When the substrate 400 has a small thickness, the weight of the semiconductor device including the transistor can be reduced. When the substrate 400 has a small thickness, even in the case of using glass or the like, the substrate 400 may have elasticity or a property of returning to its original shape when bending or pulling is stopped. Therefore, an impact applied to the semiconductor device over the substrate 400, which is caused by dropping or the like, can be reduced. That is, a durable semiconductor device can be provided.

[0150]

For the substrate 400 which is a flexible substrate, metal, an alloy, resin, glass, or fiber thereof can be used, for example. The flexible substrate 400 preferably has a lower coefficient of linear expansion because deformation due to an environment is suppressed. The flexible substrate 400 is formed using, for example, a material whose coefficient of linear expansion is lower than or equal to 1×10^{-3}/K, lower than or equal to 5×10^{-5}/K, or lower than or equal to 1×10^{-5}/K. Examples of the resin include polyester, polyolefin, polyamide (e.g., nylon or aramid), polyimide, polycarbonate, and acrylic. In particular, aramid is preferably used for the flexible substrate 400 because of its low coefficient of linear expansion.

[0151]

At least part of this embodiment can be implemented in combination with any of the embodiments described in this specification as appropriate.

[0152]

(Embodiment 3)

<Method 1 for manufacturing transistor>

A method for manufacturing the transistor of the present invention in FIGS. 1A to 1C will be described below with reference to FIGS. 15A to 15C, FIGS. 16A to 16C, FIGS. 17A to 17C, FIGS. 18A to 18C, FIGS. 19A to 19C, FIGS. 20A to 20C, FIGS. 21A to 21C, and FIGS. 22A to 22C.

[0153]

First, the substrate 400 is prepared.

[0154]

Then, the insulator 402 is formed. The insulator 402 may be formed by a sputtering method, a chemical vapor deposition (CVD) method, a molecular beam epitaxy (MBE) method, a pulsed laser deposition (PLD) method, an atomic layer deposition (ALD) method, or the like.

[0155]

Note that CVD methods can be classified into a plasma enhanced CVD (PECVD) method using plasma, a thermal CVD (TCVD) method using heat, a photo CVD method using light, and the like. Moreover, the CVD method can include a metal CVD (MCVD) method and a metal organic CVD (MOCVD) method depending on a source gas.

[0156]

In the case of a PECVD method, a high quality film can be obtained at relatively low temperature. Furthermore, a TCVD method does not use plasma and thus causes less plasma damage to an object. For example, a wiring, an electrode, an element (e.g., transistor or capacitor), or the like included in a semiconductor device might be charged up by receiving electric charges from plasma. In that case, accumulated electric charges might break the wiring, electrode, element, or the like included in the semiconductor device. Such plasma damage is not caused in the case of using a TCVD method, and thus the yield of a semiconductor device can be increased. In addition, since plasma damage does not occur in the deposition by a TCVD method, a film with few defects can be obtained.

[0157]

An ALD method also causes less plasma damage to an object. An ALD method does not cause plasma damage during deposition, so that a film with few defects can be obtained.

[0158]

Unlike in a deposition method in which particles ejected from a target or the like are deposited, in a CVD method and an ALD method, a film is formed by reaction at a surface of an object. Thus, a CVD method and an ALD method enable favorable step coverage almost regardless of the shape of an object. In particular, an ALD method enables excellent step coverage and excellent thickness uniformity and can be favorably used for covering a surface of an opening with a high aspect ratio, for example. On the other hand, an ALD method has a

relatively low deposition rate; thus, it is sometimes preferable to combine an ALD method with another deposition method with a high deposition rate such as a CVD method.

[0159]

When a CVD method or an ALD method is used, composition of a film to be formed can be controlled with a flow rate ratio of the source gases. For example, by the CVD method or the ALD method, a film with a desired composition can be formed by adjusting the flow ratio of a source gas. Moreover, with a CVD method or an ALD method, by changing the flow rate ratio of the source gases while forming the film, a film whose composition is continuously changed can be formed. In the case where the film is formed while changing the flow rate ratio of the source gases, as compared to the case where the film is formed using a plurality of deposition chambers, time taken for the deposition can be reduced because time taken for transfer and pressure adjustment is omitted. Thus, semiconductor devices can be manufactured with improved productivity.

[0160]

Next, treatment to add oxygen to the insulator 402 may be performed. Examples of the treatment for adding oxygen to the insulator 402 include ion implantation and plasma treatment. Note that oxygen added to the insulator 402 is excess oxygen.

[0161]

Next, an insulator to be the insulator 406a is deposited over the insulator 402. The insulator to be the insulator 406a can be deposited by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like.

[0162]

Next, treatment to add oxygen to the insulator to be the insulator 406a may be performed. Examples of the treatment for adding oxygen to the insulator to be the insulator 406a include ion implantation and plasma treatment. Note that oxygen added to the insulator to be the insulator 406a is excess oxygen. Oxygen is preferably added to a layer corresponding to the insulator to be the insulator 406a. Next, the semiconductor to be the semiconductor 406b is formed over the insulator to be the insulator 406a.

[0163]

Next, first heat treatment is preferably performed. The first heat treatment can be performed at a temperature higher than or equal to 250 °C and lower than or equal to 650 °C, preferably higher than or equal to 450 °C and lower than or equal to 600 °C, further preferably higher than or equal to 520 °C and lower than or equal to 570 °C. The first heat treatment is performed in an inert gas atmosphere or an atmosphere containing an oxidizing gas at 10 ppm or more, 1 % or more, or 10 % or more. The first heat treatment may be performed under a

reduced pressure. Alternatively, the first heat treatment may be performed in such a manner that heat treatment is performed in an inert gas atmosphere, and then another heat treatment is performed in an atmosphere containing an oxidizing gas at 10 ppm or more, 1 % or more, or 10 % or more in order to compensate desorbed oxygen. By the first heat treatment, crystallinity of the semiconductor can be increased and impurities such as hydrogen and moisture can be removed, for example. Alternatively, in the first heat treatment, plasma treatment using oxygen may be performed under a reduced pressure. The plasma treatment containing oxygen is preferably performed using an apparatus including a power source for generating high-density plasma using microwaves, for example. Alternatively, a power source for applying a radio frequency (RF) to a substrate side may be provided. The use of high-density plasma enables high-density oxygen radicals to be produced, and application of the RF to the substrate side allows oxygen radicals generated by the high-density plasma to be efficiently introduced into the semiconductor 406b. Alternatively, after plasma treatment using an inert gas with the apparatus, plasma treatment using oxygen in order to compensate released oxygen may be performed.

[0164]

Next, a conductor to be a conductor 415 is formed over the semiconductor to be the semiconductor 406b. The conductor can be formed by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like. Then, the insulator to be the insulator 406a, the semiconductor to be the semiconductor 406b, and the conductor to be the conductor 415 are processed by a lithography method or the like to form a multilayer film including the insulator 406a, the semiconductor 406b, and the conductor 415. Here, a top surface of the semiconductor to be the semiconductor 406b is damaged when the conductor is formed, whereby the region 407 is formed. The region 407 includes a region in which the resistance of the semiconductor 406b is reduced; thus, contact resistance between the conductor 415 and the semiconductor 406b is reduced. Note that when the multilayer film is formed, the insulator 402 is also subjected etching to have a thinned region in some cases. That is, the insulator 402 may have a protruding portion in a region in contact with the multilayer film (see FIGS. 15A to 15C).

[0165]

In the lithography method, first, a resist is exposed to light through a photomask. Next, a region exposed to light is removed or left using a developing solution, so that a resist mask is formed. Then, etching through the resist mask is conducted. As a result, the conductor, the semiconductor, the insulator, or the like can be processed into a desired shape. The resist mask is formed by, for example, exposure of the resist to light using KrF excimer laser light, ArF excimer laser light, extreme ultraviolet (EUV) light, or the like. Alternatively, a liquid

immersion technique may be employed in which a portion between a substrate and a projection lens is filled with liquid (e.g., water) to perform light exposure. An electron beam or an ion beam may be used instead of the above-mentioned light. Note that a photomask is not necessary in the case of using an electron beam or an ion beam. Note that dry etching treatment such as ashing or wet etching treatment can be used for removal of the resist mask. Alternatively, wet etching treatment is performed after dry etching treatment. Further alternatively, dry etching treatment is performed after wet etching treatment.

[0166]

As a dry etching apparatus, a capacitively coupled plasma (CCP) etching apparatus including parallel plate type electrodes can be used. The capacitively coupled plasma etching apparatus including the parallel plate type electrodes may have a structure in which a high-frequency power source is applied to one of the parallel plate type electrodes. Alternatively, the capacitively coupled plasma etching apparatus may have a structure in which different high-frequency power sources are applied to one of the parallel plate type electrodes. Alternatively, the capacitively coupled plasma etching apparatus may have a structure in which high-frequency power sources with the same frequency are applied to the parallel plate type electrodes. Alternatively, the capacitively coupled plasma etching apparatus may have a structure in which high-frequency power sources with different frequencies are applied to the parallel plate type electrodes. Alternatively, a dry etching apparatus including a high-density plasma source can be used. As the dry etching apparatus including a high-density plasma source, an inductively coupled plasma (ICP) etching apparatus can be used, for example.

[0167]

Next, an insulator 410a is formed. The insulator 410a can be formed by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like. Alternatively, the insulator 410a can be formed by a spin coating method, a dipping method, a droplet discharging method (such as an ink-jet method), a printing method (such as screen printing or offset printing), a doctor knife method, a roll coater method, a curtain coater method, or the like.

[0168]

The insulator 410a may be formed to have a flat top surface. For example, the top surface of the insulator 410a may have flatness immediately after the film formation. Alternatively, for example, the insulator 410a may have flatness by removing the insulator and the like from the top surface after the film formation so that the top surface of the insulator 410a becomes parallel to a reference surface such as a rear surface of the substrate. Such treatment is referred to as planarization treatment. As the planarization treatment, for example, chemical

mechanical polishing (CMP) treatment, dry etching treatment, or the like can be performed. However, the top surface of the insulator 410a is not necessarily flat.

[0169]

Next, a resist mask 411 is formed over the insulator 410a by a lithography method or the like. Here, in order to improve the adhesion between the top surface of the insulator 410a and the resist mask 411, for example, an organic coating film may be provided between the insulator 410a and the resist mask 411 (see FIGS. 16A to 16C).

[0170]

Next, first processing is performed until the opening in the insulator 410a reaches a top surface of the conductor 415 by dry etching or the like. As a gas for the dry etching in the first processing, for example, a C_4F_6 gas, a CF_4 gas, a SF_6 gas, a CHF_3 gas, or the like can be used. Alternatively, an oxygen gas, a helium gas, an argon gas, a hydrogen gas, or the like can be added to any of the above gases as appropriate. Here, a C_4F_6 gas to which an oxygen gas is added is preferably used. As a dry etching apparatus, any of the above-described dry etching apparatuses can be used; however, a dry etching apparatus in which high-frequency power sources with different frequencies are connected to parallel-plate electrodes is preferably used (see FIGS. 17A to 17C).

[0171]

Next, the conductor 415 is subjected to second processing by dry etching or the like so as to be separated into the conductor 416a1 and the conductor 416a2. As a gas for the dry etching in the second processing, for example, a C_4F_6 gas, a CF_4 gas, a SF_6 gas, a Cl_2 gas, a BCl_3 gas, a $SiCl_4$ gas, and the like can be used alone or in combination. Alternatively, an oxygen gas, a helium gas, an argon gas, or a hydrogen gas can be added to any of the above gases as appropriate. Here, a combination of a CF_4 gas, a Cl_2 gas, and an oxygen gas is preferably used. As a dry etching apparatus, the above-described dry etching apparatuses for the first processing may be used (see FIGS. 18A to 18C).

[0172]

At this time, the semiconductor 406b has a region that is exposed. The exposed region of the semiconductor 406b, which is the region 407, is removed in some cases. In the second processing, side surfaces of the semiconductor 406b are covered with the insulator 410 and thus are not exposed to a gas used for the second processing. That is, etching is not performed on the side surfaces of the semiconductor 406b in the second processing; thus, residual components of the gas used for the second processing is prevented from attaching to the surface of the semiconductor 406b. Thus, the side surfaces of the semiconductor 406b are preferably protected.

[0173]

Next, third processing is performed until the opening in an insulator to be the insulator 410 reaches the insulator 402 by dry etching or the like, whereby the insulator 410 is formed. As a dry etching gas used in the third processing, a C_4F_6 gas to which an oxygen gas is added can be used as in the first processing; however, in the third processing, for example, the flow rate of the oxygen gas to be added is preferably increased. By increasing the flow rate of the oxygen gas compared to that in the first processing, the etching rate of the resist mask 411 in the horizontal direction along a surface parallel to the rear surface the substrate is made higher than that in the first processing, and thus the etching rate of the insulator to be the insulator 410 in the horizontal direction along the surface parallel to the rear surface the substrate is made higher than that in the first processing. Thus, as denoted by dotted lines in FIGS. 19B and 19C, the opening in the insulator 410 can be formed so as to expand in the horizontal direction along the surface parallel to the rear surface the substrate (see FIGS. 19A to 19C).

[0174]

A dry etching apparatus that is similar to that used in the first processing and the second processing can be used in the third processing, for example. In the case where a dry etching apparatus in which high-frequency power sources with different frequencies are applied to the parallel plate type electrodes is used, the electric power of the high-frequency power source that is applied to one or both of the parallel plate type electrodes is preferably increased compared to the case in the first processing. As a result, the etching rate of the resist mask 411 in the horizontal direction along the surface parallel to the rear surface of the substrate can be made higher than that in the first processing, and the same effect as that obtained by increasing the flow rate of the oxygen gas added as described above can be obtained. Thus, the opening of the insulator 410 can be formed so as to expand in the horizontal direction along the surface parallel to the rear surface of the substrate.

[0175]

The same dry etching apparatus as that in the first processing and the second processing is used in the third processing; thus, the first to third processing can be successively performed without exposure to air. Therefore, contamination due to attachment of an atmospheric component to a substrate, corrosion of the insulator, the semiconductor, and the conductor due to reaction between the etching gas remaining on the substrate and the atmospheric component, and the like can be prevented. Alternatively, improvement in productivity can be expected when the first processing, the second processing, and the third processing are successively performed.

[0176]

When the first processing and the second processing are each performed by dry etching,

an impurity such as the residual components of the etching gas is attached to the exposed region of the semiconductor 406b in some cases. For example, when a chlorine-based gas is used as an etching gas, chlorine and the like are attached in some cases. Furthermore, when a hydrocarbon-based gas is used as an etching gas, carbon, hydrogen, and the like are attached in some cases. When the substrate is exposed to air after the second processing, the exposed region of the semiconductor 406b and the like corrode in some cases. Thus, plasma treatment using an oxygen gas is preferably performed successively after the second processing because the impurity can be removed and corrosion of the exposed region of the semiconductor 406b and the like can be prevented.

[0177]

Alternatively, the impurity may be reduced by cleaning treatment using diluted hydrofluoric acid or the like or cleaning treatment using ozone or the like, for example. Note that different types of cleaning treatment may be combined. In such a manner, the exposed region of the semiconductor 406b, i.e., a channel formation region has high resistance.

[0178]

Meanwhile, in the region 407 where the conductors 416a1 and 416a2 and the top surface of the semiconductor 406b overlap with each other, a value of contact resistance between the conductors 416a1 and 416a2 and the semiconductor 406b is decreased; thus, favorable transistor characteristics can be obtained.

[0179]

Next, an insulator 406c_1 is formed, and an insulator 412_1 is formed over the insulator 406c_1. The insulator 406c_1 and the insulator 412_1 can be deposited by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like. The insulator 406c_1 and the insulator 412_1 are preferably formed to have the uniform thickness along bottom and side surfaces of an opening formed in the insulator 410 and the conductors 416a1 and 416a2. Therefore, the ALD method is preferably used.

[0180]

Next, a conductor 404_1 is formed. The conductor 404_1 can be formed by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like. The conductor 404_1 is formed so as to fill the opening formed by the insulator 410 and the like. Therefore, the CVD method (the MCVD method, in particular) is preferred. A multilayer film of a conductor deposited by an ALD method or the like and a conductor deposited by a CVD method is preferred in some cases to increase adhesion of the conductor deposited by an MCVD method. For example, a multilayer film in which titanium nitride and tungsten are formed in this order or the like may be used (see FIGS. 20A to 20C).

[0181]

Next, the conductor 404_1, the insulator 412_1, and the insulator 406c_1 are polished and flattened so as to reach the top surface of the insulator 410 by CMP or the like from the top surface of the conductor 404_1, whereby the conductor 404, the insulator 412, and the insulator 406c are formed. Accordingly, the conductor 404 serving as the gate electrode can be formed in a self-aligned manner without using a lithography method. The conductor 404 serving as the gate electrode can be formed without considering alignment accuracy of the conductor 404 serving as the gate electrode and the conductors 416a1 and 416a2 serving as the source electrode and the drain electrode; as a result, the area of the semiconductor device can be reduced. Furthermore, because the lithography process is not necessary, improvement in productivity due to simplification of the process is expected (see FIGS. 21A to 21C).

[0182]

An insulator to be the insulator 408 can be formed by a sputtering method, a CVD method, a MBE method, a PLD method, an ALD method, or the like. Aluminum oxide is preferably formed as the insulator to be the insulator 408 using plasma containing oxygen, so that oxygen in the plasma can be added to the top surface of the insulator 410, a region of the insulator 412 in contact with the insulator 408, and a region of the insulator 406c in contact with the insulator 408 as excess oxygen. Here, a mixed region 414 containing a large amount of excess oxygen might be formed in the interface between the insulator 408 and the insulator 410 and the vicinity of the interface. FIGS. 22B and 22C illustrate the state where the excess oxygen is added to the vicinity of the mixed region 414 by arrows.

[0183]

Second heat treatment may be performed at any time after the formation of the insulator to be the insulator 408. By the second heat treatment, the excess oxygen contained in the insulator 410 and the mixed region 414 is moved to the semiconductor 406b through the insulators 402 and/or 406a. Furthermore, the excess oxygen contained in the insulator 410 and the mixed region 414 is moved to the semiconductor 406b through the insulator 412 and/or the insulator 406c. Since excess oxygen is moved to the semiconductor 406b by passing two paths as described above, defects (oxygen vacancies) in the semiconductor 406b can be reduced (see FIGS. 22B and 22C).

[0184]

Note that the second heat treatment may be performed at a temperature such that excess oxygen (oxygen) in the insulator 410 and the mixed region 414 is diffused to the semiconductor 406b. For example, the description of the first heat treatment may be referred to for the second heat treatment. Alternatively, the temperature of the second heat treatment is preferably lower

than that of the first heat treatment. The second heat treatment is preferably performed at a temperature lower than that of the first heat treatment by higher than or equal to 20 °C and lower than or equal to 150 °C, preferably higher than or equal to 40 °C and lower than or equal to 100 °C. Accordingly, superfluous release of excess oxygen (oxygen) from the insulator 402 can be inhibited. Note that the second heat treatment is not necessarily performed when heating during formation of the films can work as heat treatment comparable to the second heat treatment.

[0185]

Next, an opening reaching the conductor 416a1 and an opening reaching the conductor 416a2 are formed in the insulator to be the insulator 408 and the insulator 410, and the conductors 431 and 429 are embedded in their respective openings. Next, an opening reaching the conductor 404 is formed in the insulator to be the insulator 408, and the conductor 437 is embedded in the opening, whereby the insulator 408 is formed. Conductors to be the conductors 432, 430, and 438 are formed over the insulator 408 and the conductors 431, 429, and 437, and the conductors 432, 430, and 438 are formed by a lithography method or the like. Note that formation of the openings reaching the conductors 416a1 and 416a2 in the insulator to be the insulator 408 and the insulator 410, and formation of the opening reaching the conductor 404 in the insulator 408 may be performed at the same time. When the openings are formed at the same time, improvement in productivity due to simplification of the process is expected.

[0186]

Through the above steps, the transistor illustrated in FIGS. 1A to 1C can be manufactured.

[0187]

<Method 2 for manufacturing transistor>

A method for manufacturing a transistor in FIGS. 5A to 5C having a structure different from that of the transistor in FIGS. 1A to 1C will be described below with reference to FIG. 3, FIGS. 23A to 23C, FIGS. 24A to 24C, FIGS. 25A to 25C, and FIGS. 26A to 26C. The process up to the second processing is similar to that in the method 1 for manufacturing a transistor (see FIGS. 18A and 18B).

[0188]

Next, third processing is performed until the insulator to be the insulator 410 reaches the insulator 402 by dry etching or the like, whereby the insulator 410 is formed. As a dry etching gas used in the third processing, a C_4F_6 gas to which an oxygen gas is added, which is the same as that used in the first processing is used; however, in the third processing, for example, the flow rate of the oxygen gas to be added may be increased. By increasing the flow rate of the oxygen gas compared to that in the first processing, the etching rate of the resist mask 411 in the

horizontal direction along the surface parallel to the rear surface of substrate is made higher than that in the first processing, and thus the etching rate of the insulator to be the insulator 410 in the horizontal direction along the surface parallel to the rear surface of the substrate is made higher than that in the first processing. Furthermore, when a gas containing one or more kinds of gases for etching the conductors 416a1 and 416a2, e.g., a SF_6 gas, a CF_4 gas, and a Cl_2 gas, is added to a C_4F_6 gas and an oxygen gas, as denoted by dotted lines in FIGS. 23B and 23C, the opening of the insulator 410 can be formed so as to expand in the horizontal direction along the surface parallel to the rear surface of the substrate, and regions can be formed in which the side surfaces of the conductors 416a1 and 416a2 have a tapered angle 446 and a tapered angle 447, respectively. Although not shown in the figures, only top end portions of the conductors 416a1 and 416a2 may have tapered cross sections, or the top end portions of the conductors 416a1 and 416a2 may have round cross sections.

[0189]

Accordingly, coverage by the insulator 406c formed over the side surfaces of the conductors 416a1 and 416a2 and the insulator 412 serving as the gate insulator is improved. When coverage by the insulator 406c and the insulator 412 is improved, leakage current flowing through the conductor 404 serving as the gate electrode and through the conductors 416a1 and 416a2 serving as the source electrode and the drain electrode can be kept low. Alternatively, leakage current flowing between the conductor 404 serving as the gate electrode and the semiconductor 406b including a channel formation region can be kept low.

[0190]

The taper angles 446 and 447 are each greater than or equal to 10° and less than or equal to 90°, preferably, greater than or equal to 30° and less than or equal to 80°. The taper angle 446 can be controlled by changing an etching rate ratio between an etching rate of the conductor 416a1 and an etching rate of the insulator 410 in the horizontal direction along the surface parallel to rear surface of the substrate. The taper angle 447 can be controlled by changing an etching rate ratio between an etching rate of the conductor 416a2 and an etching rate of the insulator 410 in the horizontal direction along the surface parallel to the rear surface of the substrate. For example, when the etching rate ratio is 1, the taper angle 446 and the taper angle 447 are each 45° (see FIG. 3).

[0191]

A dry etching apparatus that is similar to that used in the first processing can be used in the third processing, for example.

[0192]

The same dry etching apparatus as that in the first processing and the second processing

is used in the third processing; thus, the first to third processing can be successively performed without exposure to air. Therefore, contamination due to attachment of an atmospheric component to a substrate, corrosion of the insulator, the semiconductor, and the conductor due to reaction between the etching gas remaining on the substrate and the atmospheric component, and the like can be prevented. Alternatively, improvement in productivity can be expected when the first processing, the second processing, and the third processing are successively performed.

[0193]

When the first processing and the second processing are each performed by dry etching, an impurity such as the residual components of the etching gas is attached to the exposed region of the semiconductor 406b in some cases. For example, when a chlorine-based gas is used as an etching gas, chlorine and the like are attached in some cases. Furthermore, when a hydrocarbon-based gas is used as an etching gas, carbon, hydrogen, and the like are attached in some cases. When the substrate is exposed to air after the second processing, the exposed region of the semiconductor 406b and the like corrode in some cases. Thus, plasma treatment using an oxygen gas is preferably performed successively after the second processing because the impurity can be removed and corrosion of the exposed region of the semiconductor 406b and the like can be prevented.

[0194]

Alternatively, the impurity may be reduced by cleaning treatment using diluted hydrofluoric acid or the like or cleaning treatment using ozone or the like, for example. Note that different types of cleaning treatment may be combined. In such a manner, the exposed region of the semiconductor 406b, i.e., a channel formation region has high resistance.

[0195]

Meanwhile, in the region 407 where the conductors 416a1 and 416a2 and the top surface of the semiconductor 406b overlap with each other, a value of contact resistance between the conductors 416a1 and 416a2 and the semiconductor 406b is decreased; thus, favorable transistor characteristics can be obtained.

[0196]

Next, the insulator 406c_1 is formed, and the insulator 412_1 is formed over the insulator 406c_1. The insulator 406c_1 and the insulator 412_1 can be deposited by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like. The insulator 406c_1 and the insulator 412_1 are preferably formed to have the uniform thickness along the bottom and side surfaces of the opening formed by the insulator 410 and the conductors 416a1 and 416a2. Therefore, the ALD method is preferably used.

[0197]

Next, the conductor 404_1 is formed. The conductor 404_1 can be formed by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like. The conductor 404_1 is formed so as to fill the opening formed by the insulator 410 and the like. Therefore, the CVD method (the MCVD method, in particular) is preferred. A multilayer film of a conductor deposited by an ALD method or the like and a conductor deposited by a CVD method is preferred in some cases to increase adhesion of the conductor deposited by an MCVD method. For example, a multilayer film in which titanium nitride and tungsten are formed in this order or the like may be used (see FIGS. 24A to 24C).

[0198]

Next, the conductor 404_1, the insulator 412_1, and the insulator 406c_1 are polished and flattened so as to reach the top surface of the insulator 410 by CMP or the like from the top surface of the conductor 404_1, whereby the conductor 404, the insulator 412, and the insulator 406c are formed. Accordingly, the conductor 404 serving as the gate electrode can be formed in a self-aligned manner without using a lithography method. The conductor 404 serving as the gate electrode can be formed without considering alignment accuracy of the conductor 404 serving as the gate electrode and the conductors 416a1 and 416a2 serving as the source electrode and the drain electrode; as a result, the area of the semiconductor device can be reduced. Furthermore, because the lithography process is not necessary, improvement in productivity due to simplification of the process is expected (see FIGS. 25A to 25C).

[0199]

The insulator to be the insulator 408 can be formed by a sputtering method, a CVD method, a MBE method, a PLD method, an ALD method, or the like. Aluminum oxide is preferably formed as the insulator to be the insulator 408 using plasma containing oxygen, so that oxygen in the plasma can be added to the top surface of the insulator 410, a region of the insulator 412 in contact with the insulator 408, and a region of the insulator 406c in contact with the insulator 408 as excess oxygen. Here, a mixed region 414 containing a large amount of excess oxygen might be formed in the interface between the insulator 408 and the insulator 410 and the vicinity of the interface. FIGS. 26B and 26C illustrate the state where the excess oxygen is added to the vicinity of the mixed region 414 by arrows.

[0200]

Second heat treatment may be performed at any time after the formation of the insulator to be the insulator 408. By the second heat treatment, the excess oxygen contained in the insulator 410 and the mixed region 414 is moved to the semiconductor 406b through the insulators 402 and/or 406a. Furthermore, the excess oxygen contained in the insulator 410 and the mixed region 414 is moved to the semiconductor 406b through the insulator 412 and/or the

insulator 406c. Since excess oxygen is moved to the semiconductor 406b by passing two paths as described above, defects (oxygen vacancies) in the semiconductor 406b can be reduced (see FIGS. 26A and 26B).

[0201]

Note that the second heat treatment may be performed at a temperature such that excess oxygen (oxygen) in the insulator 410 and the mixed region 414 is diffused to the semiconductor 406b. For example, the description of the first heat treatment may be referred to for the second heat treatment. Alternatively, the temperature of the second heat treatment is preferably lower than that of the first heat treatment. The second heat treatment is preferably performed at a temperature lower than that of the first heat treatment by higher than or equal to 20 °C and lower than or equal to 150 °C, preferably higher than or equal to 40 °C and lower than or equal to 100 °C. Accordingly, superfluous release of excess oxygen (oxygen) from the insulator 402 can be inhibited. Note that the second heat treatment is not necessarily performed when heating during formation of the films can work as heat treatment comparable to the second heat treatment.

[0202]

Next, an opening reaching the conductor 416a1 and an opening reaching the conductor 416a2 are formed in the insulator to be the insulator 408 and the insulator 410, and the conductors 431 and 429 are embedded in their respective openings. Next, an opening reaching the conductor 404 is formed in the insulator to be the insulator 408, and the conductor 437 is embedded in the opening, whereby the insulator 408 is formed. Conductors to be the conductors 432, 430, and 438 are formed over the insulator 408 and the conductors 431, 429, and 437, and the conductors 432, 430, and 438 are formed by a lithography method or the like. Note that formation of the openings reaching the conductors 416a1 and 416a2 in the insulator to be the insulator 408 and the insulator 410, and formation of the opening reaching the conductor 404 in the insulator 408 may be performed at the same time. When the openings are formed at the same time, improvement in productivity due to simplification of the process is expected.

[0203]

Through the above steps, the transistor illustrated in FIGS. 5A to 5C can be manufactured.

[0204]

<Method 3 for manufacturing transistor>

A method for manufacturing a transistor in FIGS. 1A to 1C which is different from Method 1 for manufacturing a transistor is described with reference to FIGS. 27A to 27C, FIGS. 28A to 28C, FIGS. 29A to 29C, FIGS. 30A to 30C, FIGS. 31A to 31C, FIGS. 32A to 32C, and FIGS. 33A to 33C. The process up to the formation of the multilayer film including the

insulator 406a, the semiconductor 406b, and the conductor 415 is similar to that in the Method 1 for manufacturing a transistor and Method 2 for manufacturing a transistor (see FIGS. 15A and 15B).

[0205]

Next, the insulator 410a is formed. The insulator 410a can be formed by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like. Alternatively, the insulator 410a can be formed by a spin coating method, a dipping method, a droplet discharging method (such as an ink-jet method), a printing method (such as screen printing or offset printing), a doctor knife method, a roll coater method, a curtain coater method, or the like.

[0206]

The insulator 410a may be formed to have a flat top surface. For example, the top surface of the insulator 410a may have flatness immediately after the film formation. Alternatively, for example, the top surface of the insulator 410a may have flatness by removing the upper portion of the insulator and the like after the film formation so that the top surface of the insulator 410a becomes parallel to a reference surface such as a rear surface of the substrate. Such treatment is referred to as planarization treatment. As the planarization treatment, for example, chemical mechanical polishing (CMP) treatment, dry etching treatment, or the like can be performed. However, the top surface of the insulator 410a is not necessarily flat.

[0207]

Next, the resist mask 411 is formed over the insulator 410a by a lithography method or the like. Here, an organic coating film may be provided between the insulator 410a and the resist mask 411 in order to improve the adhesion between the top surface of the insulator 410a and the resist mask 411. An opening in the resist mask 411 is formed so as to be larger than that formed by Method 1 for manufacturing a transistor and Method 2 for manufacturing a transistor (see FIGS. 27A, 27B, and 27C).

[0208]

Next, first processing is performed until the opening in the insulator 410a reaches the top surface of the conductor 415 and the top surface of the insulator 402 by dry etching or the like, whereby the insulator 410 is formed. As a gas for the dry etching in the first processing, for example, a C_4F_6 gas, a CF_4 gas, a SF_6 gas, a CHF_3 gas, or the like can be used. Alternatively, an oxygen gas, a helium gas, an argon gas, a hydrogen gas, or the like can be added to any of the above gases as appropriate. Here, a C_4F_6 gas to which an oxygen gas is added is preferably used. As a dry etching apparatus, any of the above-described dry etching apparatuses can be used; however, a dry etching apparatus in which high-frequency power

sources with different frequencies are connected to the parallel-plate electrodes is preferably used (see FIGS. 28A to 28C).

[0209]

Next, plasma is generated using a gas containing carbon and halogen with a dry etching apparatus and an organic substance 413 is deposited on the resist mask 411, the semiconductor 406b, and the side surfaces of the insulator 410 by plasma. Examples of the gas to be used include CHF_3, and C_4F_8. The dry etching apparatus may be the same as that used in the first processing. Alternatively, a dry etching apparatus using a high-density plasma source may be used; for example, an inductively-coupled plasma etching apparatus can be used (see FIGS. 29A to 29C). Although the above is the film formation method of an organic film using a dry etching apparatus, the present invention is not limited to this, and an apparatus different from the dry etching apparatus may be used. Alternatively, an inorganic film may be formed.

[0210]

Next, the conductor 415 is subjected to the second processing by dry etching or the like so as to be separated into the conductor 416a1 and the conductor 416a2. Since the organic substance 413 is formed on the side surfaces of the insulator 410, the conductor 415 is etched along the side surfaces of the organic substance 413 on the side surfaces of the insulator 410, and as shown in FIG. 30B, the side surfaces of the 416a1 and 416a2 are positioned inward from the side surfaces of the insulator 410. As a gas for the dry etching in the second processing, for example, a C_4F_6 gas, a CF_4 gas, a SF_6 gas, a Cl_2 gas, a BCl_3 gas, a $SiCl_4$ gas, and the like can be used alone or in combination. Alternatively, an oxygen gas, a helium gas, an argon gas, or a hydrogen gas can be added to any of the above gases as appropriate. Here, a combination of a CF_4 gas, a Cl_2 gas, and an oxygen gas is preferably used. As a dry etching apparatus, the above-described dry etching apparatuses for the first processing may be used (see FIGS. 30A to 30C).

[0211]

As a dry etching apparatus used in the second processing, a dry etching apparatus that is similar to that used in the first processing can be used.

[0212]

The deposition of the organic substance 413 and the second processing are performed using the same dry etching apparatus as that in the first processing; thus, the first processing, the deposition of the organic substance 413, and the second processing can be successively performed without exposure to air. Therefore, contamination due to attachment of an atmospheric component to a substrate, corrosion of the insulator, the semiconductor, and the conductor due to reaction between the etching gas remaining on the substrate and the

atmospheric component, and the like can be prevented. Alternatively, improvement in productivity can be expected by successively performing the first processing, the deposition of the organic substance 413, and the second processing.

[0213]

When the first processing, the deposition of the organic substance 413, and the second processing are each performed by dry etching, an impurity such as the residual components of the etching gas is attached to the exposed region of the semiconductor 406b in some cases. For example, when a chlorine-based gas is used as an etching gas, chlorine and the like are attached in some cases. Furthermore, when a hydrocarbon-based gas is used as an etching gas, carbon, hydrogen, and the like are attached in some cases. When the substrate is exposed to air after the second processing, the exposed region of the semiconductor 406b and the like corrode in some cases. Thus, plasma treatment using an oxygen gas is preferably performed successively after the second processing because the impurity can be removed and corrosion of the exposed region of the semiconductor 406b and the like can be prevented. Furthermore, the organic substance 413 on the side surfaces of the insulator 410 can be removed by the plasma treatment using an oxygen gas.

[0214]

Alternatively, the impurity may be reduced by cleaning treatment using diluted hydrofluoric acid or the like or cleaning treatment using ozone or the like, for example. Note that different types of cleaning treatment may be combined. In such a manner, the exposed region of the semiconductor 406b, i.e., a channel formation region has high resistance.

[0215]

Meanwhile, in the region 407 where the conductors 416a1 and 416a2 and the top surface of the semiconductor 406b overlap with each other, a value of contact resistance between the conductors 416a1 and 416a2 and the semiconductor 406b is decreased; thus, favorable transistor characteristics can be obtained.

[0216]

Next, the insulator 406c_1 is formed, and the insulator 412_1 is formed over the insulator 406c_1. The insulator 406c_1 and the insulator 412_1 can be deposited by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like. The insulator 406c_1 and the insulator 412_1 are preferably formed to have the uniform thickness along the bottom and side surfaces of the opening formed by the insulator 410 and the conductors 416a1 and 416a2. Therefore, the ALD method is preferably used.

[0217]

Next, the conductor 404_1 is formed. The conductor 404_1 can be formed by a

sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like. The conductor 404_1 is formed so as to fill the opening formed by the insulator 410 and the like. Therefore, the CVD method (the MCVD method, in particular) is preferred. A multilayer film of a conductor deposited by an ALD method or the like and a conductor deposited by a CVD method is preferred in some cases to increase adhesion of the conductor deposited by an MCVD method. For example, a multilayer film in which titanium nitride and tungsten are formed in this order or the like may be used (see FIGS. 31A to 31C).

[0218]

Next, the conductor 404_1, the insulator 412_1, and the insulator 406c_1 are polished and flattened so as to reach the top surface of the insulator 410 by CMP or the like from the top surface of the conductor 404_1, whereby the conductor 404, the insulator 412, and the insulator 406c are formed. Accordingly, the conductor 404 serving as the gate electrode can be formed in a self-aligned manner without using a lithography method. The conductor 404 serving as the gate electrode can be formed without considering alignment accuracy of the conductor 404 serving as the gate electrode and the conductors 416a1 and 416a2 serving as the source electrode and the drain electrode; as a result, the area of the semiconductor device can be reduced. Furthermore, because the lithography process is not necessary, improvement in productivity due to simplification of the process is expected (see FIGS. 32A to 32C).

[0219]

The insulator to be the insulator 408 can be formed by a sputtering method, a CVD method, a MBE method, a PLD method, an ALD method, or the like. Aluminum oxide is preferably formed as the insulator to be the insulator 408 using plasma containing oxygen, so that oxygen in the plasma can be added to the top surface of the insulator 410, the region of the insulator 412 in contact with the insulator 408, and the region of the insulator 406c in contact with the insulator 408 as excess oxygen. Here, the mixed region 414 containing a large amount of excess oxygen might be formed in the interface between the insulator 408 and the insulator 410 and the vicinity of the interface. FIGS. 33B and 33C illustrate the state where the excess oxygen is added to the vicinity of the mixed region 414 by arrows.

[0220]

Second heat treatment may be performed at any time after the formation of the insulator to be the insulator 408. By the second heat treatment, the excess oxygen contained in the insulator 410 and the mixed region 414 is moved to the semiconductor 406b through the insulators 402 and/or 406a. Furthermore, the excess oxygen contained in the insulator 410 and the mixed region 414 is moved to the semiconductor 406b through the insulator 412 and/or the insulator 406c. Since excess oxygen is moved to the semiconductor 406b by passing two paths

as described above, defects (oxygen vacancies) in the semiconductor 406b can be reduced (see FIGS. 33A and 33B).

[0221]

Note that the second heat treatment may be performed at a temperature such that excess oxygen (oxygen) in the insulator 410 and the mixed region 414 is diffused to the semiconductor 406b. For example, the description of the first heat treatment may be referred to for the second heat treatment. Alternatively, the temperature of the second heat treatment is preferably lower than that of the first heat treatment. The second heat treatment is preferably performed at a temperature lower than that of the first heat treatment by higher than or equal to 20 °C and lower than or equal to 150 °C, preferably higher than or equal to 40 °C and lower than or equal to 100 °C. Accordingly, superfluous release of excess oxygen (oxygen) from the insulator 402 can be inhibited. Note that the second heat treatment is not necessarily performed when heating during formation of the films can work as heat treatment comparable to the second heat treatment.

[0222]

Next, the opening reaching the conductor 416a1 and the opening reaching the conductor 416a2 are formed in the insulator to be the insulator 408 and the insulator 410, and the conductors 431 and 429 are embedded in their respective openings. Next, the opening reaching the conductor 404 is formed in the insulator to be the insulator 408, and the conductor 437 is embedded in the opening, whereby the insulator 408 is formed. The conductors to be the conductors 432, 430, and 438 are formed over the insulator 408 and the conductors 431, 429, and 437, and the conductors 432, 430, and 438 are formed by a lithography method or the like. Note that formation of the openings reaching the conductors 416a1 and 416a2 in the insulator to be the insulator 408 and the insulator 410, and formation of the opening reaching the conductor 404 in the insulator 408 may be performed at the same time. When the openings are formed at the same time, improvement in productivity due to simplification of the process is expected.

[0223]

Through the above steps, the transistor in FIGS. 1A to 1C can be manufactured by a method different from the Method 1 for manufacturing a transistor.

[0224]

<Method 4 for manufacturing transistor>

A method for manufacturing the transistor in FIGS. 5A to 5C which is different from Method 2 for manufacturing a transistor is described with reference to FIG. 3, FIGS. 34A to 34C, FIGS. 35A to 35C, FIGS. 36A to 36C, and FIGS. 37A to 37C. The process up to the deposition of the organic substance 413 on the resist mask 411, the semiconductor 406b, and the side surfaces of the insulator 410 is similar to that in Method 3 for manufacturing a transistor (see

FIGS. 29A and 29B).

[0225]

Next, the conductor 415 is subjected to the second processing by dry etching or the like, so as to be separated into the conductor 416a1 and the conductor 416a2. As a gas for the dry etching in the second processing, for example, a C_4F_6 gas, a CF_4 gas, a SF_6 gas, a Cl_2 gas, a BCl_3 gas, a $SiCl_4$ gas, or the like can be used alone or in combination. Alternatively, an oxygen gas, a helium gas, an argon gas, a hydrogen gas, or the like can be added to any of the above gases as appropriate. Here, the flow rate of the oxygen gas may be increased compared to that in the etching gas used in the second processing in Method 3 for manufacturing a transistor. By increasing the flow rate of the oxygen gas, the etching rate of the organic film deposited on the side surfaces of the insulator 410 in the horizontal direction along the surface parallel to the rear surface of the substrate is made higher than that in the second processing by Method 3 for manufacturing a transistor, and thus, as denoted by dotted lines in FIGS. 34B and 34C, the organic substance 413 on the side surfaces of the insulator 410 is etched in the horizontal direction along the surface parallel to the rear surface substrate and the regions can be formed in which the side surfaces of the conductors 416a1 and 416a2 have the tapered angle 446 and the tapered angle 447, respectively. Although not shown in the figures, only top end portions of the conductors 416a1 and 416a2 may have cross sections with tapered shape, or the top end portions of the conductors 416a1 and 416a2 may have round cross sections.

[0226]

Accordingly, coverage by the insulator 406c formed over the side surfaces of the conductors 416a1 and 416a2 and the insulator 412 serving as the gate insulator is improved. When coverage by the insulator 406c and the insulator 412 is improved, leakage current flowing through the conductor 404 serving as the gate electrode and through the conductors 416a1 and 416a2 serving as the source electrode and the drain electrode can be kept low. Alternatively, leakage current flowing between the conductor 404 serving as the gate electrode and the semiconductor 406b including the channel formation region can be kept low.

[0227]

The taper angles 446 and 447 are each greater than or equal to 10° and less than or equal to 90°, preferably, greater than or equal to 30° and less than or equal to 80°. The taper angle 446 can be controlled by changing an etching rate ratio between the etching rate of the conductor 416a1 and an etching rate of the organic substance 413 deposited on the insulator 410 in the horizontal direction along the surface parallel to the rear surface of the substrate. The taper angle 447 can be controlled by changing an etching rate ratio between the etching rate of the conductor 416a2 and an etching rate of the organic substance 413 deposited on the insulator 410

in the horizontal direction along the surface parallel to the rear surface of the substrate. For example, when the etching rate ratio is 1, the taper angle 446 and the taper angle 447 are each 45° (see FIG. 3)

[0228]

As a dry etching apparatus used in the second processing, a dry etching apparatus that is similar to that used in the first processing can be used.

[0229]

The deposition of the organic substance 413 and the second processing are performed using the same dry etching apparatus as that in the first processing; thus, the first processing, the deposition of the organic substance 413, and the second processing can be successively performed without exposure to air. Therefore, contamination due to attachment of an atmospheric component to a substrate, corrosion of the insulator, the semiconductor, and the conductor due to reaction between the etching gas remaining on the substrate and the atmospheric component, and the like can be prevented. Alternatively, improvement in productivity can be expected by successively performing the first processing, the second processing, and the third processing.

[0230]

When the first processing, the deposition of the organic substance 413, and the second processing are each performed by dry etching, an impurity such as the residual components of the etching gas may be attached to the exposed region of the semiconductor 406b. For example, when a chlorine-based gas is used as an etching gas, chlorine and the like may be attached. Furthermore, when a hydrocarbon-based gas is used as an etching gas, carbon, hydrogen, and the like may be attached. When the substrate is exposed to air after the second processing, the exposed region of the semiconductor 406b and the like may corrode. Thus, plasma treatment using an oxygen gas that is successively performed after the second processing is preferably performed because the impurity can be removed and corrosion of the exposed region of the semiconductor 406b and the like can be prevented. Furthermore, the organic substance 413 on the side surfaces of the insulator 410 can be removed by the plasma treatement using an oxygen gas.

[0231]

Alternatively, the impurity may be reduced by cleaning treatment using diluted hydrofluoric acid or the like or cleaning treatment using ozone or the like, for example. Note that different types of cleaning treatment may be combined. In such a manner, the exposed region of the semiconductor 406b, i.e., a channel formation region has high resistance.

[0232]

Meanwhile, in the region 407 where the conductors 416a1 and 416a2 and the top surface of the semiconductor 406b overlap with each other, a value of contact resistance between the conductors 416a1 and 416a2 and the semiconductor 406b is decreased; thus, favorable transistor characteristics can be obtained.

[0233]

Next, the insulator 406c_1 is formed, and the insulator 412_1 is formed over the insulator 406c_1. The insulator 406c_1 and the insulator 412_1 can be deposited by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like. The insulator 406c_1 and the insulator 412_1 are preferably formed to have the uniform thickness along the bottom and side surfaces of the opening formed by the insulator 410 and the conductors 416a1 and 416a2. Therefore, the ALD method is preferably used.

[0234]

Next, the conductor 404_1 is formed. The conductor 404_1 can be formed by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like. The conductor 404_1 is formed so as to fill the opening formed by the insulator 410 and the like. Therefore, the CVD method (the MCVD method, in particular) is preferred. A multilayer film of a conductor deposited by an ALD method or the like and a conductor deposited by a CVD method is preferred in some cases to increase adhesion of the conductor deposited by an MCVD method. For example, a multilayer film in which titanium nitride and tungsten are formed in this order or the like may be used (see FIGS. 35A to 35C).

[0235]

Next, the conductor 404_1, the insulator 412_1, and the insulator 406c_1 are polished and flattened so that the opening reaches the top surface of the insulator 410 by CMP or the like from the top surface of the conductor 404_1, whereby the conductor 404, the insulator 412, and the insulator 406c are formed. Accordingly, the conductor 404 serving as the gate electrode can be formed in a self-aligned manner without using a lithography method. The conductor 404 serving as the gate electrode can be formed without considering alignment accuracy of the conductor 404 serving as the gate electrode and the conductors 416a1 and 416a2 serving as the source electrode and the drain electrode; as a result, the area of the semiconductor device can be reduced. Furthermore, because the lithography process is not necessary, improvement in productivity due to simplification of the process is expected (see FIGS. 36A to 36C).

[0236]

The insulator to be the insulator 408 can be formed by a sputtering method, a CVD method, a MBE method, a PLD method, an ALD method, or the like. Aluminum oxide is preferably formed as the insulator to be the insulator 408 using plasma containing oxygen, so

that oxygen in the plasma can be added to the top surface of the insulator 410, the region of the insulator 412 in contact with the insulator 408, and the region of the insulator 406c in contact with the insulator 408 as excess oxygen. Here, the mixed region 414 containing a large amount of excess oxygen might be formed in the interface between the insulator 408 and the insulator 410 and the vicinity of the interface. FIGS. 37B and 37C illustrate the state where the excess oxygen is added to the vicinity of the mixed region 414 by arrows.

[0237]

Second heat treatment may be performed at any time after the formation of the insulator to be the insulator 408. By the second heat treatment, the excess oxygen contained in the insulator 410 and the mixed region 414 is moved to the semiconductor 406b through the insulators 402 and/or 406a. Furthermore, the excess oxygen contained in the insulator 410 and the mixed region 414 is moved to the semiconductor 406b through the insulator 412 and/or the insulator 406c. Since excess oxygen is moved to the semiconductor 406b by passing two paths as described above, defects (oxygen vacancies) in the semiconductor 406b can be reduced (see FIGS. 37A and 37B).

[0238]

Note that the second heat treatment may be performed at a temperature such that excess oxygen (oxygen) in the insulator 410 and the mixed region 414 is diffused to the semiconductor 406b. For example, the description of the first heat treatment may be referred to for the second heat treatment. Alternatively, the temperature of the second heat treatment is preferably lower than that of the first heat treatment. The second heat treatment is preferably performed at a temperature lower than that of the first heat treatment by higher than or equal to 20 °C and lower than or equal to 150 °C, preferably higher than or equal to 40 °C and lower than or equal to 100 °C. Accordingly, superfluous release of excess oxygen (oxygen) from the insulator 402 can be inhibited. Note that the second heat treatment is not necessarily performed when heating during formation of the films can work as heat treatment comparable to the second heat treatment.

[0239]

Next, the opening reaching the conductor 416a1 and the opening reaching the conductor 416a2 are formed in the insulator to be the insulator 408 and the insulator 410, and the conductors 431 and 429 are embedded in their respective openings. Next, the opening reaching the conductor 404 is formed in the insulator to be the insulator 408, and the conductor 437 is embedded in the opening, whereby the insulator 408 is formed. The conductors to be the conductors 432, 430, and 438 are formed over the insulator 408 and the conductors 431, 429, and 437, and the conductors 432, 430, and 438 are formed by a lithography method or the like. Note that formation of the openings reaching the conductors 416a1 and 416a2 in the insulator to

be the insulator 408 and the insulator 410, and formation of the opening reaching the conductor 404 in the insulator 408 may be performed at the same time. When the openings are formed at the same time, improvement in productivity due to simplification of the process is expected.

[0240]

Through the above steps, the transistor in FIGS. 5A to 5C can be manufactured by a method different from the Method 2 for manufacturing a transistor. At least part of this embodiment can be implemented in combination with any of the embodiments described in this specification as appropriate.

[0241]

(Embodiment 4)

<Memory Device 1>

An example of a semiconductor device (memory device) which includes the transistor of one embodiment of the present invention, which can retain stored data even when not powered, and which has an unlimited number of write cycles is shown in FIGS. 38A and 38B.

[0242]

The semiconductor device illustrated in FIG. 38A includes a transistor 3200 using a first semiconductor, a transistor 3300 using a second semiconductor, and a capacitor 3400. Note that any of the above-described transistors can be used as the transistor 3300.

[0243]

Note that the transistor 3300 is preferably a transistor with a low off-state current. For example, a transistor using an oxide semiconductor can be used as the transistor 3300. Since the off-state current of the transistor 3300 is low, stored data can be retained for a long period at a predetermined node of the semiconductor device. In other words, power consumption of the semiconductor device can be reduced because refresh operation becomes unnecessary or the frequency of refresh operation can be extremely low.

[0244]

In FIG. 38A, a first wiring 3001 is electrically connected to a source of the transistor 3200. A second wiring 3002 is electrically connected to a drain of the transistor 3200. A third wiring 3003 is electrically connected to one of the source and the drain of the transistor 3300. A fourth wiring 3004 is electrically connected to the gate of the transistor 3300. The gate of the transistor 3200 and the other of the source and the drain of the transistor 3300 are electrically connected to one electrode of the capacitor 3400. A fifth wiring 3005 is electrically connected to the other electrode of the capacitor 3400.

[0245]

The semiconductor device in FIG. 38A has a feature that the potential of the gate of the

transistor 3200 can be retained, and thus enables writing, retaining, and reading of data as follows.

[0246]

Writing and retaining of data are described. First, the potential of the fourth wiring 3004 is set to a potential at which the transistor 3300 is on, so that the transistor 3300 is turned on. Accordingly, the potential of the third wiring 3003 is supplied to a node FG where the gate of the transistor 3200 and the one electrode of the capacitor 3400 are electrically connected to each other. That is, a predetermined electric charge is supplied to the gate of the transistor 3200 (writing). Here, one of two kinds of electric charges providing different potential levels (hereinafter referred to as a low-level electric charge and a high-level electric charge) is supplied. After that, the potential of the fourth wiring 3004 is set to a potential at which the transistor 3300 is off, so that the transistor 3300 is turned off. Thus, the electric charge is held at the node FG (retaining).

[0247]

Since the off-state current of the transistor 3300 is low, the electric charge of the node FG is retained for a long time.

[0248]

Next, reading of data is described. An appropriate potential (a reading potential) is supplied to the fifth wiring 3005 while a predetermined potential (a constant potential) is supplied to the first wiring 3001, whereby the potential of the second wiring 3002 varies depending on the amount of electric charge retained in the node FG. This is because in the case of using an n-channel transistor as the transistor 3200, an apparent threshold voltage V_{th_H} at the time when the high-level electric charge is given to the gate of the transistor 3200 is lower than an apparent threshold voltage V_{th_L} at the time when the low-level electric charge is given to the gate of the transistor 3200. Here, an apparent threshold voltage refers to the potential of the fifth wiring 3005 which is needed to make the transistor 3200 be in "on state." Thus, the potential of the fifth wiring 3005 is set to a potential V_0 which is between V_{th_H} and V_{th_L}, whereby electric charge supplied to the node FG can be determined. For example, in the case where the high-level electric charge is supplied to the node FG in writing and the potential of the fifth wiring 3005 is V_0 ($>V_{th_H}$), the transistor 3200 is brought into "on state." In the case where the low-level electric charge is supplied to the node FG in writing, even when the potential of the fifth wiring 3005 is V_0 ($<V_{th_L}$), the transistor 3200 still remains in "off state." Thus, the data retained in the node FG can be read by determining the potential of the second wiring 3002.

[0249]

Note that in the case where memory cells are arrayed, it is necessary that data of a

desired memory cell be read in read operation. The fifth wiring 3005 of memory cells from which data is not read may be supplied with a potential at which the transistor 3200 is turned off regardless of the electric charge supplied to the node FG, that is, a potential lower than V_{th_H}, whereby only data of a desired memory cell can be read. Alternatively, the fifth wiring 3005 of the memory cells from which data is not read may be supplied with a potential at which the transistor 3200 is brought into "on state" regardless of the electric charge supplied to the node FG, that is, a potential higher than V_{th_L}, whereby only data of a desired memory cell can be read.

[0250]

<Structure 1 of semiconductor device>

FIG. 39 is a cross-sectional view of the semiconductor device in FIG. 38A. The semiconductor device shown in FIG. 39 includes the transistor 3200, the transistor 3300, and the capacitor 3400. The transistor 3300 and the capacitor 3400 are provided over the transistor 3200. Although an example where the transistor illustrated in FIGS. 1A to 1C is used as the transistor 3300 is shown, a semiconductor device of one embodiment of the present invention is not limited thereto. The description of the above transistor is referred to.

[0251]

The transistor 3200 illustrated in FIG. 39 is a transistor using a semiconductor substrate 450. The transistor 3200 includes a region 474a in the semiconductor substrate 450, a region 474b in the semiconductor substrate 450, an insulator 462, and a conductor 454.

[0252]

In the transistor 3200, the regions 474a and 474b have a function as a source region and a drain region. The insulator 462 has a function as a gate insulator. The conductor 454 has a function as a gate electrode. Therefore, resistance of a channel formation region can be controlled by a potential applied to the conductor 454. In other words, conduction or non-conduction between the region 474a and the region 474b can be controlled by the potential applied to the conductor 454.

[0253]

For the semiconductor substrate 450, a single-material semiconductor substrate of silicon, germanium, or the like or a compound semiconductor substrate of silicon carbide, silicon germanium, gallium arsenide, indium phosphide, zinc oxide, gallium oxide, or the like may be used, for example. A single crystal silicon substrate is preferably used as the semiconductor substrate 450.

[0254]

For the semiconductor substrate 450, a semiconductor substrate including impurities imparting n-type conductivity is used. However, a semiconductor substrate including

impurities imparting p-type conductivity may be used as the semiconductor substrate 450. In that case, a well including impurities imparting the n-type conductivity may be provided in a region where the transistor 3200 is formed. Alternatively, the semiconductor substrate 450 may be an i-type semiconductor substrate.

[0255]

The top surface of the semiconductor substrate 450 preferably has a (110) plane. Thus, on-state characteristics of the transistor 3200 can be improved.

[0256]

The regions 474a and 474b are regions including impurities imparting the p-type conductivity. Accordingly, the transistor 3200 has a structure of a p-channel transistor.

[0257]

Note that although the transistor 3200 is illustrated as a p-channel transistor, the transistor 3200 may be an n-channel transistor.

[0258]

Note that the transistor 3200 is separated from an adjacent transistor by the region 460 and the like. The region 460 is an insulating region.

[0259]

The semiconductor illustrated in FIG. 39 includes an insulator 464, an insulator 466, an insulator 468, an insulator 470, an insulator 472, an insulator 475, the insulator 402, the insulator 410, the insulator 408, an insulator 428, an insulator 465, an insulator 467, an insulator 469, an insulator 498, a conductor 480a, a conductor 480b, a conductor 480c, a conductor 478a, a conductor 478b, a conductor 478c, a conductor 476a ,a conductor 476b, a conductor 476c, a conductor 479a, a conductor 479b, a conductor 479c, a conductor 477a, a conductor 477b, a conductor 477c, a conductor 484a, a conductor 484b, a conductor 484c, a conductor 484d, a conductor 483a, a conductor 483b, a conductor 483c, a conductor 483d, a conductor 483e, a conductor 483f, a conductor 485a, a conductor 485b, a conductor 485c, a conductor 485d, a conductor 487a, a conductor 487b, a conductor 487c, a conductor 488a, a conductor 488b, a conductor 488c, a conductor 490a, a conductor 490b, a conductor 489a, a conductor 489b, a conductor 491a, a conductor 491b, a conductor 491c, a conductor 492a, a conductor 492b, a conductor 492c, a conductor 494, a conductor 496, an insulator 406a, a semiconductor 406b, and an insulator 406c.

[0260]

The insulator 464 is provided over the transistor 3200. The insulator 466 is over the insulator 464. The insulator 468 is over the insulator 466. The insulator 470 is placed over the insulator 468. The insulator 472 is placed over the insulator 470. The insulator 475 is

placed over the insulator 472. The transistor 3300 is provided over the insulator 475. The insulator 408 is provided over the transistor 3300. The insulator 428 is provided over the insulator 408. The insulator 465 is over the insulator 428. The capacitor 3400 is provided over the insulator 465. The insulator 469 is provided over the capacitor 3400.

[0261]

The insulator 464 includes an opening reaching the region 474a, an opening reaching the region 474b, and an opening reaching the conductor 454, in which the conductor 480a, the conductor 480b, and the conductor 480c are embedded, respectively.

[0262]

In addition, the insulator 466 includes an opening reaching the conductor 480a, an opening reaching the conductor 480b, and an opening reaching the conductor 480c, in which the conductor 478a, the conductor 478b, and the conductor 478c are embedded, respectively.

[0263]

In addition, the insulator 468 includes an opening reaching the conductor 478a, an opening reaching the conductor 478b, and an opening reaching the conductor 478c, in which the conductor 476a, the conductor 476b, and the conductor 476c are embedded, respectively.

[0264]

The conductor 479a in contact with the conductor 476a, the conductor 479b in contact with the conductor 476b, and the conductor 479c in contact with the conductor 476c are over the insulator 468. The insulator 472 includes an opening reaching the conductor 479a through the insulator 470, an opening reaching the conductor 479b through the insulator 470, and an opening reaching the conductor 479c through the insulator 470. In the openings, the conductor 477a, the conductor 477b, or the conductor 477c is embedded.

[0265]

The insulator 475 includes an opening overlapping with the channel formation region of the transistor 3300, an opening reaching the conductor 477a, an opening reaching the conductor 477b, and an opening reaching the conductor 477c. In the openings, the conductor 484a, the conductor 484b, the conductor 484c, and the conductor 484d is embedded.

[0266]

The conductor 484d may have a function as a bottom gate electrode of the transistor 3300. Alternatively, for example, electric characteristics such as the threshold voltage of the transistor 3300 may be controlled by application of a constant potential to the conductor 484d. Further alternatively, for example, the conductor 484d and the top gate electrode of the transistor 3300 may be electrically connected to each other. Thus, the on-state current of the transistor 3300 can be increased. A punch-through phenomenon can be suppressed; thus, stable electric

characteristics in the saturation region of the transistor 3300 can be obtained.

[0267]

In addition, the insulator 402 includes an opening reaching the conductor 484a, an opening reaching the conductor 484c, and an opening reaching the conductor 484b.

[0268]

The insulator 428 includes two openings reaching the conductor 484a and the conductor 484b through the insulator 408, the insulator 410, and the insulator 402, two openings reaching a conductor of one of the source electrode and the drain electrode of the transistor 3300 through the insulator 408 and the insulator 410, and an opening reaching a conductor of the gate electrode of the transistor 3300 through the insulator 408. In the openings, the conductor 483a, the conductor 483c, the conductor 483e, the conductor 483f, and the conductor 483d are embedded.

[0269]

The conductor 485a in contact with the conductors 483a and 483e, the conductor 485b in contact with the conductor 483b, the conductor 485c in contact with the conductor 483c and the conductor 483f, and the conductor 485d in contact with the conductor 483d are over the insulator 428. The insulator 465 has an opening reaching the conductor 485a, an opening reaching the conductor 485b, and an opening reaching the conductor 485c. In the openings, the conductor 487a, the conductor 487b, and the conductor 487c are embedded.

[0270]

The conductor 488a in contact with the conductor 487a, the conductor 488b in contact with the conductor 487b, and the conductor 488c in contact with the conductor 487c are over the insulator 465. In addition, the insulator 467 includes an opening reaching the conductor 488a and an opening reaching the conductor 488b. In the openings, the conductor 490a and the conductor 490b are embedded. The conductor 488c is in contact with the conductor 494 which is one of the electrodes of the capacitor 3400.

[0271]

The conductor 489a in contact with the conductor 490a and the conductor 489b in contact with the conductor 490b are over the insulator 467. The insulator 469 includes an opening reaching the conductor 489a, an opening reaching the conductor 489b, an opening reaching the conductor 496 which is the other of electrodes of the capacitor 3400. In the openings, the conductor 491a, the conductor 491b, and the conductor 491c are embedded.

[0272]

The conductor 492a in contact with the conductor 491a, the conductor 492b in contact with the conductor 491b, and the conductor 492c in contact with the conductor 491c are over the

insulator 469.

[0273]

The insulators 464, 466, 468, 470, 472, 475, 402, 410, 408, 428, 465, 467, 469, and 498 may each be formed to have, for example, a single-layer structure or a stacked-layer structure including an insulator containing boron, carbon, nitrogen, oxygen, fluorine, magnesium, aluminum, silicon, phosphorus, chlorine, argon, gallium, germanium, yttrium, zirconium, lanthanum, neodymium, hafnium, or tantalum. The insulator 401 may be formed of, for example, aluminum oxide, magnesium oxide, silicon oxide, silicon oxynitride, silicon nitride oxide, silicon nitride, gallium oxide, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, or tantalum oxide.

[0274]

The insulator that has a function of blocking oxygen and impurities such as hydrogen is preferably included in at least one of the insulators 464, 466, 468, 470, 472, 475, 402, 410, 408, 428, 465, 467, 469, and 498. When an insulator that has a function of blocking oxygen and impurities such as hydrogen is placed near the transistor 3300, the electric characteristics of the transistor 3300 can be stable.

[0275]

An insulator with a function of blocking oxygen and impurities such as hydrogen may have a single-layer structure or a stacked-layer structure including an insulator containing, for example, boron, carbon, nitrogen, oxygen, fluorine, magnesium, aluminum, silicon, phosphorus, chlorine, argon, gallium, germanium, yttrium, zirconium, lanthanum, neodymium, hafnium, or tantalum may be used.

[0276]

Each of the conductors 480a, 480b, 480c, 478a, 478b, 478c, 476a, 476b, 476c, 479a, 479b, 479c, 477a, 477b, 477c, 484a, 484b, 484c, 484d, 483a, 483b, 483c, 483d, 483e, 483f, 485a, 485b, 485c, 485d, 487a, 487b, 487c, 488a, 488b, 488c, 490a, 490b, 489a, 489b, 491a, 491b, 491c, 492a, 492b, 492c, 494, and 496 may have a single-layer structure or a stacked-layer structure including a conductor containing, for example, one or more kinds of boron, nitrogen, oxygen, fluorine, silicon, phosphorus, aluminum, titanium, chromium, manganese, cobalt, nickel, copper, zinc, gallium, yttrium, zirconium, molybdenum, ruthenium, silver, indium, tin, tantalum, and tungsten. An alloy or a compound may be used, for example, and a conductor containing aluminum, a conductor containing copper and titanium, a conductor containing copper and manganese, a conductor containing indium, tin, and oxygen, a conductor containing titanium and nitrogen, or the like may be used.

[0277]

An oxide semiconductor is preferably used as the semiconductor 406b. However, silicon (including strained silicon), germanium, silicon germanium, silicon carbide, gallium arsenide, aluminum gallium arsenide, indium phosphide, gallium nitride, an organic semiconductor, or the like can be used in some cases.

[0278]

As the insulator 406a and the insulator 406c, oxides containing one or more, or two or more elements other than oxygen included in the semiconductor 406b are preferably used. However, silicon (including strained silicon), germanium, silicon germanium, silicon carbide, gallium arsenide, aluminum gallium arsenide, indium phosphide, gallium nitride, an organic semiconductor, or the like can be used in some cases.

[0279]

The source or drain of the transistor 3200 is electrically connected to the conductor that is one of the source electrode and the drain electrode of the transistor 3300 through the conductor 480a, the conductor 478a, the conductor 476a, the conductor 479a, the conductor 477a, the conductor 484a, the conductor 483a, the conductor 485a, and the conductor 483e. The conductor 454 that is the gate electrode of the transistor 3200 is electrically connected to the conductor that is the other of the source electrode and the drain electrode of the transistor 3300 through the conductor 480c, the conductor 478c, the conductor 476c, the conductor 479c, the conductor 477c, the conductor 484c, the conductor 483c, the conductor 485c, and the conductor 483f.

[0280]

The capacitor 3400 includes the conductor 494 which is one of the electrodes of the capacitor 3400 and electrically connected to one of the source electrode and the drain electrode of the transistor 3300 through the conductor 483f, the conductor 485c, the conductor 487c, and the conductor 488c, the insulator 498, the conductor 496 which is the other electrode of the capacitor 3400. The capacitor 3400 is preferably formed above or below the transistor 3300 because the semiconductor can be reduced in size.

[0281]

For the structures of other components, the description of FIGS. 1A to 1C and the like can be referred to as appropriate.

[0282]

A semiconductor device in FIG. 40 is the same as the semiconductor device in FIG. 39 except the structure of the transistor 3200. Therefore, the description of the semiconductor device in FIG. 39 is referred to for the semiconductor device in FIG. 40. Specifically, in the semiconductor device in FIG. 40, the transistor 3200 is a FIN-type transistor. The effective

channel width is increased in the FIN-type transistor 3200, whereby the on-state characteristics of the transistor 3200 can be improved. In addition, since contribution of the electric field of the gate electrode can be increased, the off-state characteristics of the transistor 3200 can be improved. Note that the transistor 3200 may be a p-channel transistor or an n-channel transistor.

[0283]

Although an example in which the transistor 3300 is over the transistor 3200 and the capacitor 3400 is over the transistor 3300 is illustrated in this embodiment, one or more transistors including a semiconductor similar to the transistor 3300 may be provided over the transistor 3200. With such a structure, the degree of integration of the semiconductor device can be further increased.

[0284]

<Memory device 2>

The semiconductor device in FIG. 38B is different from the semiconductor device in FIG. 38A in that the transistor 3200 is not provided. Also in this case, data can be written and retained in a manner similar to that of the semiconductor device in FIG. 38A.

[0285]

Reading of data in the semiconductor device in FIG. 38B is described. When the transistor 3300 is turned on, the third wiring 3003 which is in a floating state and the capacitor 3400 are electrically connected to each other, and the charge is redistributed between the third wiring 3003 and the capacitor 3400. As a result, the potential of the third wiring 3003 is changed. The amount of change in potential of the third wiring 3003 varies depending on the potential of the one of the electrode of the capacitor 3400 (or the charge accumulated in the capacitor 3400).

[0286]

For example, the potential of the third wiring 3003 after the charge redistribution is $(C_B \times V_{B0} + C \times V)$ $(C_B + C)$, where V is the potential of the one electrode of the capacitor 3400, C is the capacitance of the capacitor 3400, C_B is the capacitance component of the third wiring 3003, and V_{B0} is the potential of the third wiring 3003 before the charge redistribution. Thus, it can be found that, assuming that the memory cell is in either of two states in which the potential of the one electrode of the capacitor 3400 is V_1 and V_0 ($V_1 > V_0$), the potential of the third wiring 3003 in the case of retaining the potential V_1 $(=(C_B \times V_{B0} + C \times V_1) / (C_B + C))$ is higher than the potential of the third wiring 3003 in the case of retaining the potential V_0 $(=(C_B \times V_{B0} + C \times V_0) / (C_B + C))$.

[0287]

Then, by comparing the potential of the third wiring 3003 with a predetermined potential, data can be read.

[0288]

In this case, a transistor including the first semiconductor may be used for a driver circuit for driving a memory cell, and a transistor including the second semiconductor may be stacked over the driver circuit as the transistor 3300.

[0289]

When including a transistor using an oxide semiconductor and having an low off-state current, the semiconductor device described above can retain stored data for a long time. In other words, refresh operation becomes unnecessary or the frequency of the refresh operation can be extremely low, which leads to a sufficient reduction in power consumption. Moreover, stored data can be retained for a long time even when power is not supplied (note that a potential is preferably fixed).

[0290]

Further, in the semiconductor device, high voltage is not needed for writing data and deterioration of elements is less likely to occur. Unlike in a conventional nonvolatile memory, for example, it is not necessary to inject and extract electrons into and from a floating gate; thus, a problem such as deterioration of an insulator is not caused. That is, the semiconductor device of one embodiment of the present invention does not have a limit on the number of times data can be rewritten, which is a problem of a conventional nonvolatile memory, and the reliability thereof is drastically improved. Furthermore, data is written depending on the state of the transistor (on or off), whereby high-speed operation can be easily achieved. At least part of this embodiment can be implemented in combination with any of the embodiments described in this specification as appropriate.

[0291]

(Embodiment 5)

<Structure 2 of semiconductor device>

In this embodiment, an example of a circuit including the transistor of one embodiment of the present invention is described with reference to drawings.

<Cross-Sectional Structure>

FIGS. 41A and 41B are cross-sectional views of a semiconductor device of one embodiment of the present invention. In FIG. 41A, X1-X2 direction represents a channel length direction, and in FIG. 41B, Y1-Y2 direction represents a channel width direction. The semiconductor device illustrated in FIGS. 41A and 41B includes a transistor 2200 containing a first semiconductor material in a lower portion and a transistor 2100 containing a second

semiconductor material in an upper portion. In FIGS. 41A and 41B, an example is illustrated in which the transistor illustrated in FIGS. 1A to 1C is used as the transistor 2100 containing the second semiconductor material.

[0292]

Here, the first semiconductor material and the second semiconductor material are preferably materials having different band gaps. For example, the first semiconductor material can be a semiconductor material other than an oxide semiconductor (examples of such a semiconductor material include silicon (including strained silicon), germanium, silicon germanium, silicon carbide, gallium arsenide, aluminum gallium arsenide, indium phosphide, gallium nitride, and an organic semiconductor), and the second semiconductor material can be an oxide semiconductor. A transistor using a material other than an oxide semiconductor, such as single crystal silicon, can operate at high speed easily. In contrast, a transistor using an oxide semiconductor and described in the above embodiment as an example has excellent subthreshold characteristics and a minute structure. Furthermore, the transistor can operate at a high speed because of its high switching speed and has low leakage current because of its low off-state current.

[0293]

The transistor 2200 may be either an n-channel transistor or a p-channel transistor, and an appropriate transistor may be used in accordance with a circuit. Furthermore, the specific structure of the semiconductor device, such as the material or the structure used for the semiconductor device, is not necessarily limited to those described here except for the use of the transistor of one embodiment of the present invention which uses an oxide semiconductor.

[0294]

FIGS. 41A and 41B illustrate a structure in which the transistor 2100 is provided over the transistor 2200 with an insulator 2201, an insulator 2207, and an insulator 2208 provided therebetween. A plurality of wirings 2202 are provided between the transistor 2200 and the transistor 2100. Furthermore, wirings and electrodes provided over and under the insulators are electrically connected to each other through a plurality of plugs 2203 embedded in the insulators. An insulator 2204 covering the transistor 2100 and a wiring 2205 over the insulator 2204 are provided.

[0295]

The stack of the two kinds of transistors reduces the area occupied by the circuit, allowing a plurality of circuits to be highly integrated.

[0296]

Here, in the case where a silicon-based semiconductor material is used for the transistor

2200 provided in a lower portion, hydrogen in an insulator provided in the vicinity of the semiconductor film of the transistor 2200 terminates dangling bonds of silicon; accordingly, the reliability of the transistor 2200 can be improved. Meanwhile, in the case where an oxide semiconductor is used for the transistor 2100 provided in an upper portion, hydrogen in an insulator provided in the vicinity of the semiconductor film of the transistor 2100 becomes a factor of generating carriers in the oxide semiconductor; thus, the reliability of the transistor 2100 might be decreased. Therefore, in the case where the transistor 2100 using an oxide semiconductor is provided over the transistor 2200 using a silicon-based semiconductor material, it is particularly effective that the insulator 2207 having a function of preventing diffusion of hydrogen is provided between the transistors 2100 and 2200. The insulator 2207 makes hydrogen remain in the lower portion, thereby improving the reliability of the transistor 2200. In addition, since the insulator 2207 suppresses diffusion of hydrogen from the lower portion to the upper portion, the reliability of the transistor 2100 also can be improved.

[0297]

The insulator 2207 can be, for example, formed using aluminum oxide, aluminum oxynitride, gallium oxide, gallium oxynitride, yttrium oxide, yttrium oxynitride, hafnium oxide, hafnium oxynitride, or yttria-stabilized zirconia (YSZ).

[0298]

Furthermore, a blocking film having a function of preventing diffusion of hydrogen is preferably formed over the transistor 2100 to cover the transistor 2100 including an oxide semiconductor film. For the blocking film, a material that is similar to that of the insulator 2207 can be used, and in particular, an aluminum oxide film is preferably used. Using the aluminum oxide film, excess oxygen can be added to the insulator under the aluminum oxide film in the deposition, and the excess oxygen moves to the oxide semiconductor layer of the transistor 2100 by heat treatment, which has an effect of repairing a defect in the oxide semiconductor layer. The aluminum oxide film has a high shielding (blocking) effect of preventing penetration of both oxygen and impurities such as hydrogen and moisture. Thus, by using the aluminum oxide film as the blocking film covering the transistor 2100, release of oxygen from the oxide semiconductor film included in the transistor 2100 and entry of water and hydrogen into the oxide semiconductor film can be prevented. Note that as the block film, the insulator 2204 having a stacked-layer structure may be used, or the block film may be provided under the insulator 2204.

[0299]

Note that the transistor 2200 can be a transistor of various types without being limited to a planar type transistor. For example, the transistor 2200 can be a fin-type transistor, a tri-gate

transistor, or the like. An example of a cross-sectional view in this case is shown in FIGS. 41E and 41F. An insulator 2212 is provided over a semiconductor substrate 2211. The semiconductor substrate 2211 includes a projecting portion with a thin tip (also referred to a fin). Note that an insulator may be provided over the projecting portion. The insulator functions as a mask for preventing the semiconductor substrate 2211 from being etched when the projecting portion is formed. The projecting portion does not necessarily have the thin tip; a projecting portion with a cuboid-like projecting portion and a projecting portion with a thick tip are permitted, for example. A gate insulator 2214 is provided over the projecting portion of the semiconductor substrate 2211, and a gate electrode 2213 is provided over the gate insulator 2214. Source and drain regions 2215 are formed in the semiconductor substrate 2211. Note that here is shown an example in which the semiconductor substrate 2211 includes the projecting portion; however, a semiconductor device of one embodiment of the present invention is not limited thereto. For example, a semiconductor region having a projecting portion may be formed by processing an SOI substrate.

[0300]

At least part of this embodiment can be implemented in combination with any of the embodiments described in this specification as appropriate.

[0301]

(Embodiment 6)

[CMOS circuit]

A circuit diagram in FIG. 41C shows a configuration of a so-called CMOS circuit in which a p-channel transistor 2200 and an n-channel transistor 2100 are connected to each other in series and in which gates of them are connected to each other.

[0302]

[Analog switch]

A circuit diagram in FIG. 41D shows a configuration in which sources of the transistors 2100 and 2200 are connected to each other and drains of the transistors 2100 and 2200 are connected to each other. With such a configuration, the transistors can function as a so-called analog switch. At least part of this embodiment can be implemented in combination with any of the embodiments described in this specification as appropriate.

[0303]

(Embodiment 7)

<CPU>

A CPU including a semiconductor device such as any of the above-described transistors or the above-described memory device is described below.

[0304]

FIG. 42 is a block diagram illustrating a configuration example of a CPU including any of the above-described transistors as a component.

[0305]

The CPU illustrated in FIG. 42 includes, over a substrate 1190, an arithmetic logic unit (ALU) 1191, an ALU controller 1192, an instruction decoder 1193, an interrupt controller 1194, a timing controller 1195, a register 1196, a register controller 1197, a bus interface 1198, a rewritable ROM 1199, and an ROM interface 1189. A semiconductor substrate, an SOI substrate, a glass substrate, or the like is used as the substrate 1190. The ROM 1199 and the ROM interface 1189 may be provided over a separate chip. Needless to say, the CPU in FIG. 42 is just an example of a simplified structure, and an actual CPU may have a variety of structures depending on the application. For example, the CPU may have the following configuration: a structure including the CPU illustrated in FIG. 42 or an arithmetic circuit is considered as one core; a plurality of the cores are included; and the cores operate in parallel. The number of bits that the CPU can process in an internal arithmetic circuit or in a data bus can be 8, 16, 32, or 64, for example.

[0306]

An instruction that is input to the CPU through the bus interface 1198 is input to the instruction decoder 1193 and decoded therein, and then, input to the ALU controller 1192, the interrupt controller 1194, the register controller 1197, and the timing controller 1195.

[0307]

The ALU controller 1192, the interrupt controller 1194, the register controller 1197, and the timing controller 1195 conduct various controls in accordance with the decoded instruction. Specifically, the ALU controller 1192 generates signals for controlling the operation of the ALU 1191. While the CPU is executing a program, the interrupt controller 1194 processes an interrupt request from an external input/output device or a peripheral circuit depending on its priority or a mask state. The register controller 1197 generates an address of the register 1196, and reads/writes data from/to the register 1196 depending on the state of the CPU.

[0308]

In the CPU illustrated in FIG. 42, a memory cell is provided in the register 1196. For the memory cell of the register 1196, any of the above-described transistors, the above-described memory device, or the like can be used.

[0309]

In the CPU illustrated in FIG. 42, the register controller 1197 selects operation of retaining data in the register 1196 in accordance with an instruction from the ALU 1191. That

is, the register controller 1197 selects whether data is held by a flip-flop or by a capacitor in the memory cell included in the register 1196. When data holding by the flip-flop is selected, a power supply voltage is supplied to the memory cell in the register 1196. When data holding by the capacitor is selected, the data is rewritten in the capacitor, and supply of the power supply voltage to the memory cell in the register 1196 can be stopped.

[0310]

FIG. 43 is an example of a circuit diagram of a memory element that can be used as the register 1196. A memory element 1200 includes a circuit 1201 in which stored data is volatile when power supply is stopped, a circuit 1202 in which stored data is nonvolatile even when power supply is stopped, a switch 1203, a switch 1204, a logic element 1206, a capacitor 1207, and a circuit 1220 having a selecting function. The circuit 1202 includes a capacitor 1208, a transistor 1209, and a transistor 1210. Note that the memory element 1200 may further include another element such as a diode, a resistor, or an inductor, as needed.

[0311]

Here, the above-described memory device can be used as the circuit 1202. When supply of a power supply voltage to the memory element 1200 is stopped, GND (0 V) or a potential at which the transistor 1209 in the circuit 1202 is turned off continues to be input to a gate of the transistor 1209. For example, the gate of the transistor 1209 is grounded through a load such as a resistor.

[0312]

Shown here is an example in which the switch 1203 is a transistor 1213 having one conductivity type (e.g., an n-channel transistor) and the switch 1204 is a transistor 1214 having a conductivity type opposite to the one conductivity type (e.g., a p-channel transistor). A first terminal of the switch 1203 corresponds to one of a source and a drain of the transistor 1213, a second terminal of the switch 1203 corresponds to the other of the source and the drain of the transistor 1213, and conduction or non-conduction between the first terminal and the second terminal of the switch 1203 (i.e., the on/off state of the transistor 1213) is selected by a control signal RD input to a gate of the transistor 1213. A first terminal of the switch 1204 corresponds to one of a source and a drain of the transistor 1214, a second terminal of the switch 1204 corresponds to the other of the source and the drain of the transistor 1214, and conduction or non-conduction between the first terminal and the second terminal of the switch 1204 (i.e., the on/off state of the transistor 1214) is selected by the control signal RD input to a gate of the transistor 1214.

[0313]

One of a source and a drain of the transistor 1209 is electrically connected to one of a

pair of electrodes of the capacitor 1208 and a gate of the transistor 1210. Here, the connection portion is referred to as a node M2. One of a source and a drain of the transistor 1210 is electrically connected to a line which can supply a low power supply potential (e.g., a GND line), and the other thereof is electrically connected to the first terminal of the switch 1203 (the one of the source and the drain of the transistor 1213). The second terminal of the switch 1203 (the other of the source and the drain of the transistor 1213) is electrically connected to the first terminal of the switch 1204 (the one of the source and the drain of the transistor 1214). The second terminal of the switch 1204 (the other of the source and the drain of the transistor 1214) is electrically connected to a line which can supply a power supply potential VDD. The second terminal of the switch 1203 (the other of the source and the drain of the transistor 1213), the first terminal of the switch 1204 (the one of the source and the drain of the transistor 1214), an input terminal of the logic element 1206, and one of a pair of electrodes of the capacitor 1207 are electrically connected to each other. Here, the connection portion is referred to as a node M1. The other of the pair of electrodes of the capacitor 1207 can be supplied with a constant potential. For example, the other of the pair of electrodes of the capacitor 1207 can be supplied with a low power supply potential (e.g., GND) or a high power supply potential (e.g., VDD). The other of the pair of electrodes of the capacitor 1207 is electrically connected to the line which can supply a low power supply potential (e.g., a GND line). The other of the pair of electrodes of the capacitor 1208 can be supplied with a constant potential. For example, the other of the pair of electrodes of the capacitor 1208 can be supplied with a low power supply potential (e.g., GND) or a high power supply potential (e.g., VDD). The other of the pair of electrodes of the capacitor 1208 is electrically connected to the line which can supply a low power supply potential (e.g., a GND line).

[0314]

The capacitor 1207 and the capacitor 1208 are not necessarily provided as long as the parasitic capacitance of the transistor, the line, or the like is actively utilized.

[0315]

A control signal WE is input to a first gate (first gate electrode) of the transistor 1209. As for each of the switch 1203 and the switch 1204, a conduction state or a non-conduction state between the first terminal and the second terminal is selected by the control signal RD which is different from the control signal WE. When the first terminal and the second terminal of one of the switches are in the conduction state, the first terminal and the second terminal of the other of the switches are in the non-conduction state.

[0316]

A signal corresponding to data retained in the circuit 1201 is input to the other of the

source and the drain of the transistor 1209. FIG. 43 illustrates an example in which a signal output from the circuit 1201 is input to the other of the source and the drain of the transistor 1209. The logic value of a signal output from the second terminal of the switch 1203 (the other of the source and the drain of the transistor 1213) is inverted by the logic element 1206, and the inverted signal is input to the circuit 1201 through the circuit 1220.

[0317]

In the example of FIG. 43, a signal output from the second terminal of the switch 1203 (the other of the source and the drain of the transistor 1213) is input to the circuit 1201 through the logic element 1206 and the circuit 1220; however, one embodiment of the present invention is not limited thereto. The signal output from the second terminal of the switch 1203 (the other of the source and the drain of the transistor 1213) may be input to the circuit 1201 without its logic value being inverted. For example, in the case where the circuit 1201 includes a node in which a signal obtained by inversion of the logic value of a signal input from the input terminal is retained, the signal output from the second terminal of the switch 1203 (the other of the source and the drain of the transistor 1213) can be input to the node.

[0318]

In FIG. 43, the transistors included in the memory element 1200 except for the transistor 1209 can each be a transistor in which a channel is formed in a film formed using a semiconductor other than an oxide semiconductor or in the substrate 1190. For example, the transistor can be a transistor whose channel is formed in a silicon film or a silicon substrate. Alternatively, all the transistors in the memory element 1200 may be a transistor in which a channel is formed in an oxide semiconductor. Further alternatively, in the memory element 1200, a transistor in which a channel is formed in an oxide semiconductor can be included besides the transistor 1209, and a transistor in which a channel is formed in a layer including a semiconductor other than an oxide semiconductor or the substrate 1190 can be used for the rest of the transistors.

[0319]

As the circuit 1201 in FIG. 43, for example, a flip-flop circuit can be used. As the logic element 1206, for example, an inverter or a clocked inverter can be used.

[0320]

In a period during which the memory element 1200 is not supplied with the power supply voltage, the semiconductor device of one embodiment of the present invention can retain data stored in the circuit 1201 by the capacitor 1208 which is provided in the circuit 1202.

[0321]

The off-state current of a transistor in which a channel is formed in an oxide

semiconductor is extremely low. For example, the off-state current of a transistor in which a channel is formed in an oxide semiconductor is significantly lower than that of a transistor in which a channel is formed in silicon having crystallinity. Thus, when the transistor is used as the transistor 1209, a signal held in the capacitor 1208 is retained for a long time also in a period during which the power supply voltage is not supplied to the memory element 1200. The memory element 1200 can accordingly retain the stored content (data) also in a period during which the supply of the power supply voltage is stopped.

[0322]

Since the above-described memory element performs pre-charge operation with the switch 1203 and the switch 1204, the time required for the circuit 1201 to retain original data again after the supply of the power supply voltage is restarted can be shortened.

[0323]

In the circuit 1202, a signal retained by the capacitor 1208 is input to the gate of the transistor 1210. Therefore, after supply of the power supply voltage to the memory element 1200 is restarted, the signal retained by the capacitor 1208 can be converted into the one corresponding to the state (the on state or the off state) of the transistor 1210 to be read from the circuit 1202. Consequently, an original signal can be accurately read even when a potential corresponding to the signal retained by the capacitor 1208 varies to some degree.

[0324]

By using the above-described memory element 1200 for a memory device such as a register or a cache memory included in a processor, data in the memory device can be prevented from being lost owing to the stop of the supply of the power supply voltage. Further, shortly after the supply of the power supply voltage is restarted, the memory element can be returned to the same state as that before the power supply is stopped. Therefore, the power supply can be stopped even for a short time in the processor or one or a plurality of logic circuits included in the processor. Accordingly, power consumption can be suppressed.

[0325]

Although the memory element 1200 is used in a CPU in this embodiment, the memory element 1200 can also be used in an LSI such as a digital signal processor (DSP), a custom LSI, or a programmable logic device (PLD), and a radio frequency (RF) tag.

[0326]

At least part of this embodiment can be implemented in combination with any of the embodiments described in this specification as appropriate.

[0327]

(Embodiment 8)

<Imaging device>

FIG. 44A is a top view illustrating an example of an imaging device 200 of one embodiment of the present invention. The imaging device 200 includes a pixel portion 210 and peripheral circuits for driving the pixel portion 210 (a peripheral circuit 260, a peripheral circuit 270, a peripheral circuit 280, and a peripheral circuit 290). The pixel portion 210 includes a plurality of pixels 211 arranged in a matrix with p rows and q columns (p and q are each a natural number greater than or equal to 2). The peripheral circuit 260, the peripheral circuit 270, the peripheral circuit 280, and the peripheral circuit 290 are each connected to a plurality of pixels 211, and a signal for driving the plurality of pixels 211 is supplied. In this specification and the like, in some cases, "a peripheral circuit" or "a driver circuit" indicates all of the peripheral circuits 260, 270, 280, and 290. For example, the peripheral circuit 260 can be regarded as part of the peripheral circuit.

[0328]

The imaging device 200 preferably includes a light source 291. The light source 291 can emit detection light P1.

[0329]

The peripheral circuit includes at least one of a logic circuit, a switch, a buffer, an amplifier circuit, and a converter circuit. The peripheral circuit may be formed over a substrate where the pixel portion 210 is formed. Alternatively, a semiconductor device such as an IC chip may be used as part or the whole of the peripheral circuit. Note that as the peripheral circuit, one or more of the peripheral circuits 260, 270, 280, and 290 may be omitted.

[0330]

As illustrated in FIG. 44B, the pixels 211 may be provided to be inclined in the pixel portion 210 included in the imaging device 200. When the pixels 211 are obliquely arranged, the distance between pixels (pitch) can be shortened in the row direction and the column direction. Accordingly, the quality of an image taken with the imaging device 200 can be improved.

[0331]

<Configuration Example 1 of Pixel>

The pixel 211 included in the imaging device 200 is formed with a plurality of subpixels 212, and each subpixel 212 is combined with a filter which transmits light with a specific wavelength band (color filter), whereby data for achieving color image display can be obtained.

[0332]

FIG. 45A is a top view showing an example of the pixel 211 with which a color image is obtained. The pixel 211 illustrated in FIG. 45A includes the subpixel 212 provided with a color

filter that transmits light with a red (R) wavelength band (also referred to as a subpixel 212R), a subpixel 212 provided with a color filter that transmits light with a green (G) wavelength band (also referred to as a subpixel 212G), and a subpixel 212 provided with a color filter that transmits light with a blue (B) wavelength band (also referred to as a subpixel 212B). The subpixel 212 can function as a photosensor.

[0333]

The subpixel 212 (the subpixel 212R, the subpixel 212G, and the subpixel 212B) is electrically connected to a wiring 231, a wiring 247, a wiring 248, a wiring 249, and a wiring 250. In addition, the subpixel 212R, the subpixel 212G, and the subpixel 212B are connected to respective wirings 253 which are independent from one another. In this specification and the like, for example, the wiring 248, the wiring 249, and the wiring 250 that are connected to the pixel 211 in the n-th row are referred to as a wiring 248[n], a wiring 249[n], and a wiring 250[n], respectively. For example, the wiring 253 connected to the pixel 211 in the m-th column is referred to as a wiring 253[m]. Note that in FIG. 45A, the wirings 253 connected to the subpixel 212R, the subpixel 212G, and the subpixel 212B in the pixel 211 in the m-th column are referred to as a wiring 253[m]R, a wiring 253[m]G, and a wiring 253[m]B. The subpixels 212 are electrically connected to the peripheral circuit through the above wirings.

[0334]

The imaging device 200 has a structure in which the subpixel 212 is electrically connected to the subpixel 212 in an adjacent pixel 211 that is provided with a color filter that transmits light with the same wavelength band as the subpixel 212, via a switch. FIG. 45B shows a connection example of the subpixels 212: the subpixel 212 in the pixel 211 arranged in an n-th (n is an integer greater than or equal to 1 and less than or equal to p) row and an m-th (m is an integer greater than or equal to 1 and less than or equal to q) column and the subpixel 212 in the adjacent pixel 211 arranged in an (n+1)-th row and the m-th column. In FIG. 45B, the subpixel 212R arranged in the n-th row and the m-th column and the subpixel 212R arranged in the (n+1)-th row and the m-th column are connected to each other via a switch 201. The subpixel 212G arranged in the n-th row and the m-th column and the subpixel 212G arranged in the (n+1)-th row and the m-th column are connected to each other via a switch 202. The subpixel 212B arranged in the n-th row and the m-th column and the subpixel 212B arranged in the (n+1)-th row and the m-th column are connected to each other via a switch 203.

[0335]

The color filter used in the subpixel 212 is not limited to red (R), green (G), and blue (B) color filters, and color filters that transmit light of cyan (C), yellow (Y), and magenta (M) may be used. By provision of the subpixels 212 that sense light with three different wavelength

bands in one pixel 211, a full-color image can be obtained.

[0336]

The pixel 211 including the subpixel 212 provided with a color filter transmitting yellow (Y) light may be provided, in addition to the subpixels 212 provided with the color filters transmitting red (R), green (G), and blue (B) light. The pixel 211 including the subpixel 212 provided with a color filter transmitting blue (B) light may be provided, in addition to the subpixels 212 provided with the color filters transmitting cyan (C), yellow (Y), and magenta (M) light. When the subpixels 212 sensing light with four different wavelength bands are provided in one pixel 211, the reproducibility of colors of an obtained image can be increased.

[0337]

For example, in FIG. 45A, in regard to the subpixel 212 sensing a red wavelength band, the subpixel 212 sensing a green wavelength band, and the subpixel 212 sensing a blue wavelength band, the pixel number ratio (or the light receiving area ratio) thereof is not necessarily 1:1:1. For example, it is possible to employ the Bayer arrangement, in which the ratio of the number of pixels (the ratio of light-receiving areas) is set to red : green : blue = 1:2:1. Alternatively, the pixel number ratio (the ratio of light receiving area) of red and green to blue may be 1:6:1.

[0338]

Although the number of subpixels 212 provided in the pixel 211 may be one, two or more subpixels are preferably provided. For example, when two or more subpixels 212 sensing the same wavelength band are provided, the redundancy is increased, and the reliability of the imaging device 200 can be increased.

[0339]

When an infrared (IR) filter that transmits infrared light and absorbs or reflects visible light is used as the filter, the imaging device 200 that senses infrared light can be achieved.

[0340]

Furthermore, when a neutral density (ND) filter (dark filter) is used, output saturation which occurs when a large amount of light enters a photoelectric conversion element (light-receiving element) can be prevented. With a combination of ND filters with different dimming capabilities, the dynamic range of the imaging device can be increased.

[0341]

Besides the above-described filter, the pixel 211 may be provided with a lens. An arrangement example of the pixel 211, a filter 254, and a lens 255 is described with cross-sectional views in FIGS. 46A and 46B. With the lens 255, the photoelectric conversion element provided in the subpixel 212 can receive incident light efficiently. Specifically, as

illustrated in FIG. 46A, light 256 enters a photoelectric conversion element 220 through the lens 255, the filter 254 (a filter 254R, a filter 254G, and a filter 254B), a pixel circuit 230, and the like which are provided in the pixel 211.

[0342]

However, part of the light 256 indicated by arrows might be blocked by some wirings 257 as indicated by a region surrounded with dashed-dotted lines. Thus, a preferable structure is such that the lens 255 and the filter 254 are provided on the photoelectric conversion element 220 side as illustrated in FIG. 46B, whereby the photoelectric conversion element 220 can efficiently receive the light 256. When the light 256 enters the photoelectric conversion element 220 from the photoelectric conversion element 220 side, the imaging device 200 with high sensitivity can be provided.

[0343]

As the photoelectric conversion element 220 illustrated in FIGS. 46A and 46B, a photoelectric conversion element in which a p-n junction or a p-i-n junction is formed may be used.

[0344]

The photoelectric conversion element 220 may be formed using a substance that has a function of absorbing a radiation and generating electric charges. Examples of the substance that has a function of absorbing a radiation and generating electric charges include selenium, lead iodide, mercury iodide, gallium arsenide, cadmium telluride, and cadmium zinc alloy.

[0345]

For example, when selenium is used for the photoelectric conversion element 220, the photoelectric conversion element 220 can have a light absorption coefficient in a wide wavelength range, such as visible light, ultraviolet light, infrared light, X-rays, and gamma rays.

[0346]

One pixel 211 included in the imaging device 200 may include the subpixel 212 with a first filter in addition to the subpixel 212 illustrated in FIGS. 46A and 46B.

[0347]

<Configuration Example 2 of Pixel>

An example of a pixel including a transistor using silicon and a transistor using an oxide semiconductor according to one embodiment of the present invention is described below.

[0348]

FIGS. 47A and 47B are each a cross-sectional view of an element included in an imaging device.

[0349]

The imaging device illustrated in FIG. 47A includes a transistor 351 including silicon over a silicon substrate 300, transistors 353 and 354 which include an oxide semiconductor and are stacked over the transistor 351, and a photodiode 360 provided in a silicon substrate 300 and including an anode 361 and a cathode 362. The transistors and the photodiode 360 are electrically connected to various plugs 370 and wirings 371. In addition, an anode 361 of the photodiode 360 is electrically connected to the plug 370 through a low-resistance region 363

[0350]

The imaging device includes a layer 305 including the transistor 351 provided on the silicon substrate 300 and the photodiode 360 provided in the silicon substrate 300, a layer 320 which is in contact with the layer 305 and includes the wirings 371, a layer 331 which is in contact with the layer 320 and includes the transistors 353 and 354, and a layer 340 which is in contact with the layer 331 and includes a wiring 372 and a wiring 373.

[0351]

Note that in the example of cross-sectional view in FIG. 47A, a light-receiving surface of the photodiode 360 is provided on the side opposite to a surface of the silicon substrate 300 where the transistor 351 is formed. With the structure, an optical path can be obtained without the influence by the transistors or wirings, and therefore, a pixel with a high aperture ratio can be formed. Thus, a pixel with a high aperture ratio can be formed. Note that the light-receiving surface of the photodiode 360 can be the same as the surface where the transistor 351 is formed.

[0352]

In the case where a pixel is formed with use of only transistors using an oxide semiconductor, the layer 305 may include the transistor using an oxide semiconductor. Alternatively, the layer 305 may be omitted, and the pixel may include only transistors using an oxide semiconductor.

[0353]

In addition, in the cross-sectional view in FIG. 47A, the photodiode 360 in the layer 305 and the transistor in the layer 331 can be formed so as to overlap with each other. Thus, the degree of integration of pixels can be increased. In other words, the resolution of the imaging device can be increased.

[0354]

An imaging device shown in FIG. 47B includes a photodiode 365 in the layer 340 and over the transistor. In FIG. 47B, the layer 305 includes the transistor 351 and a transistor 352 using silicon, the layer 320 includes the wiring 371, the layer 331 includes the transistors 353 and 354 using an oxide semiconductor layer, the layer 340 includes the photodiode 365. The photodiode 365 includes a semiconductor layer 366, a semiconductor layer 367, and a

semiconductor layer 368, and is electrically connected to the wiring 373 and a wiring 374 through the plug 370.

[0355]

The element structure shown in FIG. 47B can increase the aperture ratio.

[0356]

Alternatively, a PIN diode element formed using an amorphous silicon film, a microcrystalline silicon film, or the like may be used as the photodiode 365. In the photodiode 365, an n-type semiconductor layer 368, an i-type semiconductor layer 367, and a p-type semiconductor layer 366 are stacked in this order. The i-type semiconductor layer 367 is preferably formed using amorphous silicon. The p-type semiconductor layer 366 and the n-type semiconductor layer 368 can each be formed using amorphous silicon, microcrystalline silicon, or the like which includes a dopant imparting the corresponding conductivity type. A photodiode in which the photodiode 365 is formed using amorphous silicon has high sensitivity in a visible light wavelength region, and therefore can easily sense weak visible light.

[0357]

Here, an insulator 380 is provided between the layer 305 including the transistor 351 and the photodiode 360 and the layer 331 including the transistors 353 and 354. However, there is no limitation on the position of the insulator 380.

[0358]

Hydrogen in an insulator provided in the vicinity of a channel formation region of the transistor 351 terminates dangling bonds of silicon; accordingly, the reliability of the transistor 351 can be improved. In contrast, hydrogen in the insulator provided in the vicinity of the transistor 353, the transistor 354, and the like becomes one of factors generating a carrier in the oxide semiconductor. Thus, the hydrogen may cause a reduction of the reliability of the transistor 354, the transistor 354, and the like. Therefore, in the case where the transistor using an oxide semiconductor is provided over the transistor using a silicon-based semiconductor, it is preferable that the insulator 380 having a function of blocking hydrogen be provided between the transistors. When the hydrogen is confined below the insulator 380, the reliability of the transistor 351 can be improved. In addition, the hydrogen can be prevented from being diffused from a part below the insulator 380 to a part above the insulator 380; thus, the reliability of the transistor 353, the transistor 354, and the like can be increased. It is preferable to form the insulator 381 over the transistors 353 and 354 because oxygen diffusion can be prevented in the oxide semiconductor.

[0359]

At least part of this embodiment can be implemented in combination with any of the

embodiments described in this specification as appropriate.

[0360]

(Embodiment 9)

<RF tag>

In this embodiment, an RF tag that includes the transistor described in the above embodiments or the memory device described in the above embodiment is described with reference to FIG. 48.

[0361]

The RF tag of this embodiment includes a memory circuit, stores necessary data in the memory circuit, and transmits and receives data to/from the outside by using contactless means, for example, wireless communication. With these features, the RF tag can be used for an individual authentication system in which an object or the like is recognized by reading the individual information, for example. Note that the RF tag is required to have extremely high reliability in order to be used for this purpose.

[0362]

A configuration of the RF tag will be described with reference to FIG. 48. FIG. 48 is a block diagram illustrating a configuration example of an RF tag.

[0363]

As shown in FIG. 48, an RF tag 800 includes an antenna 804 which receives a radio signal 803 that is transmitted from an antenna 802 connected to a communication device 801 (also referred to as an interrogator, a reader/writer, or the like). The RF tag 800 includes a rectifier circuit 805, a constant voltage circuit 806, a demodulation circuit 807, a modulation circuit 808, a logic circuit 809, a memory circuit 810, and a ROM 811. A transistor having a rectifying function included in the demodulation circuit 807 may be formed using a material which enables a reverse current to be low enough, for example, an oxide semiconductor. This can suppress the phenomenon of a rectifying function becoming weaker due to generation of a reverse current and prevent saturation of the output from the demodulation circuit. In other words, the input to the demodulation circuit and the output from the demodulation circuit can have a relation closer to a linear relation. Note that data transmission methods are roughly classified into the following three methods: an electromagnetic coupling method in which a pair of coils is provided so as to face each other and communicates with each other by mutual induction, an electromagnetic induction method in which communication is performed using an induction field, and a radio wave method in which communication is performed using a radio wave. Any of these methods can be used in the RF tag 800 described in this embodiment.

[0364]

Next, a structure of each circuit will be described. The antenna 804 exchanges the radio signal 803 with the antenna 802 which is connected to the communication device 801. The rectifier circuit 805 generates an input potential by rectification, for example, half-wave voltage doubler rectification of an input alternating signal generated by reception of a radio signal at the antenna 804 and smoothing of the rectified signal with a capacitor provided in a later stage in the rectifier circuit 805. Note that a limiter circuit may be provided on an input side or an output side of the rectifier circuit 805. The limiter circuit controls electric power so that electric power which is higher than or equal to certain electric power is not input to a circuit in a later stage if the amplitude of the input alternating signal is high and an internal generation voltage is high.

[0365]

The constant voltage circuit 806 generates a stable power supply voltage from an input potential and supplies it to each circuit. Note that the constant voltage circuit 806 may include a reset signal generation circuit. The reset signal generation circuit is a circuit which generates a reset signal of the logic circuit 809 by utilizing rise of the stable power supply voltage.

[0366]

The demodulation circuit 807 demodulates the input alternating signal by envelope detection and generates the demodulated signal. Further, the modulation circuit 808 performs modulation in accordance with data to be output from the antenna 804.

[0367]

The logic circuit 809 analyzes and processes the demodulated signal. The memory circuit 810 holds the input data and includes a row decoder, a column decoder, a memory region, and the like. Further, the ROM 811 stores an identification number (ID) or the like and outputs it in accordance with processing.

[0368]

Note that the decision whether each circuit described above is provided or not can be made as appropriate as needed.

[0369]

Here, the memory circuit described in the above embodiment can be used as the memory circuit 810. Since the memory circuit of one embodiment of the present invention can retain data even when not powered, the memory circuit can be favorably used for an RF tag. Furthermore, the memory circuit of one embodiment of the present invention needs power (voltage) needed for data writing significantly lower than that needed in a conventional nonvolatile memory; thus, it is possible to prevent a difference between the maximum communication range in data reading and that in data writing. Furthermore, it is possible to

suppress malfunction or incorrect writing which is caused by power shortage in data writing.

[0370]

Since the memory circuit of one embodiment of the present invention can be used as a nonvolatile memory, it can also be used as the ROM 811. In this case, it is preferable that a manufacturer separately prepare a command for writing data to the ROM 811 so that a user cannot rewrite data freely. Since the manufacturer gives identification numbers before shipment and then starts shipment of products, instead of putting identification numbers to all the manufactured RF tags, it is possible to put identification numbers to only good products to be shipped. Thus, the identification numbers of the shipped products are in series and customer management corresponding to the shipped products is easily performed.

[0371]

This embodiment can be combined as appropriate with any of the other embodiments in this specification.

[0372]

(Embodiment 10)

<Display device>

A display device of one embodiment of the present invention is described below with reference to FIGS. 49A to 49C and FIGS. 50A and 50B.

[0373]

Examples of a display element provided in the display device include a liquid crystal element (also referred to as a liquid crystal display element) and a light-emitting element (also referred to as a light-emitting display element). The light-emitting element includes, in its category, an element whose luminance is controlled by a current or voltage, and specifically includes, in its category, an inorganic electroluminescent (EL) element, an organic EL element, and the like. A display device including an EL element (EL display device) and a display device including a liquid crystal element (liquid crystal display device) are described below as examples of the display device.

[0374]

Note that the display device described below includes in its category a panel in which a display element is sealed and a module in which an IC such as a controller is mounted on the panel.

[0375]

The display device described below refers to an image display device or a light source (including a lighting device). The display device includes any of the following modules: a module provided with a connector such as an FPC or TCP; a module in which a printed wiring

board is provided at the end of TCP; and a module in which an integrated circuit (IC) is mounted directly on a display element by a COG method.

[0376]

FIGS. 49A to 49C illustrate an example of an EL display device of one embodiment of the present invention. FIG. 49A is a circuit diagram of a pixel in an EL display device. FIG. 49B is a top view showing the whole of the EL display device. FIG. 49C is a cross-sectional view taken along part of dashed-dotted line M-N in FIG. 49B.

[0377]

FIG. 49A illustrates an example of a circuit diagram of a pixel used in an EL display device.

[0378]

Note that in this specification and the like, it might be possible for those skilled in the art to constitute one embodiment of the invention even when portions to which all the terminals of an active element (e.g., a transistor or a diode), a passive element (e.g., a capacitor or a resistor), or the like are connected are not specified. In other words, one embodiment of the invention can be clear even when connection portions are not specified. Further, in the case where a connection portion is disclosed in this specification and the like, it can be determined that one embodiment of the invention in which a connection portion is not specified is disclosed in this specification and the like, in some cases. Particularly in the case where the number of portions to which a terminal is connected might be more than one, it is not necessary to specify the portions to which the terminal is connected. Therefore, it might be possible to constitute one embodiment of the invention by specifying only portions to which some of terminals of an active element (e.g., a transistor or a diode), a passive element (e.g., a capacitor or a resistor), or the like are connected.

[0379]

Note that in this specification and the like, it might be possible for those skilled in the art to specify the invention when at least the connection portion of a circuit is specified. Alternatively, it might be possible for those skilled in the art to specify the invention when at least a function of a circuit is specified. In other words, when a function of a circuit is specified, one embodiment of the present invention can be clear. Further, it can be determined that one embodiment of the present invention whose function is specified is disclosed in this specification and the like. Therefore, when a connection portion of a circuit is specified, the circuit is disclosed as one embodiment of the invention even when a function is not specified, and one embodiment of the invention can be constituted. Alternatively, when a function of a circuit is specified, the circuit is disclosed as one embodiment of the invention even when a connection

portion is not specified, and one embodiment of the invention can be constituted.

[0380]

The EL display device illustrated in FIG. 49A includes a switching element 743, a transistor 741, a capacitor 742, and a light-emitting element 719.

[0381]

Note that FIG. 49A and the like each illustrate an example of a circuit structure; therefore, a transistor can be provided additionally. In contrast, for each node in FIG. 49A and the like, it is possible not to provide an additional transistor, switch, passive element, or the like.

[0382]

A gate of the transistor 741 is electrically connected to one terminal of the switching element 743 and one electrode of the capacitor 742. A source of the transistor 741 is electrically connected to the other electrode of the capacitor 742 and one electrode of the light-emitting element 719. A power supply potential VDD is supplied to a drain of the transistor 741. The other terminal of the switching element 743 is electrically connected to a signal line 744. A constant potential is supplied to the other electrode of the light-emitting element 719. The constant potential is a ground potential GND or a potential lower than the ground potential GND.

[0383]

It is preferable to use a transistor as the switching element 743. When the transistor is used as the switching element, the area of a pixel can be reduced, so that the EL display device can have high resolution. As the switching element 743, a transistor formed through the same step as the transistor 741 can be used, so that EL display devices can be manufactured with high productivity. Note that as the transistor 741 and/or the switching element 743, the transistor illustrated in FIGS. 1A to 1C can be used, for example.

[0384]

FIG. 49B is a top view of the EL display device. The EL display device includes a substrate 700, a substrate 750, a sealant 734, a driver circuit 735, a driver circuit 736, a pixel 737, and an FPC 732. The sealant 734 is provided between the substrate 700 and the substrate 750 so as to surround the pixel 737, the driver circuit 735, and the driver circuit 736. Note that the driver circuit 735 and/or the driver circuit 736 may be provided outside the sealant 734.

[0385]

FIG. 49C is a cross-sectional view of the EL display device taken along part of dashed-dotted line M-N in FIG. 49B.

[0386]

FIG. 49C illustrates a structure of the transistor 741 including an insulator 712 over the

substrate700; a conductor 704a; an insulator 706a that is over the insulator 712a and the conductor 704a and partly overlaps with the conductor 704a; a semiconductor 706b over the insulator 706a; conductors 716a1 and 716a2 in contact with a top surface of the semiconductor 706b; an insulator 710 over the conductors 716a1 and 716a2; an insulator 706c over the semiconductor 706b; an insulator 718b over the insulator 706c; and a conductor 714 that is over the insulator 718b and overlaps with the semiconductor 706b. Note that the structure of the transistor 741 is just an example; the transistor 741 may have a structure different from that illustrated in FIG. 49C.

[0387]

In the transistor 741 illustrated in FIG. 49C, the conductor 704a serves as a gate electrode, the insulator 712a serves as a gate insulator, the conductor 716a1 serves as a source electrode, the conductor 716a2 serves as a drain electrode, the insulator 718b serves as a gate insulator, and the conductor 714a serves as a gate electrode. Note that in some cases, electric characteristics of the insulator 706a, the semiconductor 706b, and the insulator 706c change if light enters the insulator 706a, the semiconductor 706b, and the insulator 706c. To prevent this, it is preferable that one or more of the conductor 704a, the conductor 716a1, the conductor 716a2, and the conductor 714a have a light-blocking property.

[0388]

FIG. 49C illustrates a structure of the capacitor 742 including an insulator 706d that is over a conductor 704b provided over the substrate 700 and partly overlaps with the conductor 704b; a semiconductor 706e over the insulator 706d; conductors 716a3 and 716a4 in contact with a top surface of the semiconductor 706e; the insulator 710 over the conductors 716a3 and 716a4; an insulator 706f over the semiconductor 706e; the insulator 718b over the insulator 706f; and a conductor 714b that is over the insulator 718b and overlaps with the semiconductor 706e.

[0389]

In the capacitor 742, the conductor 704b serves as one electrode and the conductor 714b serves as the other electrode.

[0390]

Thus, the capacitor 742 can be formed using a film of the transistor 741. The conductor 704a and the conductor 704b are preferably conductors of the same kind, in which case the conductor 704a and the conductor 704b can be formed through the same step. Furthermore, the conductor 714a and the conductor 714b are preferably conductors of the same kind, in which case the conductor 714a and the conductor 714b can be formed through the same step.

[0391]

The capacitor 742 illustrated in FIG. 49C has a large capacitance per area occupied by the capacitor. Therefore, the EL display device illustrated in FIG. 49C has high display quality. Note that the structure of the capacitor 742 is just an example and may be different from that illustrated in FIG. 49C.

[0392]

An insulator 728 is provided over the transistor 741 and the capacitor 742, and an insulator 720 is provided over the insulator 728. Here, the insulator 728 and the insulator 720 may have an opening reaching the conductor 716a1 that serves as the source electrode of the transistor 741. A conductor 781 is provided over the insulator 720. The conductor 781 may be electrically connected to the transistor 741 through the opening in the insulator 728 and the insulator 720.

[0393]

A partition wall 784 having an opening reaching the conductor 781 is provided over the conductor 781. A light-emitting layer 782 in contact with the conductor 781 through the opening provided in the partition wall 784 is provided over the partition wall 784. A conductor 783 is provided over the light-emitting layer 782. A region where the conductor 781, the light-emitting layer 782, and the conductor 783 overlap with one another serves as the light-emitting element 719. In FIG. 49C, the FPC 732 is connected to the wiring 733a via a terminal 731. Note that the wiring 733a may be formed using the same kind of conductor as the conductor of the transistor 741 or using the same kind of semiconductor as the semiconductor of the transistor 741.

[0394]

So far, examples of the EL display device are described. Next, an example of a liquid crystal display device is described.

[0395]

FIG. 50A is a circuit diagram showing a structural example of a pixel of the liquid crystal display device. A pixel illustrated in FIG. 50A includes a transistor 751, a capacitor 752, and an element (liquid crystal element) 753 in which a space between a pair of electrodes is filled with a liquid crystal.

[0396]

One of a source and a drain of the transistor 751 is electrically connected to a signal line 755, and a gate of the transistor 751 is electrically connected to a scan line 754.

[0397]

One electrode of the capacitor 752 is electrically connected to the other of the source and the drain of the transistor 751, and the other electrode of the capacitor 752 is electrically

connected to a wiring for supplying a common potential.

[0398]

One electrode of the liquid crystal element 753 is electrically connected to the other of the source and the drain of the transistor 751, and the other electrode of the liquid crystal element 753 is electrically connected to a wiring to which a common potential is supplied. The common potential supplied to the wiring electrically connected to the other electrode of the capacitor 752 may be different from that supplied to the other electrode of the liquid crystal element 753.

[0399]

Note the description of the liquid crystal display device is made on the assumption that the top view of the liquid crystal display device is similar to that of the EL display device. FIG. 50B is a cross-sectional view of the liquid crystal display device taken along dashed-dotted line M-N in FIG. 49B. In FIG. 50B, the FPC 732 is connected to the wiring 733a via the terminal 731. Note that the wiring 733a may be formed using the same kind of conductor as the conductor of the transistor 751 or using the same kind of semiconductor as the semiconductor of the transistor 751.

[0400]

For the transistor 751, the description of the transistor 741 is referred to. For the capacitor 752, the description of the capacitor 742 is referred to. Note that the structure of the capacitor 752 in FIG. 50B corresponds to, but is not limited to, the structure of the capacitor 742 in FIG. 49C.

[0401]

Note that in the case where an oxide semiconductor is used as the semiconductor of the transistor 751, the off-state current of the transistor 751 can be extremely small. Therefore, an electric charge held in the capacitor 752 is unlikely to leak, so that the voltage applied to the liquid crystal element 753 can be maintained for a long time. Accordingly, the transistor 751 can be kept off during a period in which moving images with few motions or a still image are/is displayed, whereby power for the operation of the transistor 751 can be saved in that period; accordingly a liquid crystal display device with low power consumption can be provided. Furthermore, the area occupied by the capacitor 752 can be reduced; thus, a liquid crystal display device with a high aperture ratio or a high-resolution liquid crystal display device can be provided.

[0402]

An insulator 721 is provided over the transistor 751 and the capacitor 752. The insulator 721 has an opening portion reaching the transistor 751. A conductor 791 is provided

over the insulator 721. The conductor 791 is electrically connected to the transistor 751 through the opening portion in the insulator 721.

[0403]

An insulator 792 serving as an alignment film is provided over the conductor 791. A liquid crystal layer 793 is provided over the insulator 792. An insulator 794 serving as an alignment film is provided over the liquid crystal layer 793. A spacer 795 is provided over the insulator 794. A conductor 796 is provided over the spacer 795 and the insulator 794. A substrate 797 is provided over the conductor 796.

[0404]

Owing to the above-described structure, a display device including a capacitor occupying a small area, a display device with high display quality, or a high-resolution display device can be provided.

[0405]

For example, in this specification and the like, a display element, a display device which is a device including a display element, a light-emitting element, and a light-emitting device which is a device including a light-emitting element can employ various modes or can include various elements. The display element, the display device, the light-emitting element, or the light-emitting device includes at least one of an electroluminescence (EL) element (e.g., an EL element including organic and inorganic materials, an organic EL element, or an inorganic EL element), an LED (e.g., a white LED, a red LED, a green LED, or a blue LED), a transistor (a transistor that emits light depending on current), an electron emitter, a liquid crystal element, electronic ink, an electrophoretic element, a grating light valve (GLV), a plasma display panel (PDP), a display element using micro electro mechanical systems (MEMS), a digital micromirror device (DMD), a digital micro shutter (DMS), an interferometric modulator display (IMOD) element, a MEMS shutter display element, an optical-interference-type MEMS display element, an electrowetting element, a piezoelectric ceramic display, a display element including a carbon nanotube, and the like. Other than the above, display media whose contrast, luminance, reflectivity, transmittance, or the like is changed by electrical or magnetic effect may be included.

[0406]

Note that examples of display devices having EL elements include an EL display. Examples of a display device including an electron emitter include a field emission display (FED), an SED-type flat panel display (SED: surface-conduction electron-emitter display), and the like. Examples of display devices including liquid crystal elements include a liquid crystal display (e.g., a transmissive liquid crystal display, a transflective liquid crystal display, a

reflective liquid crystal display, a direct-view liquid crystal display, or a projection liquid crystal display). Examples of a display devices having electronic ink or an electrophoretic element include electronic paper. In the case of a transflective liquid crystal display or a reflective liquid crystal display, some of or all of pixel electrodes function as reflective electrodes. For example, some or all of pixel electrodes are formed to contain aluminum, silver, or the like. In such a case, a memory circuit such as an SRAM can be provided under the reflective electrodes, leading to lower power consumption.

[0407]

Note that in the case of using an LED, graphene or graphite may be provided under an electrode or a nitride semiconductor of the LED. Graphene or graphite may be a multilayer film in which a plurality of layers are stacked. As described above, provision of graphene or graphite enables easy formation of a nitride semiconductor thereover, such as an n-type GaN semiconductor including crystals. Furthermore, a p-type GaN semiconductor including crystals or the like can be provided thereover, and thus the LED can be formed. Note that an AlN layer may be provided between the n-type GaN semiconductor including crystals and graphene or graphite. The GaN semiconductors included in the LED may be formed by MOCVD. Note that when the graphene is provided, the GaN semiconductors included in the LED can also be formed by a sputtering method.

[0408]

This embodiment can be combined as appropriate with any of the other embodiments in this specification.

[0409]

(Embodiment 11)

In this embodiment, a display module using a semiconductor device of one embodiment of the present invention is described with reference to FIG. 51.

[0410]

<Display module>

In a display module 6000 in FIG. 51, a touch panel 6004 connected to an FPC 6003, a display panel 6006 connected to an FPC 6005, a backlight unit 6007, a frame 6009, a printed board 6010, and a battery 6011 are provided between an upper cover 6001 and a lower cover 6002. Note that the backlight unit 6007, the battery 6011, the touch panel 6004, and the like are not provided in some cases.

[0411]

The semiconductor device of one embodiment of the present invention can be used for, for example, the display panel 6006 and an integrated circuit mounted on a printed circuit board.

[0412]

The shapes and sizes of the upper cover 6001 and the lower cover 6002 can be changed as appropriate in accordance with the sizes of the touch panel 6004 and the display panel 6006.

[0413]

The touch panel 6004 can be a resistive touch panel or a capacitive touch panel and may be formed to overlap with the display panel 6006. A counter substrate (sealing substrate) of the display panel 6006 can have a touch panel function. A photosensor may be provided in each pixel of the display panel 6006 so that an optical touch panel function is added. An electrode for a touch sensor may be provided in each pixel of the display panel 6006 so that a capacitive touch panel function is added.

[0414]

The backlight unit 6007 includes a light source 6008. The light source 6008 may be provided at an end portion of the backlight unit 6007 and a light diffusing plate may be used.

[0415]

The frame 6009 protects the display panel 6006 and also functions as an electromagnetic shield for blocking electromagnetic waves generated from the printed board 6010. The frame 6009 may function as a radiator plate.

[0416]

The printed board 6010 has a power supply circuit and a signal processing circuit for outputting a video signal and a clock signal. As a power source for supplying power to the power supply circuit, an external commercial power source or the battery 6011 provided separately may be used. Note that the battery 6011 is not necessary in the case where a commercial power source is used.

[0417]

The display module 6000 can be additionally provided with a member such as a polarizing plate, a retardation plate, or a prism sheet.

[0418]

This embodiment can be combined as appropriate with any of the other embodiments in this specification.

[0419]

(Embodiment 12)

<Package using a lead frame interposer>

FIG. 52A is a perspective view illustrating a cross-sectional structure of a package using a lead frame interposer. In the package illustrated in FIG. 52A, a chip 551 corresponding to the semiconductor device of one embodiment of the present invention is connected to a terminal 552

over an interposer 550 by wire bonding. The terminal 552 is placed on a surface of the interposer 550 on which the chip 551 is mounted. The chip 551 may be sealed by a mold resin 553, in which case the chip 551 is sealed such that part of each of the terminals 552 is exposed.

[0420]

FIG. 52B illustrates the structure of a module of an electronic device (mobile phone) in which a package is mounted on a circuit board. In the module of the mobile phone in FIG. 52B, a package 602 and a battery 604 are mounted on a printed wiring board 601. The printed wiring board 601 is mounted on a panel 600 including a display element by an FPC 603.

[0421]

This embodiment can be combined as appropriate with any of the other embodiments in this specification.

[0422]

(Embodiment 13)

In this embodiment, electronic devices and lighting devices of one embodiment of the present invention will be described with reference to drawings.

[0423]

<Electronic device>

Electronic devices and lighting devices can be fabricated using the semiconductor device of one embodiment of the present invention. In addition, highly reliable electronic devices and lighting devices can be fabricated using the semiconductor device of one embodiment of the present invention. Furthermore, electronic devices and lighting devices including touch sensors with improved detection sensitivity can be fabricated using the semiconductor device of one embodiment of the present invention.

[0424]

Examples of electronic devices include a television set (also referred to as a television or a television receiver), a monitor of a computer or the like, a digital camera, a digital video camera, a digital photo frame, a mobile phone (also referred to as a mobile phone device), a portable game machine, a portable information terminal, an audio reproducing device, a large game machine such as a pinball machine, and the like.

[0425]

In the case of having flexibility, the light-emitting device or lighting device of one embodiment of the present invention can be incorporated along a curved inside/outside wall surface of a house or a building or a curved interior/exterior surface of a car.

[0426]

Furthermore, the electronic device of one embodiment of the present invention may

include a secondary battery. It is preferable that the secondary battery be capable of being charged by non-contact power transmission.

[0427]

As examples of the secondary battery, a lithium ion secondary battery such as a lithium polymer battery (lithium ion polymer battery) using a gel electrolyte, a lithium ion battery, a nickel-hydride battery, a nickel-cadmium battery, an organic radical battery, a lead-acid battery, an air secondary battery, a nickel-zinc battery, and a silver-zinc battery can be given.

[0428]

The electronic device of one embodiment of the present invention may include an antenna. When a signal is received by the antenna, the electronic device can display an image, data, or the like on a display portion. When the electronic device includes a secondary battery, the antenna may be used for contactless power transmission.

[0429]

FIG. 53A illustrates a portable game machine including a housing 7101, a housing 7102, a display portion 7103, a display portion 7104, a microphone 7105, speakers 7106, an operation key 7107, a stylus 7108, and the like. The semiconductor device of one embodiment of the present invention can be used for an integrated circuit, a CPU, or the like incorporated in the housing 7101. When the light-emitting device according of one embodiment of the present invention is used as the display portion 7103 or 7104, it is possible to provide a user-friendly portable game machine with quality that hardly deteriorates. Although the portable game machine illustrated in FIG. 53A includes two display portions, the display portion 7103 and the display portion 7104, the number of display portions included in the portable game machine is not limited to two.

[0430]

FIG. 53B illustrates a smart watch, which includes a housing 7302, a display portion 7304, operation buttons 7311 and 7312, a connection terminal 7313, a band 7321, a clasp 7322, and the like. The semiconductor device of one embodiment of the present invention can be used for a memory, a CPU, or the like incorporated in the housing 7302.

[0431]

FIG. 53C illustrates a portable information terminal, which includes a display portion 7502 incorporated in a housing 7501, operation buttons 7503, an external connection port 7504, a speaker 7505, a microphone 7506, and the like. The semiconductor device of one embodiment of the present invention can be used for a mobile memory, a CPU, or the like incorporated in the housing 7501. Note that the display portion 7502 is small- or medium-sized but can perform full high vision, 4k, or 8k display because it has greatly high definition;

therefore, a significantly clear image can be obtained.

[0432]

FIG. 53D illustrates a video camera, which includes a first housing 7701, a second housing 7702, a display portion 7703, operation keys 7704, a lens 7705, a joint 7706, and the like. The operation keys 7704 and the lens 7705 are provided for the first housing 7701, and the display portion 7703 is provided for the second housing 7702. The first housing 7701 and the second housing 7702 are connected to each other with the joint 7706, and the angle between the first housing 7701 and the second housing 7702 can be changed with the joint 7706. Images displayed on the display portion 7703 may be switched in accordance with the angle at the joint 7706 between the first housing 7701 and the second housing 7702. The imaging device in one embodiment of the present invention can be provided in a focus position of the lens 7705. The semiconductor device of one embodiment of the present invention can be used for an integrated circuit, a CPU, or the like incorporated in the first housing 7701.

[0433]

FIG. 53E illustrates a digital signage including a display portion 7922 provided on a utility pole 7921. The display device of one embodiment of the present invention can be used for a control circuit of the display portion 7922.

[0434]

FIG. 54A illustrates a notebook personal computer, which includes a housing 8121, a display portion 8122, a keyboard 8123, a pointing device 8124, and the like. The semiconductor device of one embodiment of the present invention can be used for a CPU, a memory, or the like incorporated in the housing 8121. Note that the display portion 8122 is small- or medium-sized but can perform 8k display because it has greatly high definition; therefore, a significantly clear image can be obtained.

[0435]

FIG. 54B is an external view of an automobile 9700. FIG. 54C illustrates a driver's seat of the automobile 9700. The automobile 9700 includes a car body 9701, wheels 9702, a dashboard 9703, lights 9704, and the like. The semiconductor device of one embodiment of the present invention can be used in a display portion and a control integrated circuit of the automobile 9700. For example, the semiconductor device of one embodiment of the present invention can be used in display portions 9710 to 9715 illustrated in FIG. 54C.

[0436]

The display portion 9710 and the display portion 9711 are display devices or input/output devices provided in an automobile windshield. The display device or input/output device of one embodiment of the present invention can be a see-through display device or

input/output device, through which the opposite side can be seen, by using a light-transmitting conductive material for its electrodes. Such a see-through display device or input/output device does not hinder driver's vision during the driving of the automobile 9700. Therefore, the display device or input/output device of one embodiment of the present invention can be provided in the windshield of the automobile 9700. Note that in the case where a transistor or the like for driving the display device or input/output device is provided in the display device or input/output device, a transistor having light-transmitting properties, such as an organic transistor using an organic semiconductor material or a transistor using an oxide semiconductor, is preferably used.

[0437]

The display portion 9712 is a display device provided on a pillar portion. For example, an image taken by an imaging unit provided in the car body is displayed on the display portion 9712, whereby the view hindered by the pillar portion can be compensated. The display portion 9713 is a display device provided on the dashboard. For example, an image taken by an imaging unit provided in the car body is displayed on the display portion 9713, whereby the view hindered by the dashboard can be compensated. That is, by displaying an image taken by an imaging unit provided on the outside of the automobile, blind areas can be eliminated and safety can be increased. Displaying an image to compensate for the area which a driver cannot see, makes it possible for the driver to confirm safety easily and comfortably.

[0438]

FIG. 54D illustrates the inside of a car in which a bench seat is used as a driver seat and a front passenger seat. A display portion 9721 is a display device or input/output device provided in a door portion. For example, an image taken by an imaging unit provided in the car body is displayed on the display portion 9721, whereby the view hindered by the door can be compensated. A display portion 9722 is a display device provided in a steering wheel. A display portion 9723 is a display device provided in the middle of a seating face of the bench seat. Note that the display device can be used as a seat heater by providing the display device on the seating face or backrest and by using heat generation of the display device as a heat source.

[0439]

The display portion 9714, the display portion 9715, and the display portion 9722 can display a variety of kinds of information such as navigation data, a speedometer, a tachometer, a mileage, a fuel meter, a gearshift indicator, and air-condition setting. The content, layout, or the like of the display on the display portions can be changed freely by a user as appropriate. The information listed above can also be displayed on the display portions 9710 to 9713, 9721, and

9723. The display portions 9710 to 9715 and 9721 to 9723 can also be used as lighting devices. The display portions 9710 to 9715 and 9721 to 9723 can also be used as heating devices.

[0440]

FIG. 55A illustrates an external view of a camera 8000. The camera 8000 includes a housing 8001, a display portion 8002, an operation button 8003, a shutter button 8004, a connection portion 8005, and the like. A lens 8006 can be put on the camera 8000.

[0441]

The connection portion 8005 includes an electrode to connect with a finder 8100, which is described below, a stroboscope, or the like.

[0442]

Although the lens 8006 of the camera 8000 here is detachable from the housing 8001 for replacement, the lens 8006 may be included in a housing.

[0443]

Images can be taken at the touch of the shutter button 8004. In addition, images can be taken at the touch of the display portion 8002 which serves as a touch panel.

[0444]

The display device or input/output device of one embodiment of the present invention can be used in the display portion 8002.

[0445]

FIG. 55B shows the camera 8000 with the finder 8100 connected.

[0446]

The finder 8100 includes a housing 8101, a display portion 8102, a button 8103, and the like.

[0447]

The housing 8101 includes a connection portion for the camera 8000 and the connection portion 8005, and the finder 8100 can be connected to the camera 8000. The connection portion includes an electrode, and an image or the like received from the camera 8000 through the electrode can be displayed on the display portion 8102.

[0448]

The button 8103 has a function of a power button, and the display portion 8102 can be turned on and off with the button 8103.

[0449]

The semiconductor device of one embodiment of the present invention can be used for an integrated circuit and an image sensor included in the housing 8101.

[0450]

Although the camera 8000 and the finder 8100 are separate and detachable electronic devices in FIGS. 55A and 55B, the housing 8001 of the camera 8000 may include a finder having the display device or input/output device of one embodiment of the present invention.

[0451]

FIG. 55C illustrates an external view of a head-mounted display 8200.

[0452]

The head-mounted display 8200 includes a mounting portion 8201, a lens 8202, a main body 8203, a display portion 8204, a cable 8205, and the like. The mounting portion 8201 includes a battery 8206.

[0453]

Power is supplied from the battery 8206 to the main body 8203 through the cable 8205. The main body 8203 includes a wireless receiver or the like to receive video data, such as image data, and display it on the display portion 8204. In addition, the movement of the eyeball and the eyelid of a user can be captured by a camera in the main body 8203 and then coordinates of the points the user looks at can be calculated using the captured data to utilize the eye of the user as an input means.

[0454]

The mounting portion 8201 may include a plurality of electrodes to be in contact with the user. The main body 8203 may be configured to sense current flowing through the electrodes with the movement of the user's eyeball to recognize the direction of his or her eyes. The main body 8203 may be configured to sense current flowing through the electrodes to monitor the user's pulse. The mounting portion 8201 may include sensors, such as a temperature sensor, a pressure sensor, or an acceleration sensor so that the user's biological information can be displayed on the display portion 8204. The main body 8203 may be configured to sense the movement of the user's head or the like to move an image displayed on the display portion 8204 in synchronization with the movement of the user's head or the like.

[0455]

The semiconductor device of one embodiment of the present invention can be used for an integrated circuit included in the main body 8203.

[0456]

At least part of this embodiment can be implemented in combination with any of the embodiments described in this specification as appropriate.

[0457]

(Embodiment 14)

In this embodiment, application examples of an RF tag using the semiconductor device

of one embodiment of the present invention will be described with reference to FIGS. 56A to 56F.

[0458]

<Application examples of RF tag>

The RF tag is widely used and can be provided for, for example, products such as bills, coins, securities, bearer bonds, documents (e.g., driver's licenses or resident's cards, see FIG. 56A), vehicles (e.g., bicycles, see FIG. 56B), packaging containers (e.g., wrapping paper or bottles, see FIG. 56C), recording media (e.g., DVD or video tapes, see FIG. 56D), personal belongings (e.g., bags or glasses), foods, plants, animals, human bodies, clothing, household goods, medical supplies such as medicine and chemicals, and electronic devices (e.g., liquid crystal display devices, EL display devices, television sets, or cellular phones), or tags on products (see FIGS. 56E and 56F).

[0459]

An RF tag 4000 of one embodiment of the present invention is fixed to a product by being attached to a surface thereof or embedded therein. For example, the RF tag 4000 is fixed to each product by being embedded in paper of a book, or embedded in an organic resin of a package. Since the RF tag 4000 of one embodiment of the present invention can be reduced in size, thickness, and weight, it can be fixed to a product without spoiling the design of the product. Furthermore, bills, coins, securities, bearer bonds, documents, or the like can have an identification function by being provided with the RF tag 4000 of one embodiment of the present invention, and the identification function can be utilized to prevent counterfeiting. Moreover, the efficiency of a system such as an inspection system can be improved by providing the RF tag of one embodiment of the present invention for packaging containers, recording media, personal belongings, foods, clothing, household goods, electronic devices, or the like. Vehicles can also have higher security against theft or the like by being provided with the RF tag of one embodiment of the present invention.

[0460]

As described above, by using the RF tag including the semiconductor device of one embodiment of the present invention for each application described in this embodiment, power for operation such as writing or reading of data can be reduced, which results in an increase in the maximum communication distance. Moreover, data can be held for an extremely long period even in the state where power is not supplied; thus, the RF tag can be preferably used for application in which data is not frequently written or read.

[0461]

This embodiment can be combined as appropriate with any of the other embodiments in

this specification.

EXPLANATION OF REFERENCE

[0462]

200: imaging device, 201: switch, 202: switch, 203: switch, 210: pixel portion, 211: pixel, 212: subpixel, 212B: subpixel, 212G: subpixel, 212R: subpixel, 220: photoelectric conversion element, 230: pixel circuit, 231: wiring, 247: wiring, 248: wiring, 249: wiring, 250: wiring, 253: wiring, 254: filter, 254B: filter, 254G: filter, 254R: filter, 255: lens, 256: light, 257: wiring, 260: peripheral circuit, 270: peripheral circuit, 280: peripheral circuit, 290: peripheral circuit, 291: light source, 300: silicon substrate, 301: insulator, 303: insulator, 305: layer, 310: conductor, 320: layer, 330: transistor, 331: layer, 340: layer, 351: transistor, 352: transistor, 353: transistor, 354: transistor, 360: photodiode, 361: anode, 362: cathode, 363: low-resistance region, 365: photodiode, 366: semiconductor layer, 367: semiconductor layer, 368: semiconductor layer, 370: plug, 371: wiring, 372: wiring, 373: wiring, 374: wiring, 380: insulator, 381: insulator, 400: substrate, 401: insulator, 402: insulator, 404: conductor, 404_1: conductor, 404w: gate line width, 406a: insulator, 406b: semiconductor, 406c: insulator, 406c_1: insulator, 407: region, 408: insulator, 410: insulator, 410_1: insulator, 410a: insulator, 411: resist mask, 412: insulator, 412_1: insulator, 413: organic substance, 414: mixed region, 415: conductor, 416a1: conductor, 416a2: conductor, 416w1: opening width, 416w2: opening width, 428: insulator, 429: conductor, 430: conductor, 431: conductor, 432: conductor, 437: conductor, 438: conductor, 440: conductor, 442: conductor, 444: conductor, 446: taper angle, 447: taper angle, 450: semiconductor substrate, 454: conductor, 460: region, 462: insulator, 464: insulator, 465: insulator, 466: insulator, 467: insulator, 468: insulator, 469: insulator, 470: insulator, 472: insulator, 474a: region, 474b: region, 475: insulator, 476a: conductor, 476b: conductor, 476c: conductor, 477a: conductor, 477b: conductor, 477c: conductor, 478a: conductor, 478b: conductor, 478c: conductor, 479a: conductor, 479b: conductor, 479c: conductor, 480a : conductor, 480b: conductor, 480c: conductor, 483a: conductor, 483b: conductor, 483c: conductor, 483d: conductor, 483e: conductor, 483f: conductor, 484a: conductor, 484b: conductor, 484c: conductor, 484d: conductor, 485a: conductor, 485b: conductor, 485c: conductor, 485d: conductor, 487a: conductor, 487b: conductor, 487c: conductor, 488a: conductor, 488b: conductor, 488c: conductor, 489a: conductor, 489b: conductor, 490a: conductor, 490b: conductor, 491a: conductor, 491b: conductor, 491c: conductor, 492a: conductor,492b: conductor, 492c: conductor, 494: conductor, 496: conductor, 498: insulator, 550: interposer, 551: chip, 552: terminal, 553: mold resin, 600: panel, 601: printed wiring board, 602: package, 603: FPC, 604: battery, 700: substrate, 704a: conductor, 704b: conductor, 706a: insulator, 706b: semiconductor, 706c: insulator, 706d: insulator, 706e: semiconductor, 706f:

insulator, 710: insulator, 712a: insulator, 714a: conductor, 714b: conductor, 716a1: conductor, 716a2: conductor, 716a3: conductor, 716a4: conductor, 718b: insulator, 719: light-emitting element, 720: insulator, 721: insulator, 728: insulator, 731: terminal, 732: FPC, 733a: wiring, 734: sealant, 735: driver circuit, 736: driver circuit, 737: pixel, 741: transistor, 742: capacitor, 743: switching element, 744: signal line, 750: substrate, 751: transistor, 752: capacitor, 753: liquid crystal element, 754: scan line, 755: signal line, 781: conductor, 782: light-emitting layer, 783: conductor, 784: partition wall, 791: conductor, 792: insulator, 793: liquid crystal layer, 794: insulator, 795: spacer, 796: conductor,797: substrate, 800: RF tag, 801: communication device, 802: antenna, 803: radio signal, 804: antenna, 805: rectifier circuit, 806: constant voltage circuit, 807: demodulation circuit, 808: modulation circuit, 809: logic circuit, 810: memory circuit, 811: ROM, 1189: ROM interface, 1190: substrate, 1191: ALU, 1192: ALU controller, 1193: instruction decoder, 1194: interrupt controller, 1195: timing controller, 1196: register, 1197: register controller, 1198: bus interface, 1199: ROM, 1200: memory element, 1201: circuit, 1202: circuit, 1203: switch, 1204: switch, 1206: logic element, 1207: capacitor, 1208: capacitor, 1209: transistor, 1210: transistor, 1213: transistor, 1214: transistor, 1220: circuit, 2100: transistor, 2200: transistor, 2201: insulator, 2202: wiring, 2203: plug, 2204: insulator, 2205: wiring, 2207: insulator, 2210: intermediate layer, 2211: semiconductor substrate, 2212: insulator, 2213: gate electrode, 2214: gate insulator, 2215: source and drain regions, 3001: wiring, 3002: wiring, 3003: wiring, 3004: wiring, 3005: wiring, 3200: transistor, 3300: transistor, 3400: capacitor, 4000: RF tag, 5100: pellet, 5120: substrate, 5161: region, 6000: display module, 6001: upper cover, 6002: lower cover, 6003: FPC, 6004: touch panel, 6005: FPC, 6006: display panel, 6007: backlight unit, 6008: light source, 6009: frame, 6010: printed board, 6011: battery, 7101: housing, 7102: housing, 7103: display portion, 7104: display portion, 7105: microphone, 7106: speaker, 7107: operation key, 7108: stylus, 7302: housing, 7304: display portion, 7311: operation button, 7312: operation button, 7313: connection terminal, 7321: band, 7322: clasp, 7501: housing, 7502: display portion, 7503: operation button, 7504: external connection port, 7505: speaker, 7506: microphone, 7701: housing, 7702: housing, 7703: display portion, 7704: operation key, 7705: lens, 7706: joint, 7901: utility pole, 7902: display portion, 8000: camera, 8001: housing, 8002: display portion, 8003: operation button, 8004: shutter button, 8005: connection portion, 8006: lens, 8100: finder, 8101: housing, 8102: display portion, 8103: button, 8121: housing, 8122: display portion, 8123: keyboard, 8124: pointing device, 8200: head-mounted display, 8201: mounting portion, 8202: lens, 8203: main body, 8204: display portion, 8205: cable, 8206: battery, 9700: automobile, 9701: car body, 9702: wheels, 9703: dashboard, 9704: lights, 9710: display portion, 9711: display portion, 9712: display portion, 9713: display portion, 9714: display portion, 9715: display portion, 9721: display portion, 9722: display portion, 9723: display

portion

This application is based on Japanese Patent Application serial no. 2015-041204 filed with Japan Patent Office on March 3, 2015, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A semiconductor device comprising:

a first conductor layer and a second conductor layer over an oxide semiconductor;

a third insulator over the first conductor layer and the second conductor layer, the third insulator comprising an opening;

a fourth insulator over the third insulator, the first conductor layer, the second conductor layer, and the oxide semiconductor;

a fifth insulator over the fourth insulator; and

a third conductor over the fifth insulator,

wherein in the opening of the third insulator, a side surface of the third insulator overlaps with a side surface of the third conductor with the fourth insulator and the fifth insulator positioned therebetween, and

wherein in the opening of the third insulator, part of top surfaces of the first conductor layer and the second conductor layer is in contact with the fourth insulator.

2. The semiconductor device according to claim 1, further comprising:

a first insulator; and

a second insulator between the first insulator and the oxide semiconductor,

wherein the second insulator comprises at least one of component elements of the oxide semiconductor other than oxygen.

3. The semiconductor device according to claim 1,

wherein the first conductor layer and the second conductor layer serve as a source electrode and a drain electrode of a transistor,

wherein the fifth insulator serves as a gate insulator of the transistor, and

wherein the third conductor serves as a gate electrode of the transistor.

4. The semiconductor device according to claim 1, wherein the fourth insulator comprises at least one of component elements of the oxide semiconductor other than oxygen.

5. The semiconductor device according to claim 1, wherein each of the first conductor layer, the second conductor layer, and the third conductor comprises a conductor that is less likely to allow passage of oxygen.

6. The semiconductor device according to claim 1,

wherein the third conductor comprises a region serving as a gate electrode of a transistor, and

wherein the transistor has a gate line width of greater than or equal to 5 nm and less than or equal to 60 nm.

7. A method for manufacturing a semiconductor device comprising the steps of:

forming a second insulator over a first insulator;

forming an oxide semiconductor over the second insulator;

forming a first conductor film over the oxide semiconductor;

forming a third insulator over the first conductor film;

forming an opening in the third insulator and the first conductor film so that the oxide semiconductor is exposed and a first conductor layer and a second conductor layer are formed from the first conductor film;

etching part of the third insulator to expand the opening to expose top surfaces of the first conductor layer and the second conductor layer;

forming a fourth insulator over the third insulator, the first conductor layer, the second conductor layer, and the oxide semiconductor;

forming a fifth insulator over the fourth insulator;

forming a third conductor over the fifth insulator; and

performing planarization treatment on the third conductor, the fifth insulator, and the fourth insulator to expose the third insulator.

8. The method for manufacturing the semiconductor device according to claim 7, further comprising the steps of:

forming a sixth insulator over the third insulator and the third conductor, the third insulator comprising excess oxygen; and

performing heat treatment to move the excess oxygen to the oxide semiconductor.

9. The method for manufacturing the semiconductor device according to claim 7, wherein each of the second insulator and the fourth insulator comprises at least one of component elements of the oxide semiconductor other than oxygen.

10. The method for manufacturing the semiconductor device according to claim 7, wherein an end portion of each of the first conductor layer and the second conductor layer has a

tapered shape.

11. The method for manufacturing the semiconductor device according to claim 7, wherein chemical mechanical polishing is performed in the step of performing planarization treatment.

12. A method for manufacturing a semiconductor device comprising the steps of:

forming a second insulator over a first insulator;

forming an oxide semiconductor over the second insulator;

forming a first conductor film over the oxide semiconductor;

forming a third insulator over the first conductor film;

forming an opening in the third insulator to expose the first insulator and the first conductor film;

forming an organic film over side surfaces of the second insulator, the oxide semiconductor, and the third insulator;

etching the first conductor film to form a first conductor layer and a second conductor layer using the organic film as a mask;

removing the organic film to expose top surfaces of the first conductor layer and the second conductor layer;

forming a fourth insulator over the third insulator, the first conductor layer, the second conductor layer, and the oxide semiconductor;

forming a fifth insulator over the fourth insulator;

forming a third conductor over the fifth insulator; and

performing planarization treatment on the third conductor, the fifth insulator, and the fourth insulator to expose the third insulator.

13. The method for manufacturing the semiconductor device according to claim 12, further comprising the steps of:

forming a sixth insulator over the third insulator and the third conductor, the third insulator comprising excess oxygen; and

performing heat treatment to move the excess oxygen to the oxide semiconductor.

14. The method for manufacturing the semiconductor device according to claim 12, wherein each of the second insulator and the fourth insulator comprises at least one of component elements of the oxide semiconductor other than oxygen.

15. The method for manufacturing the semiconductor device according to claim 12, wherein an end portion of each of the first conductor layer and the second conductor layer has a tapered shape.

16. The method for manufacturing the semiconductor device according to claim 12, wherein chemical mechanical polishing is performed in the step of performing planarization treatment.

17. The method for manufacturing the semiconductor device according to claim 12, wherein the organic film is formed by plasma using a gas containing carbon and halogen.

FIG. 1A

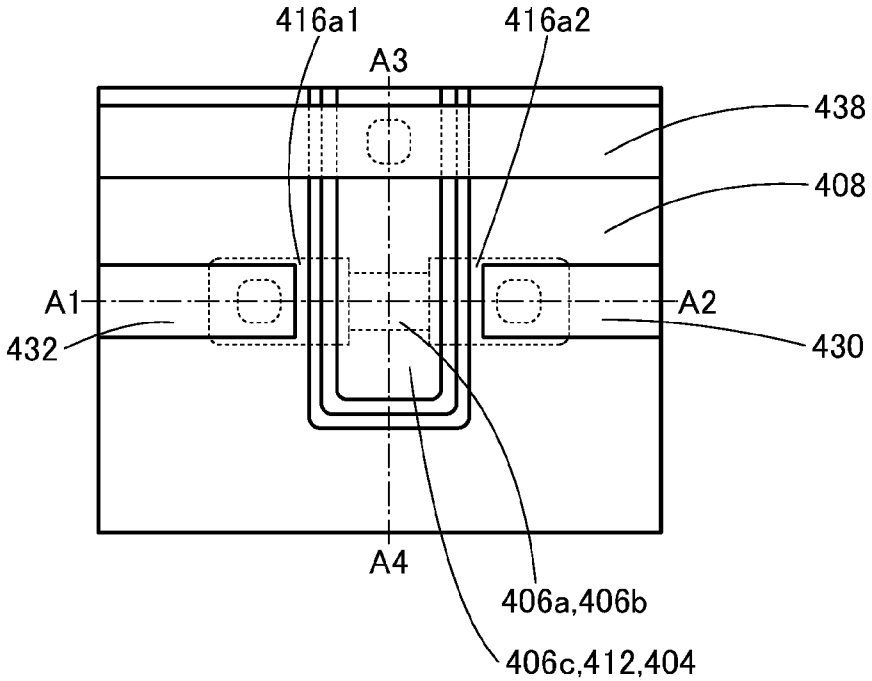


FIG. 1B

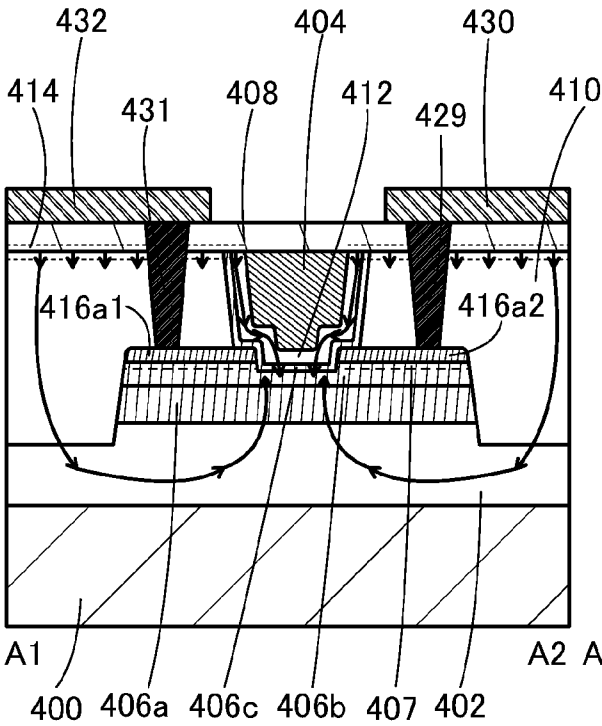


FIG. 1C

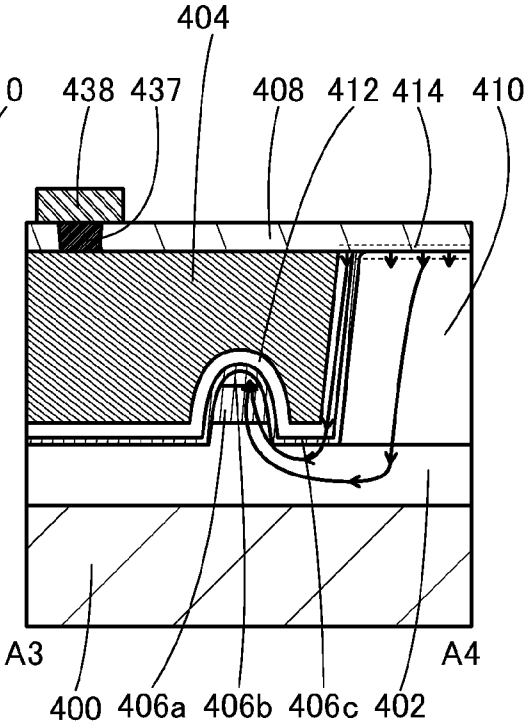


FIG. 2A

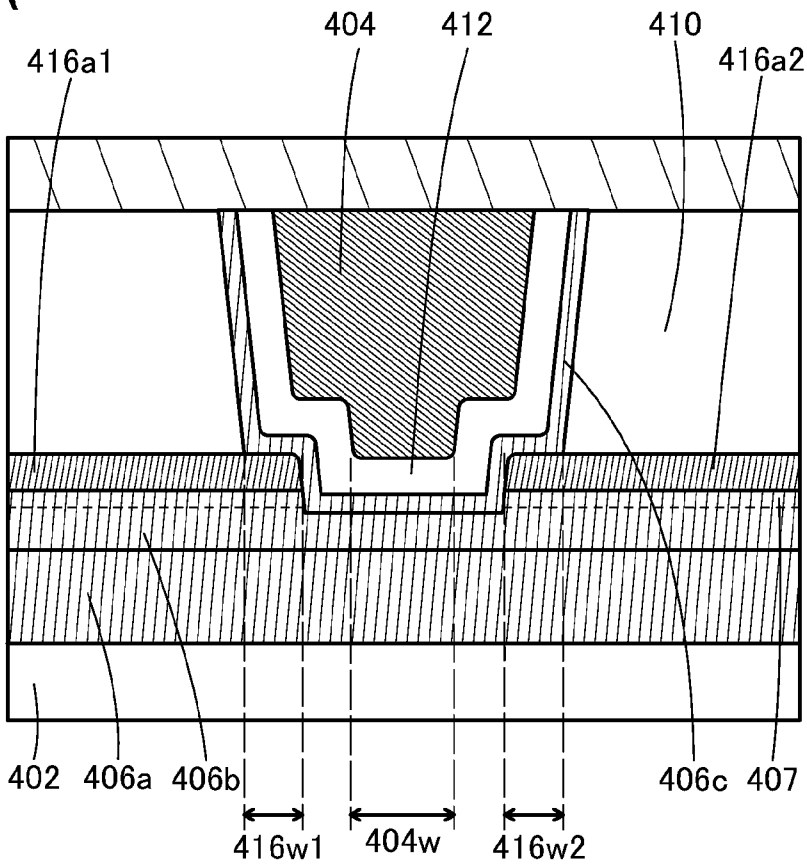

404
412
410
416a1
416a2
402
406a
406b
406c
407
416w1
404w
416w2

FIG. 2B

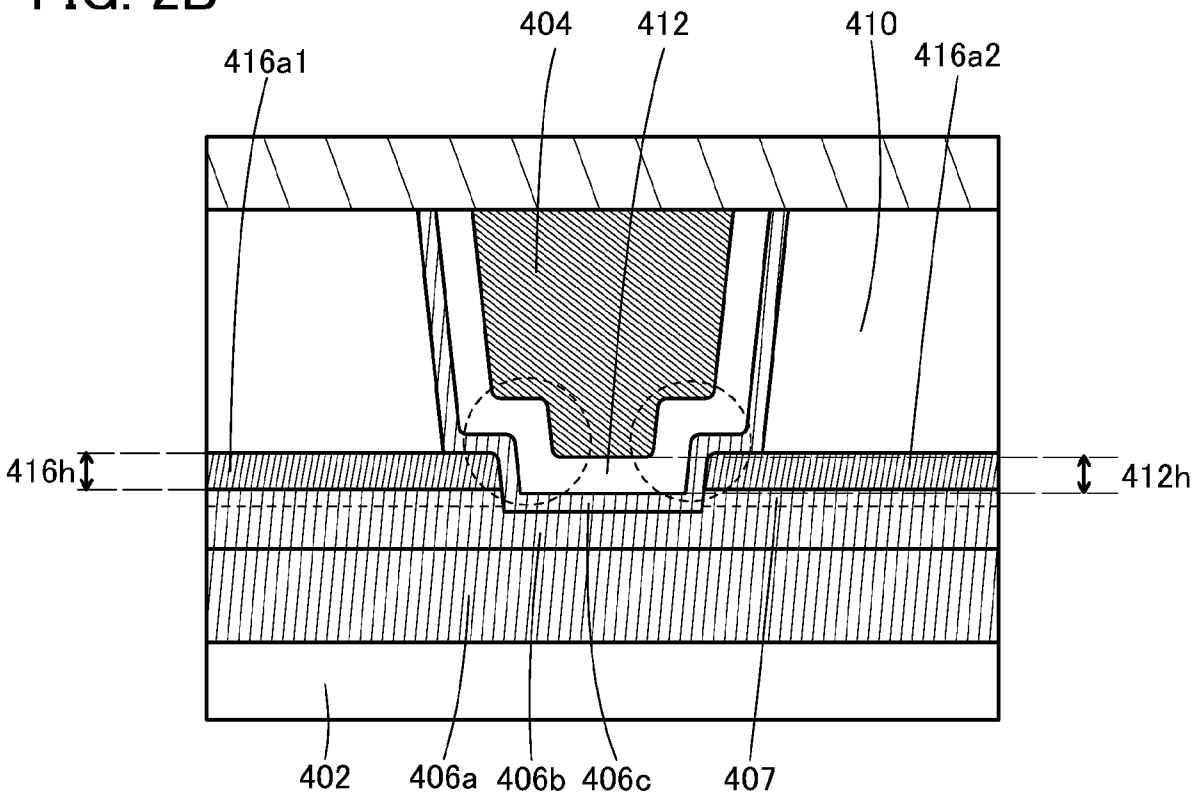

404
412
410
416a1
416a2
416h
412h
402
406a
406b
406c
407

FIG. 3

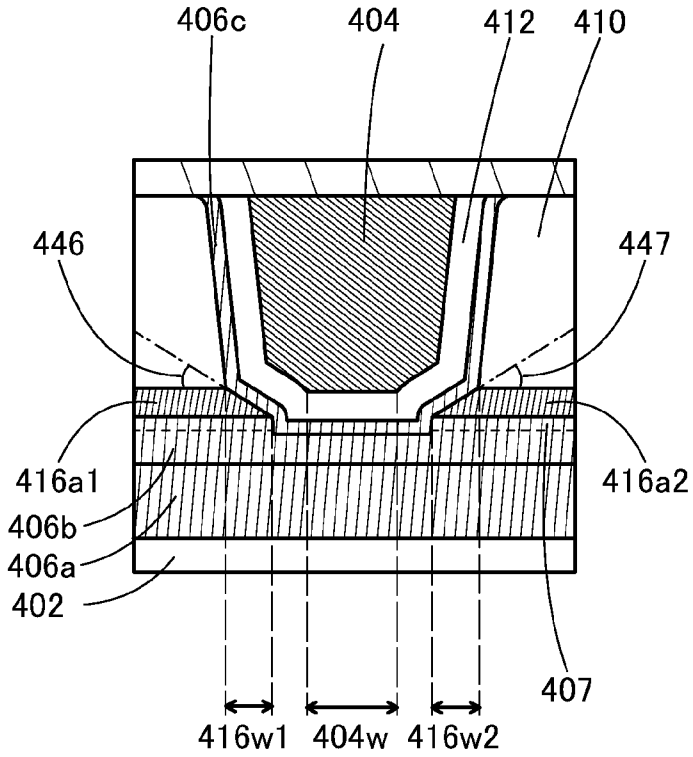

406c
404
412
410
446
447
416a1
416a2
406b
406a
402
407
416w1
404w
416w2

FIG. 4A

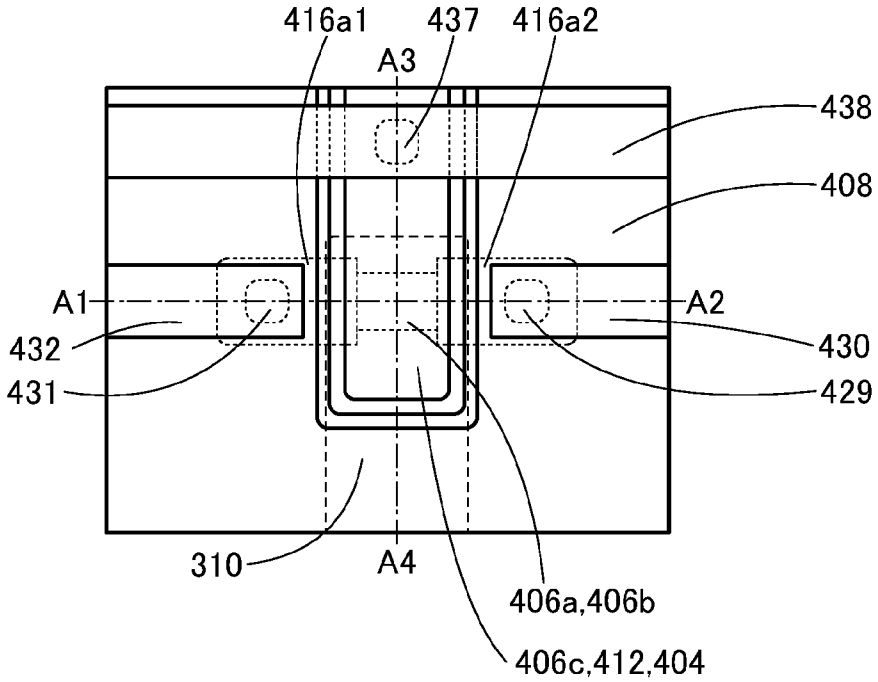


FIG. 4B

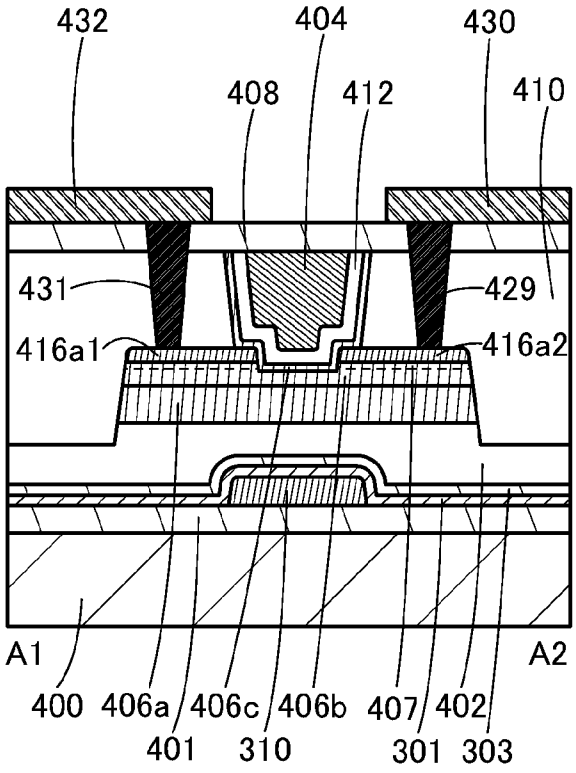


FIG. 4C

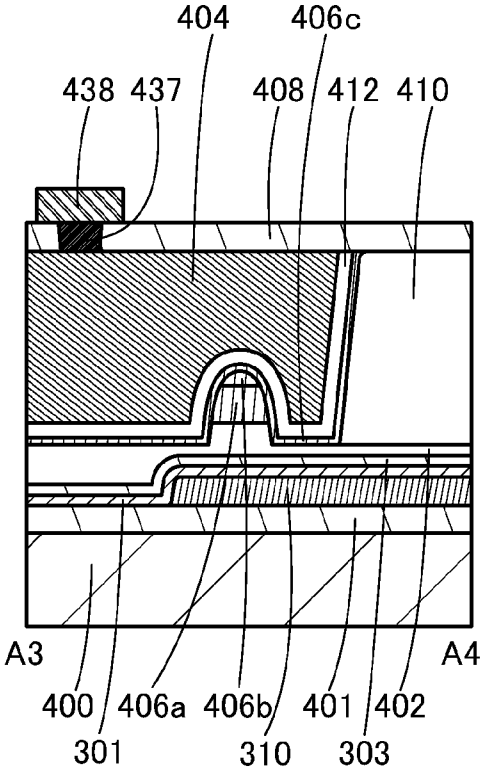


FIG. 5A

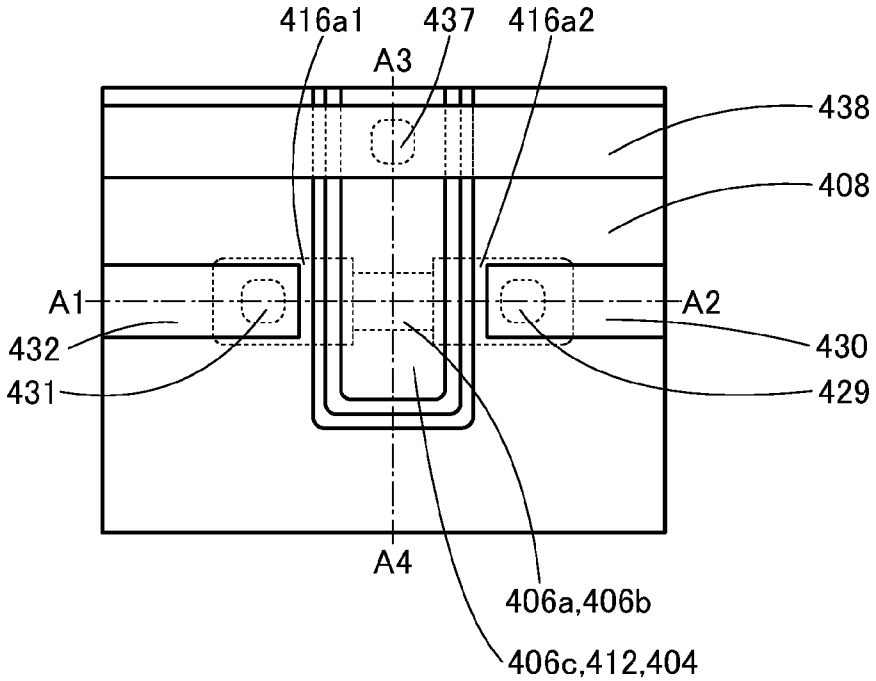


FIG. 5B

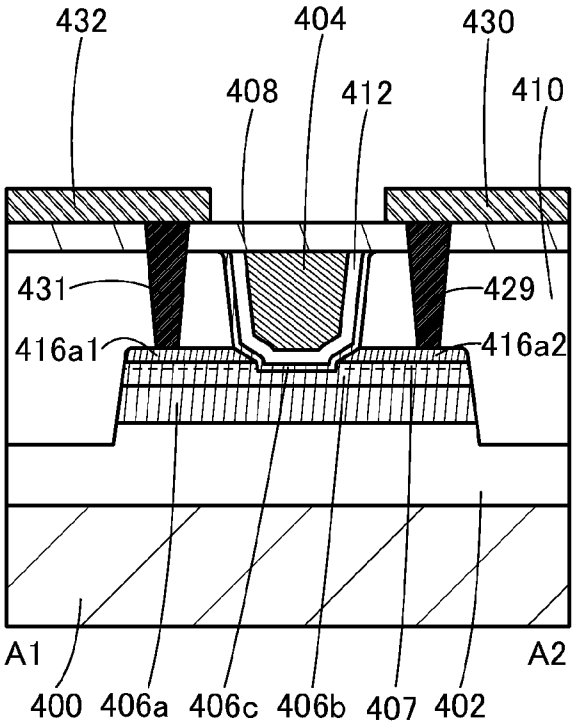


FIG. 5C

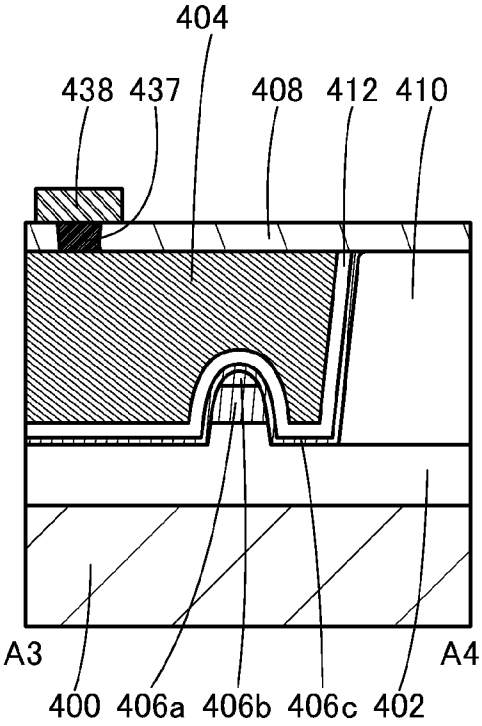


FIG. 6A

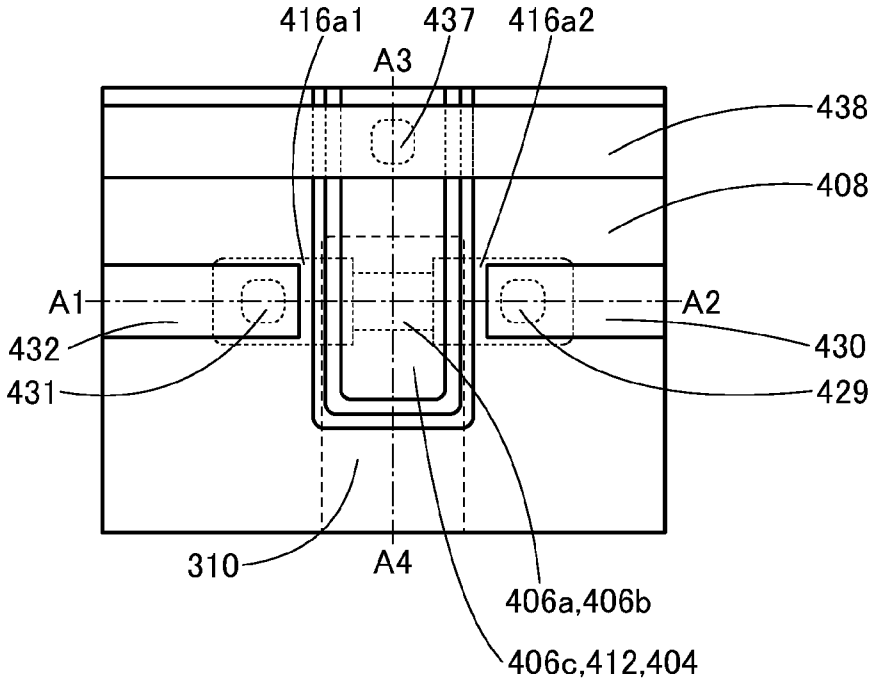


FIG. 6B

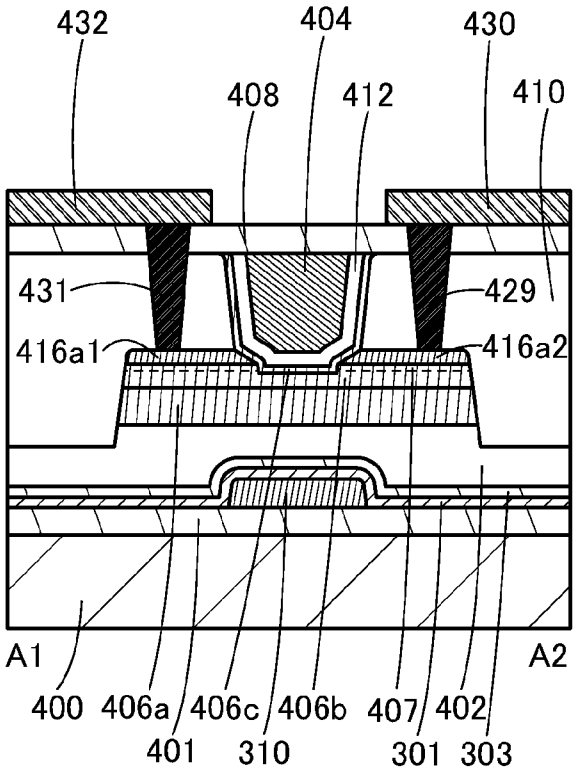


FIG. 6C

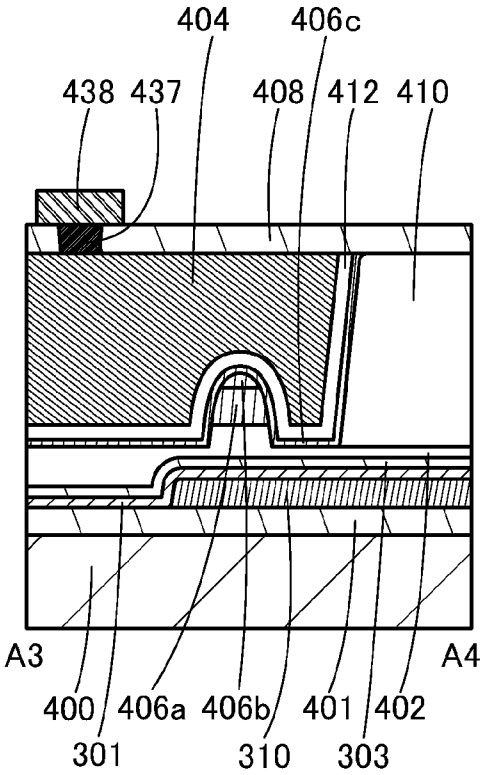


FIG. 7A

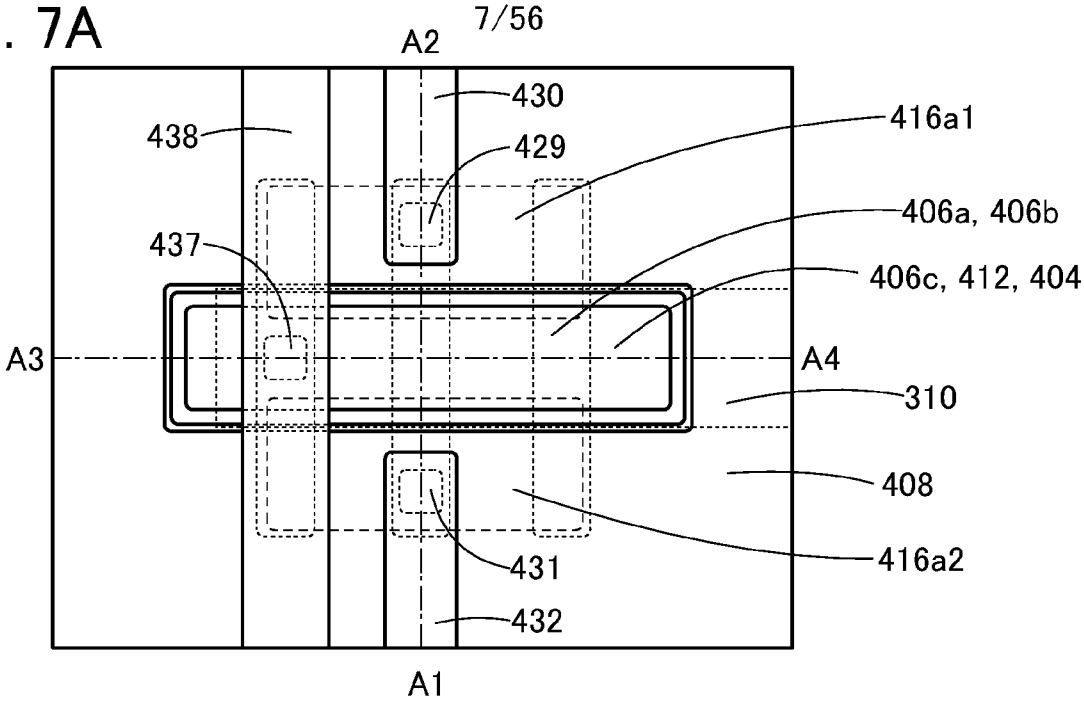


FIG. 7B

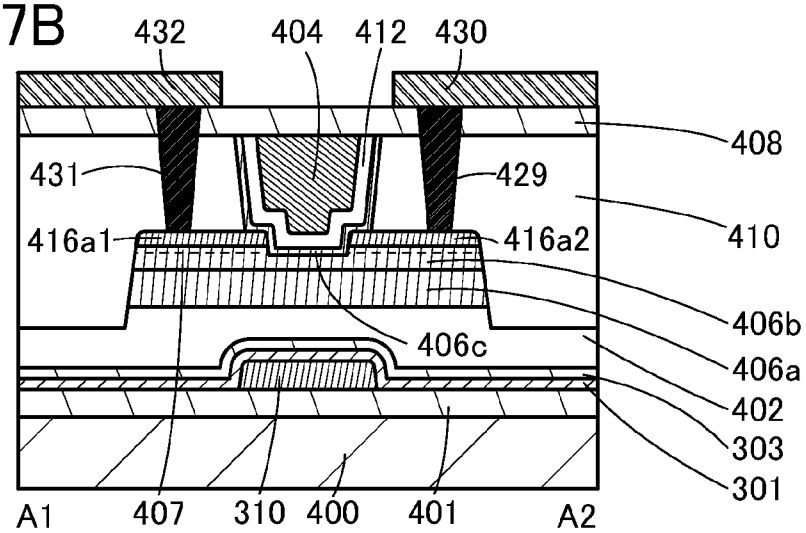


FIG. 7C

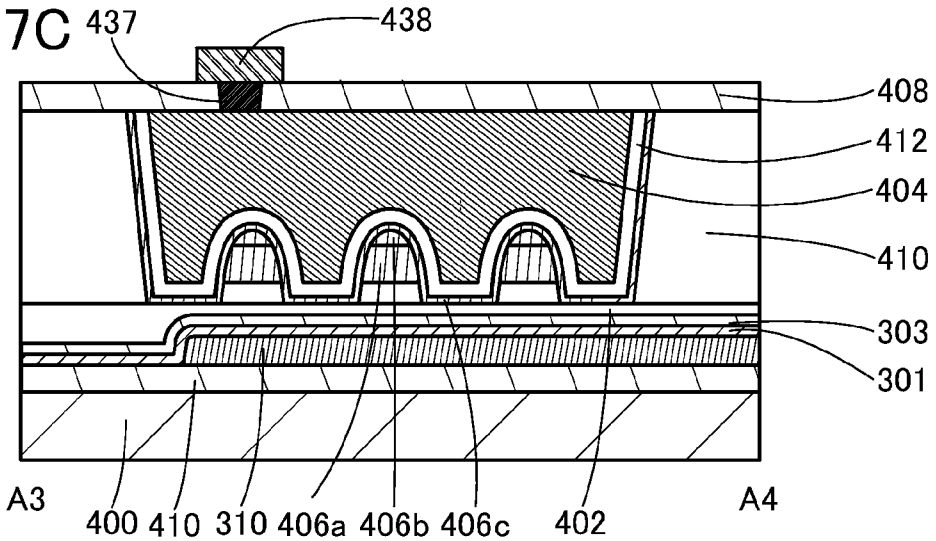


FIG. 8A

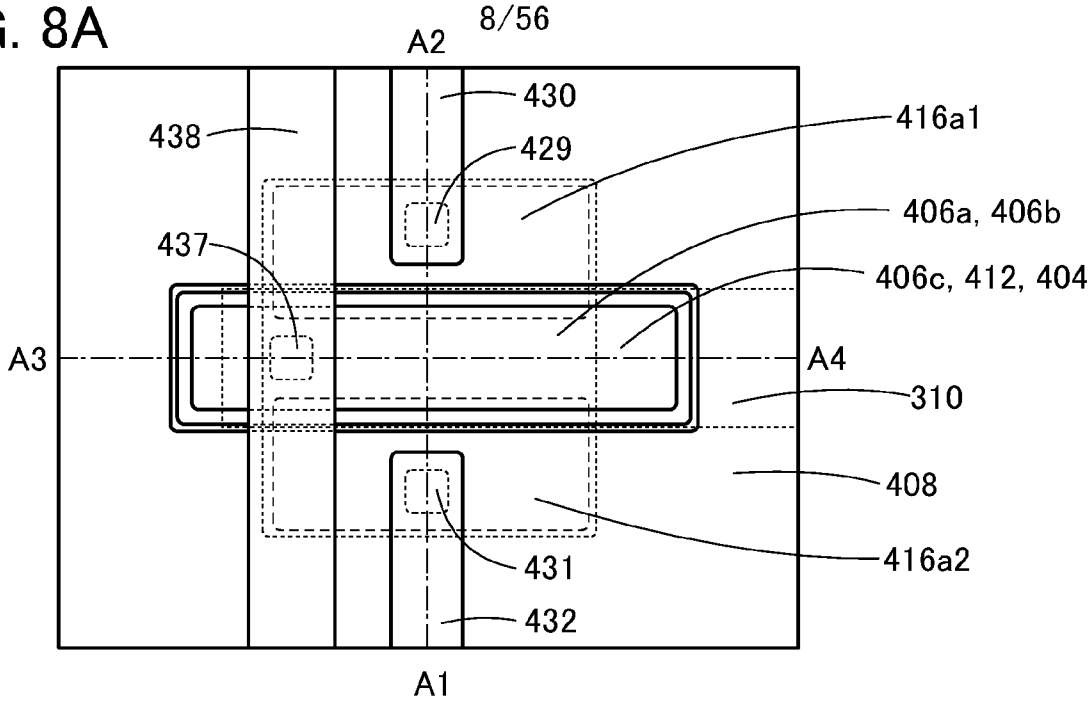


FIG. 8B

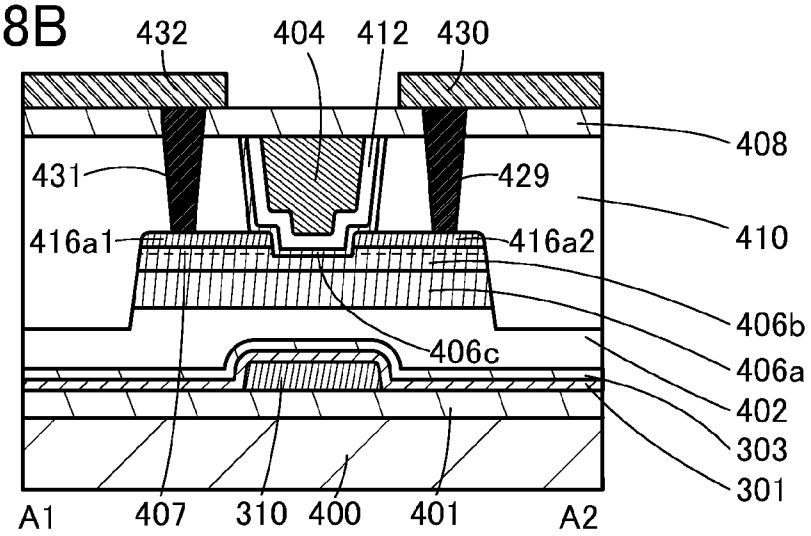


FIG. 8C

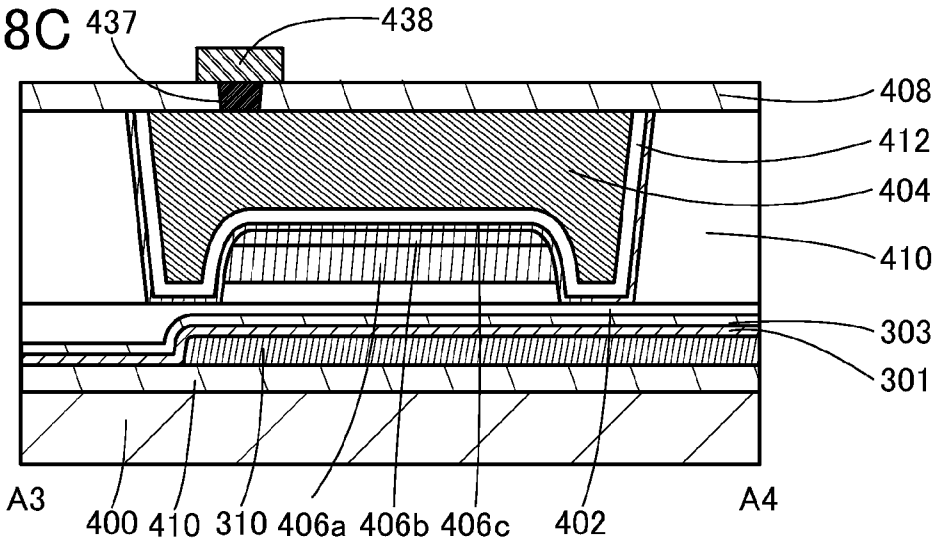


FIG. 9

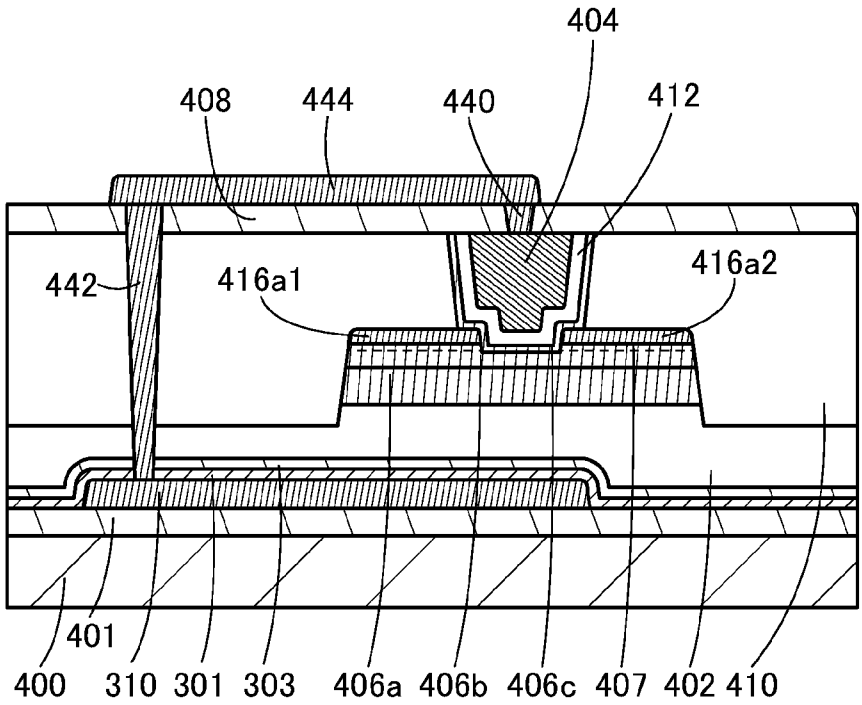

404
408
444
440
412
442
416a1
416a2
401
400
310
301
303
406a
406b
406c
407
402
410

FIG. 10A

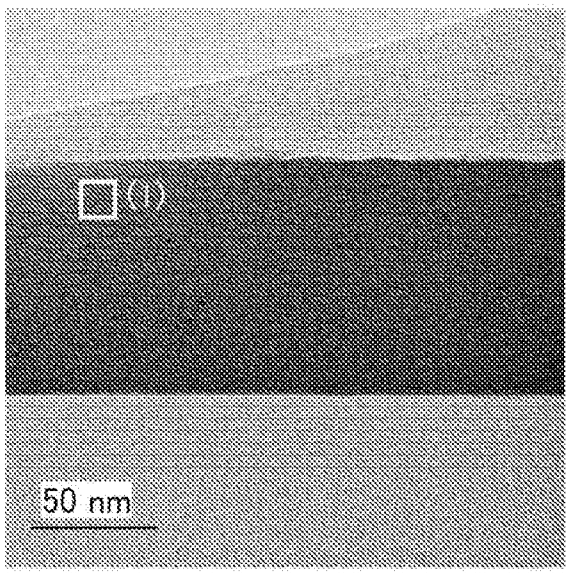


FIG. 10B

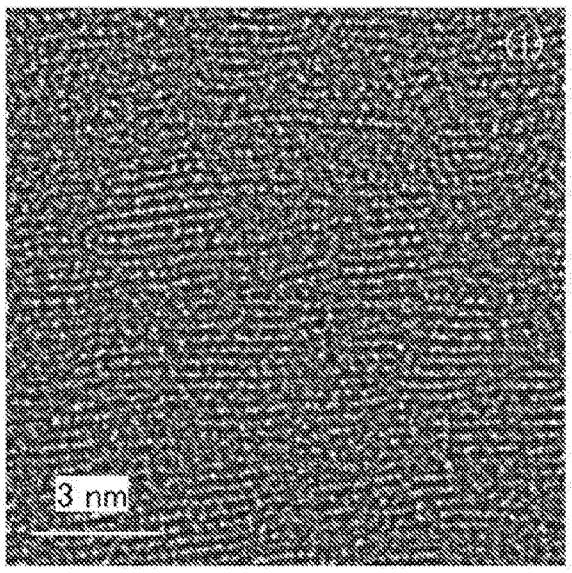


FIG. 10C

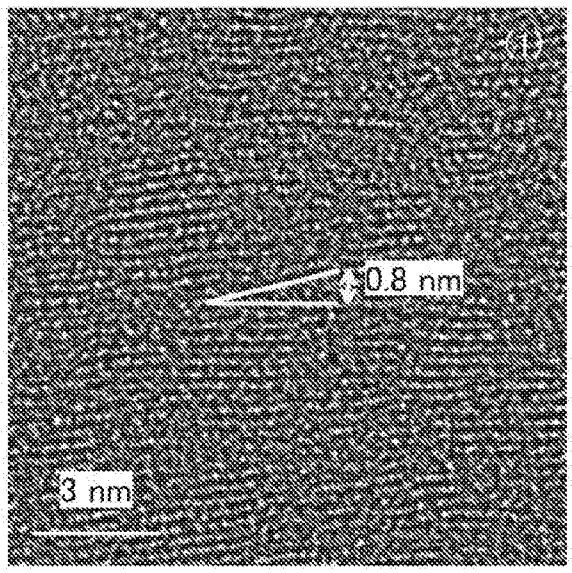


FIG. 10D

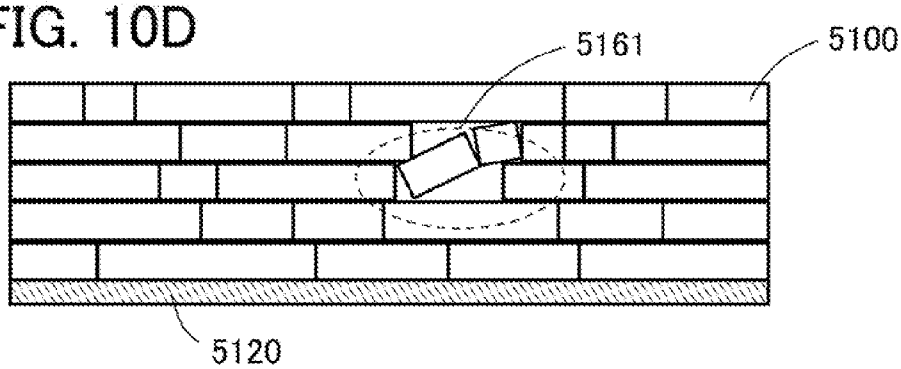


FIG. 11A

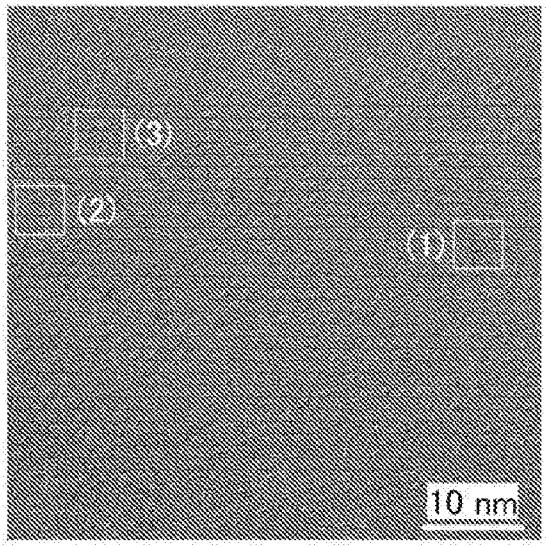


FIG. 11B

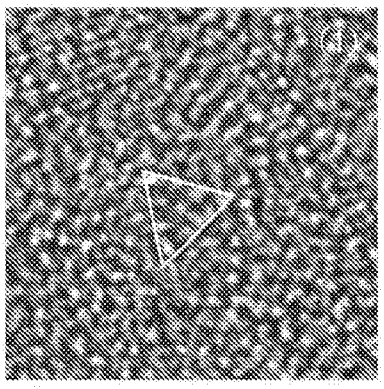


FIG. 11C

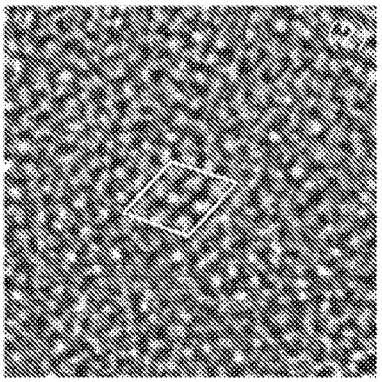


FIG. 11D

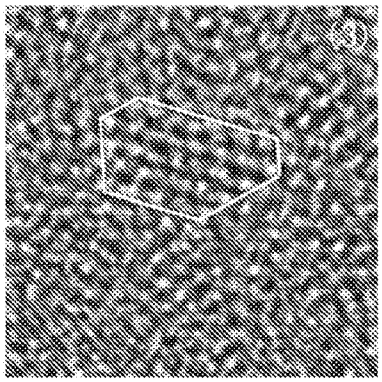


FIG. 12A

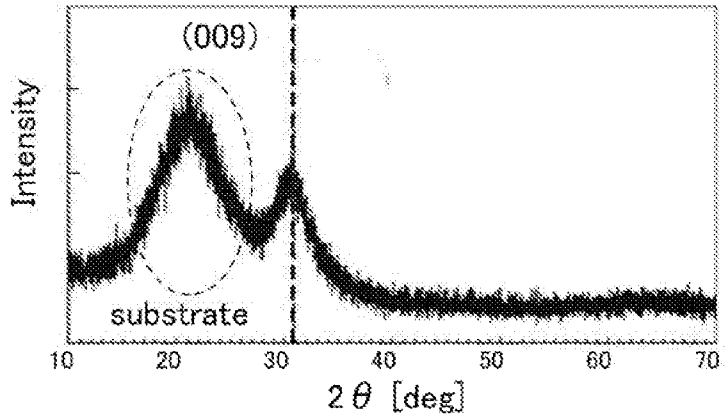


FIG. 12B

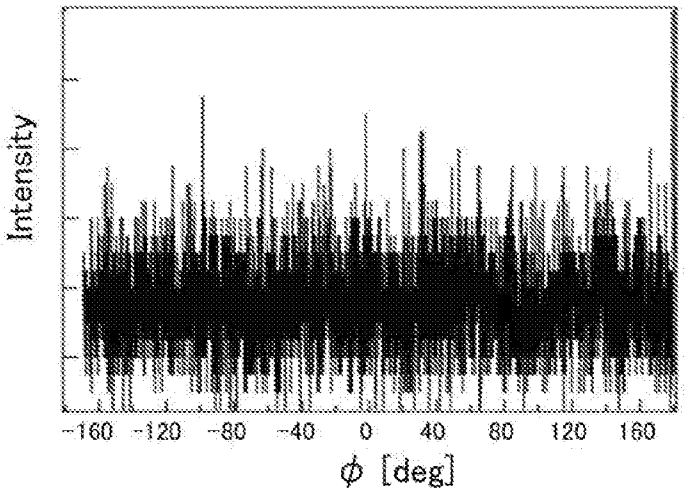


FIG. 12C

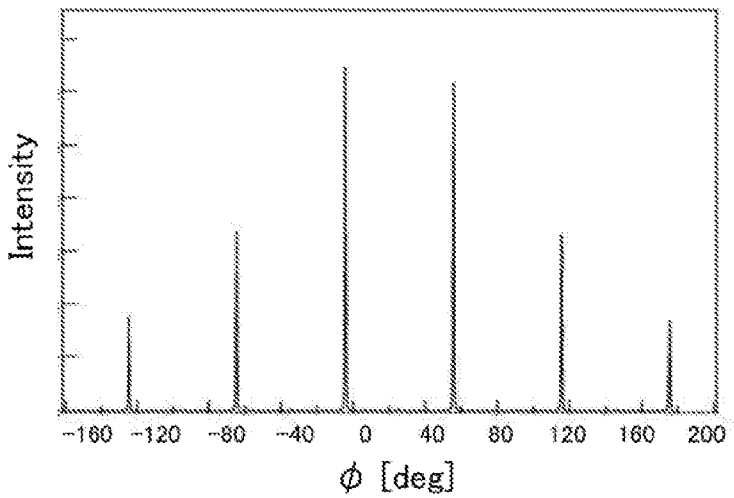


FIG. 13A

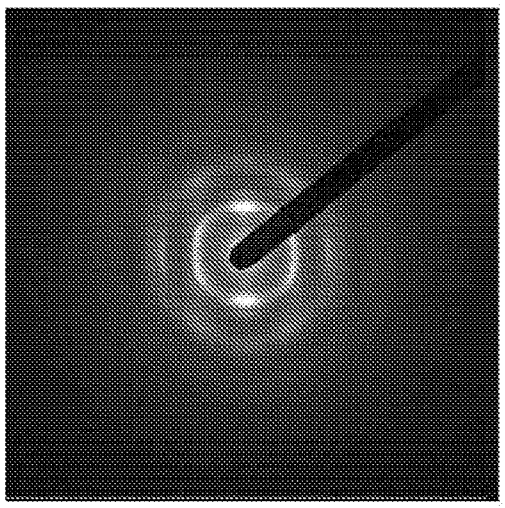


FIG. 13B

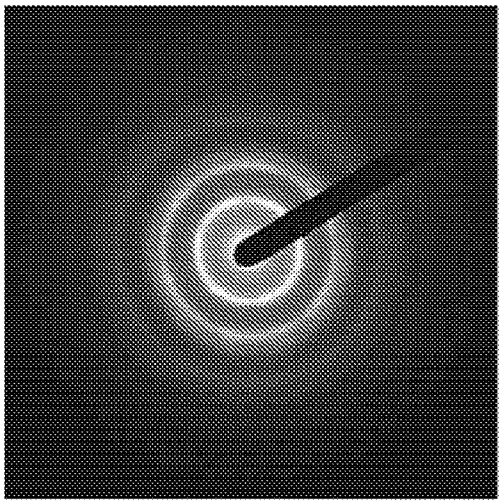


FIG. 14

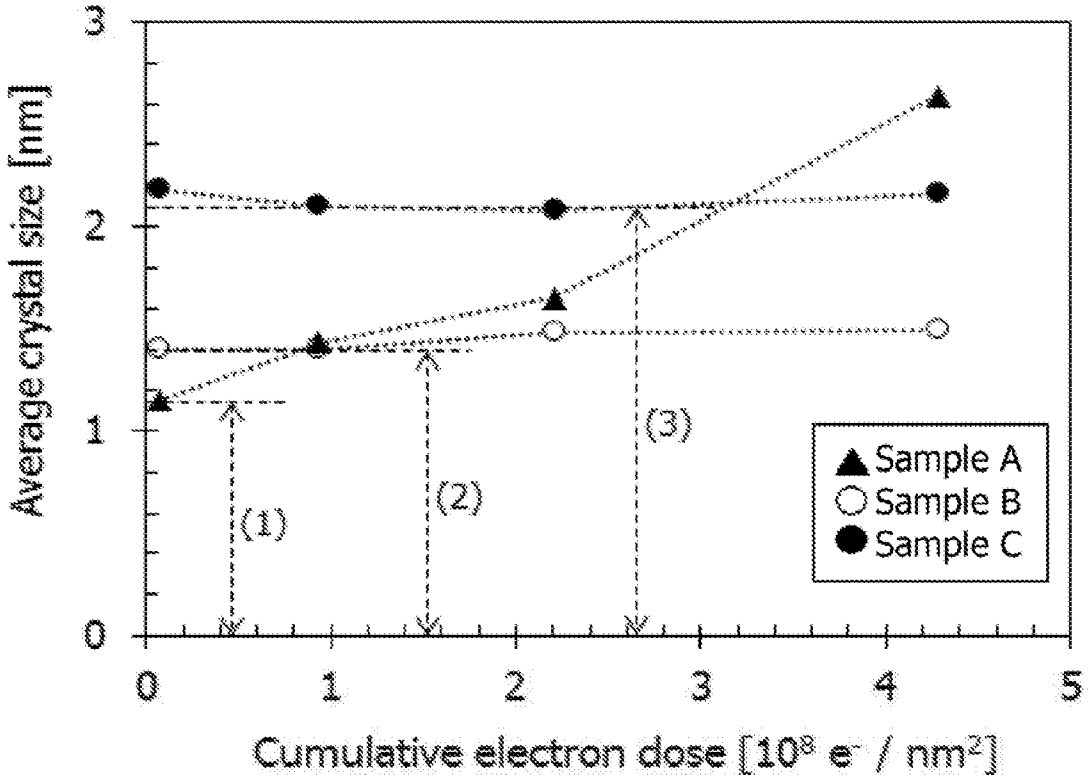

Average crystal size [nm]
Cumulative electron dose [10^8 e^- / nm^2]
0
1
2
3
4
5
(1)
(2)
(3)
Sample A
Sample B
Sample C

FIG. 15A

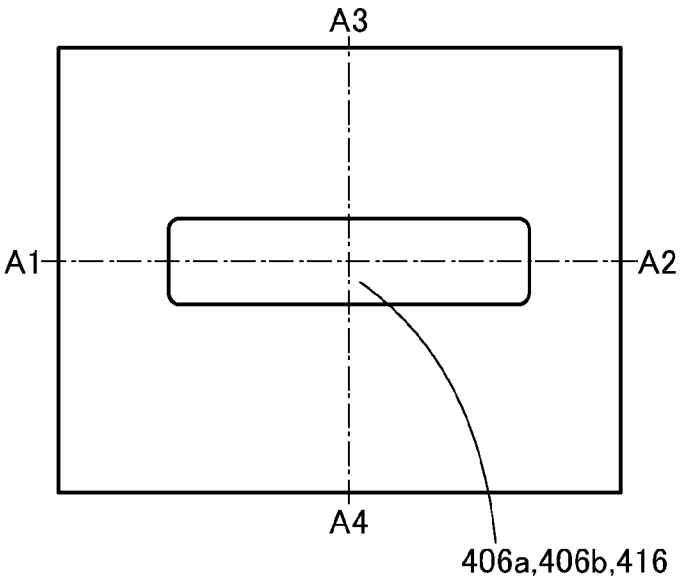


FIG. 15B

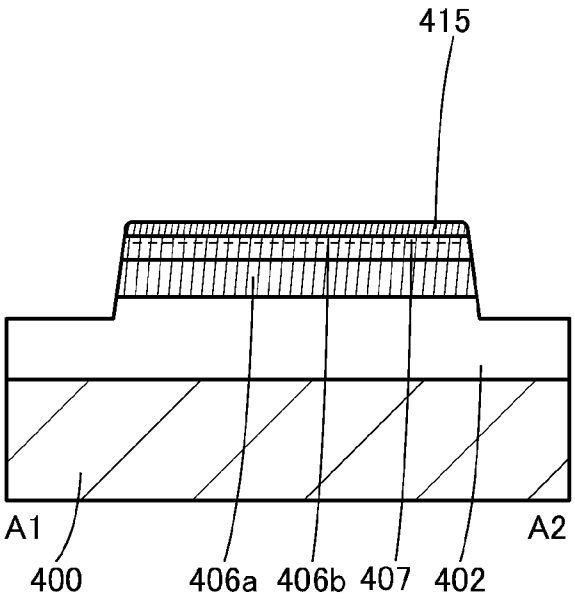


FIG. 15C

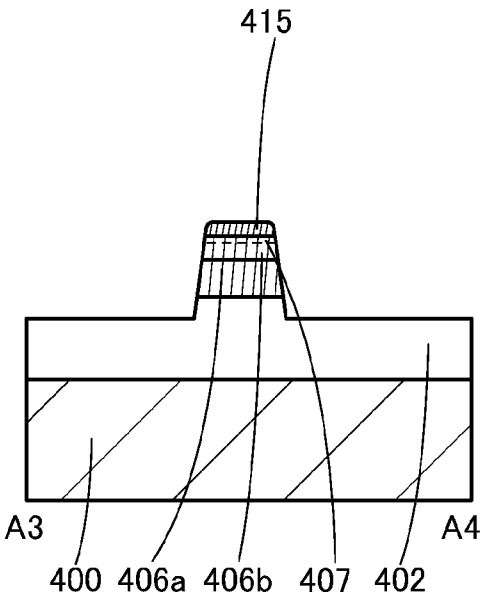


FIG. 16A

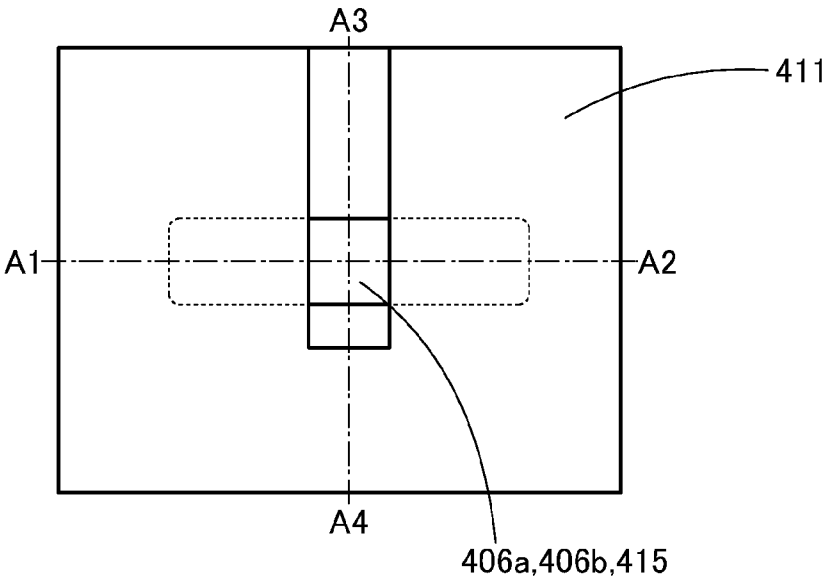


FIG. 16B

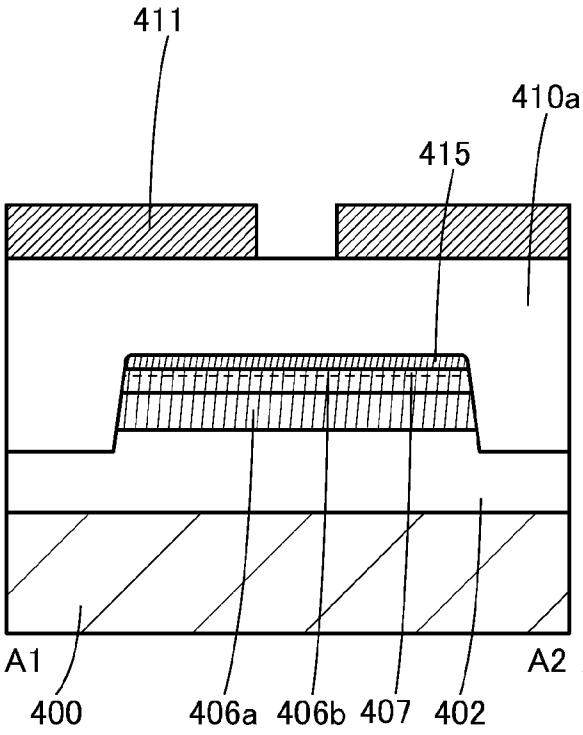


FIG. 16C

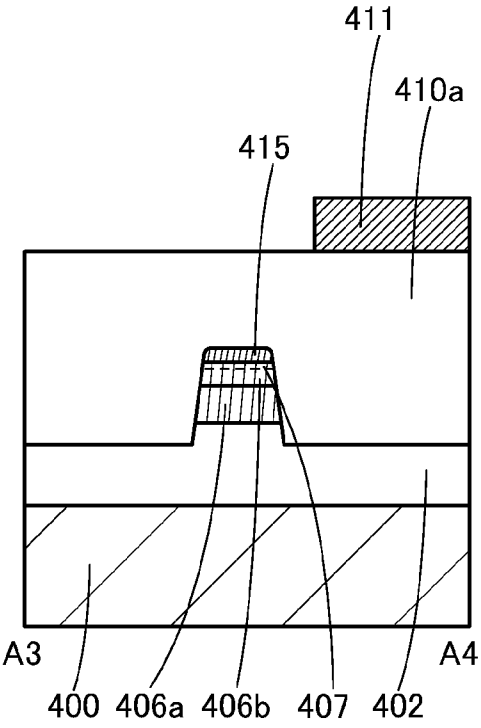


FIG. 17A

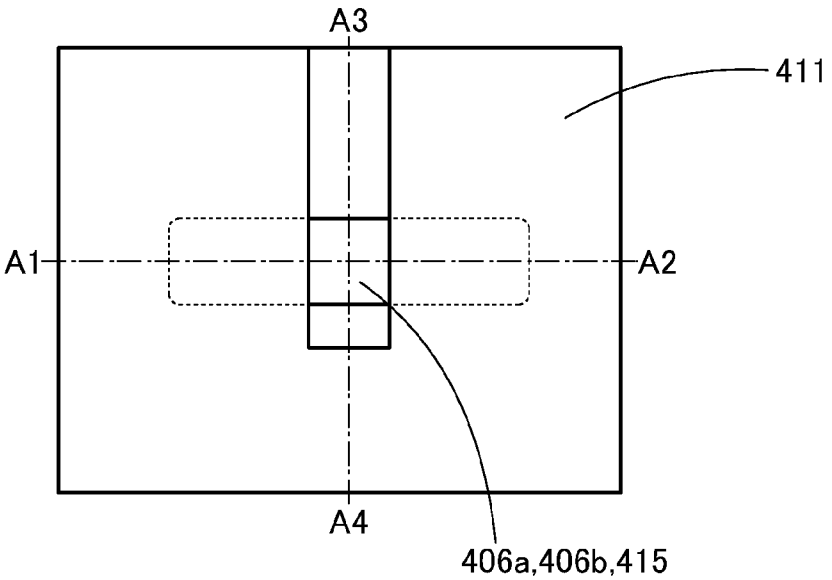


FIG. 17B

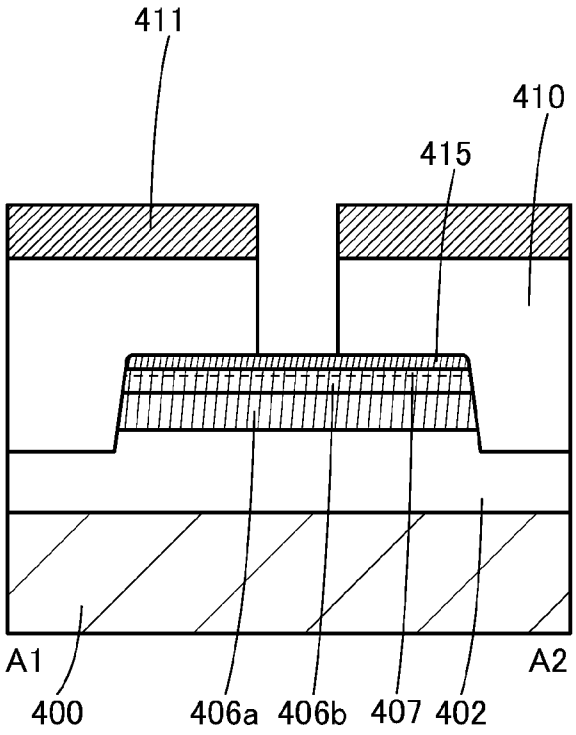


FIG. 17C

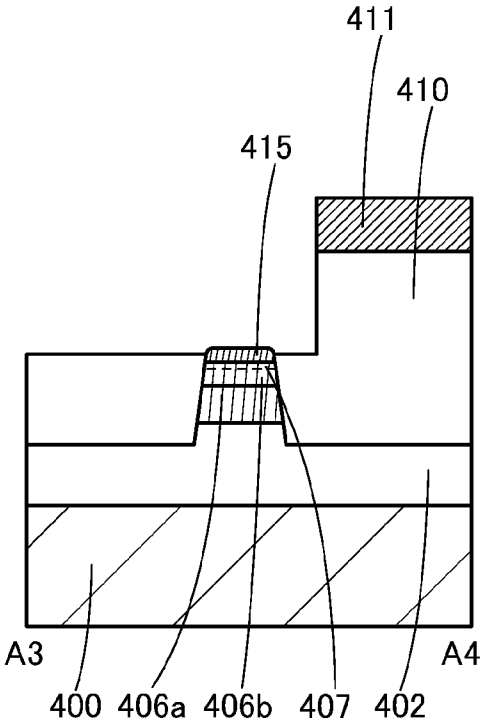


FIG. 18A

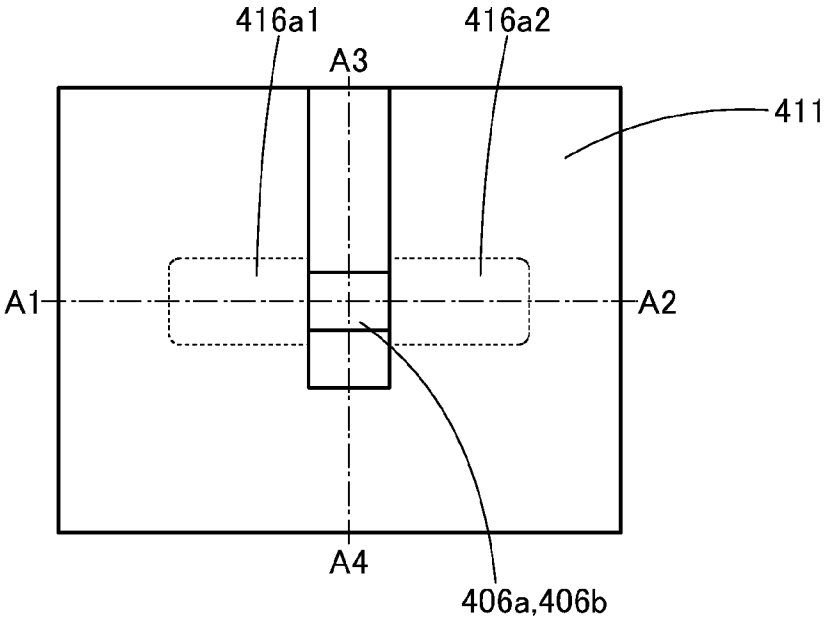


FIG. 18B

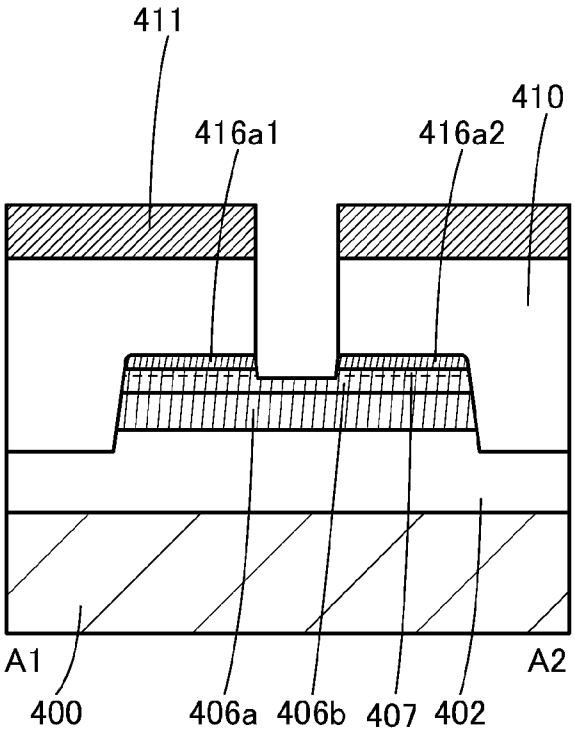


FIG. 18C

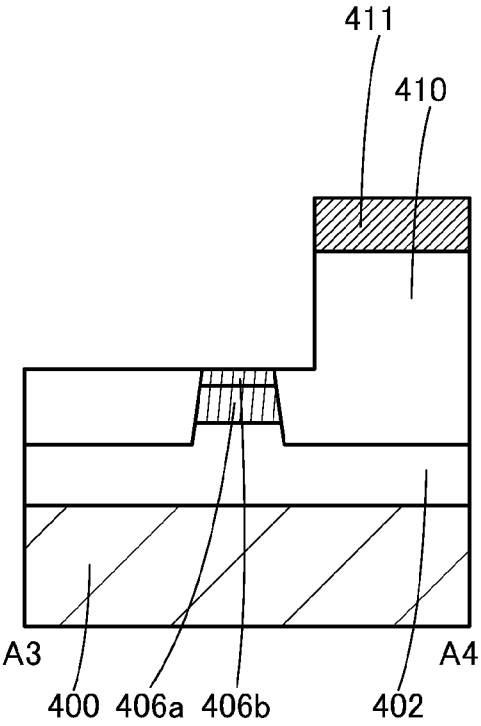


FIG. 19A

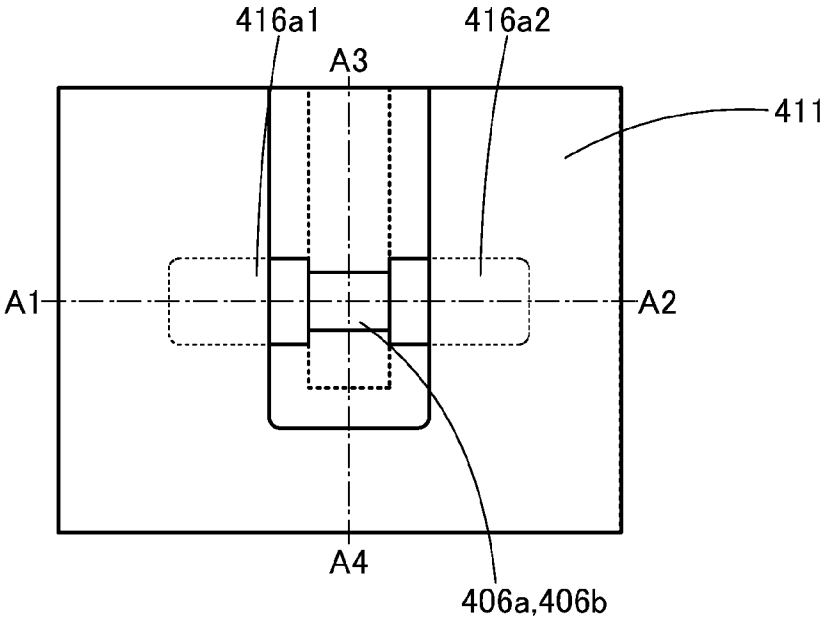


FIG. 19B

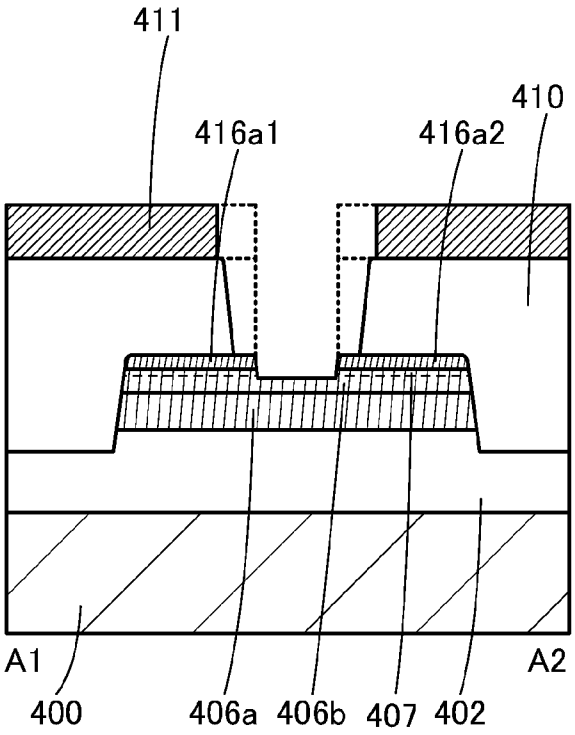


FIG. 19C

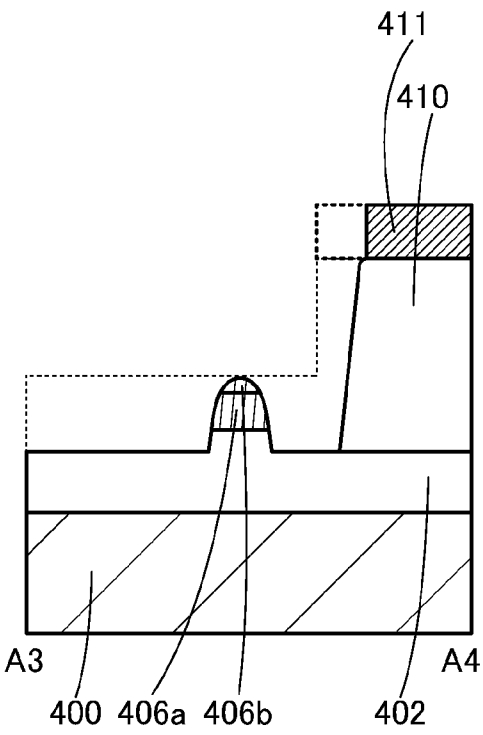


FIG. 20A

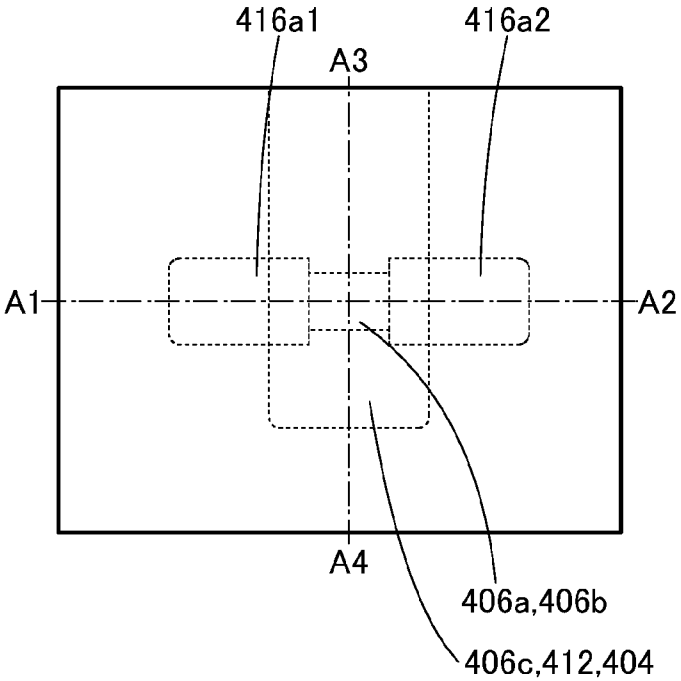


FIG. 20B

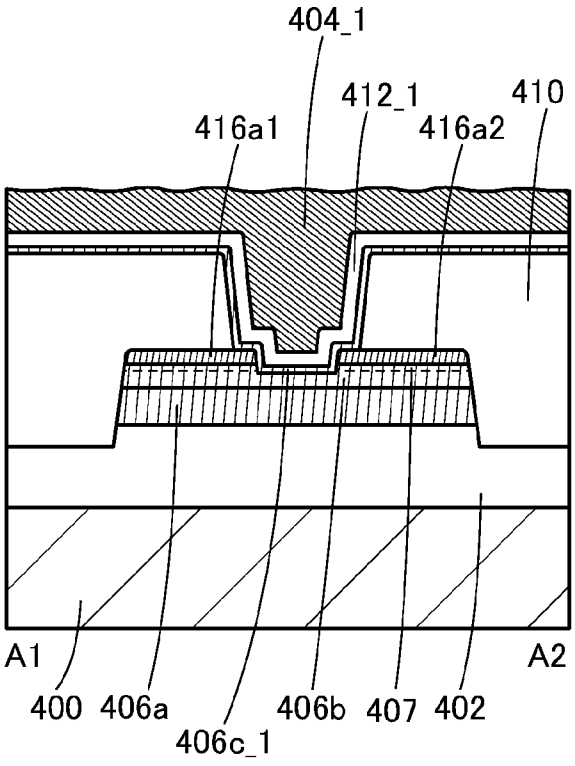


FIG. 20C

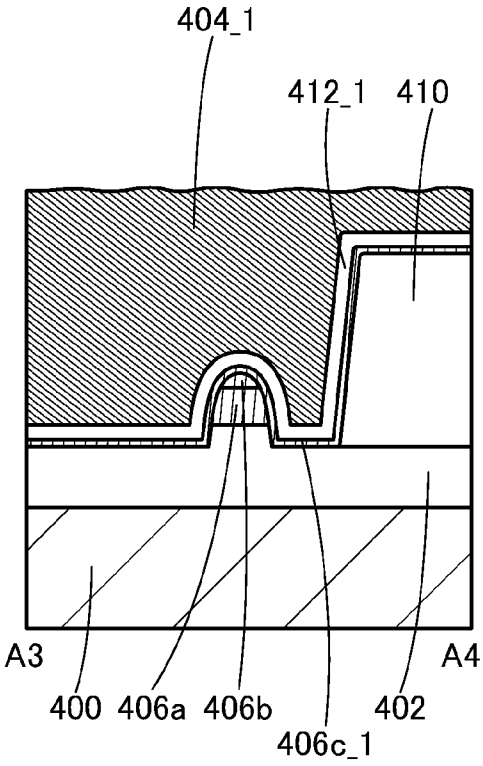


FIG. 21A

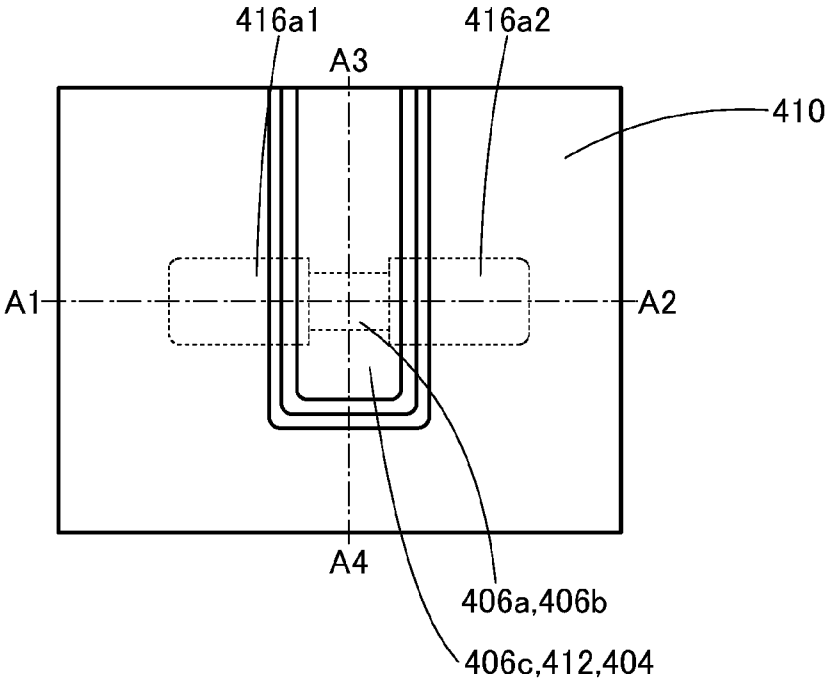


FIG. 21B

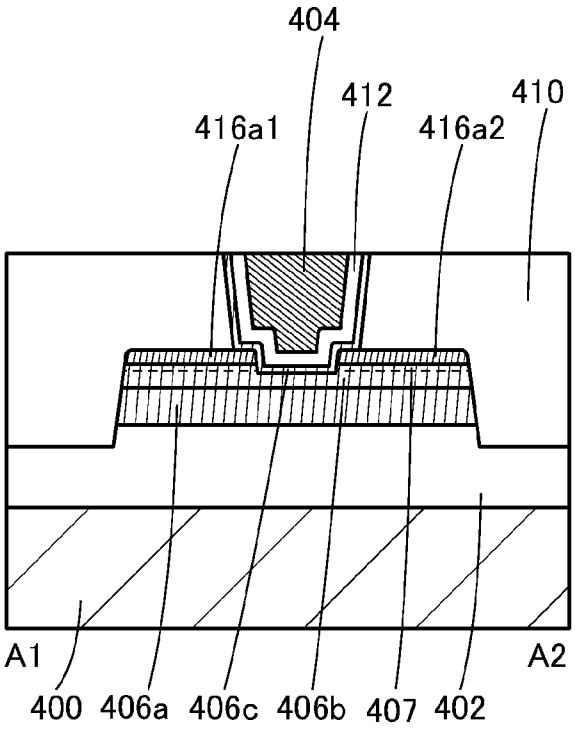


FIG. 21C

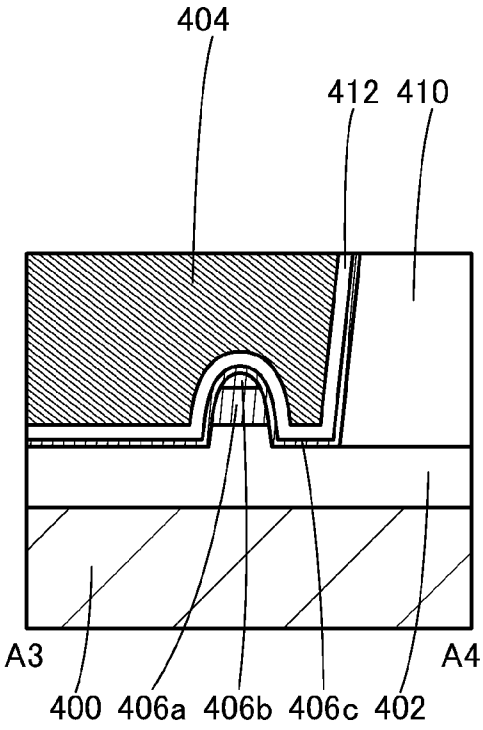


FIG. 22A

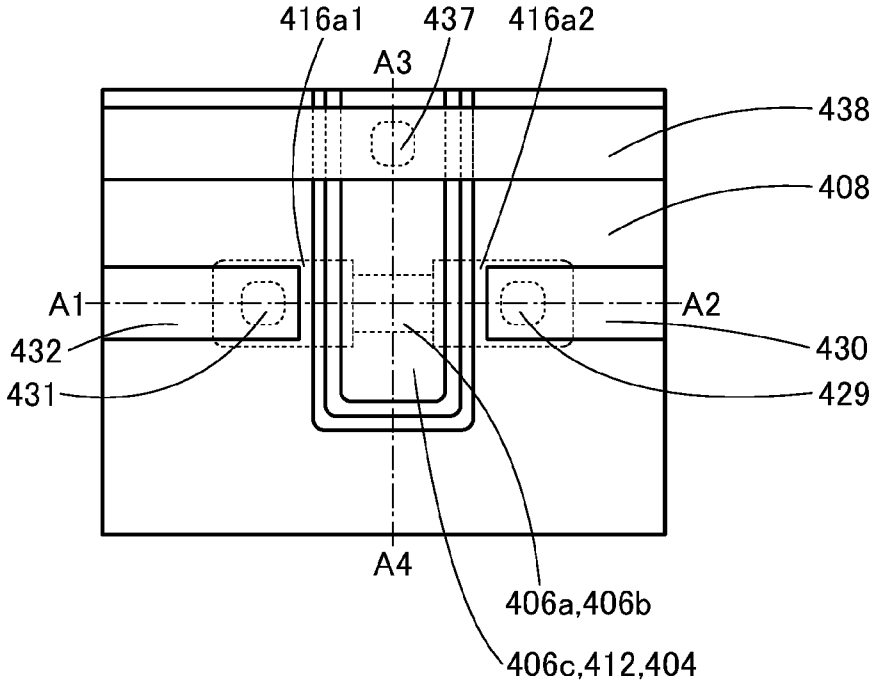


FIG. 22B

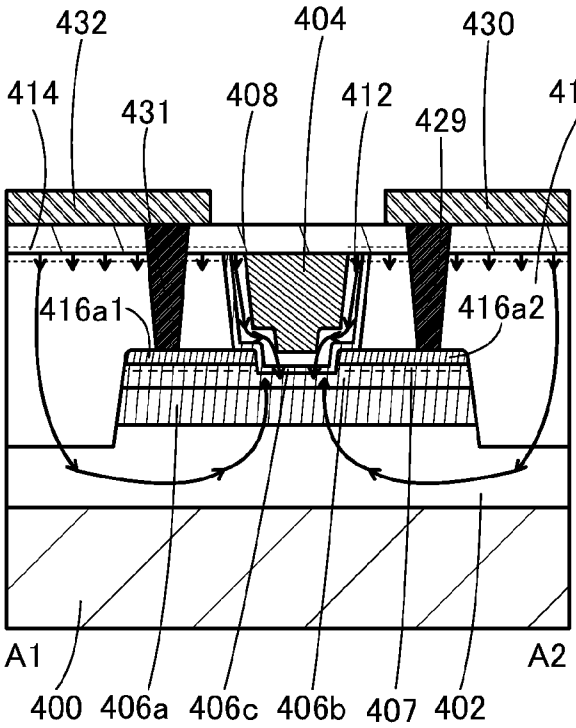


FIG. 22C

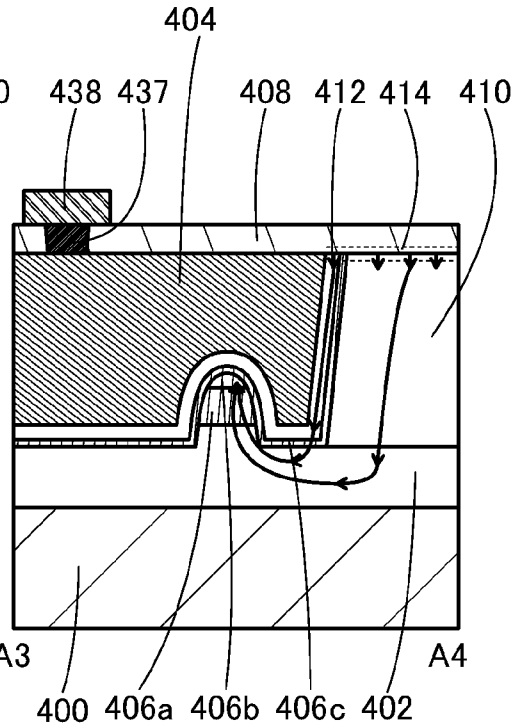


FIG. 23A

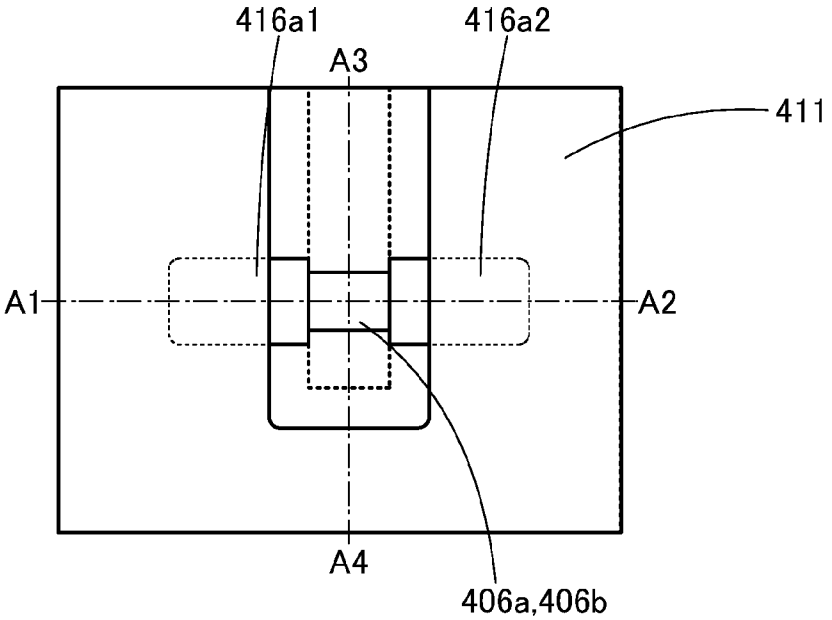


FIG. 23B

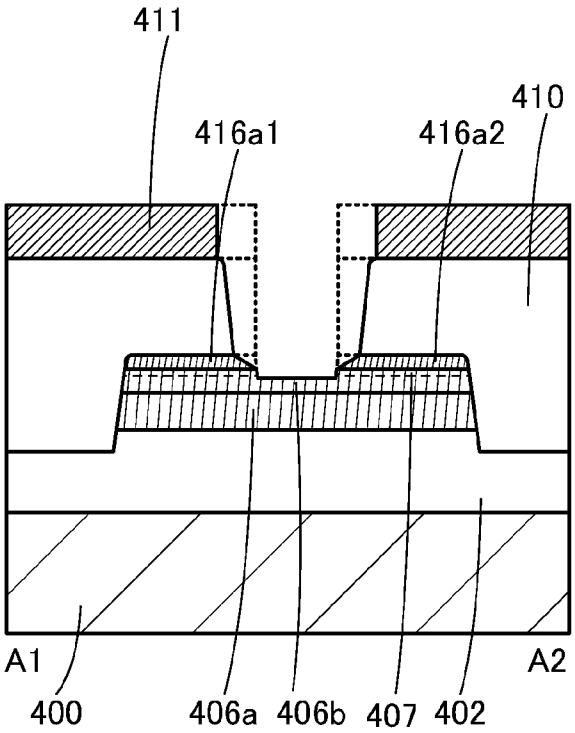


FIG. 23C

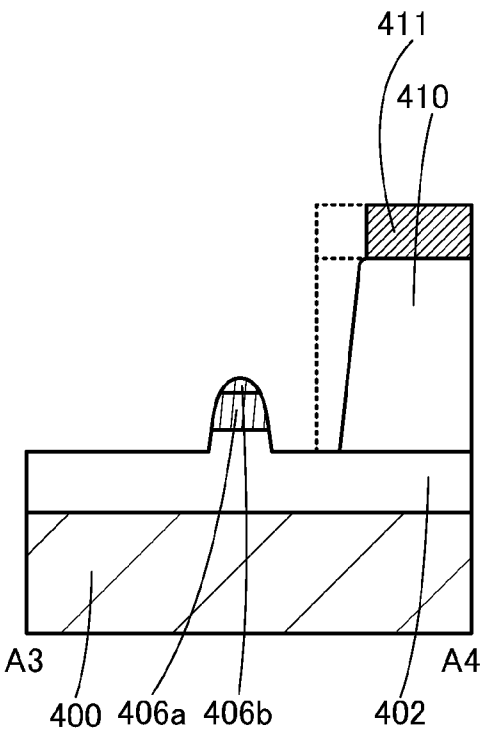


FIG. 24A

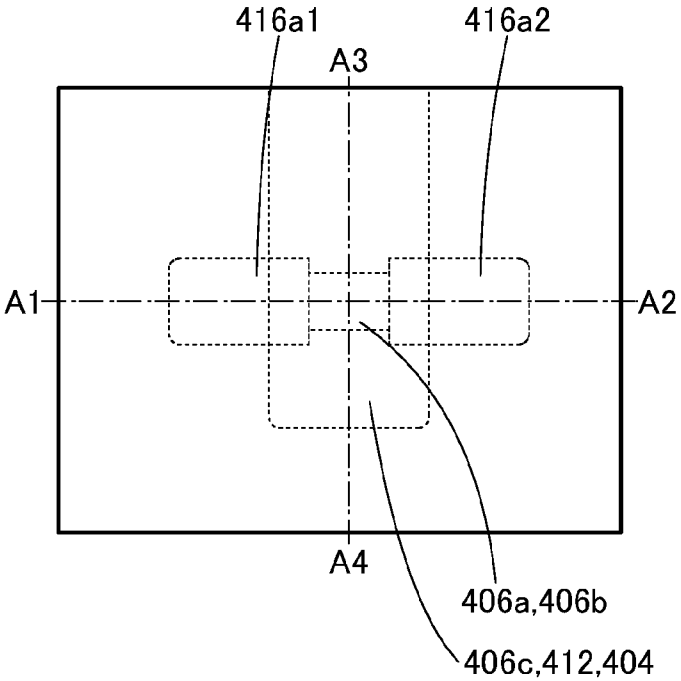


FIG. 24B

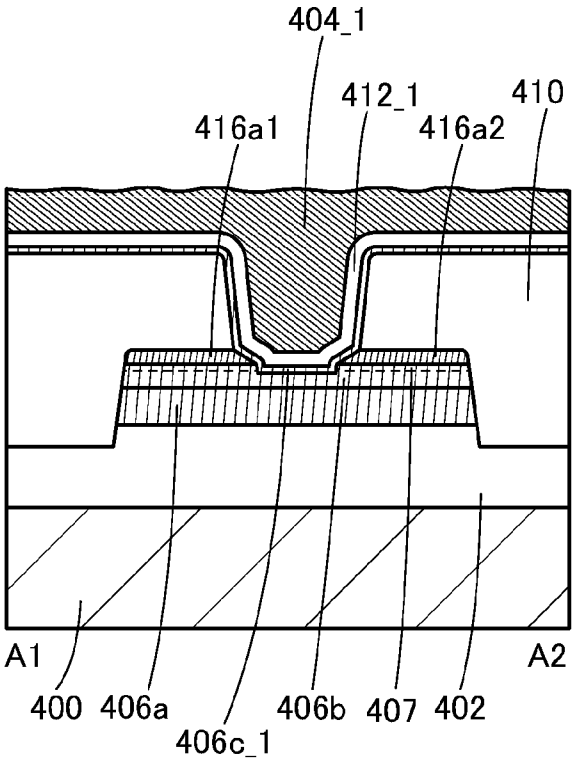


FIG. 24C

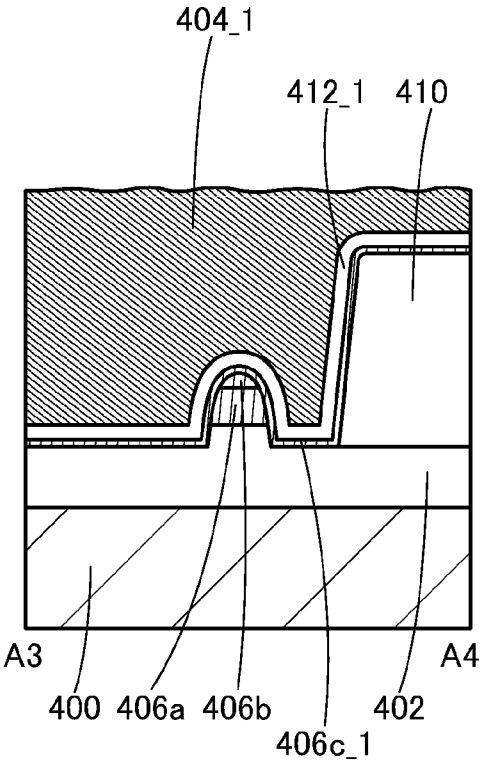


FIG. 25A

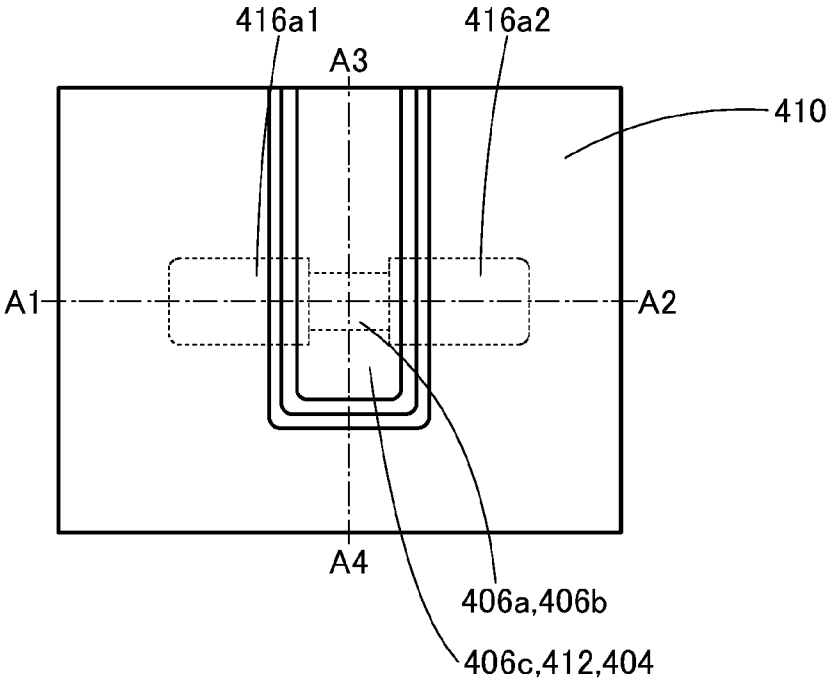


FIG. 25B

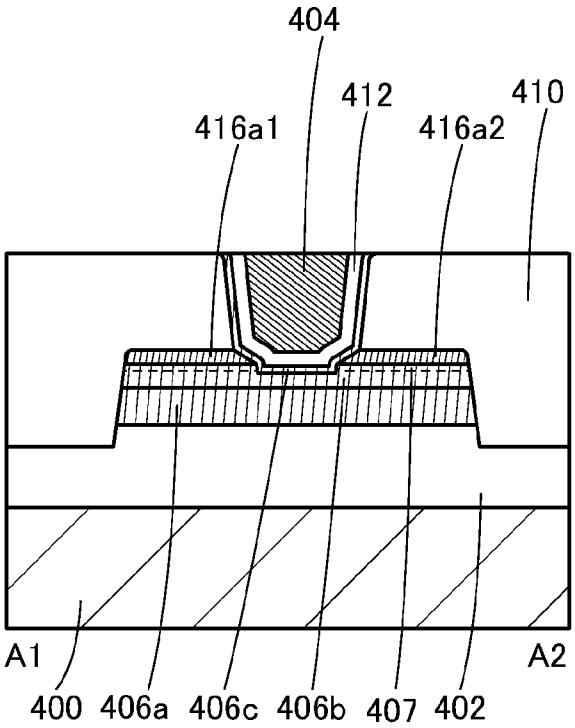


FIG. 25C

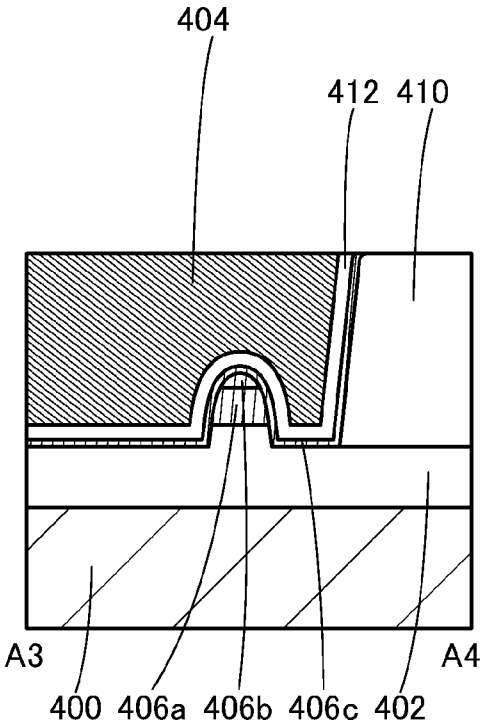


FIG. 26A

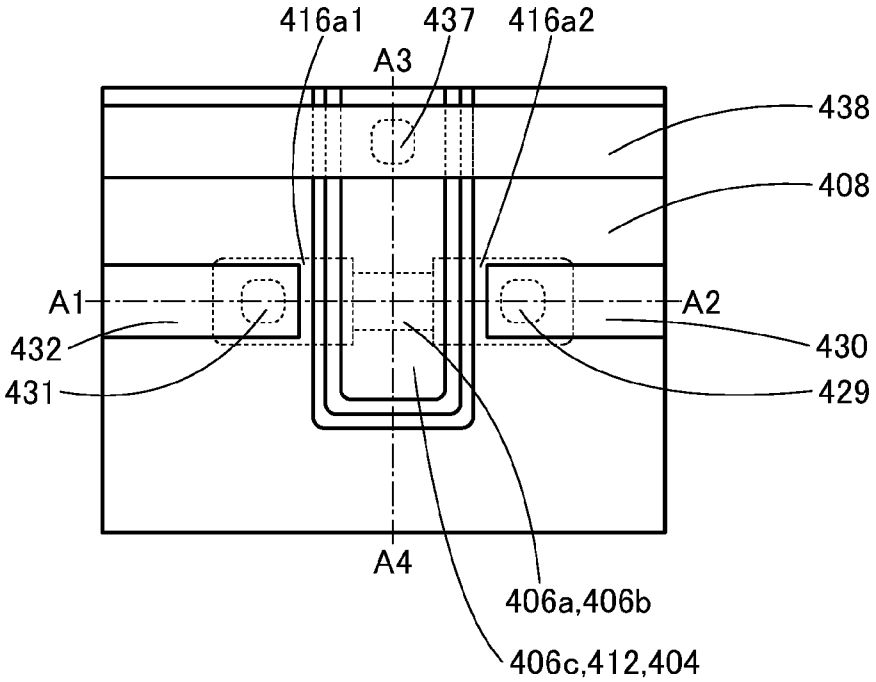


FIG. 26B

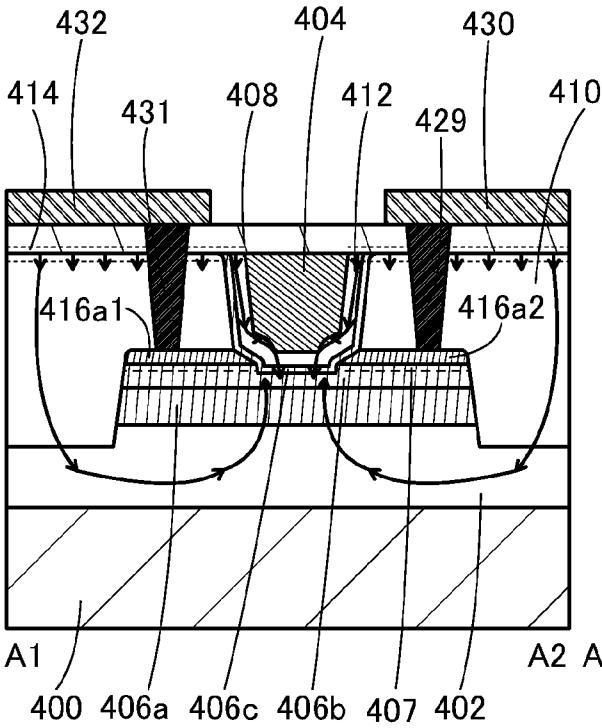


FIG. 26C

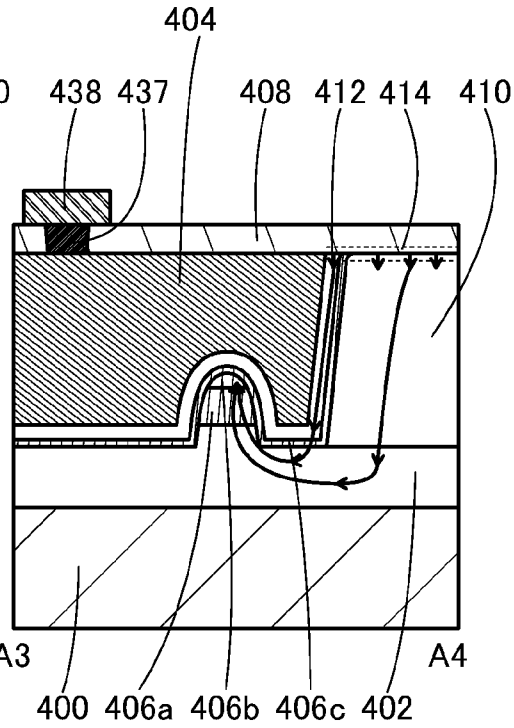


FIG. 27A

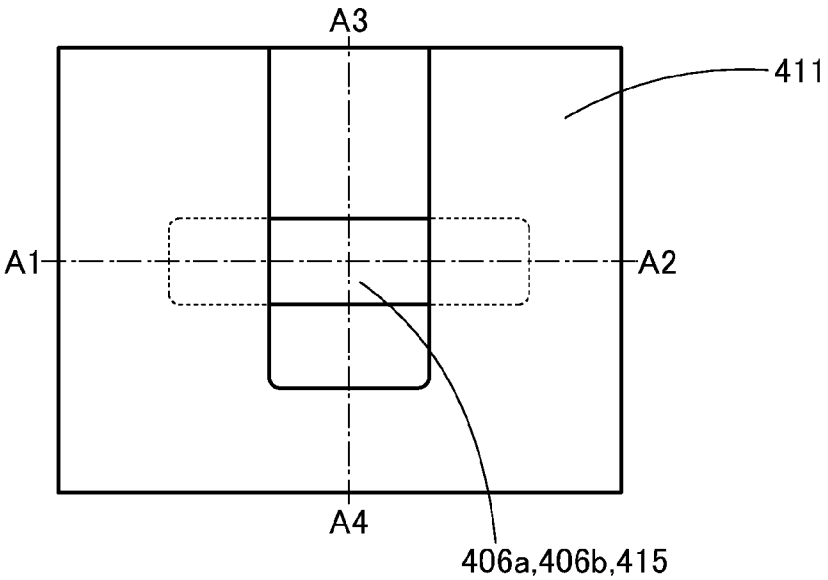


FIG. 27B

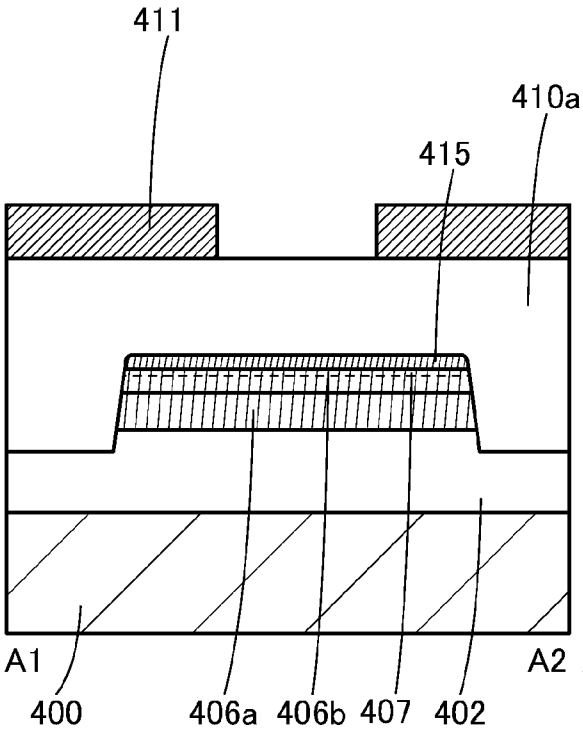


FIG. 27C

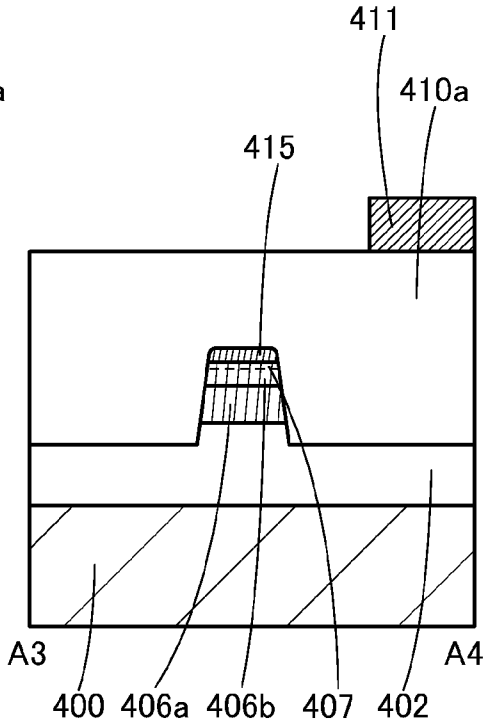


FIG. 28A

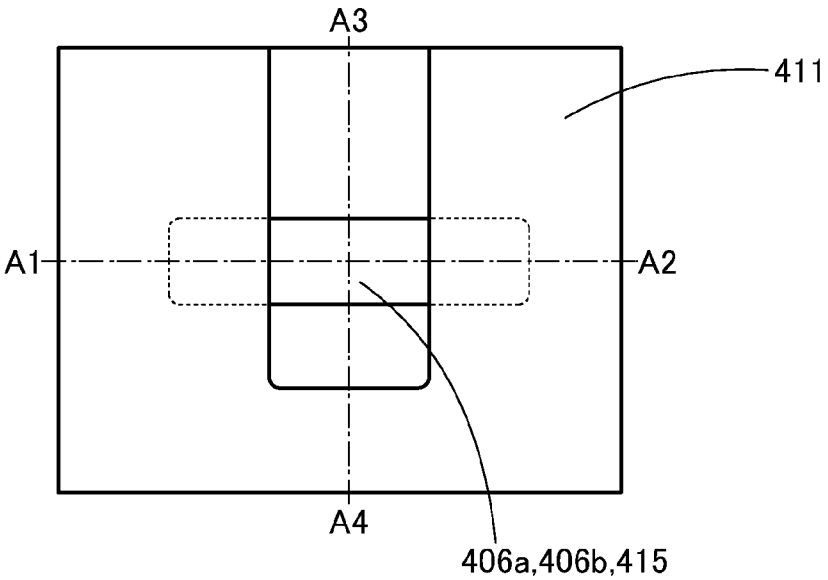


FIG. 28B

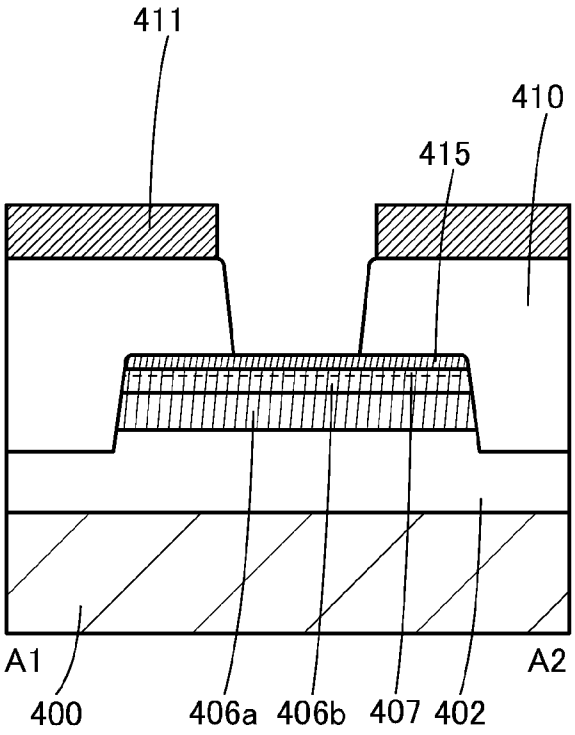


FIG. 28C

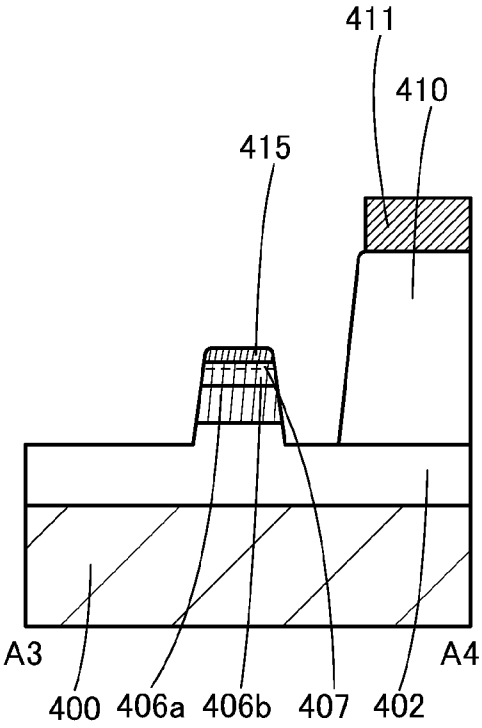


FIG. 29A

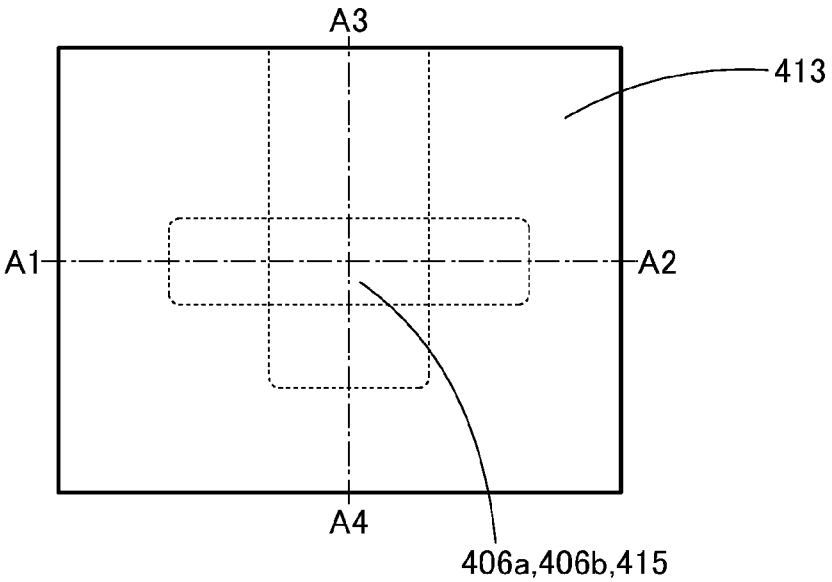


FIG. 29B

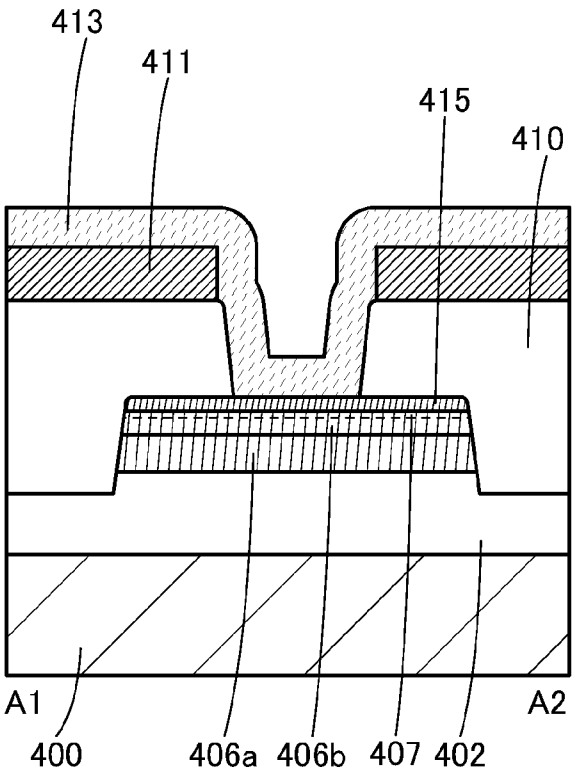


FIG. 29C

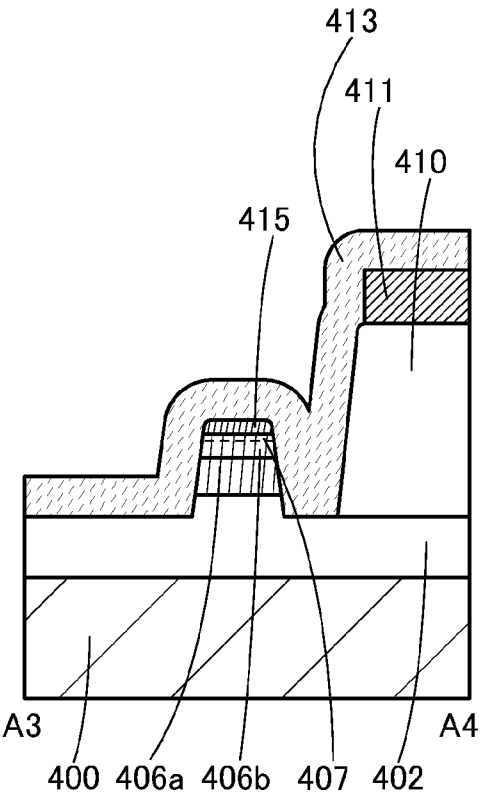


FIG. 30A

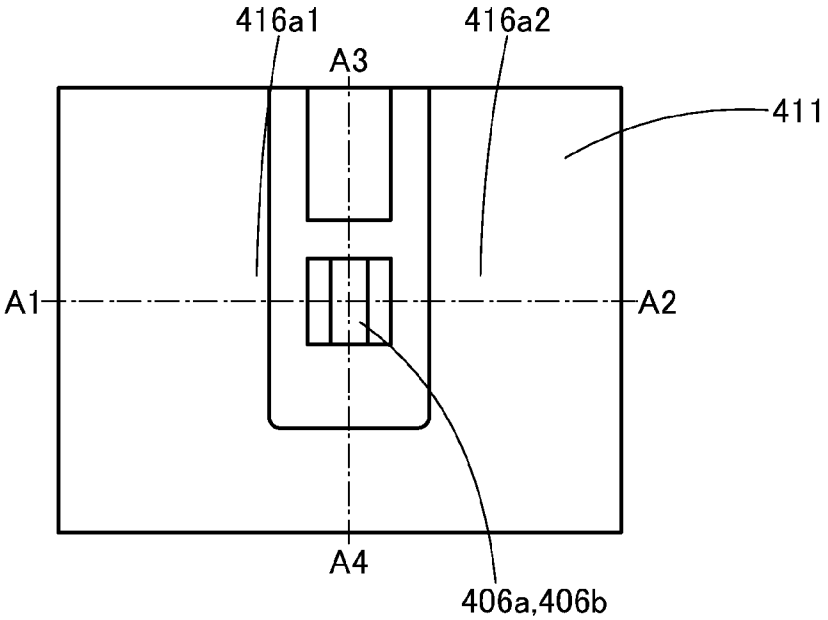


FIG. 30B

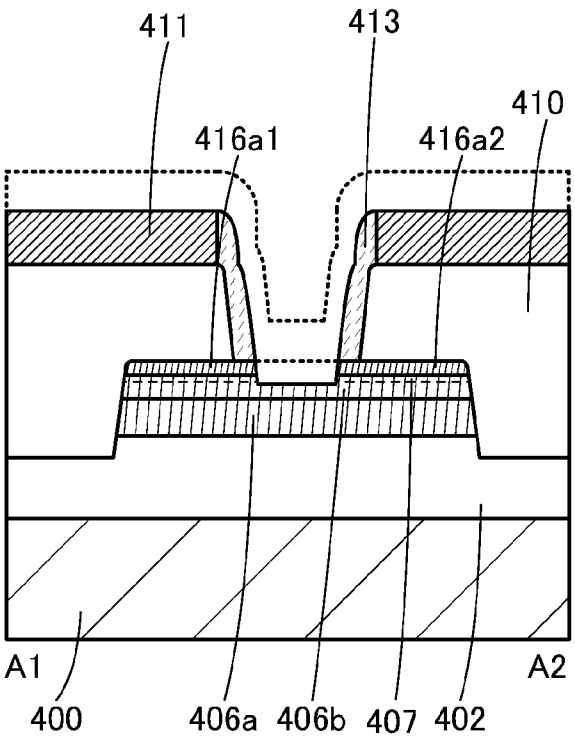


FIG. 30C

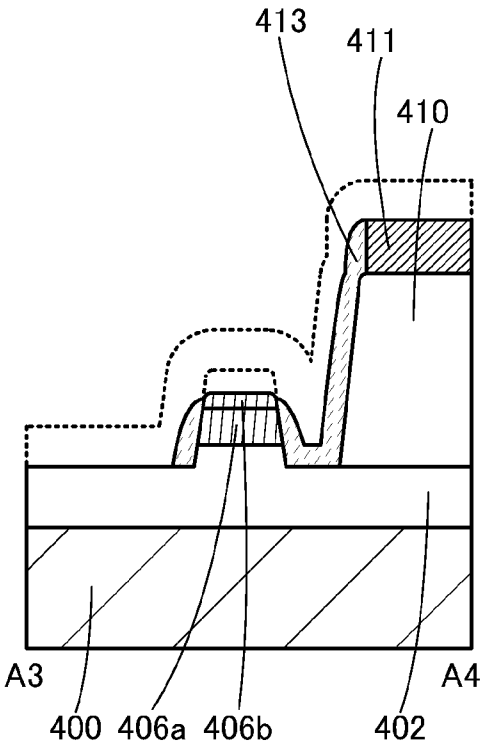


FIG. 31A

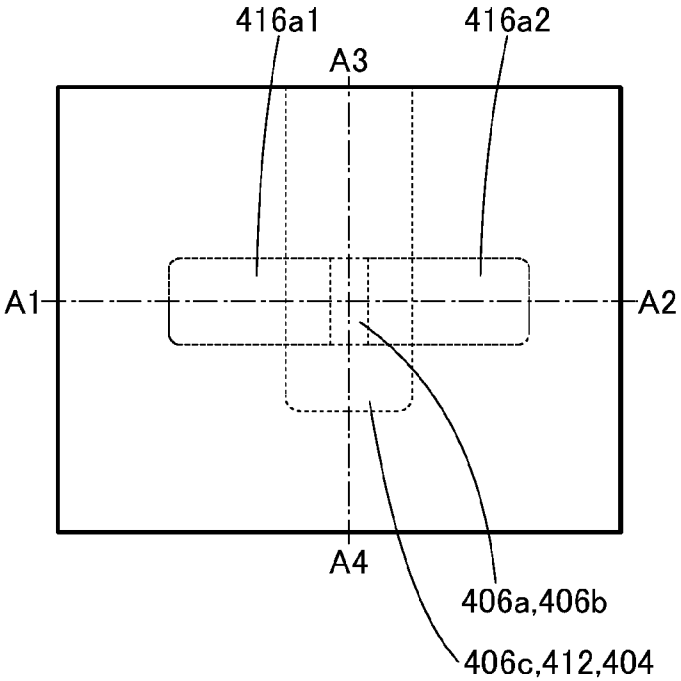


FIG. 31B

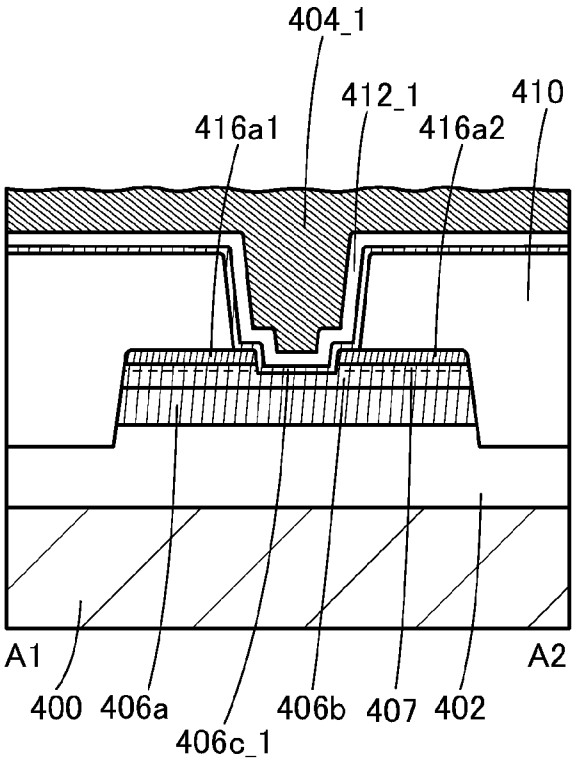


FIG. 31C

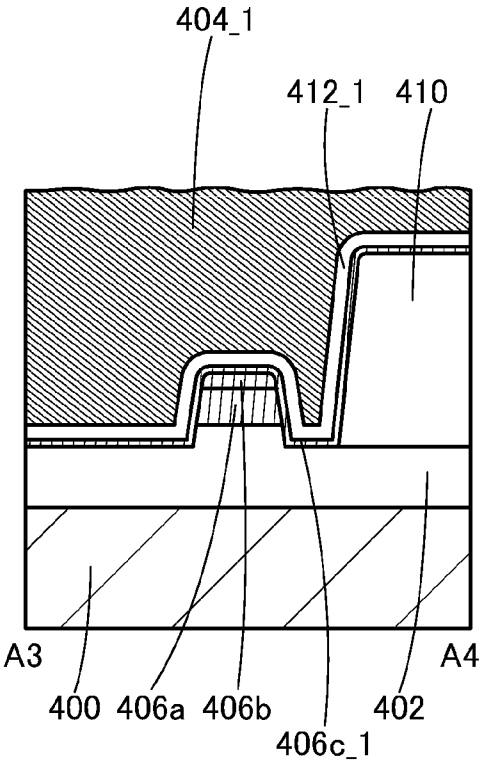


FIG. 32A

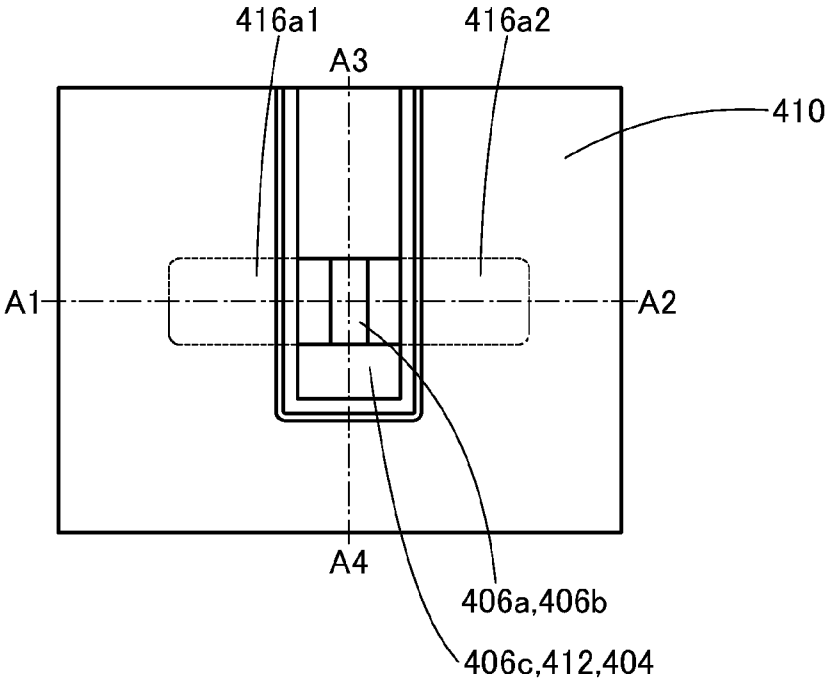


FIG. 32B

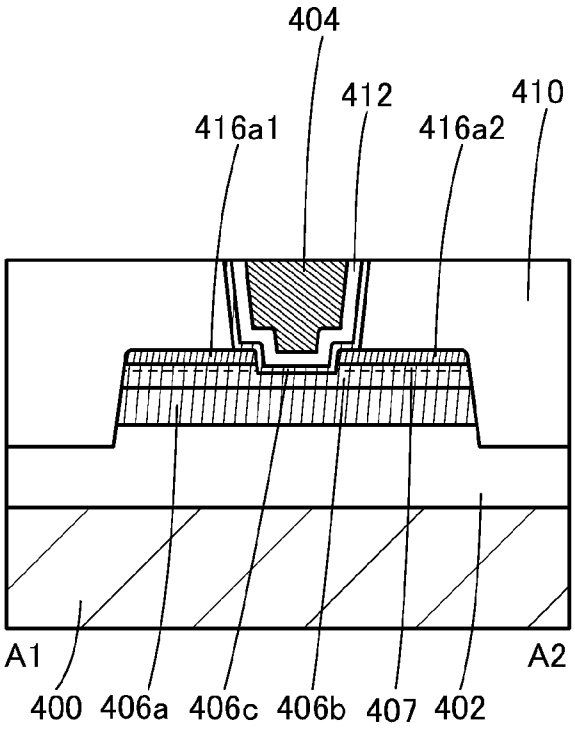


FIG. 32C

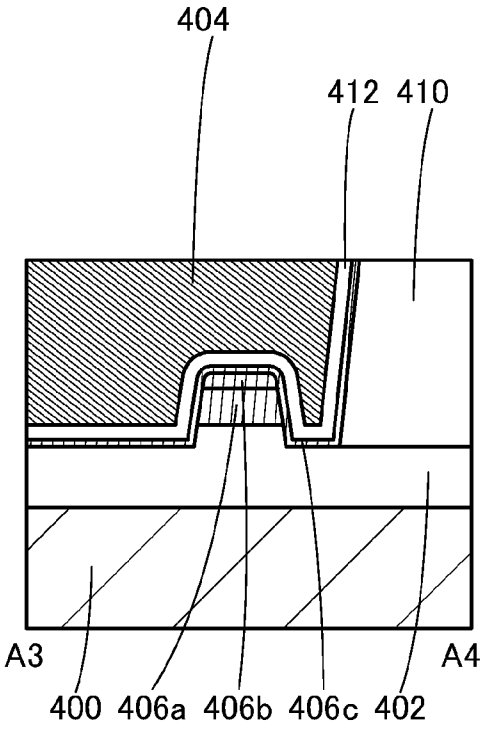


FIG. 33A

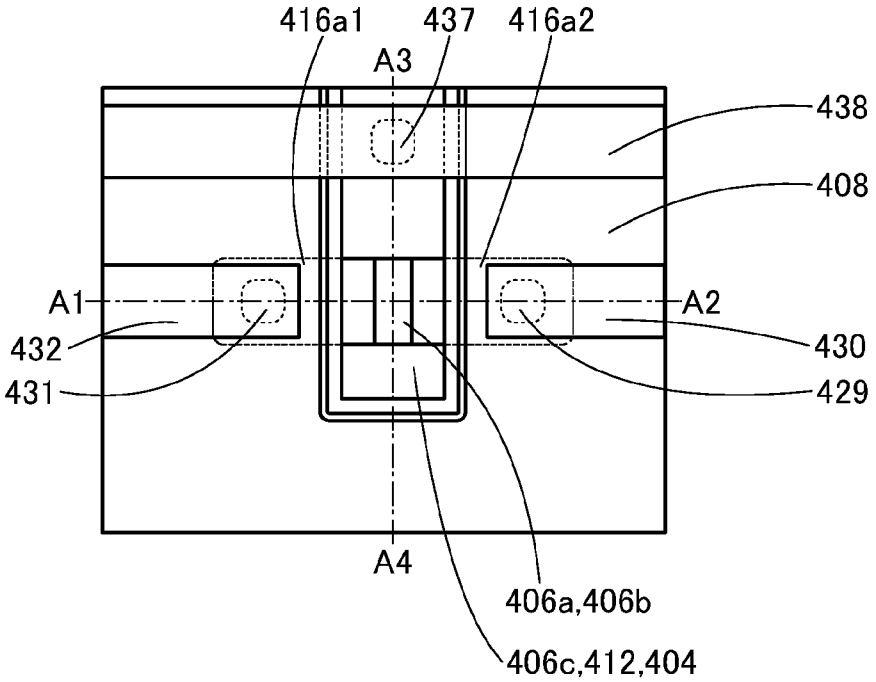


FIG. 33B

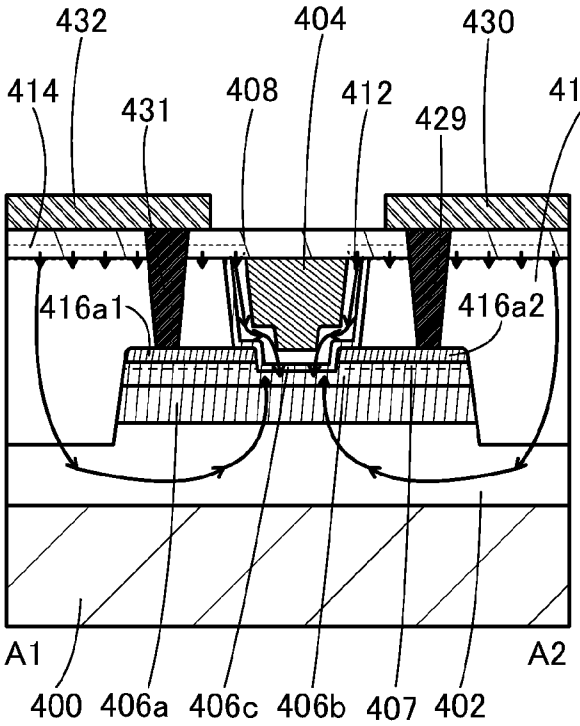


FIG. 33C

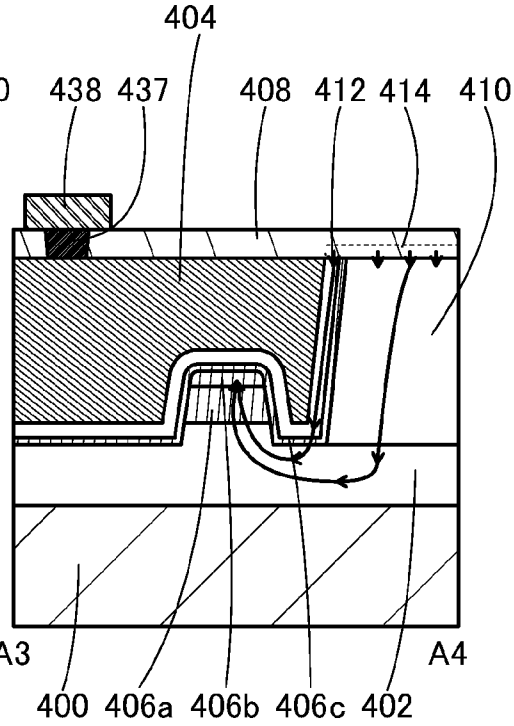


FIG. 34A

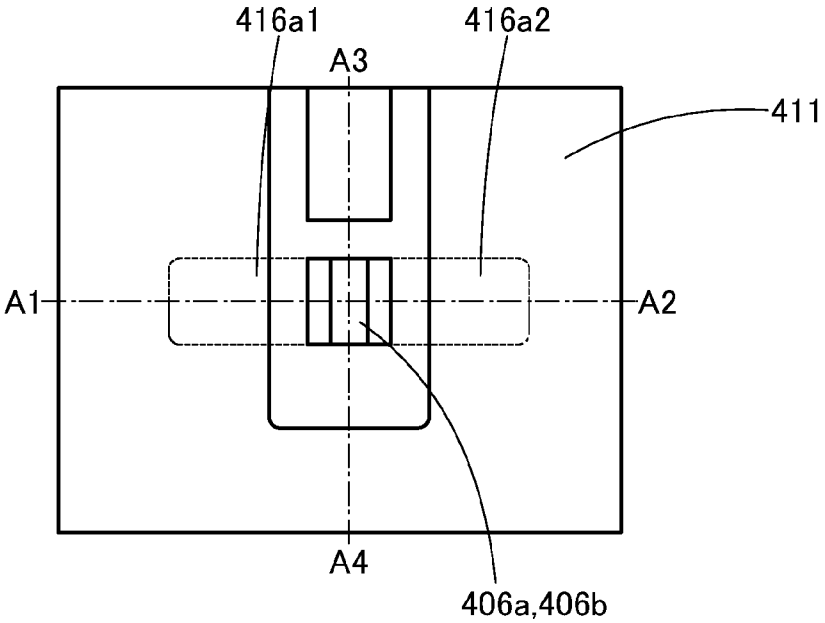


FIG. 34B

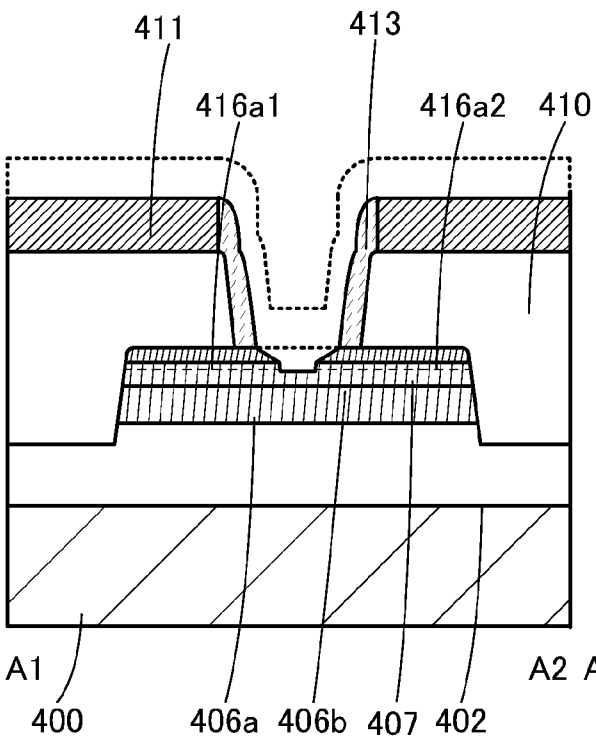


FIG. 34C

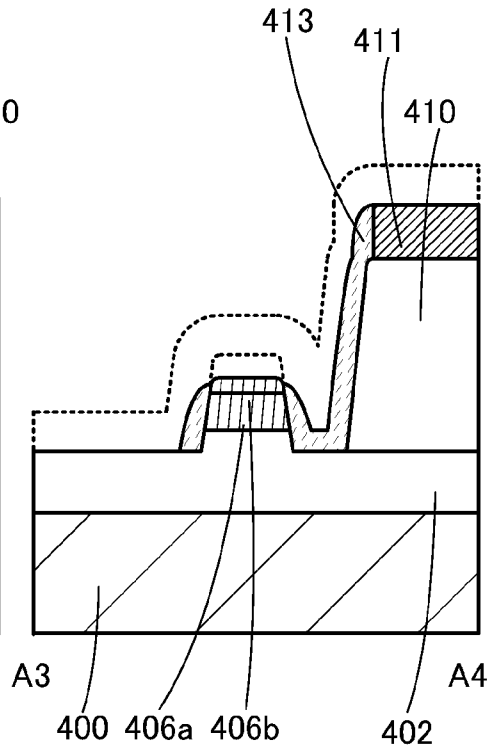


FIG. 35A

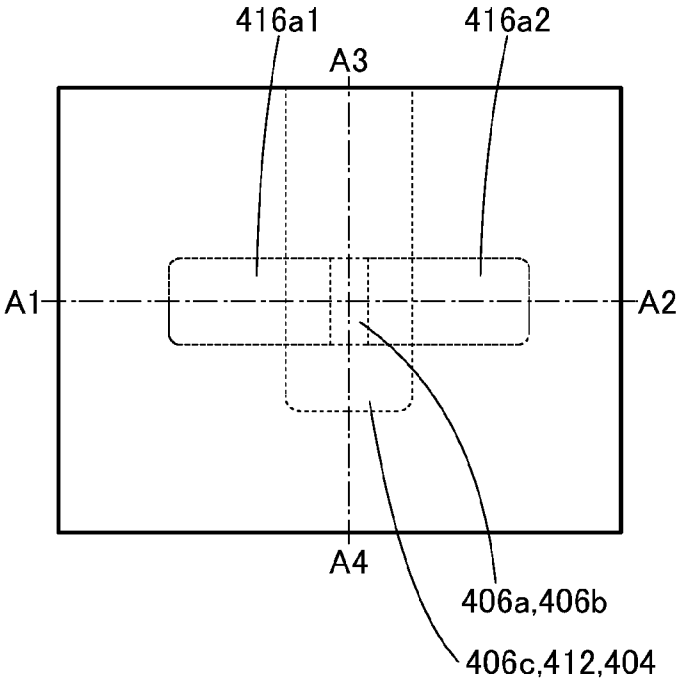


FIG. 35B

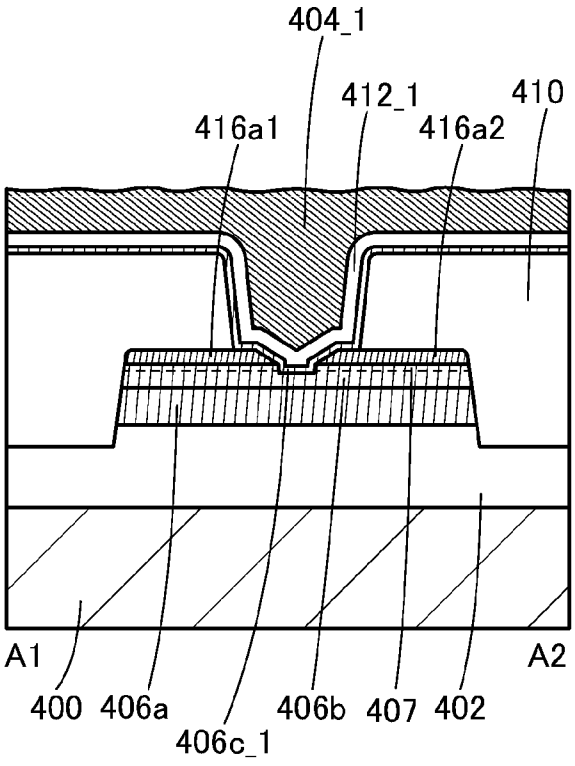


FIG. 35C

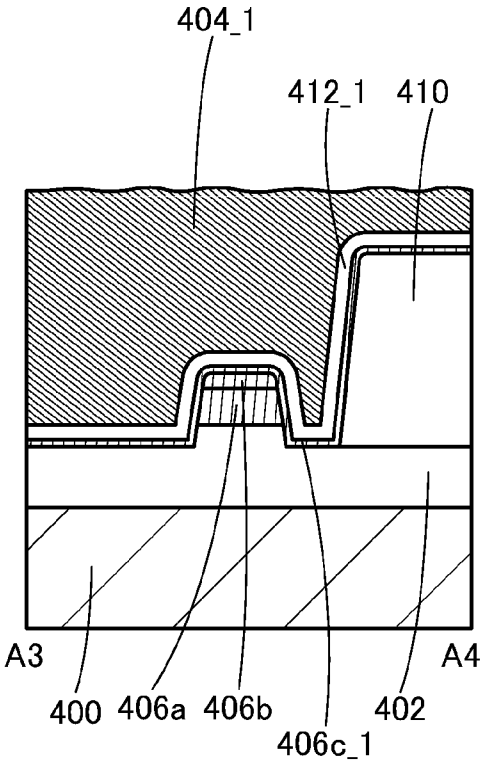


FIG. 36A

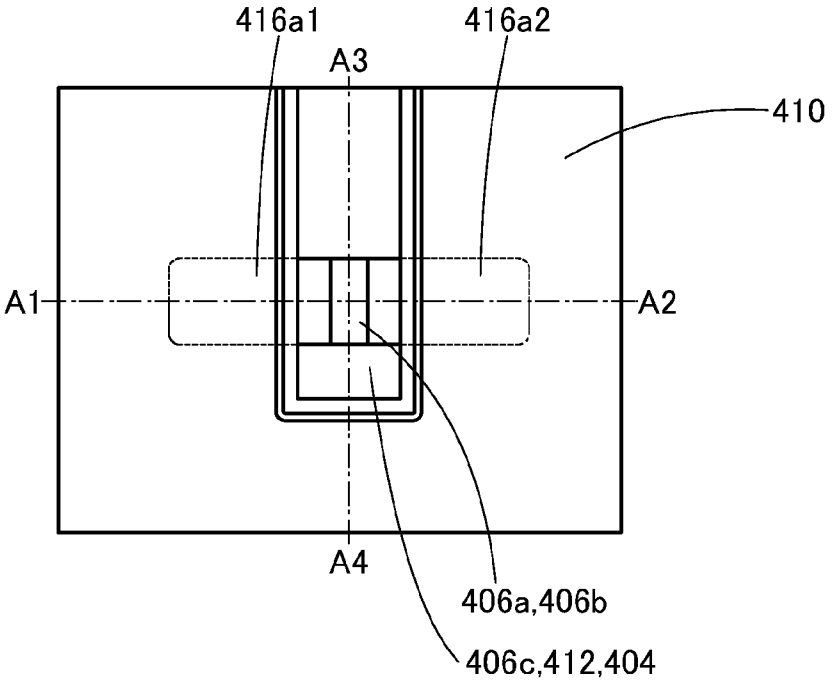


FIG. 36B

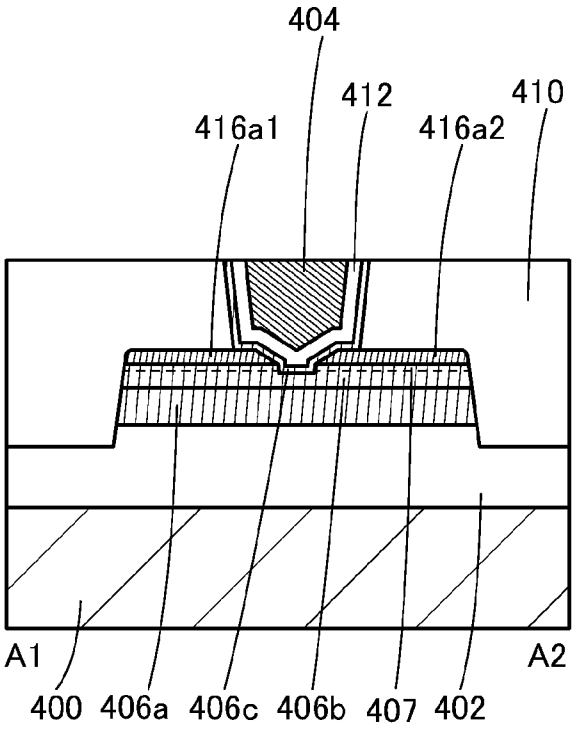


FIG. 36C

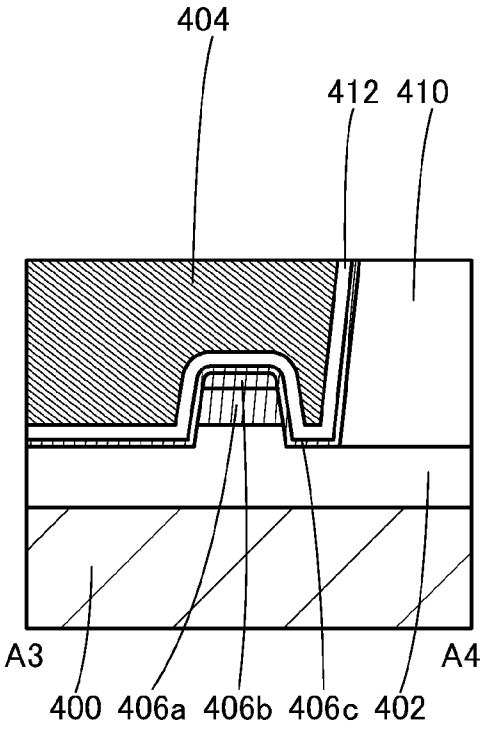


FIG. 37A

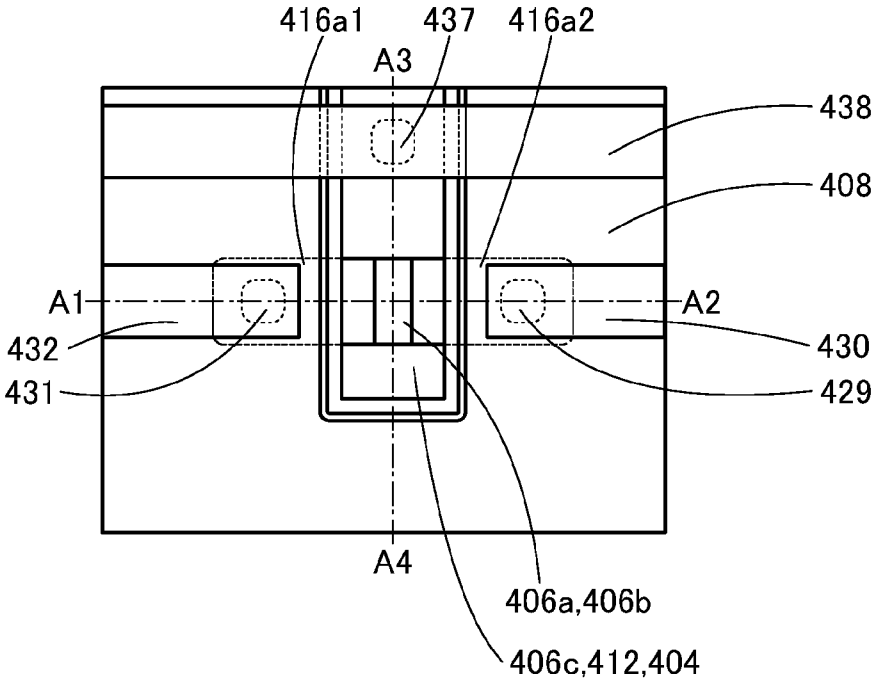


FIG. 37B

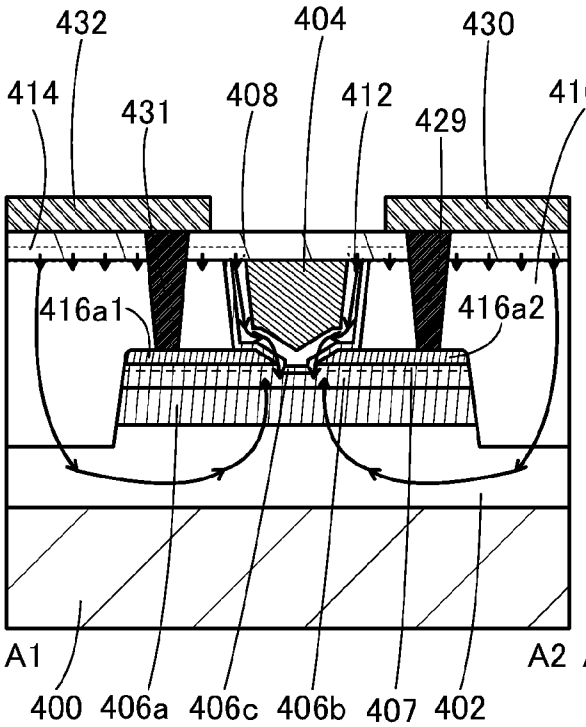


FIG. 37C

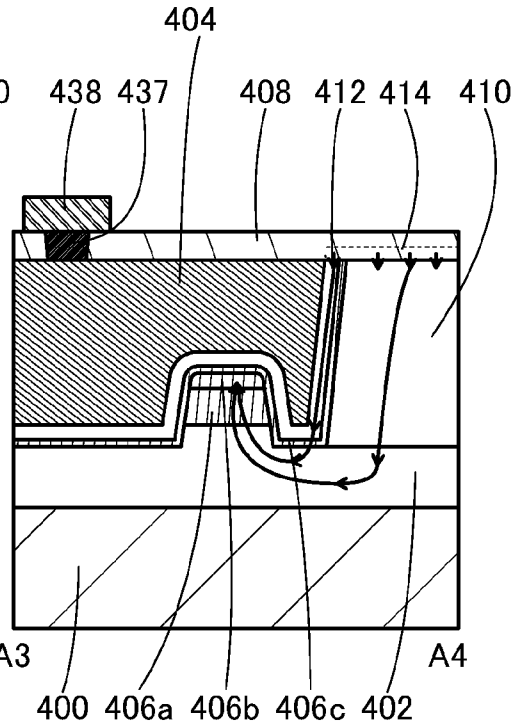


FIG. 38A

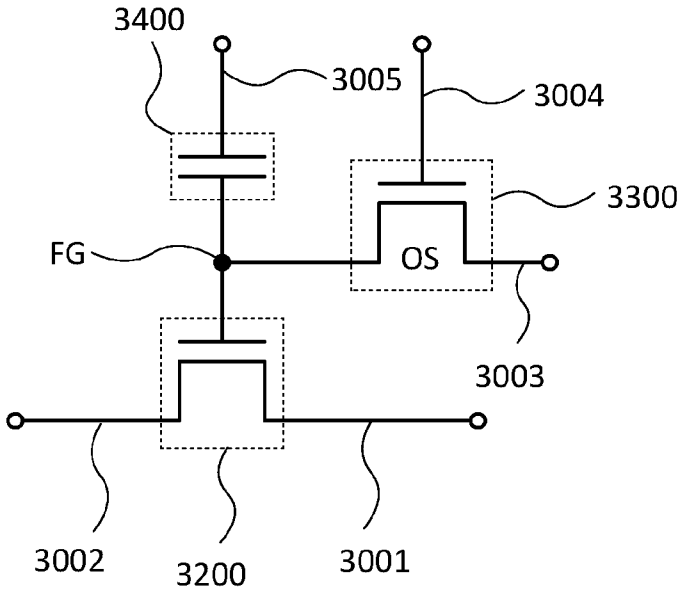


FIG. 38B

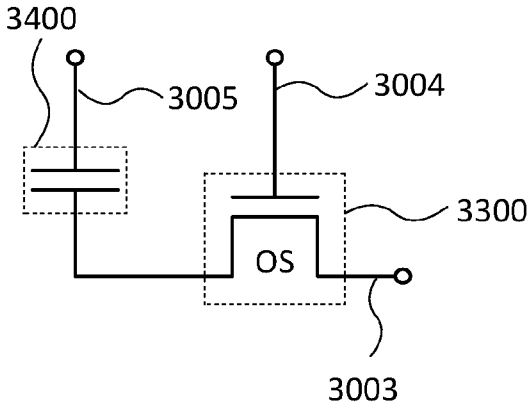


FIG. 39

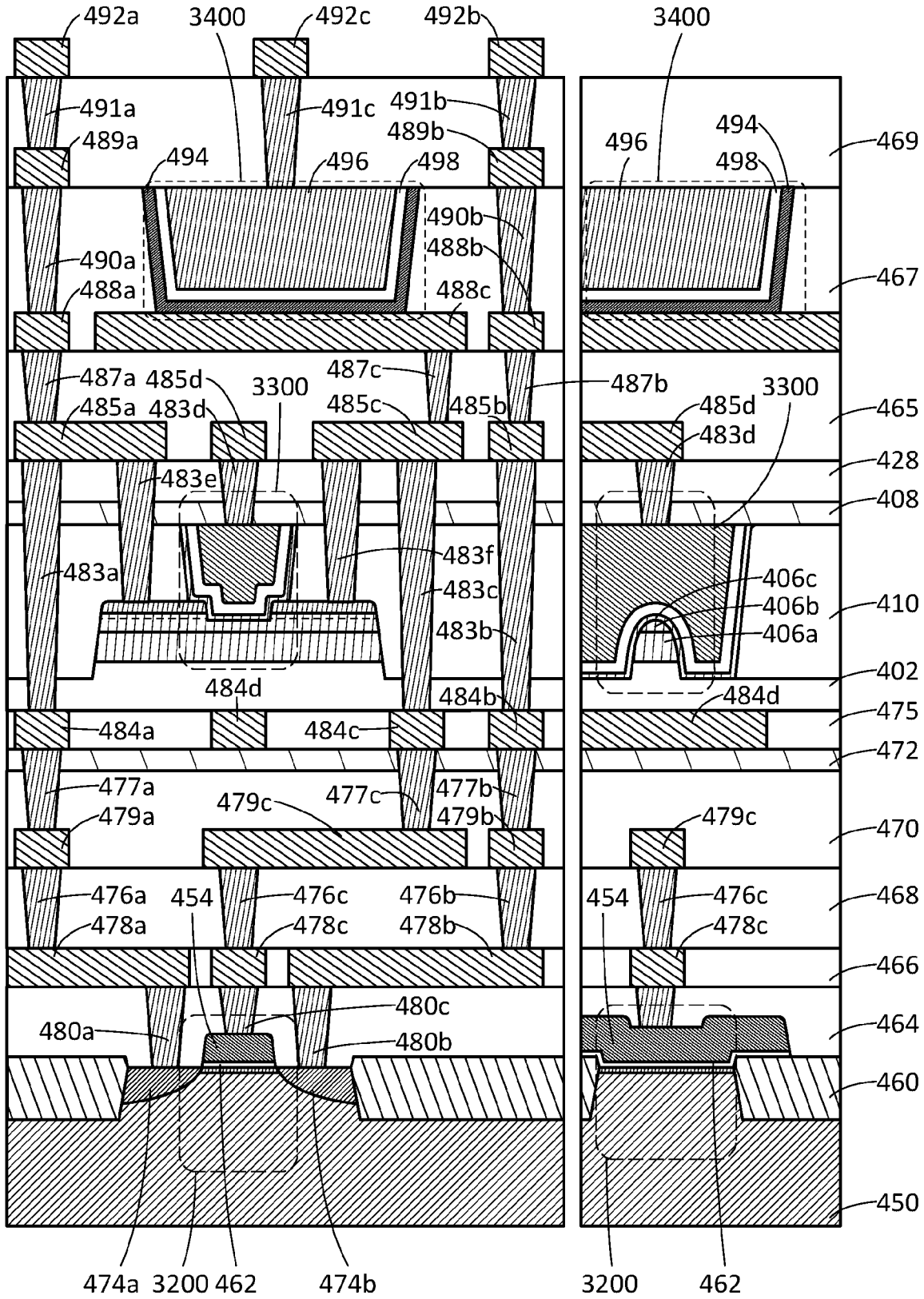

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FIG. 40

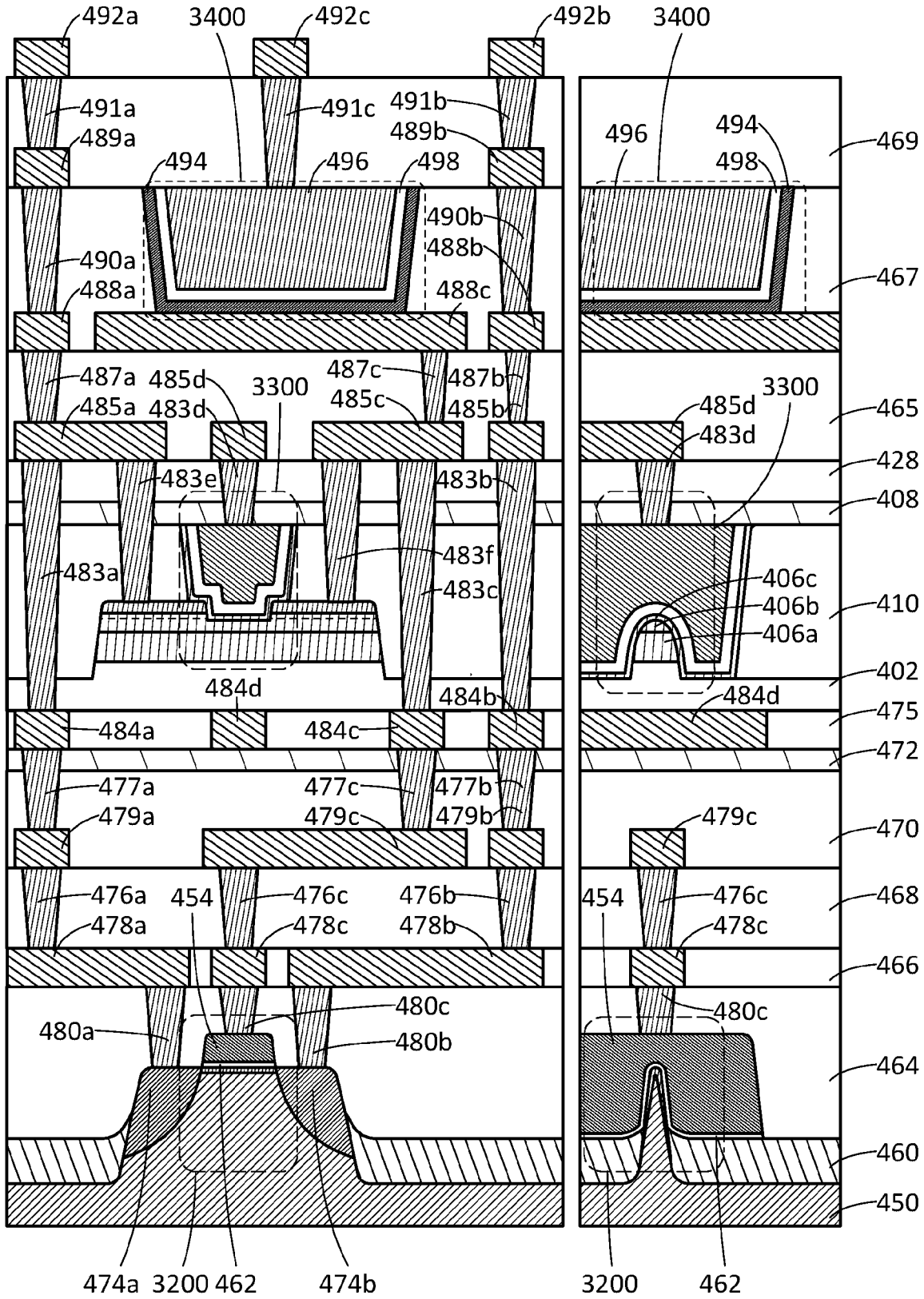

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FIG. 41A

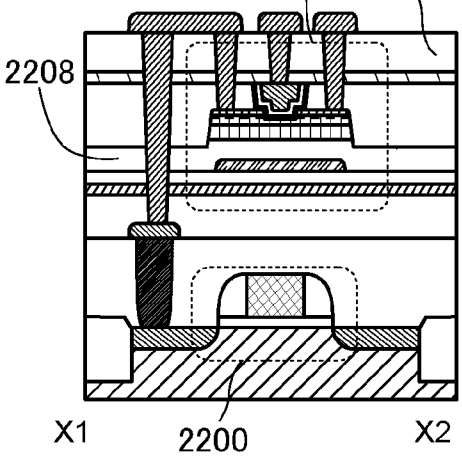


FIG. 41B

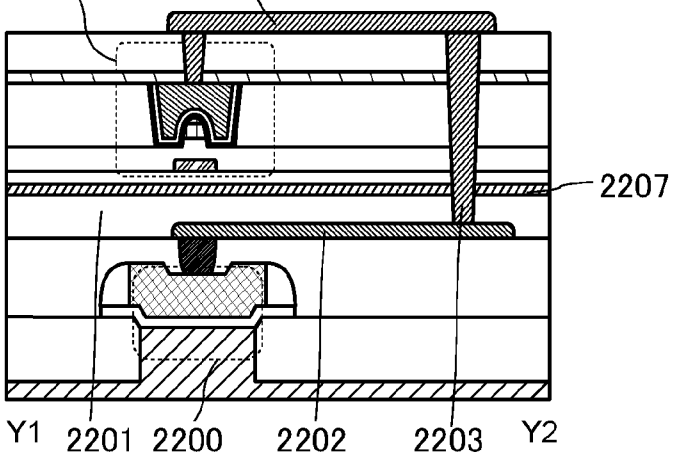


FIG. 41C

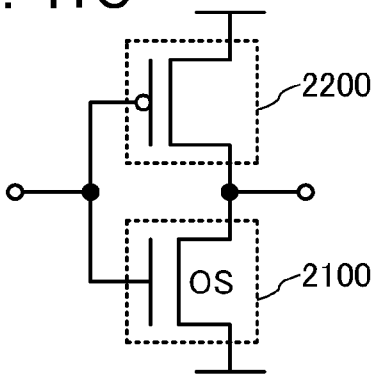


FIG. 41D

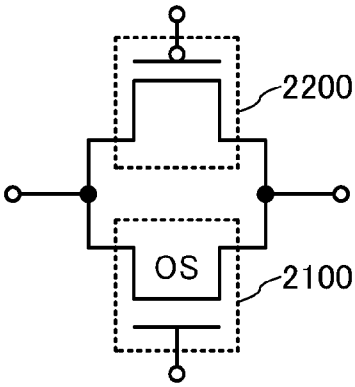


FIG. 41E

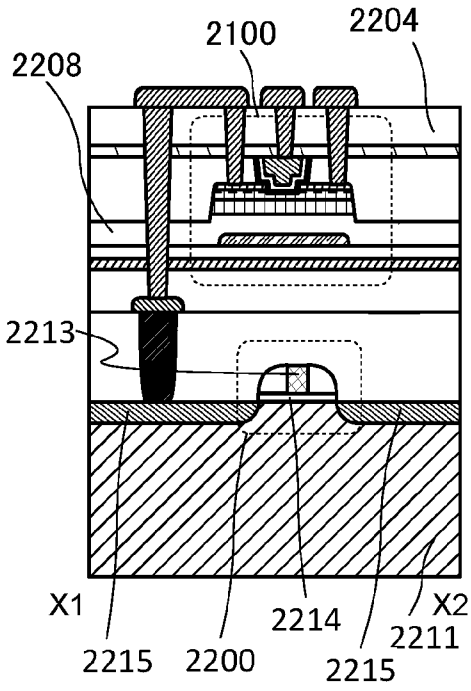


FIG. 41F

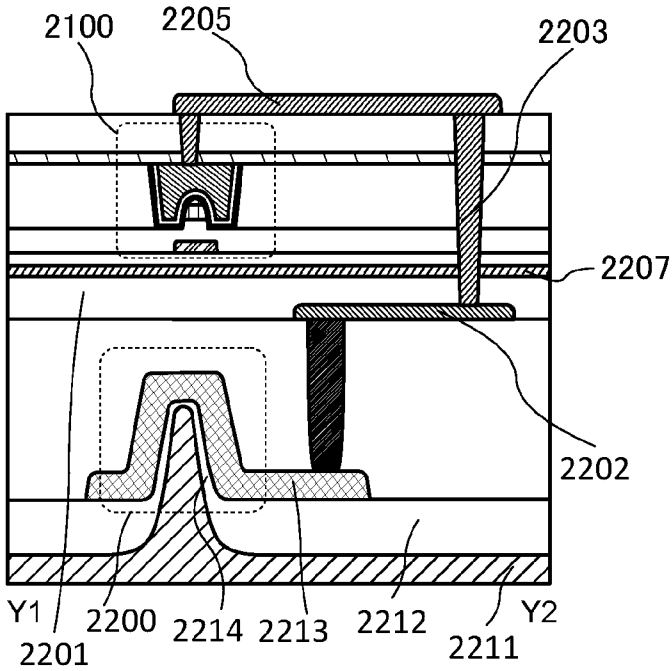


FIG. 42

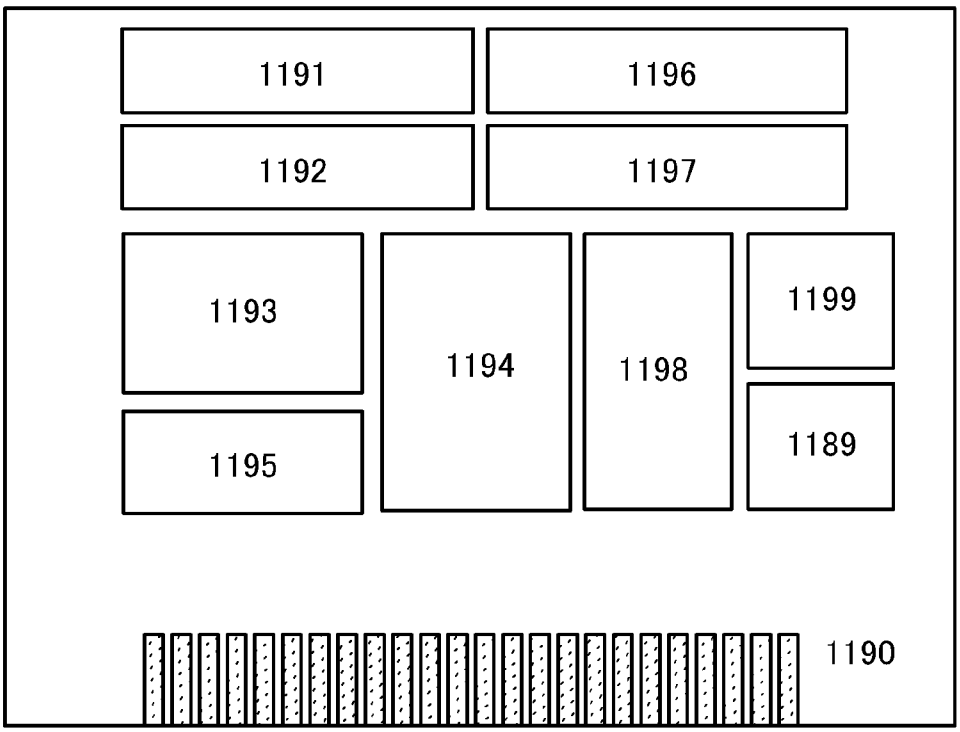


FIG. 43

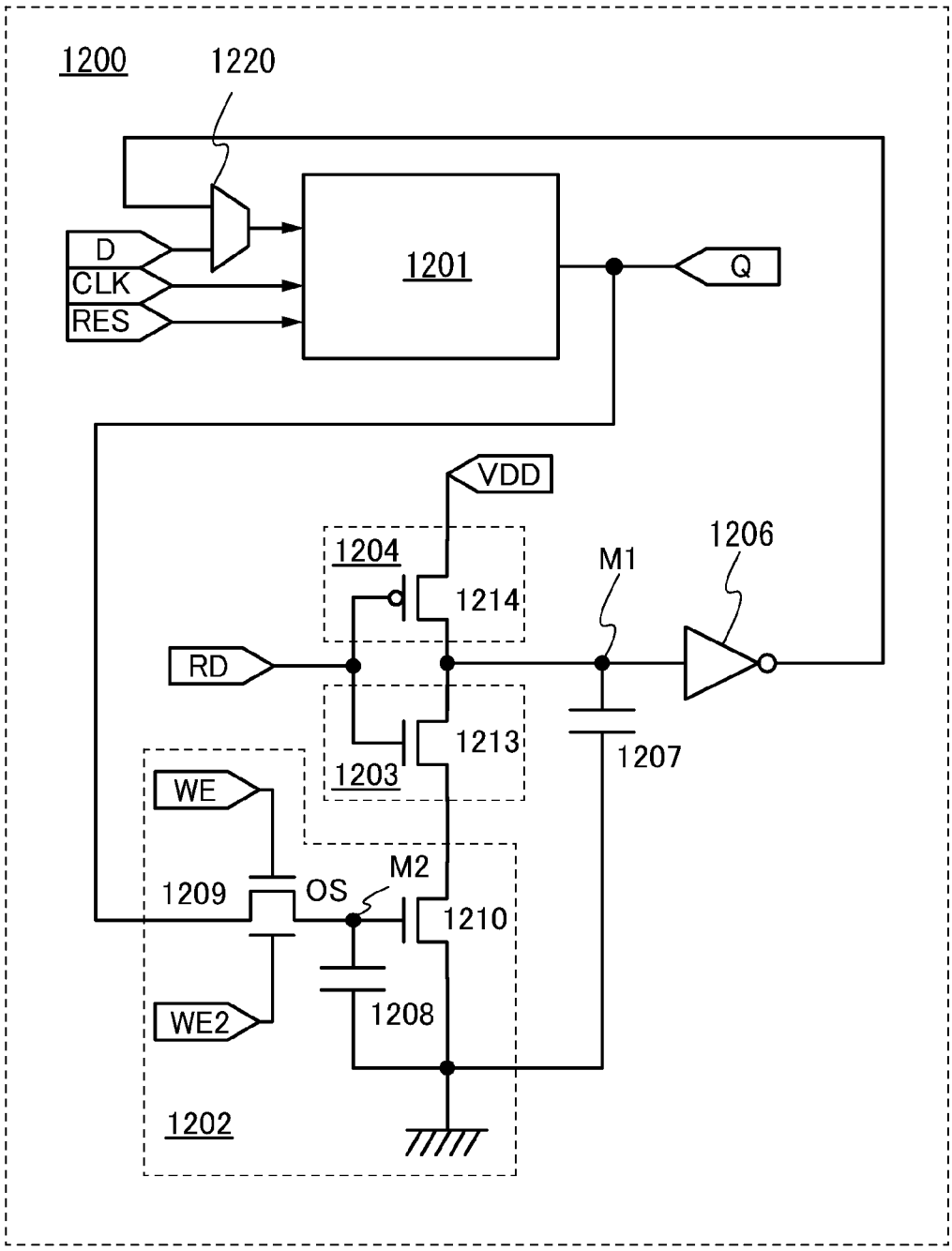

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FIG. 44A

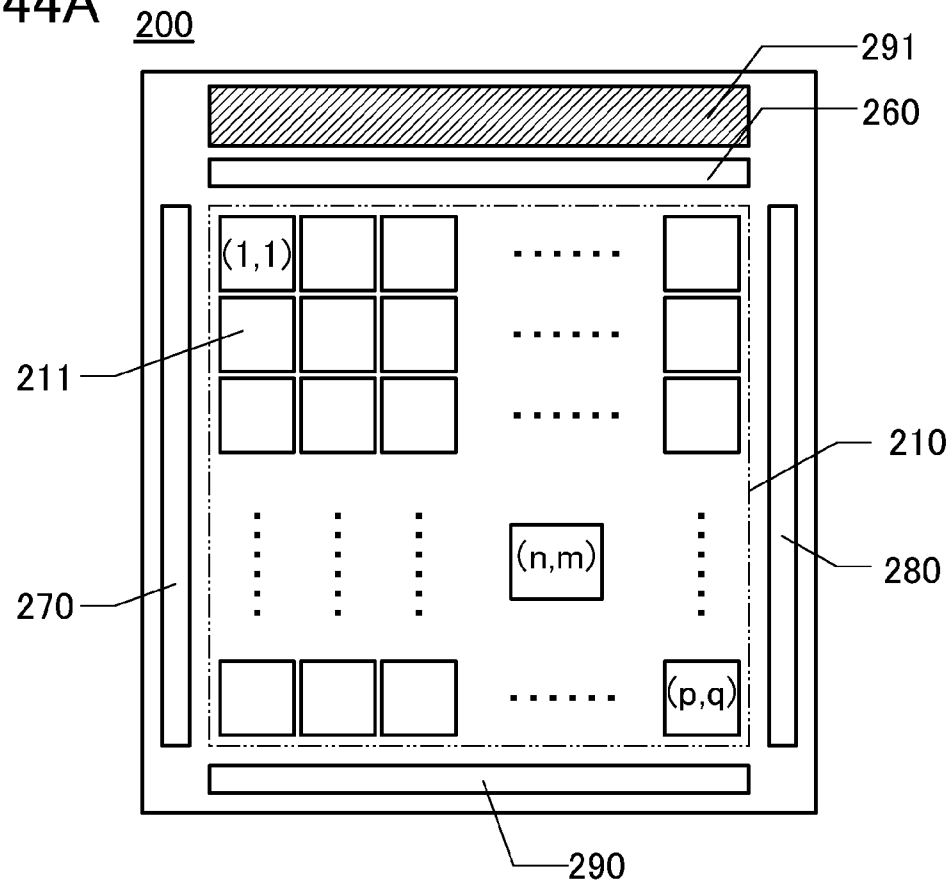


FIG. 44B

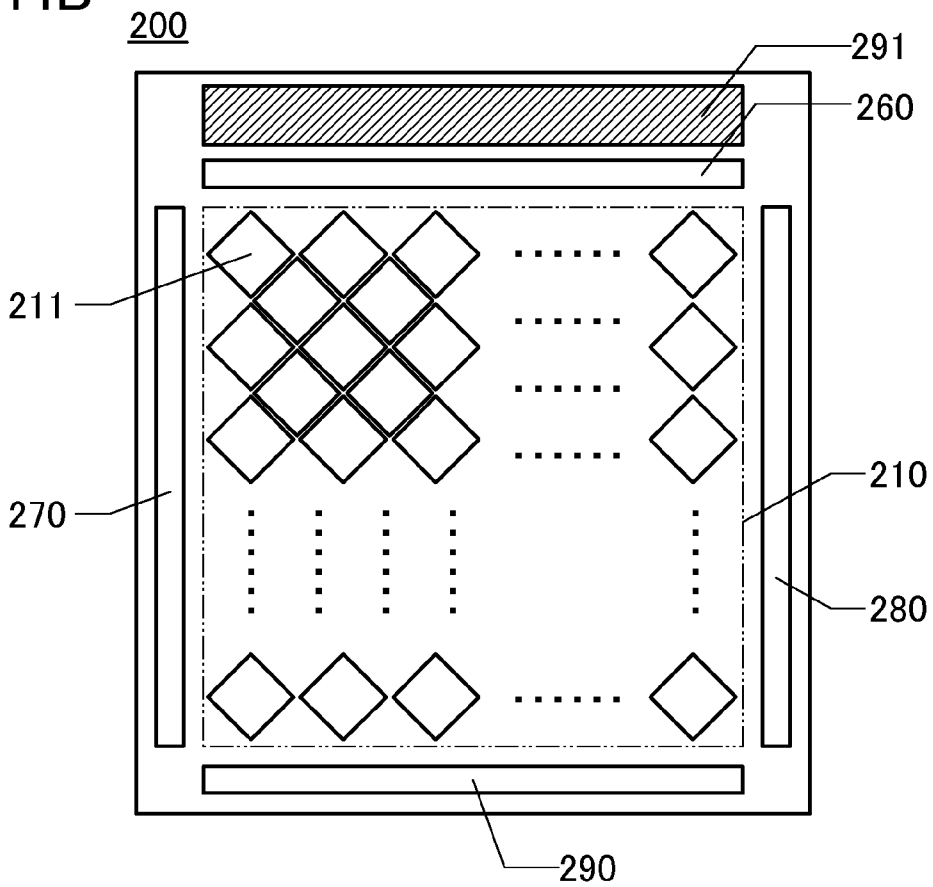


FIG. 45A

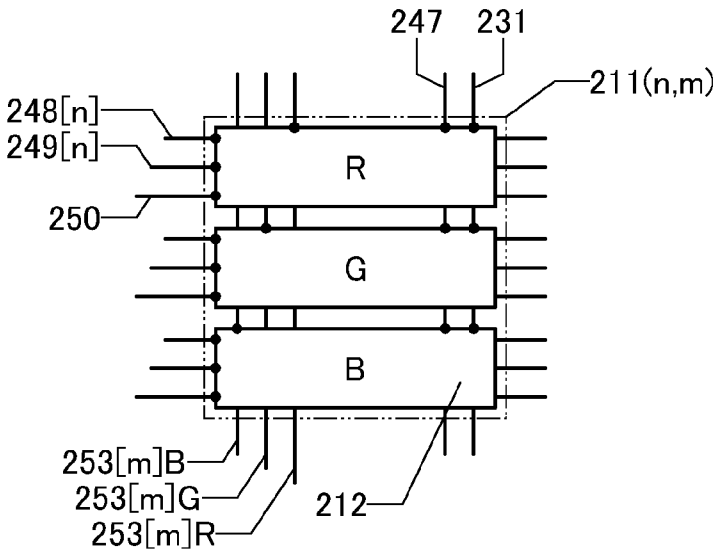


FIG. 45B

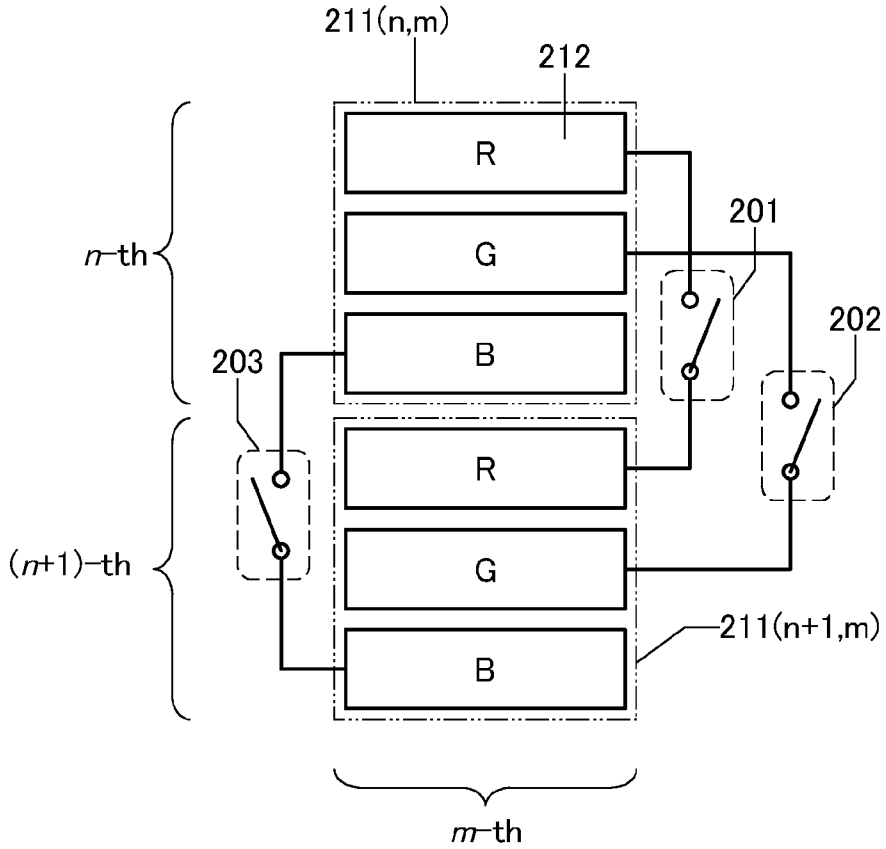


FIG. 46A

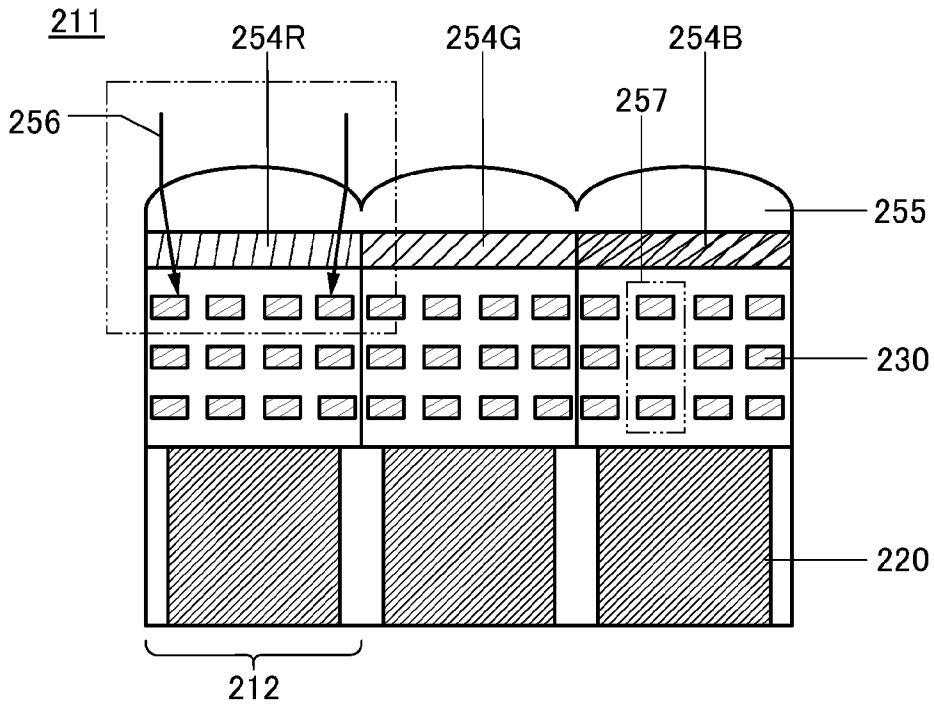


FIG. 46B

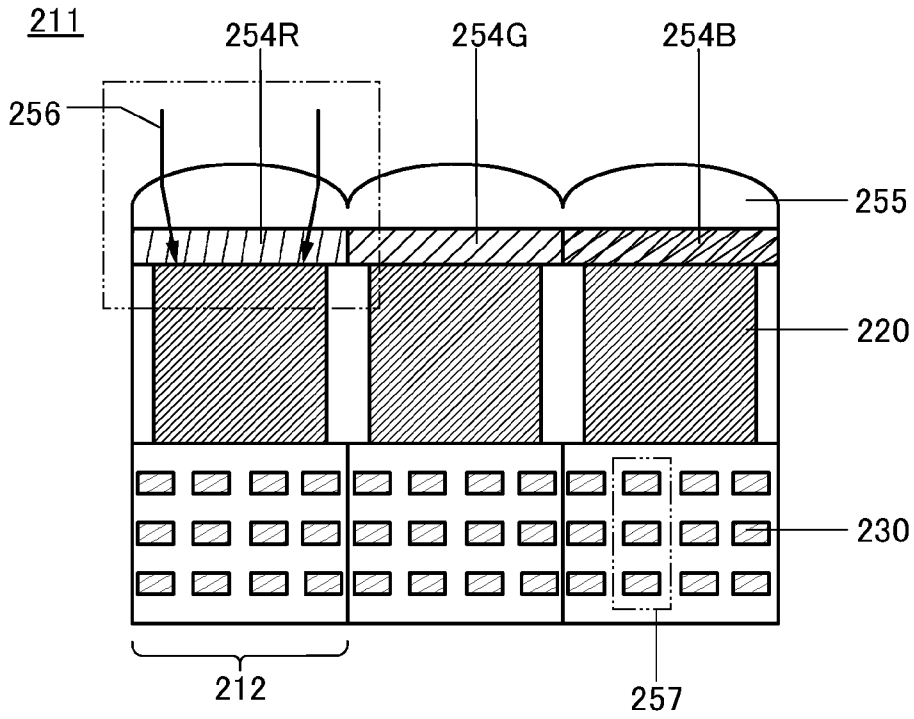


FIG. 47A

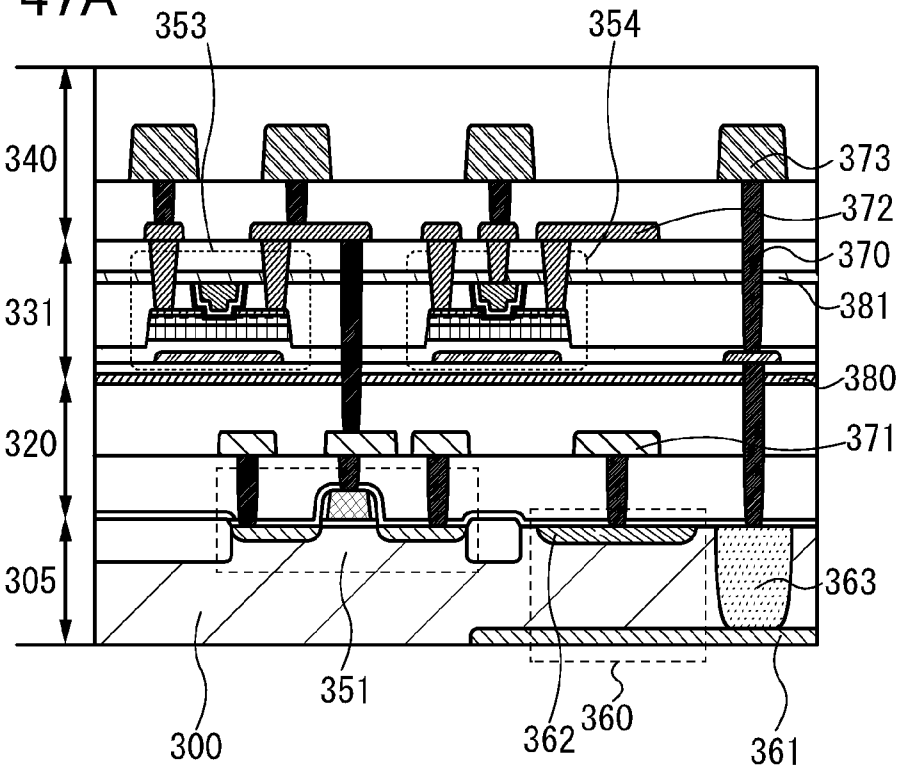


FIG. 47B

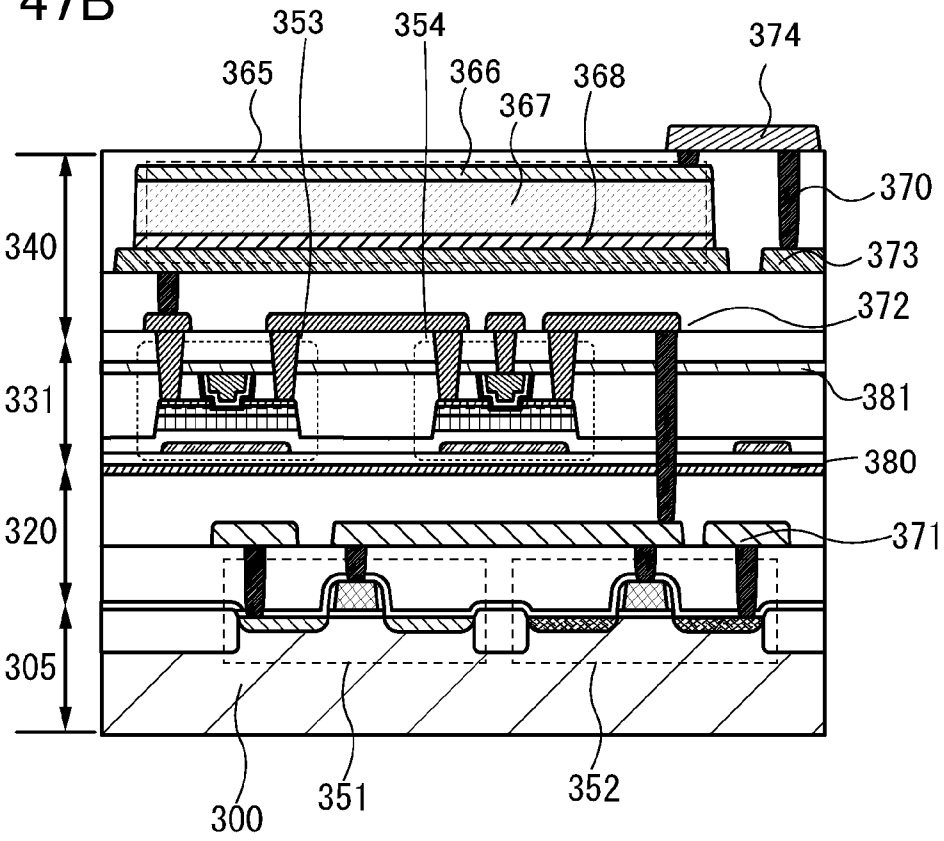


FIG. 48

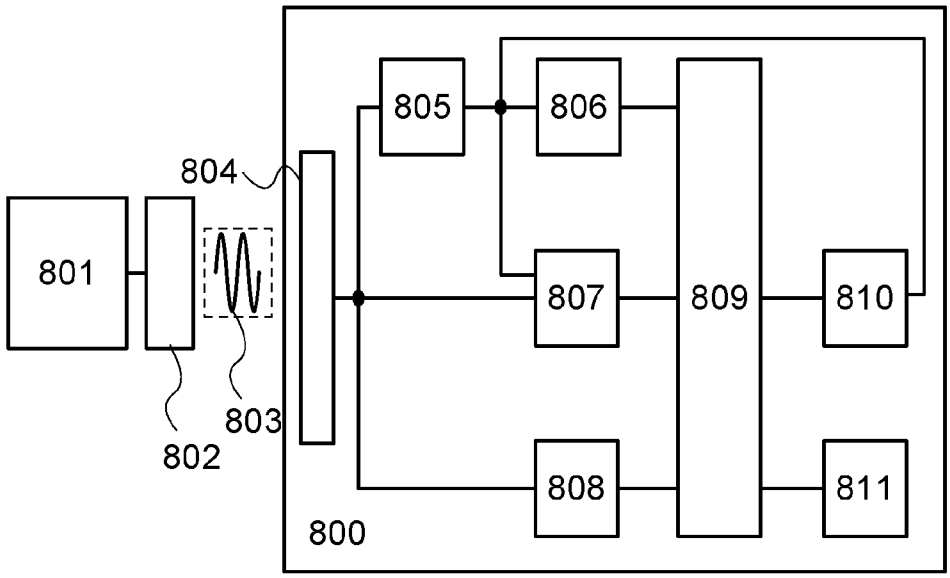


FIG. 49A

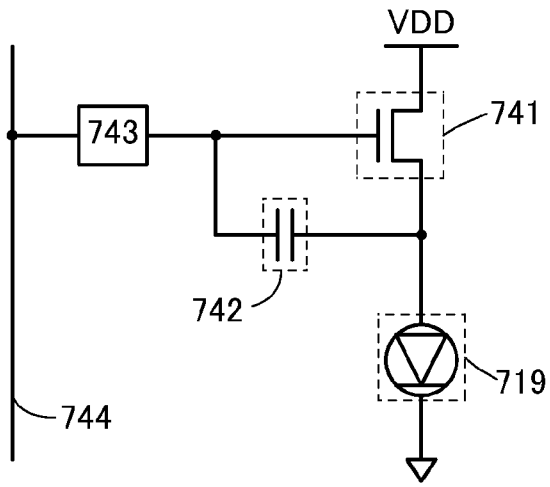


FIG. 49B

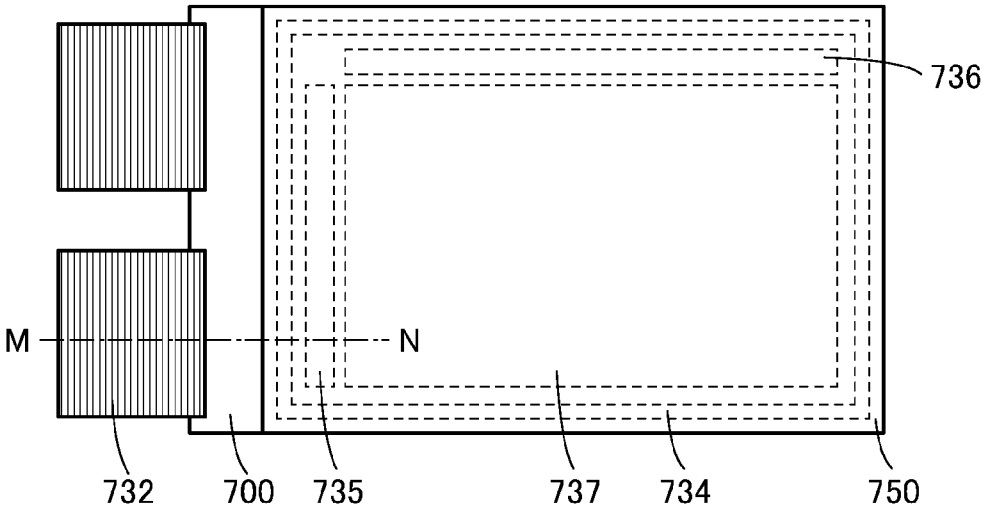


FIG. 49C

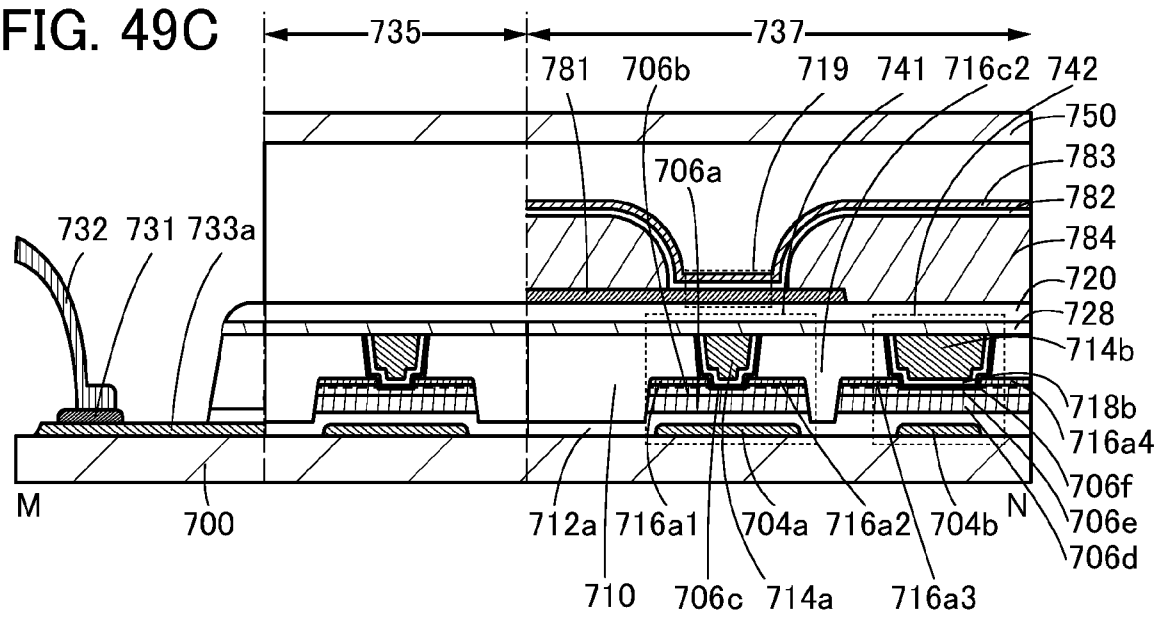


FIG. 50A

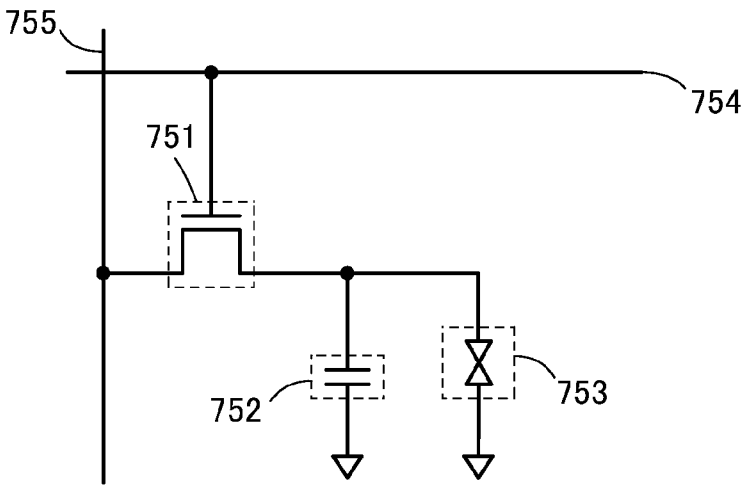


FIG. 50B

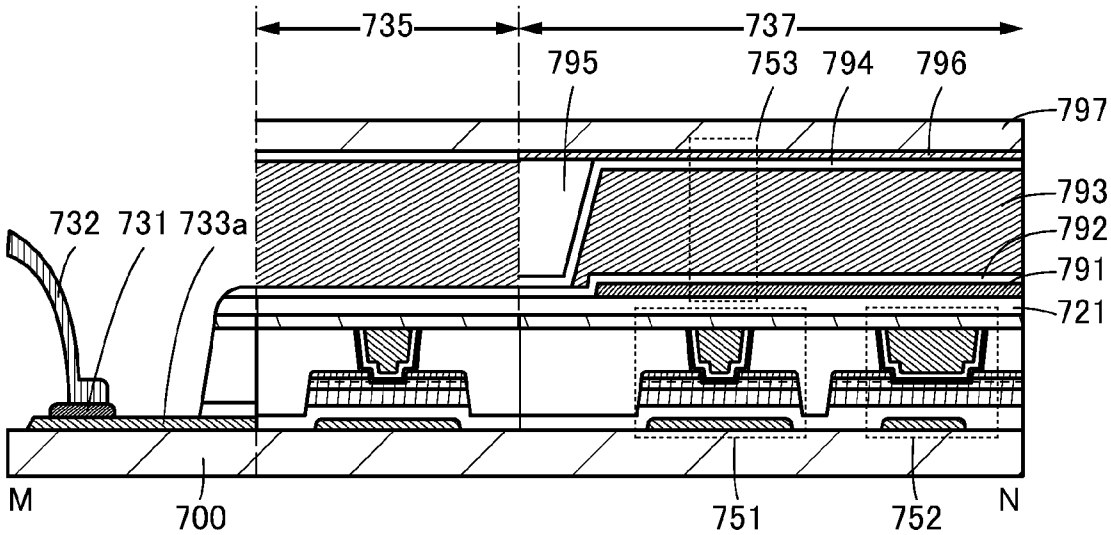


FIG. 51

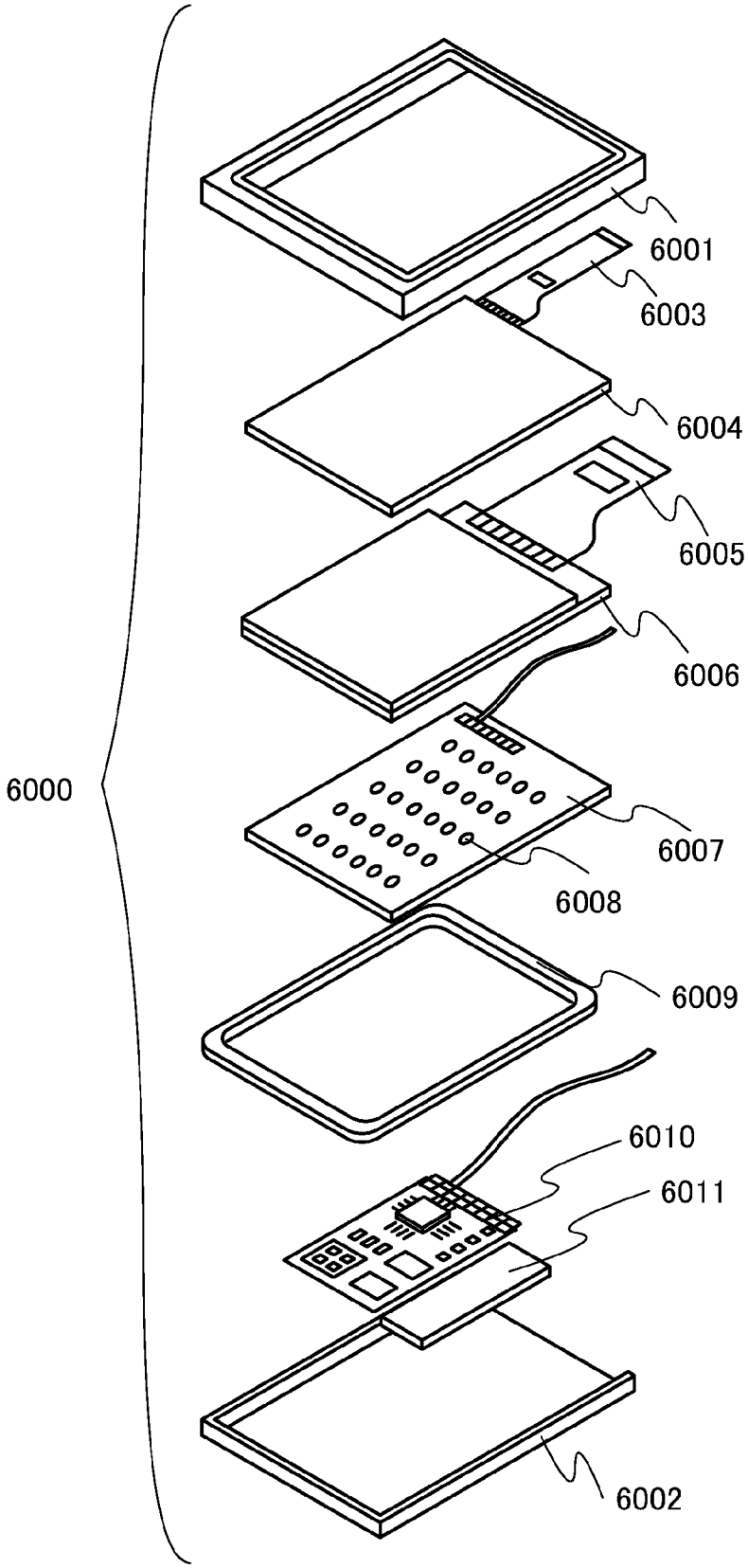


FIG. 52A

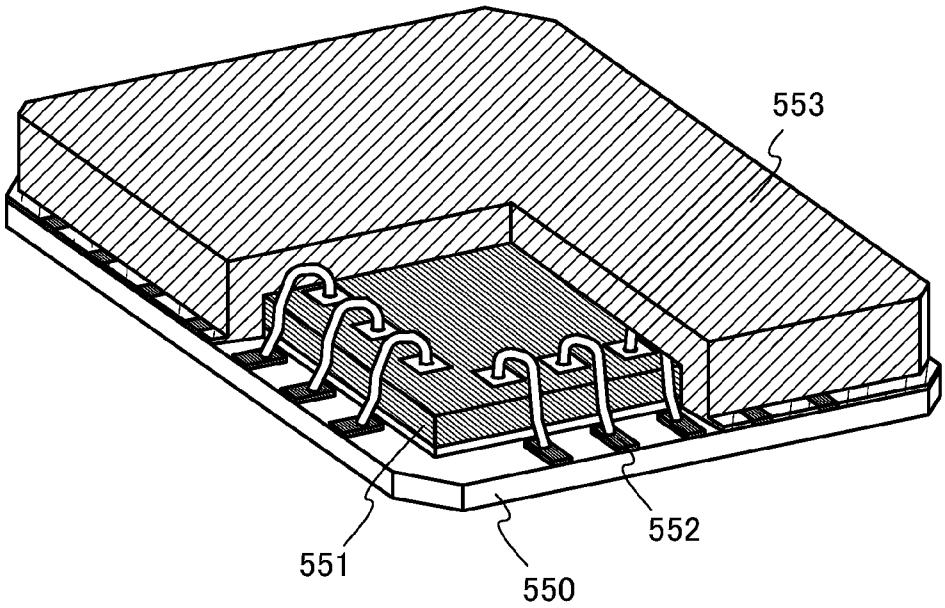


FIG. 52B

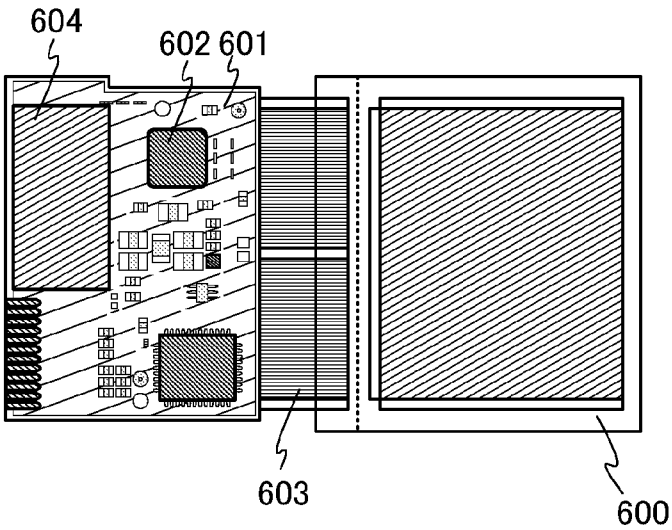


FIG. 53A

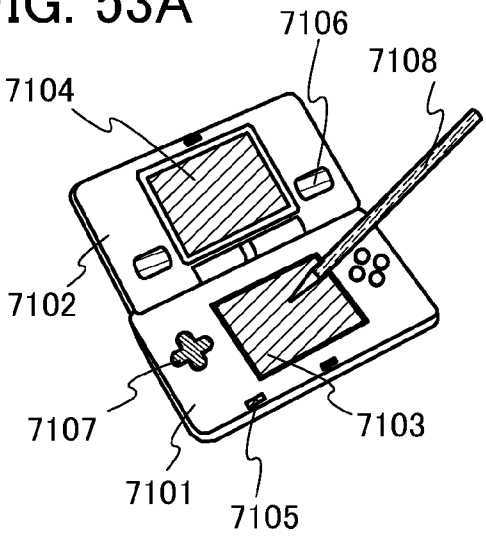


FIG. 53B

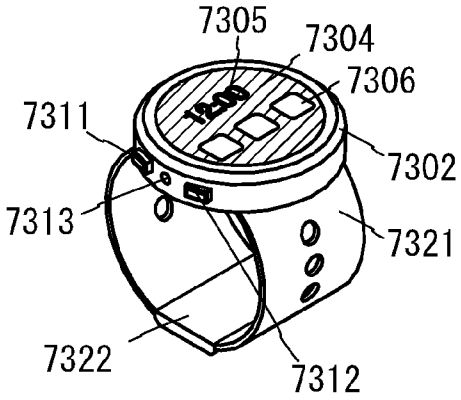


FIG. 53C

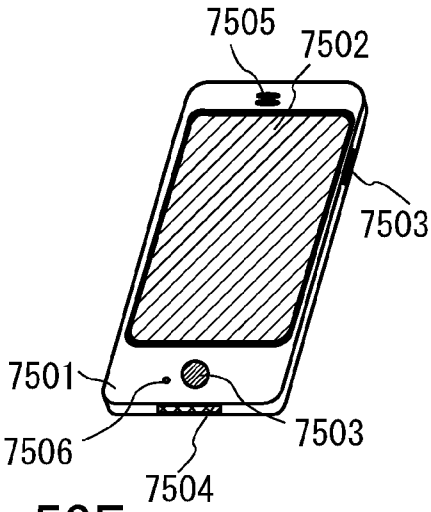


FIG. 53D

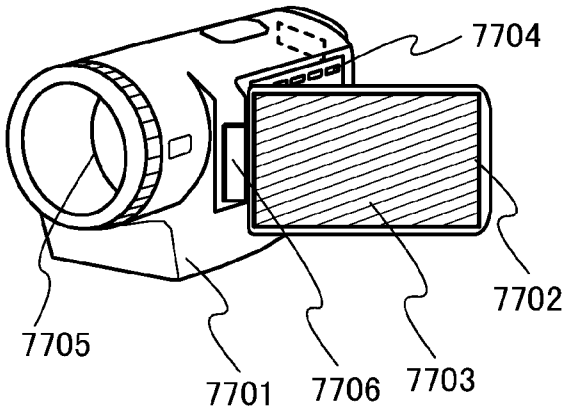


FIG. 53E

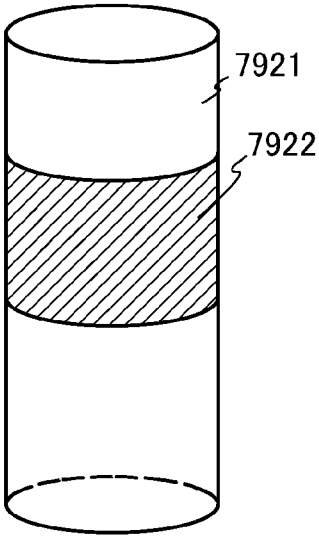


FIG. 54A

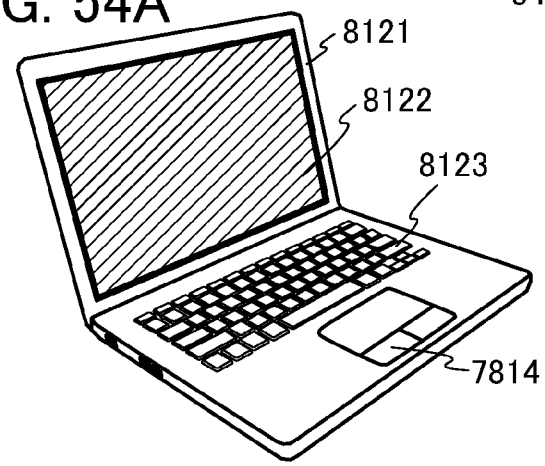


FIG. 54B

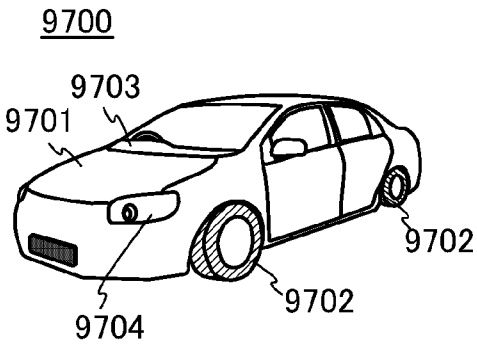


FIG. 54C

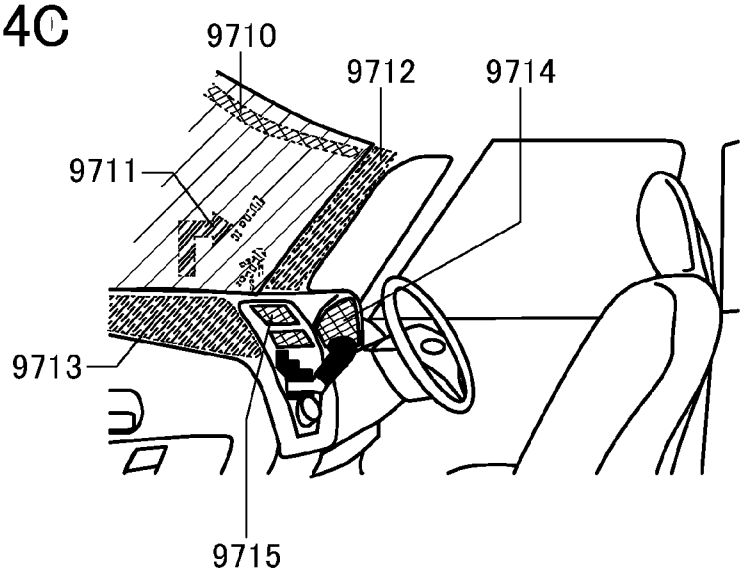


FIG. 54D

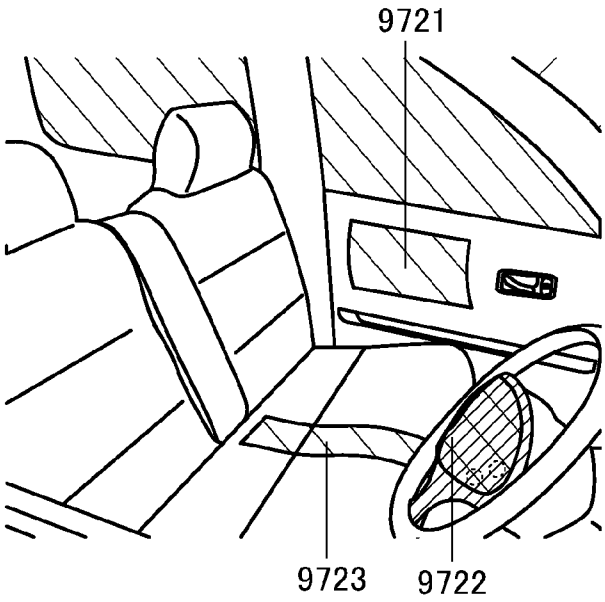


FIG. 55A

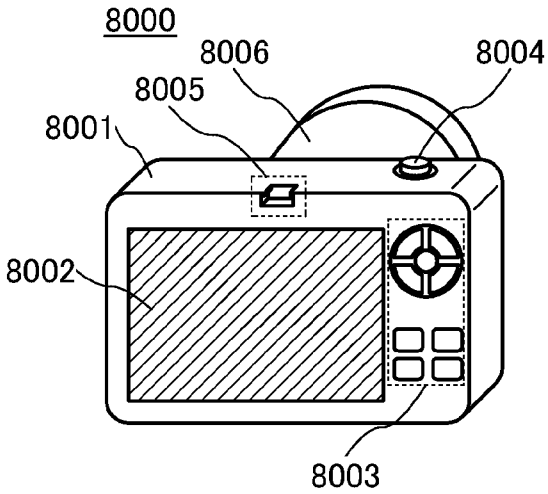


FIG. 55B

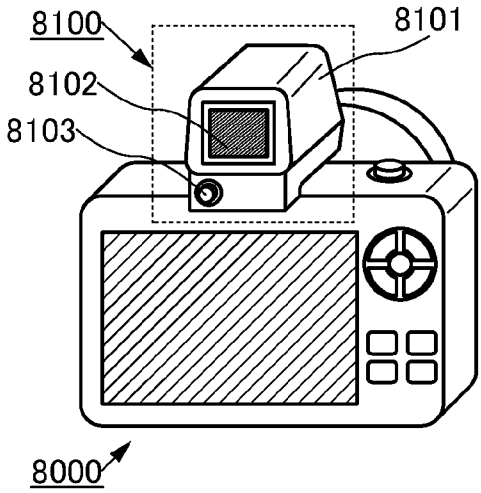


FIG. 55C

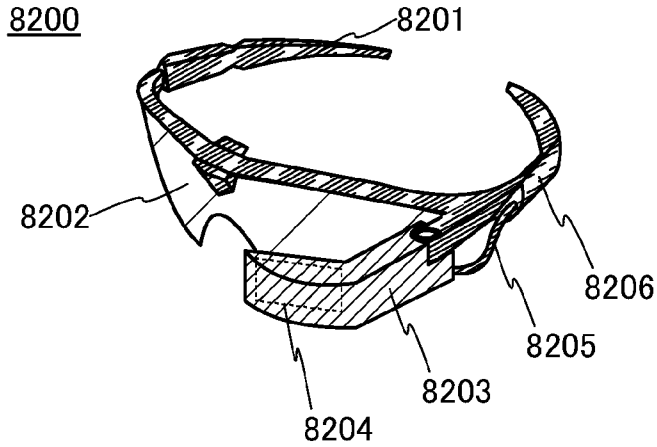


FIG. 56A

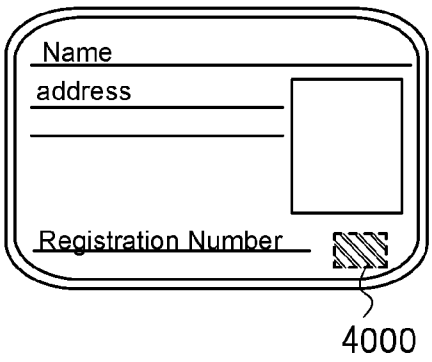


FIG. 56B

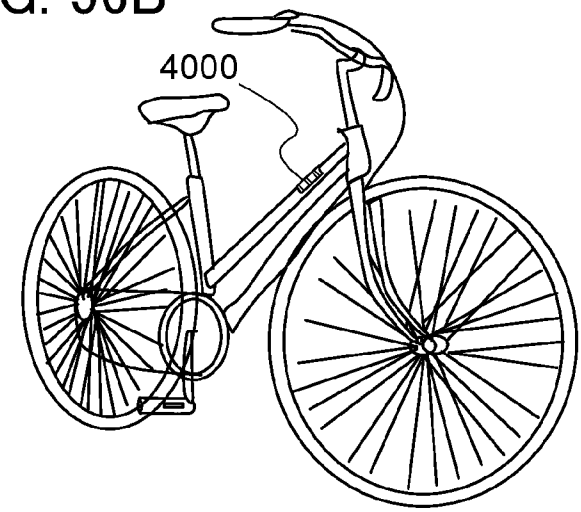


FIG. 56C

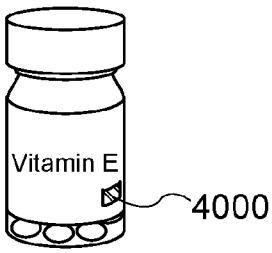


FIG. 56D

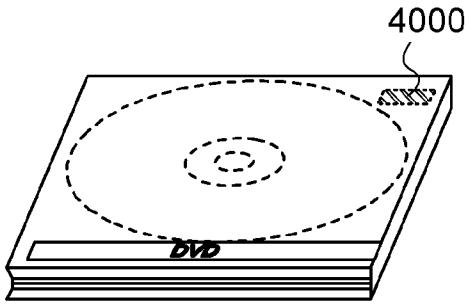


FIG. 56E

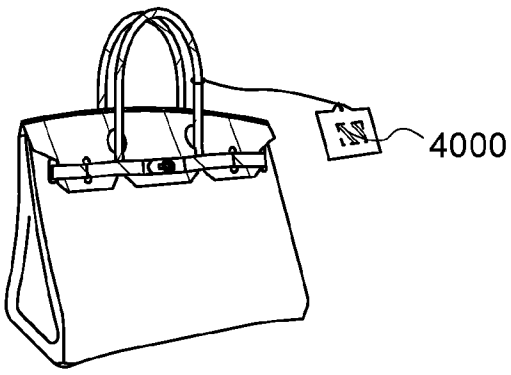
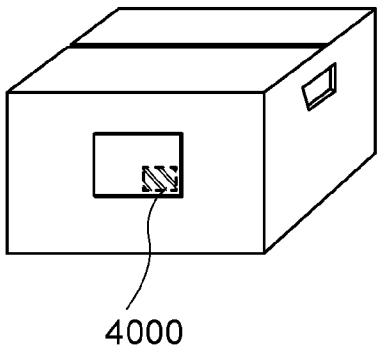


FIG. 56F



INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB2016/050923

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. H01L29/786(2006.01)i, G09F9/00(2006.01)i, G09F9/30(2006.01)i, H01L21/336(2006.01)i, H01L21/8234(2006.01)i, H01L27/088(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H01L29/786, G09F9/00, G09F9/30, H01L21/336, H01L21/8234, H01L27/088

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2016
Registered utility model specifications of Japan 1996-2016
Published registered utility model applications of Japan 1994-2016

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y A	JP 2013-251534 A (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2013.12.12, pars. 0056-0057, 0072-0133, figs. 4-5 & US 2013/0285050 A1, pars. 0071-0072, 0087-0148, Figs. 4-5, & KR 10-2013-0122554 A	1-6 7-17
Y A	JP 2014-99602 A (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2014.05.29, par. 0104, figs. 6-7 (No Family)	1-6 7-17
E, A	JP 2016-66793 A (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2016.04.28, & US 2016/087105 A1 & WO 2016/042433 A1	1-17

☑ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
11.05.2016	24.05.2016

Name and mailing address of the ISA/JP	Authorized officer
Japan Patent Office 3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan	IWAMOTO, Tsutomu 5F 9355 Telephone No. +81-3-3581-1101 Ext. 3516

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB2016/050923

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P, A	JP 2016-21559 A (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2016.02.04, & US 2015/0372009 A1 & WO 2015/193769 A1 & TW 201603282 A	1-17
P, A	JP 2015-195380 A (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2015.11.05, & US 2015/0280013 A1 & WO 2015/145292 A1 & TW 201543689 A	1-17
P, A	JP 2015-144251 A (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2015.08.06, & US 2015/0187898 A1 & WO 2015/097633 A1 & TW 201533903 A	1-17