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(54) Title: POWER AMPLIFIER CIRCUIT BASED ON A CASCODE STRUCTURE

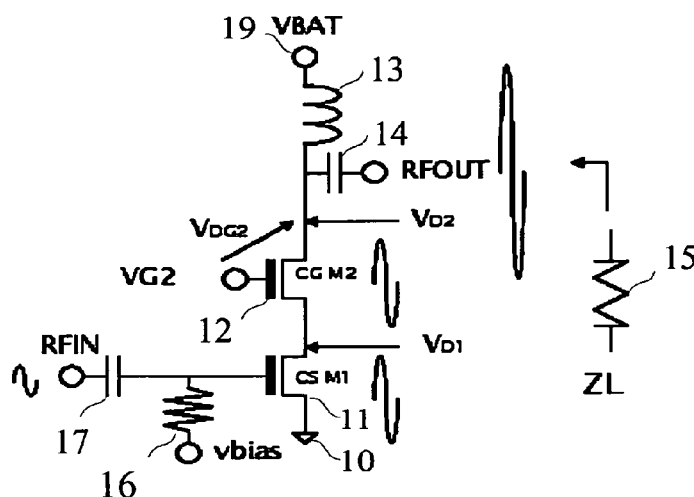


Fig. 1

(57) Abstract: A Power amplifier circuit based on a cascode structure and to be powered by a power source voltage, e.g. a battery, said circuit comprising - a first transistor (11) having a grid, source and drain terminal; said first transistor being connected in a common source mode; - a second grid source transistor (12) having grid, source and drain terminal, said second transistor being connected in common grid mode; - a biasing circuit for biasing said first transistor and said second transistor. The PA is characterized in that it includes a circuit for sensing the value of the power source voltage (VBAT) and for generating at least a first and a second biasing voltage for the grid of said second transistor (12) in accordance with the power source voltage sensed, said first biasing voltage providing substantially equal protection to said first and second transistors (11, 12) when said power source voltage (VBAT) is sensed to be at a high voltage and said second biasing voltage providing more voltage to said first transistor (11) when said power source voltage (VBAT) is sensed to be at a low voltage.

Power amplifier circuit based on a cascode structure

Technical field

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The invention relates to the field of electronic circuits and more particularly to a Power Amplifier for Radio Frequencies applications.

10 Background Art

Wireless telecommunications and Radio Frequencies (RF) standards call for linear Power Amplifiers (PA) allowing reduced power consumptions. Indeed, new modulated signals with high PAPR (*Peak to Average Power Ratio*) (6-10dB) have a
15 huge impact on the Power Amplifier design optimization. As known by a skilled man, such modulations ask for very good linearity and, last but not least, efficiency as well.

To ensure the best performances, circuit designers commonly choose to
20 directly couple the output stage to the battery voltage, when such direct coupling shows to be compatible with the maximum voltage allowed by the particular sub-micron technology being considered. Indeed, generally speaking, sub-micron MOS technology only allows limited voltages and, therefore, raises a reliability issue when higher voltages are to be considered.

25

One known solution for handling this problem is based on the use, for embodying the RF Power Amplifier, a specific technology which can sustain high voltages at their terminals. For instance, the so-called *N lateral Diffused Extended MOS* technology offering compatibility with higher voltages may be used for
30 embodying RF output power amplifiers, but at the cost of additional drawbacks, including further non-linearities and higher manufacturing costs.

A conventional power amplifier is known which, at least partly, helps to cope with such problem is the well-known cascode structure which is used for its interesting isolation between the input and the output.

5 The cascode structure is based on the connection in series of at least two transistors, respectively a common source transistor associated to a common grid transistor), thus allowing to share the high voltage of the battery (at least when fully charged) between two individual transistors. Thanks to such arrangement, only a part (half) of the battery voltage is applied to each individual transistor, thus
10 providing a "partial" protection of the individual cascode components when high voltages are being considered.

 However, in wireless communications using battery powered circuits, the level of the battery may vary to a wide extent – typically between 2.5Volt to 5Volt
15 and, therefore, the protection which is highly useful when the battery is fully charged becomes inappropriate and might even jeopardize linearity at low values.

 In particular, for low voltage values, the PA circuit tends to be less linear and the cascode based PA needs to be combined with complex circuits or feedback
20 loops to re-establish linearity and improve PAE. While the latter feedback loop shows phase issues (resulting in possible instability), the former linearization blocks are area consuming and increase total circuit complexity. Moreover it implies a coupler at the output which at the end reduces overall efficiency.

25 There is therefore a dilemma to be handled, deriving from the need of a good linearity and the need to allow large voltage swing.

 The observations above shows that, so far, there is still a difficulty in reaching a trade off between reliability (maximum voltage sustained on transistor particularly
30 when using a common "basic" sub-micron technology) and performances over a wide range of battery voltage (from 2.7 to 4.8V for instance) .

Therefore, there is still a need for a specific RF PA structure allowing direct implementation in pure CMOS technology and which still shows good linearity even with a reduced battery voltage.

5

Summary of the invention

It is an object of the present invention to provide a Power Amplifier PA, which
10 can be used for RF circuits, which show linear performance as well as reduced power consumption.

It is a further object of the present invention to provide a reliable RF Power Amplifier which offers good protection for the output transistors and, therefore, can
15 be embodied using the same technology or manufacturing process which is used for the RF circuitry handling the small signals.

It is still another object of the present invention to provide a RF Power Amplifier which is based on the Cascode circuit, comprising a Common Source
20 transistor combined with a Common Grid transistor, with a special biasing circuit for improving the reliability of the two transistors without degrading the linearity.

These and other objects of the invention are achieved by means of a Power amplifier circuit based on a cascode structure and to be powered by a power
25 source, such as a battery, which includes a first and a second transistors, having both grid, source and drain terminals, and being respectively connected in common source and common grid mode. A biasing circuit provides adequate biasing voltages to the two transistors.

30 In addition, a sensing circuit is used for sensing the value of the power source voltage and for generating at least a first and a second biasing voltage for the grid of the second transistor mounted in common grid mode in accordance with the power source voltage being sensed. For high values of the power source voltage, the biasing voltage applied to the second transistor is determined so as to provide

equal protection to both individual transistors forming the cascode structure. However, for lower values of the power source voltage, a second biasing voltage is applied so as to provide more voltage to the first transistor and have it work in a more linear region.

5

In one embodiment, the monitoring and biasing circuit comprises:

- a first, a second and a third resistor connected in series between the ground and the power source voltage being sensed, the common terminal of said second and third resistors generating the biasing voltage (VG2) connected to the grid of the second transistor. A third transistor has a source being connected to ground and a drain connected to the common terminal of the first and second resistor. The grid of the third transistor receives a control signal switching from a high voltage to a low voltage when the sensed value of the power source voltage falls below a first predetermined value.

15

- In a second embodiment, the monitoring and biasing circuit comprises a network of resistances comprising a first, a second, a third and a fourth resistor, all connected in series between the ground and the power source voltage. The common terminal of the third and fourth resistors generates the biasing voltage (VG2) applied to the grid of the second transistor. Two different transistors, individually controlled by a first and a second control signal, are used for short-circuiting two individual resistors of the network of the resistors so as to provide adequate shifting in the biasing voltage VG2 applied to the grid of the second transistor. Therefore, when the power source voltage is presumably high, the short circuit of two resistors among the four entails an equally biasing of the two transistors forming the cascode circuit so as to provide adequate protection ("protected mode") of each transistor. Conversely, when the voltage falls below a first (resp. a second) predetermined threshold, a shift in the biasing voltage (VG2) is applied so as to provide more room to the first common source transistor and keep the latter in a linear region.

25
30

- In one embodiment, the biasing of the common grid transistor is performed by means of a network of switching transistor(s) that switch(es) resistor networks to appropriately bias the gate of said second transistor in accordance with the sensed battery voltage (Vbat).

35

In one alternate embodiment, the sensing and monitoring circuit generates a biasing voltage (VG2) for the grid of common grid transistor which is a continuous value of said sensed power source voltage, so as to better adapt the cascode structure to the particular profile of the battery discharge.

In one embodiment, the Power Amplifier is used for carrying out a RF PA for a mobile terminal adapter for wireless communications.

The invention also achieves a RF circuit comprising the Power amplifier circuit defined above.

Description of the drawings

15

Other features of one or more embodiments of the invention will best be understood by reference to the following detailed description when read in conjunction with the accompanying drawings.

20

Figure 1 illustrates one embodiment of a cascode circuit based on common sub-micro CMOS technology which can be used for implementing a RF Power Amplifier.

Figure 2 shows the EVM and Pout diagrams as a function of the Battery Voltage Vbat.

Figure 3 illustrates a first embodiment of a biasing circuit for the cascode circuit of figure 1.

30

Figure 4 shows the EVM and Pout diagrams of the circuit of figure 1, when using the biasing circuit of figure 3.

Figures 5a and 5b respectively show the V_{ds} versus V_{gs} ~~V_{gs} - V_{ds}~~ diagrams of the two transistors M1 and M2 composing the cascade structure, when V_{set} = high (protected mode).

5 Figures 6a and 6b respectively show the V_{ds} versus V_{gs} ~~V_{gs} - V_{ds}~~ diagrams of the two transistors M1 and M2 composing the cascade structure, when V_{set} = Low (unprotected mode).

Figure 7 illustrates an alternative second embodiment of a biasing circuit.

10

Description of the preferred embodiment

15 It will now be described one particular embodiment of a cascode based Power Amplifier which offers good linearity and power performance over a wide range of voltage values and, therefore, is well adapted to the design of a RF power amplifier for a mobile equipment powered by a power source, such as a battery.

20 However, it should be clear that the power amplifier is not limited to such applications and may be used for embodying other power amplifiers.

To tackle with this, the proposed idea uses a classical approach of Cascode (Common Source CS transistor + Common Grid CG one). The common grid CG
25 transistor is biased to a specific point that protects the overall system in a reliable way. There are different reliability issues. One if this is life time which is mainly linked to the maximum voltage applied between drain and source V_{ds} of a transistor and relative to the input voltage applied between grid and source V_{gs} of the same transistor. The V_{ds} versus V_{gs} should not be above a specific value given for each
30 technology. This even more critical if the design does not use high voltage device for a low-cost purpose. This biasing point should be carefully chosen regarding the maximum voltage.

However, if the biased system is well suited for high voltage and does not degrade linearity performances, this is not the case with lower voltage anymore. Indeed, if V_{gate} of the CG transistor is kept to the same level as before, when V_{bat} decreases, V_{Drain} of the CG decreases, making CG transistor saturating earlier, reaching non linear region faster than before. The common source transistor is always protected by the CG one but seems to be overprotected regarding real value of its V_{DS} . The recommended approach consists in a biasing system which tunes V_{gate} of CS when V_{bat} decreases. Doing this, the CS transistor is kept into a linear region improving the linearity of the total structure in case of lower voltage.

10

Figure 1 shows one embodiment of a RF power amplifier in accordance with that approach. The cascode is based on a set of two transistors M1 11 and M2 12, each having source, drain and grid terminals. The source-drain junctions are connected in series and the two transistors M1 and M2 are respectively mounted as a common source (M1) and a common grid (M2).

15

The first transistor M1 has its source connected to a reference voltage, ie the ground 10, and its grid biased by means of an appropriate biasing network, such as for instance by illustrative resistor 16 connected to a bias voltage V_{bias} . The grid terminal of transistor M1 11 also receives an input RF signal $RFin$ through a adequate capacitor 17.

20

The second transistor M2 12 has its source connected to the drain of transistor M1 and its grid biased to a voltage $VG2$. The drain of transistor M2 12 is connected to a load, ie load ZL 15 through a decoupling capacitor 14 and is also connected to the battery voltage V_{bat} through an inductor 13.

25

As illustrated in figure 1, each of the two transistors 11 and 12 share half of the voltage swing between the ground and the battery voltage V_{bat} , with the advantage of at least a first protection of each individual transistor being highly useful when the battery is fully charged but which, however, leads to a degraded performance at lower voltage, particularly with regard to the linearity.

30

Figure 2 illustrates the performances over VBAT of a Power Amplifier (PA) designed in a cascode mode, such as the circuit of figure 1. The right vertical scale shows the Pout value in dB, while the left scale shows the linearity information expressed under the form of an Error-Vector Magnitude (EVM) figure representative of the linearity for a modulated OFDM signal. The lower in dB this value is, the more linear the PA. In the illustrative example of figure 2, it can be seen that Power amplifier PA is designed to show the best performances at a nominal voltage of 3.6V. However, the circuit needs to be protected at a value up to 4.2V (reliability). Fig 2 shows that at high voltage the system is performing well (higher power and better linearity) while a degradation of the performance is clearly shown at lower voltage (below 3.6V) with a critical increase of the EVM value, representative of a drastic fall of the linearity of the power amplifier. The figure 2 also shows a typical specification for the Pout value (SPEC) which is required by RF standards.

15

Figure 4 shows that the linearity performance can be significantly improved for the cascode based PA, while maintaining an effective protection of the sub-micron technology used for the output transistors. One sees, indeed, that for battery voltages below 3.7 Volts, it becomes possible to significant reduce the EVM factor, "starting" again to -36 dB instead of -27dB, thus drastically modifying the EVM picture of figure 3

20

Figure 3 more particularly illustrates how one may achieve such improvement in the linearity by means of a first embodiment based on a specific biasing circuit which provides at least a first and a second biasing voltage VG2 dependent on the value of the battery voltage.

25

The biasing circuit of figure 3 comprises a network of resistors 21, 22 and 23 (resp. R1, R2, and R3) which are connected in series between the ground 20 and the Vbat terminal 29 .

30

More particularly, resistor R3 23 has a first terminal connected to Vbat terminal 29 and a second terminal connected to the grid of transistor M2 12. Resistor R2 22 has a first terminal connected to the second terminal of resistor R3

and a second terminal. Resistor R1 21 has a first terminal connected to the second terminal of resistor R2 and a second terminal connected to the ground voltage reference, ie terminal 20.

5 In the first embodiment of figure 3, one sees that a first transistor M3 25 has a source, drain and grid terminal. The source is connected to the ground, while the drain is connected to the second terminal of resistor R2 22 and the first terminal of resistor R1 21.

10 In addition, the battery voltage is monitored by a specific sensing & monitoring circuit 30 which generates a control signal Vset applied to the grid of transistor M3 and which depends on voltage value Vbat.

In one embodiment, Vset is set to a high level (protected mode) when the
15 battery voltage is detected to have a value superior to a first predetermined threshold. Conversely, when the value of the battery falls below that threshold, the Vset signal is set to a low level (unprotected mode).

The biasing circuit of figure 3 operates as follows.

20

When the battery shows to be fully charged, Vset is set to a high level, thus performing a short-circuit of resistor R1 21. Consequently, the network of resistors R2-R3 are adapted to generate a VG2 voltage causing each transistor M1 and M2 to share approximately half of the voltage swing between ground and the battery
25 voltage.

With the result of a protection of the sub-micron technology transistors M1 and M2 composing the cascode structure at high value of Vbat.

30 When the battery tends to be discharged, the value Vbat falls and becomes lower than the above mentioned threshold voltage.

Monitoring circuit 30 detects such fall of voltage and then controls Vset signal to set it to a low level.

Consequently, voltage V_{G2} which is generated at the common terminal between resistor $R2$ and $R3$ is generated by the three resistors $R1$ - $R3$ and is thus increased, thus modifying the biasing circuit of cascode transistors $M1$ and $M2$.

5 In particular, the increase of voltage V_{G2} causes the common source transistor $M1$ to be kept in a linear region even though the battery voltage decreases below to 3.6 Volts. With the consequence of a EVM factor which, as shown in figure 4, is significantly lower than the corresponding EVM factor of figure 2.

10 It can be seen that, at the cost of very few additional components, it is possible to achieve a cascode based Power Amplifier circuit which is significantly more flexible since it offers two distinctive mode. A first so-called "protected" mode where the two individual transistors forming the cascode structure are substantially equally biased so as to share the voltage swing and offer best protection to the
15 individual transistors. And a second "unprotected mode" where the biasing is modified so as to improve the linearity of the cascode structure at low voltages.

While, conventionally, the total dimensioning is done at lower voltage for performances (linearity) but at the price of lower efficiency at higher voltage then,
20 entailing the need to considered specific technologies for the output PA. Here, the system is optimized at nominal voltage (3.6V for instance), protected above (4.8V for instance) and "de"protected (because no protection is no more useful) at lower voltage (3V for instance).

25 It should be noticed that, while the embodiment has been described based on the biasing of transistor $M2$ with a current flowing into a resistor network, any other embodiment can considered. In particularly, one may use a network of switching transistor(s) that switche(s) resistor networks to appropriately bias the gate of the CG transistor. This is particularly efficient when no expensive power transistor can
30 be used to protect the system.

Fig 5a and Fig 5b give a representation of the reliability in case of PA design (cascode). The main reliability issue of a cascode structure is lifetime which is related to V_{DS} versus V_{GS} voltage swing of each transistor. Figure 5a shows the

CG transistor 12 while figure 5b illustrates the CS transistor 11. A line is also drawn showing the life time threshold of each transistor for a given technology. If the VDS is high when VGS is also high a reliability lifetime reduction occurs. The design is optimized to be below and on the left of this limit. The dark shape is the maximum simulated swing for a given application. It can be seen that at 4.2V the system is quite reliable. Here $V_{set}=1.4V$, so VSET is high and the system becomes protected at high voltage.

Fig 6a and 6b give another representation of the reliability of the same PA but at lower voltage (nominal and below), i.e. when $V_{SET}=0V$. Even when the system is "de-protected", the structure shows to be safe. But, in that case, since the system is not "over-protected" anymore, the performances can be recovered better.

With respect to figure 7, there is illustrated a second embodiment for the circuit biasing transistor M2 12.

The circuit comprises a network of four resistors connected in series between the ground and the voltage battery.

A first resistor 51 has a first terminal connected to the ground and a second terminal. A second resistor 52 has a first terminal connected to the second terminal of the first resistor 51 and a second terminal. A third resistor 53 has a first terminal connected to the second terminal of the second resistor 52 and a second terminal. A fourth resistor 54 has a first terminal connected to the second terminal of the third resistor 53 and a second terminal connected to the battery voltage Vbat.

A transistor 61 has grid, source and drain terminal. The source is connected to the ground and the drain is connected to the common terminal of resistors 51-52.

A transistor 62 has grid, source and drain terminal. The source is connected to the ground and the drain is connected to the common terminal of resistors 52-53.

The grid of transistors 61 and 62 are respectively connected to receive two control signals $V_{control1}$ and $V_{control2}$ generated by a monitoring circuit 60 sensing the battery voltage V_{bat} .

5 The circuit operates as follows:

When the battery voltage is high, monitoring circuit generates a high voltage on control signal $V_{control2}$, so that the common terminal of resistors 52-53 are short-circuit to the ground.

10

Consequently, the second transistor M2 is biased by means of resistors 53-54 only, and the two individual transistors M1 and M2 composing the cascode structure are equally biased to share the voltage swing between the ground and the presumably high battery voltage V_{bat} .

15

When the battery voltage falls down below a first predetermined threshold, monitoring circuit 60 sets $V_{control1}$ to a low level and $V_{control2}$ to a high level, thus causing the V_{G2} voltage to be set by the three resistors 52-53-54. One sees that the biasing voltage V_{G2} is slightly increased so as to keep the first transistor M1 in a linear region despite the slight decrease of the battery voltage.

20

When the battery voltage decreases more and reaches a second lower predetermined threshold, then monitoring circuit 60 sets $V_{control1}$ and $V_{control2}$ to a low level, thus causing the V_{G2} voltage to result from the whole set of resistors 51-54 connected in series. With the consequence of an additional increase of the voltage V_{G2} so as to shift more the cascode transistors in an unprotected area but, still, in a linear region.

25

One sees again that very few components are required for achieving a very flexible circuit which provides balanced voltage protection of transistors and linearity of the whole cascode structure.

30

It should be noticed that, while the monitoring circuit 60 senses the battery voltage and compares the latter to two predetermined thresholds, more than two thresholds could be considered.

5 In one embodiment, the particular threshold values are chosen so as to correspond to the particular profile of the battery which is connected.

In another more sophisticated embodiment, sensing and monitoring circuit 60 directly generates a voltage V_{G2} being a continuous function $F(V_{bat})$ of the
10 battery voltage V_{bat} .

The invention allows to optimize a PA design at a nominal voltage (3.6V for instance) reaching very good performances (P_{out} , linearity and efficiency) while ensuring a reliability at high voltage (4.2V, 4.8V for instance) without sacrificing
15 performances (linearity) at lower voltage (2.7V for instance).

There is no need of any specific linearization technique to reach the performances at lower voltage and very little extra area is required. In addition, there is no variation in the input matching network and the whole circuit can be
20 implemented in pure CMOS, in digital or analog technology.

The switch structure can be designed as a current source biasing, tuning the current flowing into the resistance network.

25 At last, the whole system can be implemented in a standard technology without using high performances transistor (nextD for instance) and reducing the cost as well.

The sense of power source can be put in memory to provide a known voltage
30 distribution to the circuit. It allows to know in advance the evolution of the power source and tune the right value V_G for the transistors. This is similar to a power source "predistorsion"

The number of cascode transistor is not limited to 2 and can be higher. Total voltage is shared among all the transistor. Each gate (grid) of each transistor can be tuned with the power source regarding performances and reliability in a similar principle.

CLAIMS

- 5 1. Power amplifier circuit based on a cascode structure and able to be powered by a power source, characterized in that said circuit comprising at least
- a first transistor (11) having a grid, source and drain terminal; said first transistor being connected in a common source mode;
 - a second grid source transistor (12) having grid, source and drain terminal, said
 - 10 second transistor being connected in a common grid mode;
 - a biasing circuit for biasing said first transistor and said second transistor;

the power amplifier circuit further includes a circuit for sensing the value of the power source voltage and for generating at least a first and a second biasing

15 voltage for the grid of said second transistor (12) in accordance with the sensed power source voltage, said first biasing voltage providing protection to said first and second transistors (11, 12) when said power source voltage is sensed to be at a high voltage and said second biasing voltage providing more voltage to said first transistor (11) when said power source voltage is sensed to be at a low voltage.

20

2. Power amplifier circuit according to claim 1 characterized in that said sensing and biasing circuit comprises:
- a first (21), a second (22) and a third (23) resistor connected in series between the ground and the power source voltage, the common terminal of said second and third
 - 25 resistors generating a biasing voltage (VG2) for the grid of said second transistor (M2, 12);
 - a third transistor (25) having source, drain and grid terminals, the source of said third transistor being grounded, the drain of said third transistor being connected to the common terminal of said first and second resistor, the grid of said third transistor
 - 30 receiving a control signal switching when said power source voltage falls below a first predetermined value.

3. Power amplifier circuit according to claim 1 characterized in that said monitoring and biasing circuit comprises:

- a first (51), a second (52), a third (53) and a fourth (54) resistor connected in series between the ground and the power source voltage, the common terminal of said third and fourth resistors (53, 54) generating the biasing voltage (VG2) for the grid of said second transistor (M2, 12);
- a third transistor (61) having source, drain and grid terminal, the source of said third transistor being connected to ground, the drain of said third transistor being connected to the common terminal of said first and second resistors (51, 52), the grid of said third transistor receiving a first control signal generated by a sensing circuit (60) when said power source voltage falls below a first predetermined value;
- a fourth transistor (62) having source, drain and grid terminal, the source of said fourth transistor being grounded, the drain of said third transistor being connected to the common terminal of said second and third resistors (52, 53), the grid of said fourth transistor receiving a second control signal generated by said sensing circuit, (60) said voltage value Vbat falls below a second predetermined value lower than said first predetermined value.

4. Power amplifier circuit according to claim 1 characterized in that the biasing of said second transistor (M2, 12) is performed by means of a network of switching transistors that switch resistor networks to appropriately bias the gate of said second transistor (M2, 12) in accordance with the sensed power source voltage .

5. Power amplifier circuit according to claim 2 characterized in that said first predetermined threshold is set to approximately 3.6 Volts.

6. Power amplifier circuit according to claim 1 characterized in that said monitoring and biasing circuit generates a biasing voltage (VG2) for the grid of said second transistor (M2, 12) which is a continuous value of said sensed power source voltage (Vbat).

7. Power amplifier circuit according to anyone of the preceding claims characterized in that it is used for a mobile terminal adapter for wireless communications.

8. Mobile telephone including a RF circuit comprising the Power amplifier circuit as defined in anyone of claims 1 to 6.

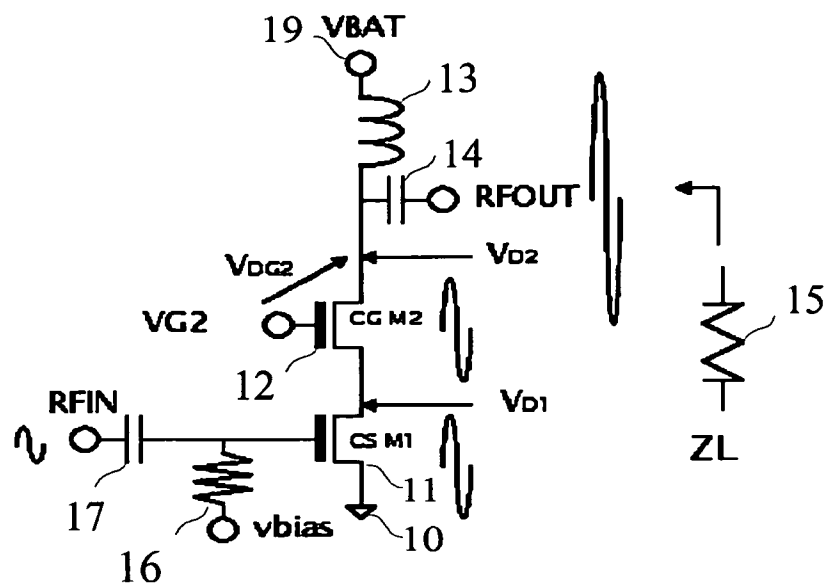


Fig. 1

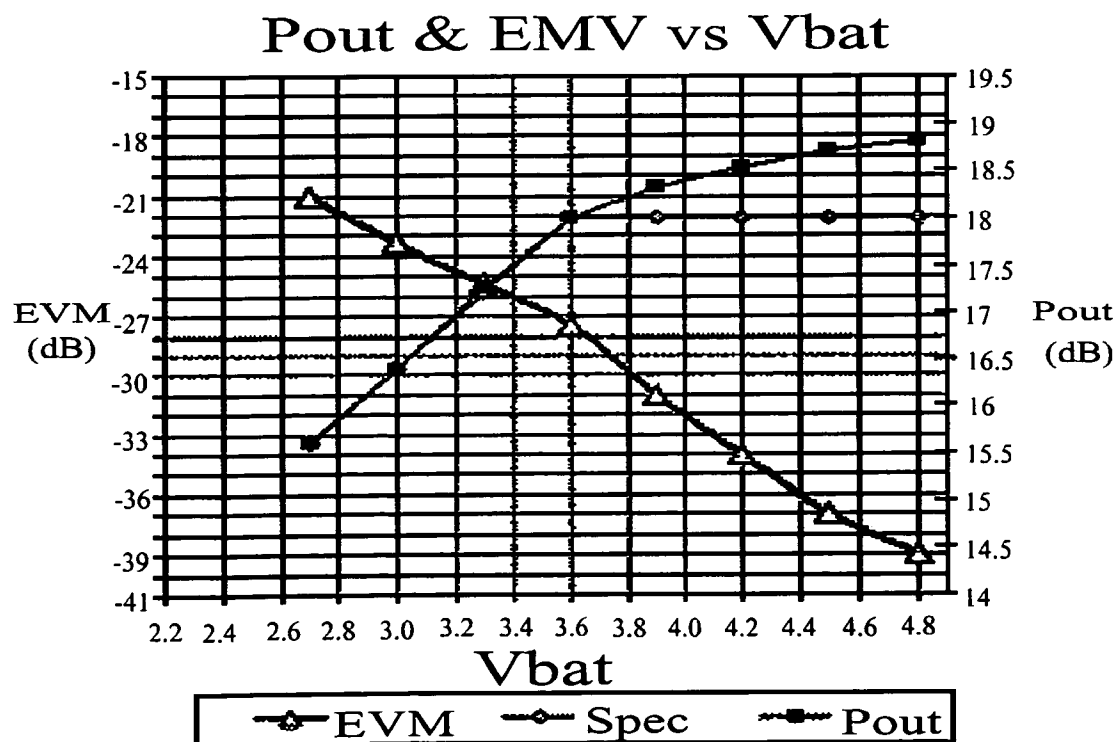


Fig. 2

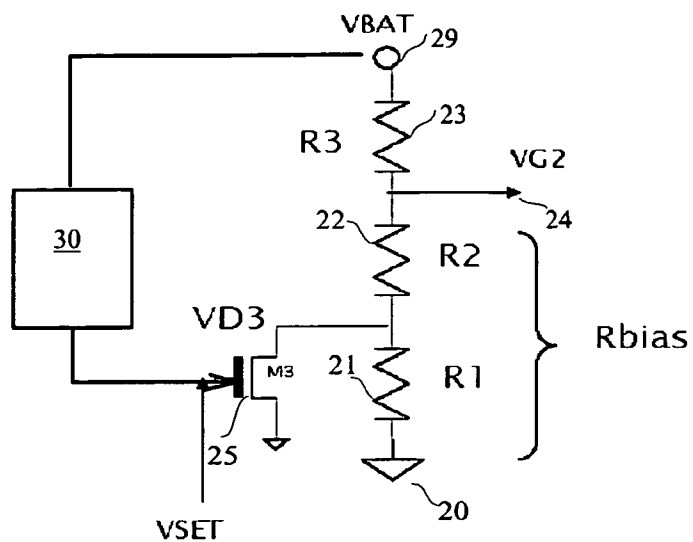


Fig. 3

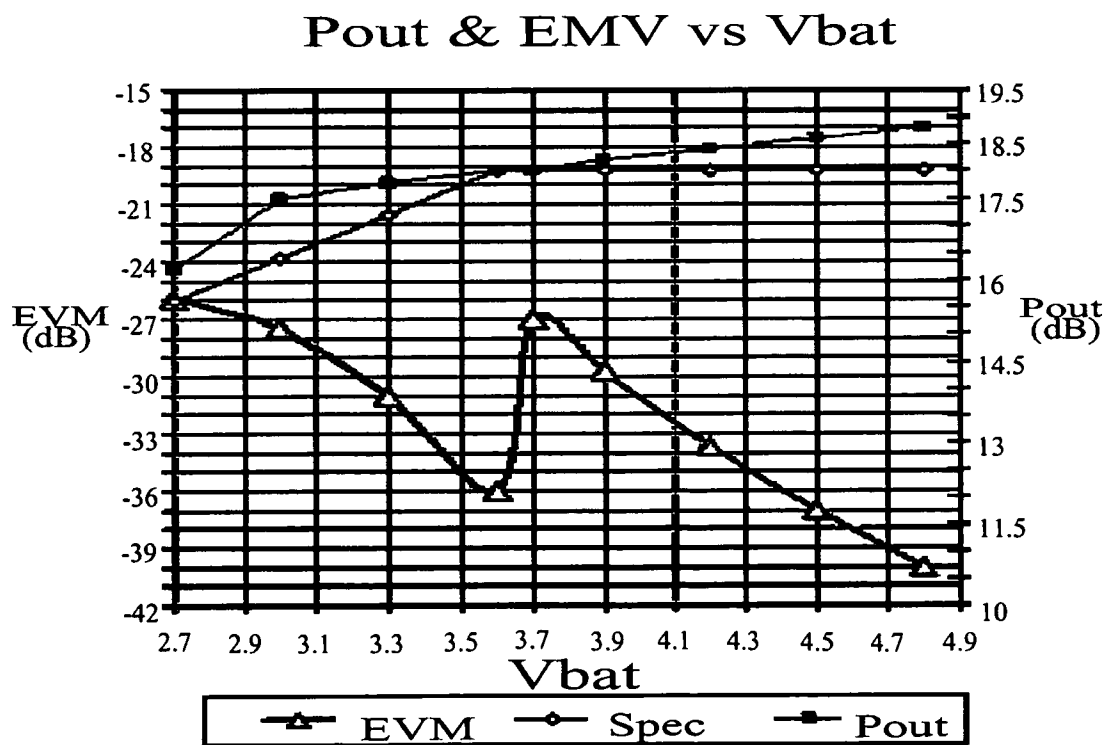


Fig. 4

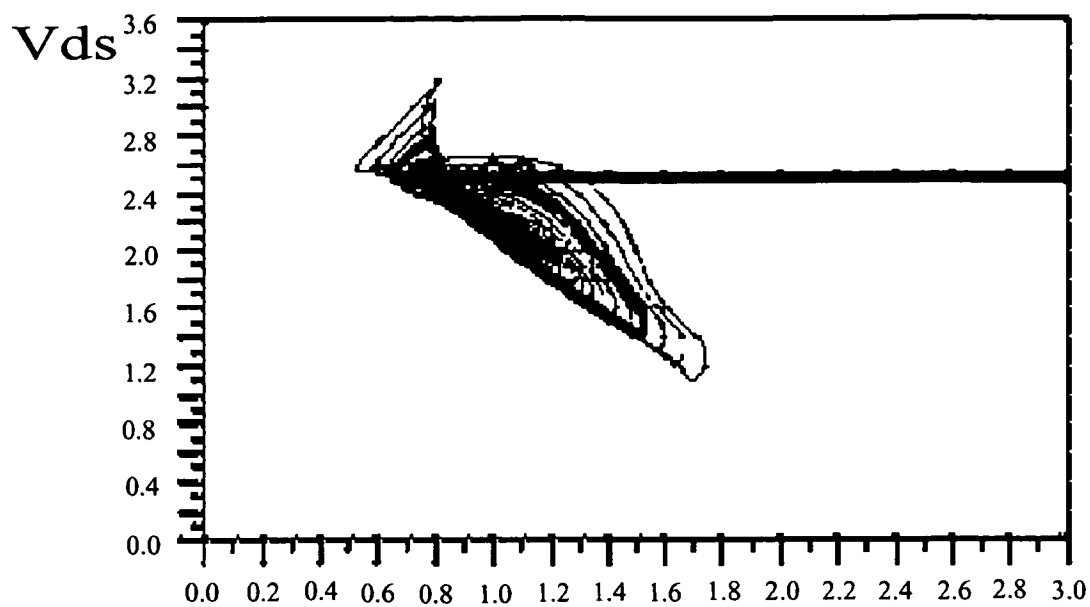


Fig. 5a Transistor M2 V_{gs}

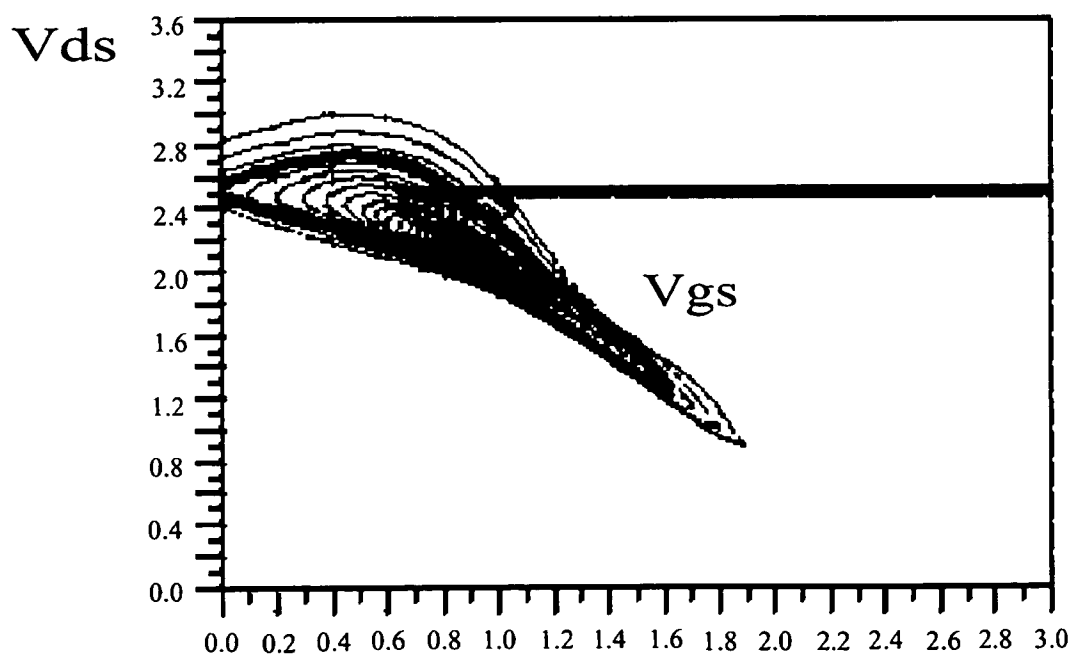


Fig. 5b Transistor M1 V_{gs}

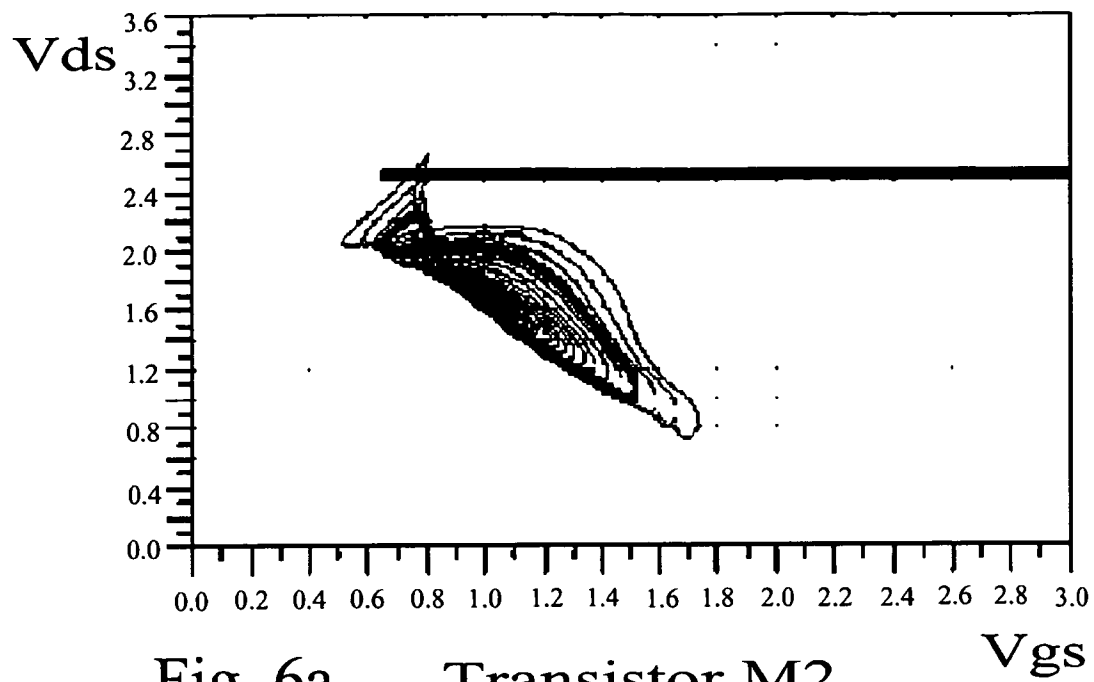


Fig. 6a Transistor M2

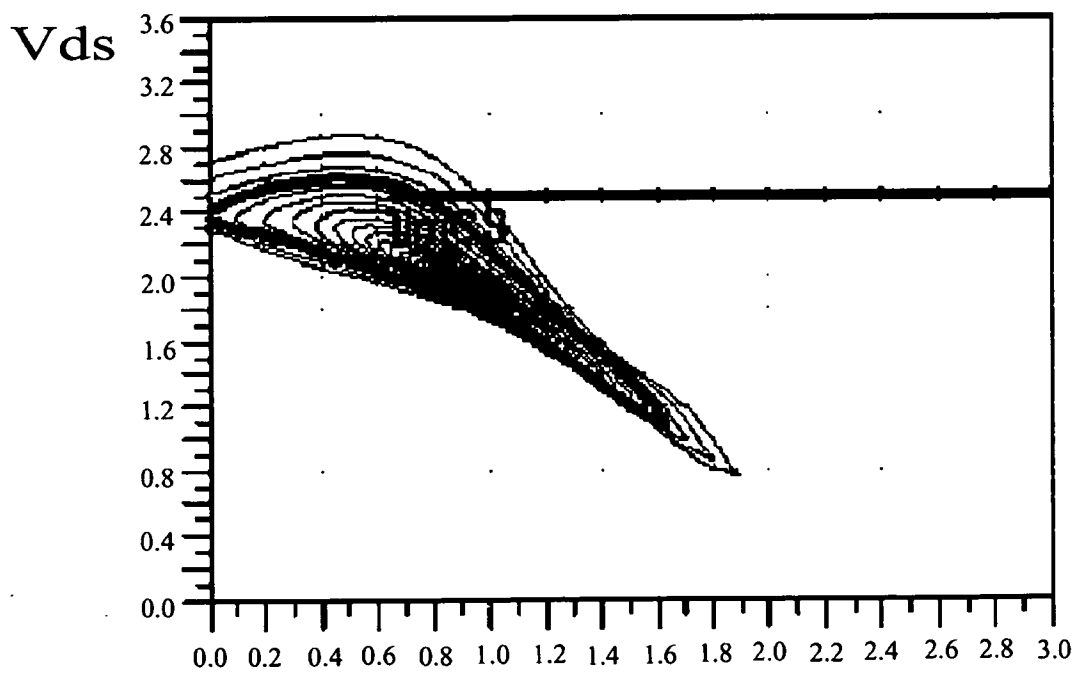


Fig. 6b Transistor M1

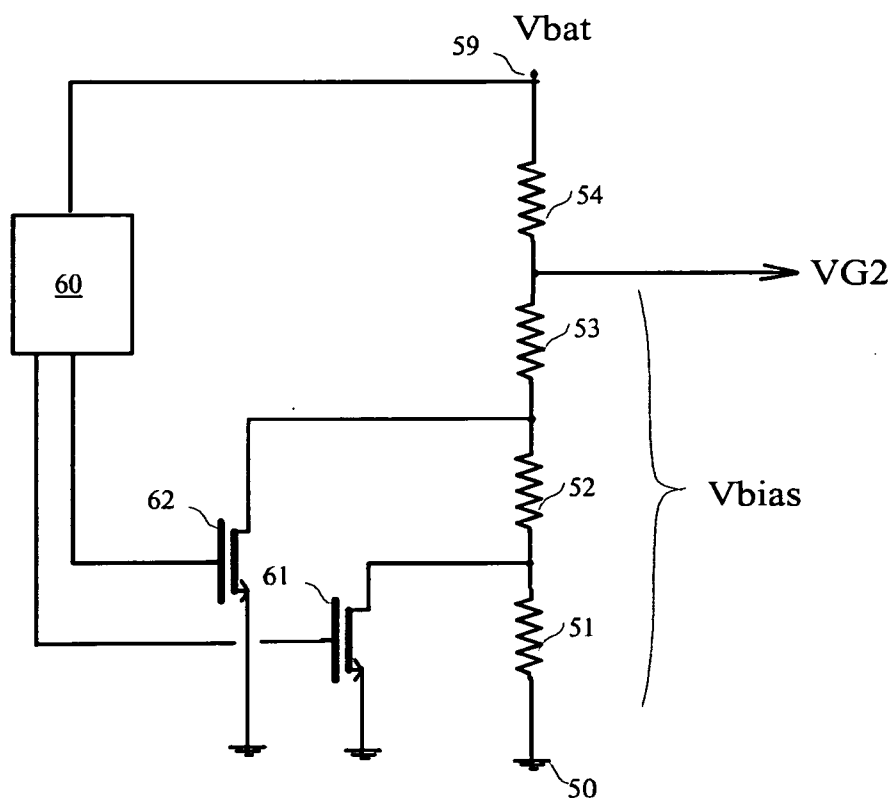


Fig. 7

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2012/001870

A. CLASSIFICATION OF SUBJECT MATTER		
INV.	H03F1/22 H03F3/24	H03F1/52 H03F3/193
	H03F1/32 H01L27/02	H03F1/02 H03F3/19
ADD.		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols) H03F H01L		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) EPO-Internal, WPI Data		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	MINGYUAN LI ET AL: "A single-chip 2.4GHz double cascode power amplifier with switched programmable feedback biasing under multiple supply voltages in 65nm CMOS for WLAN application", RADIO FREQUENCY INTEGRATED CIRCUITS SYMPOSIUM (RFIC), 2010 IEEE, IEEE, PISCATAWAY, NJ, USA, 23 May 2010 (2010-05-23), pages 391-394, XP031684144, ISBN: 978-1-4244-6240-7 page 391, left-hand column, line 12 - page 392, right-hand column, line 31; figures 1,2,3 ----- -/-	1-8
☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents : "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 15 June 2012		Date of mailing of the international search report 06/07/2012
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016		Authorized officer Fedi, Giulio

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2012/001870

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	SOWLATI T ET AL: "A 2.4-GHZ 0.18- μ m CMOS SELF-BIASED CASCODE POWER AMPLIFIER", IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE SERVICE CENTER, PISCATAWAY, NJ, USA, vol. 38, no. 8, 1 August 2003 (2003-08-01), pages 1318-1324, XP001170972, ISSN: 0018-9200, DOI: 10.1109/JSSC.2003.814417 page 1318, left-hand column, line 22 - page 1322, left-hand column, line 15; figures 1,2,3,4 -----	1,4,6-8
X	DE 10 2004 056435 A1 (UNIV STUTTGART [DE]) 1 June 2006 (2006-06-01) paragraphs [0049] - [0061]; figures 1-4 -----	1,4,6-8
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		EP 1815593 A1	08-08-2007
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