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(54) DUAL MODE TRANSISTOR

DOPPELMODUSTRANSISTOR

TRANSISTOR À DOUBLE MODE

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Description

FIELD

[0001] The present disclosure is generally related to a dual mode digital and analog transistor.

DESCRIPTION OF RELATED ART

[0002] Advances in technology have resulted in smaller and more powerful computing devices. For example, there currently exist a variety of portable personal computing devices, including wireless computing devices, such as portable wireless telephones, personal digital assistants (PDAs), and paging devices that are small, lightweight, and easily carried by users. More specifically, portable wireless telephones, such as cellular telephones and Internet protocol (IP) telephones, can communicate voice and data packets over wireless networks. Further, many such wireless telephones include other types of devices that are incorporated therein. For example, a wireless telephone can also include a digital still camera, a digital video camera, a digital recorder, and an audio file player. Also, such wireless telephones can process executable instructions, including software applications, such as a web browser application, that can be used to access the Internet. As such, these wireless telephones can include significant computing capabilities.

[0003] The circuitry within wireless telephones and other electronic devices may include transistors. Transistors may selectively enable current flow between other circuit elements within an electronic device. An amount of current generated by a transistor may be based on a supply voltage provided to the transistor. A transistor that generates relatively high current may enable faster state changes and decreases latency for other circuit components of the electronic device that are dependent on the current for digital applications (on and off two states). Typically, the amount of current generated by a transistor increases as the supply voltages increases. However, increased supply voltages may result in increased power consumption of the electronic device, decreasing battery life. Certain conventional complementary metal oxide semiconductor (CMOS) transistors are not efficient bipolar devices for high performance analog and radio frequency (RF) applications. For example, digital CMOS transistors may be used for low cost analog and RF applications; however, poor performance (e.g., low bipolar current gain (beta)) and complex circuitry may result from using digital CMOS transistors for analog and RF applications.

[0004] US 5 498 885 A describes an integrated circuit with particular application for high frequency modulation circuits, such as a mixer circuit. The circuit comprises a single device comprising a 4 or 5 terminal, gate controlled lateral bipolar junction transistor device, in the form of a merged MOS and lateral bipolar transistor. In a grounded base configuration, RF and LO signals are applied to the gate and emitter terminals respectively and provide for modulated output at the collector.

[0005] US 5 717 241 A describes a gate controlled lateral bipolar junction transistor (GCLBJT) device for an integrated circuit and a method of fabrication thereof. The GCLBJT resembles a merged field effect transistor and lateral bipolar transistor, i.e. a lateral bipolar transistor having base, emitter and collector terminals and a fourth terminal for controlling a gate electrode overlying an active base region. The device is operable as an electronically configurable lateral transistor.

[0006] US 2009/256204 A1 describes a semiconductor-on-insulator transistor device which includes a source region, a drain region, a body region, and a source-side lateral bipolar transistor. The source region has a first conductivity type. The body region has a second conductivity type and is positioned between the source region and the drain region. The source-side lateral bipolar transistor includes a base, a collector, and an emitter. A silicide region connects the base to the collector. The emitter is the body region. The collector has the second conductivity type, and the base is the source region and is positioned between the emitter and the collector.

SUMMARY

[0007] In accordance with the invention a method for biasing a first gate voltage to enable unipolar current to flow from a first region of a transistor to a second region of the transistor according to a field-effect transistor-type operation and biasing a body terminal to enable bipolar current to flow from the first region to the second region according to a bipolar junction transistor-type operation, concurrently, and a corresponding apparatus and non-transitory computer readable medium storing instructions are provided as set forth in the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008]

FIG. 1 is a diagram of a particular illustrative embodiment of a dual mode transistor;

FIG. 2 depicts particular illustrative tables corresponding to biasing characteristics for a dual mode transistor;

FIG. 3 depicts particular illustrative embodiments of field effect transistor (FET)-type configurations of a dual mode transistor;

FIG. 4 depicts particular illustrative embodiments of bipolar junction transistor (BJT)-type configurations of a dual mode transistor;

FIG. 5 depicts particular illustrative embodiments of

an inverter mixer that includes dual mode transistors;

FIG. 6 is a circuit diagram of a particular illustrative embodiment of a differential mixer that includes dual mode transistors;

FIG. 7 depicts particular illustrative embodiments of an inverter driver that includes dual mode transistors;

FIGs. 8a and 8b are diagrams of particular illustrative embodiments of a PNP dual mode transistor;

FIGs. 9a and 9b are diagrams of particular illustrative embodiments of an NPN dual mode transistor;

FIGs. 10a and 10b are particular illustrative charts depicting drain current, a current gain, and a transconductance of a dual mode transistor based on biasing characteristics;

FIG. 11 is a diagram of a particular illustrative embodiment of a silicon-on-insulator (SOI) PNP dual mode transistor;

FIG. 12 is a diagram of a particular illustrative embodiment of a SOI NPN dual mode transistor;

FIG. 13 is a flowchart of a particular embodiment of a method of biasing a dual mode transistor;

FIG. 14 is a block diagram of a wireless device including a dual mode transistor and a component operable to bias the dual mode transistor; and

FIG. 15 is a data flow diagram of a particular illustrative embodiment of a manufacturing process to manufacture electronic devices that include a dual mode transistor and a component operable to bias the dual mode transistor.

DETAILED DESCRIPTION

[0009] Referring to FIG. 1, a particular illustrative embodiment of a dual mode transistor 100 is shown. For example, the dual mode transistor 100 may concurrently operate in a digital metal oxide semiconductor (MOS) mode (e.g., a unipolar operation mode) and an analog gate control bipolar junction transistor (BJT) mode (e.g., bipolar operation mode). The illustrative embodiment in FIG. 1 depicts a cross-sectional view of the dual mode transistor 100.

[0010] The dual mode transistor 100 includes a first gate region 102, a first region 104, a second region 106, and a first body region 108. The first gate region 102 may correspond to a gate of the dual mode transistor 100. In a particular embodiment (e.g., a PNP type configuration), the first region 104 may correspond to a source of the dual mode transistor 100, and the second region 106 may correspond to a drain of the dual mode transistor 100. In another particular embodiment (e.g., an NPN type configuration), the first region 104 may correspond to a drain of the dual mode transistor 100, and the second region 106 may correspond to a source of the dual mode transistor 100. The first body region 108 may correspond to a well. A dielectric may separate the first gate region 102 from the first region 104, the second region 106, and the first body region 108. The dielectric may be an insulating layer comprised of a material with a high dielectric constant. The dual mode transistor 100 may be within a substrate region 110. As explained below, concentrations of each region 102-108 may vary based on a particular configuration of the dual mode transistor 100 (e.g., whether the dual mode transistor has an NMOS & NPN type configuration or a PMOS & PNP type configuration).

[0011] The dual mode transistor 100 also includes a first terminal 112 coupled to the first body region 108, and a second terminal 114 coupled to the substrate region 110. A first shallow trench isolation (STI) area 122 may prevent (or reduce) current leakage (from another transistor structure) from affecting the dual mode transistor 100. A second STI area 124 may prevent (or reduce) current leakage between the second terminal 114 and the second region 106. A third STI area 126 may prevent (or reduce) current leakage between the first region 104 and the first terminal 112, and a fourth STI area 128 may prevent (or reduce) current leakage (from another transistor structure) from affecting the dual mode transistor 100.

[0012] A first gate voltage of the first gate region 102 may be biased to a first voltage (V_1). Biasing the first gate voltage may enable unipolar current to flow from the first region 104 to the second region 106 according to a field effect transistor (FET)-type operation. For example, a source voltage (V_s) may be applied to the first region 104. When the gate-to-source voltage (e.g., a voltage difference between the first voltage (V_1) and the source voltage (V_s)) exceeds a particular voltage level, an inversion layer (e.g., a channel) may be formed within the first body region 108 between the first region 104 and the second region 106. In a particular embodiment, the particular voltage level may be much more than a threshold voltage (V_t) of the dual mode transistor 100 to enable a saturation region current to flow. In another particular embodiment, the particular voltage level may be just above than the threshold voltage (Vt) to enable a triode (linear) region current to flow. In another particular embodiment, the particular voltage level may be less than the threshold voltage (Vt) to turn off current. The unipolar current may flow from the first region 104 to the second region 106 via the inversion layer. Based on the configuration of the dual mode transistor 100, the unipolar current may include electrons flowing from the second region 106 to the first region 104 (e.g., a NPN type configuration), or the unipolar current may include holes flowing from the first region 104 to the second region 106 (e.g., a PNP type configuration). In the illustrated embodiment, a drain voltage

(V_d) may be applied to the second region 106, and a substrate voltage (V_{sub}) may be applied to the second terminal 114. For silicon-on-insulator (SOI) technology, the substrate region 110 may be an oxide layer and the STIs 122-128 may be deep down in the oxide layer. In SOI technology, the substrate voltage (V_{sub}) (e.g., the voltage applied to the second terminal 114) can be removed.

[0013] The first terminal 112 (coupled to the first body region 108) may be biased to a second voltage (V_2). Biasing the first terminal 112 may enable bipolar current to flow between the first region 104 and the second region 106 according to a BJT-type operation with the first terminal 112 current tuning. For example, the first terminal 112 may be biased such that an absolute value of a body-to-source voltage (e.g., a voltage difference between the second voltage (V_2) and the source voltage (V_s)) is greater than a pn forward junction voltage (V_j) of the dual mode transistor 100. To illustrate, biasing the first terminal 112 to the second voltage (V_2) may enable the first body region 108 to operate in a substantially similar manner as a base of a BJT and turn on horizontal gate controlled BJT.

[0014] As described herein, a "junction voltage" (V_j) may correspond to a forward bias voltage between a p-type region and an n-type region. For example, a positive terminal may be coupled to the p-type region and a negative terminal may be coupled to the n-type region. In a horizontal PNP configuration, the p-type region may correspond to the first region 104 and to the second region 106, and the n-type region may correspond to the first body region 108. Alternatively, in a horizontal NPN configuration, the p-type region may correspond to the first body region 108, and the n-type region may correspond to the first region 104 and to the second region 106. The forward bias voltage may be a voltage that enables holes in the p-type region and electrons in the n-type region to be "pushed" towards a junction (e.g., a p-n junction) coupling the p-type region and the n-type region. Thus, the forward bias voltage may reduce a depletion region of a p-n junction and enable bipolar current (e.g., holes and electrons) flow. Thus, biasing the first terminal 112 such that the absolute value of the body-to-source voltage is greater than the forward bias voltage (e.g., the junction voltage (Vj)) may enable bipolar current flow between the n-type region and the p-type region in either a horizontal PNP type device or a horizontal NPN type device.

[0015] As explained below, in a horizontal PNP configuration of the dual mode transistor 100, biasing the first terminal 112 may enable the first region 104 to operate in a substantially similar manner as an emitter of a BJT and may enable the second region 106 to operate in a substantially similar manner as a collector of a BJT. Alternatively, in a horizontal NPN configuration of the dual mode transistor 100, biasing the first terminal 112 may enable the first region 104 to operate in a substantially similar manner as a collector a BJT and may enable the second region 106 to operate in a substantially similar manner as an emitter of a BJT. Thus, a bipolar current (electrons and holes) according to a BJT-type operation may flow between the first region 104 and the second region 106 in response to biasing the first terminal 112 to the second voltage (V_2), and the first terminal 112 current may tune the current flow between the first region 104 and the second region 106.

[0016] In a first particular embodiment, the dual mode transistor 100 may have a PMOS and a horizontal PNP type configuration. For example, the first region 104 and the second region 106 may be doped with a P+ concentration, and the first body region 108 may be doped with an N- concentration. Thus, in the horizontal PNP type configuration, the dual mode transistor 100 may have a p-type emitter 104 and collector 106, and may have a N-type base 108 (e.g., a PNP bipolar transistor (PBJT)). The first terminal 112 may be doped with an N+ concentration, the second terminal 114 may be doped with a P+ concentration, and the substrate region 110 may be doped with a P-concentration. The first gate region 102 may include a P Metal (e.g., a metal with p-type characteristics) or may be doped with a P+ concentration (e.g., a P-Gate PFET). Alternatively, the first gate region 102 may include an N Metal (e.g., a metal with n-type characteristics) or may be doped with an N+ concentration (e.g., an N-Gate PFET).

[0017] During operation of the horizontal PNP type configuration, the first gate region 102 may be biased such that a gate voltage (e.g., the first voltage (V_1)) of the dual mode transistor 100 is lower than the source voltage (V_s) of the dual mode transistor 100. For example, a supply voltage (V_{dd}) may be applied to the first region 104 (e.g., the source), and the first voltage (V_1) is applied to the first gate region 102. Thus, the first voltage (V_1) may range from ground (e.g., zero volts) to the supply voltage (V_{dd}) such that the gate voltage is lower than the source voltage (V_s). Biasing the first gate region 102 with the first voltage (V_1) may enable P-type channel formation (e.g., formation of a P-type inversion layer) within the first body region 108 between the first region 104 and the second region 106. A unipolar current (e.g., holes) according to a PFET operation may flow from the first region 104 to the second region 106.

[0018] The first terminal 112 may be biased to a second voltage (V_2) such that an absolute value of a body-to-source voltage is greater than a junction voltage (Vj) of the dual mode transistor 100. For example, the second voltage (V_2) may be less than a difference of the supply voltage (V_{dd}) applied to the first region 104 and the junction voltage (V_j) (e.g., $V_2 < V_{dd} - V_j$). In a particular embodiment, the second voltage (V_2) applied to the first terminal 112 (coupled to the first body region 108) may be biased to a voltage that is less than a negative forward junction voltage (e.g., -0.7 V) of the dual mode transistor 100. Biasing the first terminal 112 with the second voltage (V_2) may enable the dual mode transistor 100 to operate according to a horizontal PNP BJT. For example, the first body region 108 may operate in a substantially similar

manner as a base of a BJT, the first region 104 may operate in a substantially similar manner as an emitter (e.g., forward bias) of a BJT, and the second region 106 may operate in a substantially similar manner as a collector (e.g., reverse bias) of a BJT.

[0019] The PNP BJT may operate as a current-controlled current regulator. For example, a collector current I_C (e.g., a controlled current by a base current) may flow to the second region 106 (e.g., the collector) from the first region 104 (e.g., the emitter). A base current I_B (e.g., a base controlling current) may flow to the first body region 108 (e.g., the base) from the first region 104 (e.g., the emitter), and the base current I_B may control an amount of collector current I_C. For example, the base current I_B "turns on" the PNP BJT when an absolute value of the body-to-source voltage is greater than the junction voltage (V_j), and the base current I_B enables an amount collector current I_C to flow that is proportional to the base current I_B. Electrons may flow from the first body region 108 to the first region 104, and holes may flow from the first region 104 to the second region 106.

[0020] Thus, in the PNP configuration, a bipolar current (e.g., holes and electrons) and a unipolar current (e.g., holes) may concurrently flow between the first region 104 and the second region 106. The bipolar current may be associated with a BJT operation, and the unipolar current may be associated with the FET operation. During concurrent bipolar and unipolar operation, the first gate region 102 may control a current gain (beta) of the dual mode transistor 100's horizontal PNP, a transconductance of the dual mode transistor 100, and a resistance of the dual mode transistor 100. For example, the gate voltage (e.g., the first voltage (V_1)) may be selectively decreased to enable increased holes (e.g., unipolar current) to flow between the first region 104 and the second region 106. The resistance of the dual mode transistor 100 may be proportional to current and voltage applied to the dual mode transistor 100.

[0021] In a second particular embodiment, the dual mode transistor 100 may have a NMOS type configuration. For example, the first region 104 and the second region 106 may be doped with an N+ concentration, and the first body region 108 may be doped with a P- concentration. Thus, in the NMOS type configuration, the dual mode transistor 100 may be an n-type metal oxide semiconductor (NMOS) transistor (e.g., an n-type field effect transistor (NFET). The first terminal 112 may be doped with a P+ concentration, the second terminal 114 may be doped with an N+ concentration, and the substrate region 110 may be doped with a P-concentration. In the horizontal NPN type configuration, the dual mode transistor 100 may also include a second body region (not shown) between the first body region 108 and the substrate region 110. The second body region may be doped with an N- concentration (deep Nwell) and may be coupled to the second terminal 114. The first gate region 102 may include a P Metal or may be doped with a P+ concentration (e.g., a P-Gate NFET). Alternatively, the first gate region 102 may include an N Metal or may be doped with an N+ concentration (e.g., an N-Gate NFET).

[0022] During operation of the horizontal NPN type configuration, the first gate region 102 may be biased such that a gate voltage of the dual mode transistor 100 is greater than a source voltage of the dual mode transistor 100. For example, a ground voltage (e.g., zero volts) may be applied to the second region 106 (e.g., the source), and the first voltage (V_1) is applied to the first gate region 102. Thus, the first voltage (V_1) may range from ground to the supply voltage (V_{dd}) such that the first voltage (V_1) is greater than the source voltage. Biasing the first gate region 102 with the first voltage (V_1) may enable N type channel formation (e.g., formation of an inversion N-type layer) within the first body region 108 between the first region 104 and the second region 106. A unipolar current (e.g., electrons) according to an NFET operation may flow from the first region 104 to the second region 106.

[0023] The first terminal 112 may be biased to a second voltage (V_2) such that an absolute value of a body-to-source voltage is greater than a junction voltage (V_j) of the dual mode transistor 100. For example, the second voltage (V_2) may be greater than the junction voltage (V_j) (e.g., $V_2 > V_j$). In a particular embodiment, the second voltage (V_2) applied to the first terminal 112 (coupled to the first body region 108) may be biased to a voltage that is greater than a forward junction voltage (e.g., 0.7 V) of the dual mode transistor 100. Biasing the first terminal 112 with the second voltage (V_2) may enable the dual mode transistor 100 to operate according to an NPN BJT. For example, the first body region 108 may operate in a substantially similar manner as a base of a BJT, the first region 104 may operate in a substantially similar manner as a collector (e.g., reverse bias) of a BJT, and the second region 106 may operate in a substantially similar manner as an emitter (e.g., forward bias) of a BJT.

[0024] The NPN BJT may operate as a current-controlled current regulator. For example, a collector current I_C (e.g., a controlled current by a base current) may flow to the second region 106 (e.g., the emitter) from the first region 104 (e.g., the collector). A base current I_B (e.g., a controlling current) may flow to the second region 106 (e.g., the emitter) from the first body region 108 (e.g., the base), and the base current I_B may control an amount of collector current I_C. For example, the base current I_B "turns on" the PNP BJT when the body-to-source voltage is greater than the junction voltage (V_j), and the base current I_B enables an amount of collector current I_C to flow that is proportional to the base current I_B. Holes may flow from the first body region 108 to the second region 106, and electrons may flow from the second region 106 to the first region 104.

[0025] Thus, in the NPN configuration, a bipolar current (e.g., holes and electrons) and a unipolar current (e.g., electrons) may concurrently flow between the first region 104 and the second region 106. The bipolar current may

be associated with a BJT operation, and the unipolar current may be associated with the FET operation. During concurrent bipolar and unipolar operation, the first gate region 102 may control a current gain (beta) of the dual mode transistor 100, a transconductance of the dual mode transistor 100, and a resistance of the dual mode transistor 100. For example, the gate voltage (e.g., the first voltage (V_1)) may be selectively increased to enable increased electrons (e.g., unipolar current) to flow between the first region 104 and the second region 106. The resistance of the dual mode transistor 100 may be proportional to current and voltage applied to the dual mode transistor 100.

[0026] Biasing the first terminal 112 may enable a concurrent digital MOS operation mode (e.g., a unipolar operation mode) and an analog gate control BJT operation mode (e.g., bipolar operation mode). Thus, a gate controlled horizontal NPN operation and an increased current, based on the unipolar current and the bipolar current, may flow through the dual mode transistor 100 without increasing a supply voltage (V_{dd}) applied to the dual mode transistor 100. Increasing the current without increasing the supply voltage (V_{dd}) provides increased operation efficiency and provides a gate controlled bipolar NPN transistor for high performance analog and RF application. It will be appreciated that in other embodiments, the techniques described with respect to the dual mode transistor 100 may be implemented in other transistor configurations. For example, in the illustrative embodiment, the dual mode transistor 100 may correspond to a planar CMOS transistor and a BJT device. In another particular embodiment, the dual mode transistor 100 may correspond to a three dimensional fin-type field-effect transistor (3D Finfet) CMOS and a BJT device.

[0027] Referring to FIG. 2, particular illustrative tables 200, 210 corresponding to biasing characteristics for a dual mode transistor are shown. For example, the biasing characteristics (e.g., voltages) illustrated in the first table 200 and the second table 210 may correspond to biasing characteristics for the dual mode transistor 100 of FIG. 1. The first table 200 may correspond to biasing characteristics as described with respect to the PNP type configuration of the dual mode transistor 100. The second table 210 may correspond to biasing characteristics as described with respect to the NPN type configuration of the dual mode transistor 100.

[0028] According to the PNP type configuration (e.g., the first table 200), the first voltage (V_1) applied to the first gate region 102 may be biased between ground (e.g., zero volts) and the supply voltage (V_{dd}). For example, the first voltage (V_1) may be applied such that a gate-to-source voltage (V_{GS}) of the dual mode transistor 100 enables channel formation (e.g., formation of a P type inversion layer) within the first body region 108 between the first region 104 and the second region 106. A unipolar current (e.g., holes) according to a FET operation may flow from the first region 104 to the second region 106. The first voltage (V_1) may be adjusted between ground and the supply voltage (V_{dd}) to adjust (e.g., enlarge) a current gain (beta) of the dual mode transistor 100, a transconductance of the dual mode transistor 100, and a resistance of the dual mode transistor 100 when the second voltage (V_2) turns on the horizontal PNP.

[0029] The drain voltage (V_d) applied to the second region 106 (e.g., the drain) may be biased to ground. The source voltage (V_s) applied to the first region 104 (e.g., the source) may be biased to the supply voltage (V_{dd}). The second voltage (V_2) applied to the first terminal 112 (coupled to the first body region 108) may be biased to a voltage that is less than a negative forward junction voltage (e.g., -0.7 V) of the dual mode transistor 100. For example, the second voltage (V_2) may be less than a difference of the supply voltage (V_{dd}) applied to the first region 104 and the junction voltage (V_j) (e.g., $V_2 < V_{dd} - V_j$). Electrons may flow from the first body region 108 to the first region 104, and holes may flow from the first region 104 to the second region 106. Thus, in the PNP configuration, a bipolar current (e.g., holes and electrons) and unipolar current may be generated. The bipolar current may be associated with a BJT operation, and the unipolar current may be associated with a FET operation.

[0030] According to the NPN type configuration (e.g., the second table 210), the first voltage (V_1) applied to the first gate region 102 may be biased between the supply voltage (V_{dd}) and ground (e.g., zero volts). For example, the first voltage (V_1) may be applied such that a gate-to-source voltage (V_{GS}) of the dual mode transistor 100 enables channel formation (e.g., formation of an N type inversion layer) within the first body region 108 between the first region 104 and the second region 106. A unipolar current (e.g., electrons) according to a FET operation may flow to the first region 104 from the second region 106. The first voltage (V1) may be adjusted between ground and the supply voltage (V_{dd}) to adjust (e.g., enlarge) a current gain (beta) of the dual mode transistor 100, a transconductance of the dual mode transistor 100, and a resistance of the dual mode transistor 100 when the second voltage (V_2) turns on the horizontal NPN.

[0031] The drain voltage (V_d) applied to the first region 104 (e.g., the drain) may be biased to the supply voltage (V_{dd}). The source voltage (V_s) applied to the second region 106 (e.g., the source) may be biased to ground. The second voltage (V_2) applied to the first terminal 112 (coupled to the first body region 108) may be biased to a voltage that is greater than a forward junction voltage (e.g., 0.7 V) of the dual mode transistor 100. For example, the second voltage (V_2) may be greater than a difference of the junction voltage (V_j) and the ground voltage applied to the second region 106 (e.g., $V_2 > V_j$). Holes may flow from the first body region 108 to the second region 106, and electrons may flow from the second region 106 to the first region 104. Thus in the NPN configuration, a bipolar current (e.g., holes and electrons) according to a BJT operation may be generated.

[0032] The tables 200, 210 depicted in FIG. 2 include non-limiting examples of biasing characteristics for the

dual mode transistor 100 of FIG. 1. For example, the tables 200, 210 illustrate that a unipolar current and a bipolar current may be generated concurrently by biasing the first terminal 112 with the second voltage (V_2) such that an absolute value of the body-to-source voltage is greater than a junction voltage (V_j) of the dual mode transistor 100. It will be appreciated that other (e.g., different) characteristics and/or configurations may be implemented with respect to other embodiments. Biasing the first terminal 112 with the second voltage (V_2) may enable the dual mode transistor 100 to operate according to a PNP BJT or a NPN BJT. Biasing the first gate region 102 with the first voltage (V_1) may enable the dual mode transistor 100 to operate according to a FET. Thus, the dual mode transistor 100 may concurrently operate in a digital MOS mode (e.g., a unipolar operation mode) and an analog gate control BJT mode (e.g., bipolar operation mode).

[0033] Referring to FIG. 3, particular illustrative embodiments of field effect transistor (FET)-type configurations of a dual mode transistor are shown. A first embodiment 310 and a second embodiment 320 illustrate p-type FET (PFET) configurations of a dual mode transistor. A third embodiment 330 and a fourth embodiment 340 illustrate n-type FET (NFET) configurations of a dual mode transistor. Each embodiment 310-340 may correspond to the dual mode transistor 100 of FIG. 1.

[0034] According to the first embodiment 310, the PFET configuration may include a gate that is doped with a P+ concentration or a gate that includes a P-Metal. The first embodiment 310 may enable a digital complementary metal oxide semiconductor (CMOS) mode. For example, the first embodiment 310 may enable a unipolar current (e.g., holes) to flow from a source terminal (S) to drain terminal (D). To enable the digital CMOS mode, the absolute value of a gate-to-source voltage should be larger than an absolute threshold voltage (e.g., $|V_g - V_s| > |V_t|$). The drain voltage (V_d) should be grounded, and a source voltage (Vs) should be approximately equal to a supply voltage (V_{dd}). In addition, the voltage applied to the body region should be approximately equal to a supply voltage (V_{dd}).

[0035] According to the second embodiment 320, the PFET configuration may include a gate that is doped with an N+ concentration or a gate that includes an N-Metal. The second embodiment 320 may enable a digital CMOS mode. For example, the second embodiment 320 may enable a unipolar current (e.g., holes) to flow from a source terminal (S) to drain terminal (D). To enable the digital CMOS mode, the absolute value of a gate-to-source voltage should be larger than an absolute threshold voltage (e.g., $|V_g - V_s| > |V_t|$. The drain voltage (V_d) should be grounded, and a source voltage (Vs) should be approximately equal to a supply voltage (V_{dd}). In addition, the voltage applied to the body region should be approximately equal to a supply voltage (V_{dd}).

[0036] According to the third embodiment 330, the NFET configuration may include a gate that is doped with a P+ concentration or a gate that includes a P-Metal. The third embodiment 330 may also enable a digital CMOS mode. For example, the third embodiment 330 may enable a unipolar current (e.g., electrons) to flow from a source terminal (S) to drain terminal (D). To enable the digital CMOS mode, the absolute value of a gate-to-source voltage should be larger than an absolute threshold voltage (e.g., $|V_g - V_s| > |V_t|$. The drain voltage (V_d) should be approximately equal to a supply voltage (V_{dd}), and a source voltage (Vs) should be grounded (e.g., zero volts). In addition, the voltage applied to the body region should be grounded.

[0037] According to the fourth embodiment 340, the NFET configuration may include a gate that is doped with an N+ concentration or a gate that includes an N-Metal. The fourth embodiment 340 may also enable a digital CMOS mode. For example, the fourth embodiment 340 may enable a unipolar current (e.g., electrons) to flow from a source terminal (S) to drain terminal (D). To enable the digital CMOS mode, the absolute value of a gate-to-source voltage should be larger than an absolute threshold voltage (e.g., $|V_g - V_s| > |V_t|$. The drain voltage (V_d) should be approximately equal to a supply voltage (V_{dd}), and a source voltage (Vs) should be grounded (e.g., zero volts). In addition, the voltage applied to the body region should be grounded.

[0038] Referring to FIG. 4, particular illustrative embodiments of binary junction transistor (BJT)-type configurations of a dual mode transistor are shown. A first embodiment 410 and a second embodiment 420 illustrate PNP configurations of a dual mode transistor. The first embodiment 410 may operate in conjunction with the first embodiment 310 of FIG. 3, and the second embodiment 420 may operate in conjunction with the second embodiment 320 of FIG. 3. A third embodiment 430 and a fourth embodiment 440 illustrate NPN configurations of a dual mode transistor. The third embodiment 430 may operate in conjunction with the third embodiment 330 of FIG. 3, and the fourth embodiment 440 may operate in conjunction with the fourth embodiment 340 of FIG. 3. Each embodiment 410-440 may correspond to the dual mode transistor 100 of FIG. 1.

[0039] According to the first embodiment 410, the PNP configuration may include a gate that is doped with a P+ concentration or a gate that includes a P-Metal. The first embodiment 410 may enable an analog gate control bipolar junction transistor (BJT) mode. For example, the first embodiment 410 may enable a bipolar current (e.g., holes and electrons). For example, holes may flow from an emitter terminal (E) to a collector terminal (C), and electrons may flow from a base terminal (B) to the emitter terminal (E). To enable the analog gate control BJT mode, the gate-to-emitter (source) voltage should be larger than a junction (e.g., threshold) voltage (e.g., $|V_g - V_e| > V_t|$). The emitter voltage (V_e) should be Vdd, and the collector voltage (V_c) should be approximately equal to ground. An absolute value of a base-to-emitter voltage should be larger than a junction threshold (e.g., 0.7 volts)

(e.g., $|V_b - V_e| > 0.7$ V).

[0040] According to the second embodiment 420, the PNP configuration may include a gate that is doped with an N+ concentration or a gate that includes an N-Metal. The second embodiment 420 may also enable an analog gate control BJT mode. For example, the second embodiment 420 may enable a bipolar current (e.g., holes and electrons). For example, holes may flow from an emitter terminal (E) to a collector terminal (C), and electrons may flow from a base terminal (B) to the emitter terminal (E). To enable the analog gate control BJT mode, the gate-to-emitter (source) voltage should be larger than a junction (e.g., threshold) voltage (e.g., $|V_g - V_e| > V_t|$). The emitter voltage (V_e) should be Vdd, and the collector voltage (V_c) should be approximately equal to ground. An absolute value of a base-to-emitter voltage should be larger than a junction threshold (e.g., 0.7 volts) (e.g., $|V_b - V_e| > 0.7$ V).

[0041] According to the third embodiment 430, the NPN configuration may include a gate that is doped with a P+ concentration or a gate that includes a P-Metal. The third embodiment 430 may also enable an analog gate control BJT mode. For example, the third embodiment 430 may enable a bipolar current (e.g., holes and electrons). For example, holes may flow from a base terminal (B) to an emitter terminal (E), and electrons may flow from the emitter terminal (E) to a collector terminal (C). To enable the analog gate control BJT mode, the gate-to-emitter (source) voltage should be larger than a junction (e.g., threshold) voltage (e.g., $V_g - V_e > Vt$). The emitter voltage (V_e) should be approximately equal to ground, and the collector voltage (V_c) should be Vdd. An absolute value of a base-to-emitter voltage should be larger than a junction threshold (e.g., 0.7 volts) (e.g., $|V_b - V_e| > 0.7$ V).

[0042] According to the fourth embodiment 440, the NPN configuration may include a gate that is doped with an N+ concentration or a gate that includes an N-Metal. The fourth embodiment 440 may also enable an analog gate control BJT mode. For example, the fourth embodiment 440 may enable a bipolar current (e.g., holes and electrons). For example, holes may flow from a base terminal (B) to an emitter terminal (E), and electrons may flow from the emitter terminal (E) to a collector terminal (C). To enable the analog gate control BJT mode, the gate-to-emitter (source) voltage should be larger than a junction (e.g., threshold) voltage (e.g., $V_g - V_e > Vt$). The emitter voltage (V_e) should be approximately equal to ground, and the collector voltage (V_c) should be Vdd. An absolute value of a base-to-emitter voltage should be larger than a junction threshold (e.g., 0.7 volts) (e.g., $|V_b - V_e| > 0.7$ V).

[0043] Referring to FIG. 5, particular illustrative embodiments 510, 520 of an inverter mixer that includes dual mode transistors are shown.

[0044] A first embodiment 510 of the inverter mixer includes a first dual mode transistor 512 and a second dual mode transistor 514. In a particular embodiment, the first dual mode transistor 512 and the second dual mode transistor 514 may each correspond to the dual mode transistor 100 of FIG. 1. Alternatively, or in addition, the first dual mode transistor 512 and the second dual mode transistor 514 may each correspond to any of the embodiments 310-340 of FIG. 3 and the corresponding embodiments 410-440 of FIG. 4.

[0045] In the first embodiment 510, a first body region of the first dual mode transistor 512 may be coupled to a second body region of the second dual mode transistor 514. The first body region and the second body region may also be coupled to receive a first input signal 516. The first input signal 516 may correspond to a local oscillator (LO) signal. A first gate of the first dual mode transistor 512 may be coupled to a second gate of the second dual mode transistor 514. The first gate and the second gate may also be coupled to receive a second input signal 518. The second input signal 518 may correspond to a radio frequency (RF) signal.

[0046] A first source (e.g., a first emitter) of the first dual mode transistor 512 may be coupled to receive a supply voltage (V_{dd}), and a second source (e.g., a second emitter) of the second dual mode transistor 514 may be coupled to ground (V_{ss}). A first drain (e.g., a first collector) of the first dual mode transistor 512 may be coupled to a second drain (e.g., a second collector) of the second dual mode transistor 514. The first drain and the second drain may generate an output signal 519. The output signal 519 may correspond to a sum of the RF signal and the LO signal.

[0047] The first dual mode transistor 512 may be a PMOS (PNP) transistor, and the second dual mode transistor 514 may be an NMOS (NPN) transistor. The first embodiment 510 may invert the second input signal 518 (e.g., the RF signal) and mix the inverted second input signal with the first input signal 516 (e.g., the LO signal) applied to the first body region. For example, when the second input signal 518 has a logic low voltage level, the first dual mode transistor 512 may be activated and a RF signal (e.g., 518) is inverted from the second input signal 518 to output 519 according to concurrent bipolar and unipolar operation, as described above. For example, the logic low voltage level of the second input signal 518 may enable a unipolar current (e.g., holes) to flow from the first source to the first drain and tuned by the second input signal 518, and the first input signal 516 (having a logic voltage level that is less than a negative forward junction voltage (V_j) of the first dual mode transistor 512) may enable a bipolar current to flow and tuned by the first input signal 516.

[0048] Alternatively, when the second input signal 518 has a logic high voltage level, the second dual mode transistor 514 may be activated and a RF signal (e.g., 518) is inverted from the second input signal 518 to output 519 according to concurrent bipolar and unipolar operation, as described above. For example, the logic high voltage level of the second input signal 518 may enable a unipolar current (e.g., electrons) to flow from the second source to the second drain and tuned by the second input signal

518, and the first input signal 516 (having a logic voltage level that is greater than a forward junction voltage (V_j) of the second dual mode transistor 514) may enable a bipolar current to flow and tuned by the first input signal 516.

[0049] A second embodiment 520 of the inverter mixer includes a first dual mode transistor 522 and a second dual mode transistor 524. In a particular embodiment, the first dual mode transistor 522 and the second dual mode transistor 524 may each correspond to the dual mode transistor 100 of FIG. 1. Alternatively, or in addition, the first dual mode transistor 522 and the second dual mode transistor 524 may each correspond to any of the embodiments 310-340 of FIG. 3 and the corresponding embodiments 410-440 of FIG. 4.

[0050] In the second embodiment 520, a first body region of the first dual mode transistor 522 may be coupled to receive a first input signal 516. The first input signal 526 may be a first LO signal having a voltage ranging approximately from a relatively high range (e.g., 0.4 V to 1.5 V). A second body region of the second dual mode transistor 524 may be coupled to receive a second input signal 527. The second input signal 527 may be a second LO signal having a voltage ranging approximately from a relatively low range (e.g., 0 V to 1.2 V). A first gate of the first dual mode transistor 522 may be coupled to a second gate of the second dual mode transistor 524. The first gate and the second gate may also be coupled to receive a third input signal 528. The third input signal 528 may correspond to an RF signal.

[0051] A first source (e.g., a first emitter) of the first dual mode transistor 522 may be coupled to receive a supply voltage (V_{dd}), and a second source (e.g., a second emitter) of the second dual mode transistor 524 may be coupled to ground (V_{ss}). A first drain (e.g., a first collector) of first dual mode transistor 522 may be coupled to a second drain (e.g., a second collector) of the second dual mode transistor 524. The first drain and the second drain may generate an output signal 529. The output signal 529 may correspond to a sum of the RF signal and the LO signals.

[0052] The first dual mode transistor 522 may be a PMOS (PNP) transistor, and the second dual mode transistor 524 may be an NMOS (NPN) transistor. The second embodiment 520 may invert the third input signal 528 (e.g., the RF signal) and mix the inverted third input signal with the first input signal 526 (e.g., the LO signal) applied to the first body region (and/or with the second input signal 527 applied to the second body region). For example, when the third input signal 528 has a logic low voltage level, the first dual mode transistor 522 may be activated and a RF signal (e.g., 528) is inverted from the third input signal 528 to output signal 529 according to concurrent bipolar and unipolar operation, as described above. For example, the logic low voltage level of the third input signal 528 may enable a unipolar current (e.g., holes) to flow from the first source to the first drain and tuned by the third input signal 528, and the first input signal 526 (having a logic voltage level that is less than a negative forward junction voltage (V_j) of the first dual mode transistor 522) may enable a bipolar current to flow and tuned by the first input signal 526.

[0053] Alternatively, when the third input signal 528 has a logic high voltage level, the second dual mode transistor 524 may be activated and a RF signal (e.g., 528) is inverted from the third input signal 528 to output signal 529 according to concurrent bipolar and unipolar operation, as described above. For example, the logic high voltage level of the third input signal 528 may enable a unipolar current (e.g., electrons) to flow from the second source to the second drain and tuned by the third input signal 528, and the second input signal 527 (having a logic voltage level that is greater than a forward junction voltage (V_j) of the second dual mode transistor 524) may enable a bipolar current to flow and tuned by the second input signal 527.

[0054] Referring to FIG. 6, a particular illustrative embodiment of a differential mixer 600 that includes dual mode transistors is shown. For example, the differential mixer 600 includes a first dual mode transistor 602 and a second dual mode transistor 604. In a particular embodiment, the first dual mode transistor 602 and the second dual mode transistor 604 may each correspond to the dual mode transistor 100 of FIG. 1. Alternatively, or in addition, the first dual mode transistor 602 and the second dual mode transistor 604 may each correspond to any of the embodiments 310-340 of FIG. 3 and the corresponding embodiments 410-440 of FIG. 4.

[0055] A first gate of the first dual mode transistor 602 may be coupled to receive a first signal of a first differential signal. The first differential signal may be a radio frequency (RF) signal. A second gate of the second dual mode transistor 604 may be coupled to receive a second (e.g., complementary) signal of the first differential signal. A first body region of the first dual mode transistor 602 may be coupled to receive a second signal of a second differential signal. The second differential signal may be a local oscillator (LO) signal. A second body region of the second dual mode transistor 604 may be coupled to receive a first (e.g., complementary) signal of the second differential signal.

[0056] A first source (e.g., a first emitter) of the first dual mode transistor 602 may be coupled to a second source (e.g., a second emitter) of the second dual mode transistor 604. The first drain and the second drain may generate a differential output signal. For example, the output signal may be an intermediate frequency signal.

[0057] Thus, the differential mixer 600 of FIG. 6 may include two dual mode transistors 602, 604 that are differentially driven. The differential mixer 600 may enable a relatively high native small-signal gain from NMOS and BJT modulation, which may lead to a relatively high conversion gain. Due to a single-stage operation and the relatively high conversion gain, the differential mixer 600 may generate less noise and better gain and linearity than a conventional Gilbert differential mixer (not shown).

The (two transistor) dual mode differential mixer 600 reduces stages from two to one and improves delay, power efficiency and gain. For example, the differential mixer 600 has two dual mode transistors and one stage in comparison with the six traditional transistors and two stages of the Gilbert differential mixer. The differential mixer 600 may also operate in a lower power mode and may enable single direct-current (DC) bias for mixing operations.

[0058] Referring to FIG. 7, particular illustrative embodiments 710, 720 of an inverter driver that includes dual mode transistors are shown. A first embodiment 710 of the inverter driver includes a first dual mode transistor 712 and a second dual mode transistor 714.

[0059] In a particular embodiment, the first dual mode transistor 712 and the second dual mode transistor 714 may each correspond to the dual mode transistor 100 of FIG. 1. Alternatively, or in addition, the first dual mode transistor 712 and the second dual mode transistor 714 may each correspond to any of the embodiments 310-340 of FIG. 3 and the corresponding embodiments 410-440 of FIG. 4.

[0060] In the first embodiment 710, a first body region of the first dual mode transistor 712 may be coupled to a second body region of the second dual mode transistor 714. The first body region and the second body region may also be coupled to receive a first input signal 716. A first gate of the first dual mode transistor 712 may be coupled to a second gate of the second dual mode transistor 714. The first gate and the second gate may also be coupled to receive the first input signal 516.

[0061] A first source (e.g., a first emitter) of the first dual mode transistor 712 may be coupled to receive a supply voltage (V_{dd}), and a second source (e.g., a second emitter) of the second dual mode transistor 714 may be coupled to ground (V_{ss}). A first drain (e.g., a first collector) of first dual mode transistor 712 may be coupled to a second drain (e.g., a second collector) of the second dual mode transistor 714. The first drain and the second drain may generate an output signal 719.

[0062] The first dual mode transistor 712 may be a PMOS (PNP) transistor, and the second dual mode transistor 714 may be an NMOS (NPN) transistor. The first embodiment 710 may invert the first input signal 716 and drive the inverted first input signal to an output. For example, when the first input signal 716 has a logic low voltage level, the first dual mode transistor 712 may be activated and a logic low voltage level signal (e.g., 716) is inverted from the first input signal 716 to the output signal 719 according to concurrent bipolar and unipolar operation, as described above. For example, the logic low voltage level of the first input signal 716 may enable a unipolar current (e.g., holes) to flow from the first source to the first drain and tuned by the first input signal 716. The low voltage level of the first input signal 716 may be less than a negative forward junction voltage (Vj) of the first dual mode transistor 712, enabling a bipolar current to flow when applied to the first body region and tuned by the first input signal 716.

[0063] Alternatively, when the first input signal 716 has a logic high voltage level, the second dual mode transistor 714 may be activated and a logic high voltage level signal (e.g., 716) is inverted from the first input signal 716 to the output signal 719 according to concurrent bipolar and unipolar operation, as described above. For example, the logic high voltage level of the first input signal 716 may enable a unipolar current (e.g., electrons) to flow from the second source to the second drain and tuned by the first input signal 716. The high voltage level of the first input signal 716 may be greater than a forward junction voltage (V_j) of the second dual mode transistor 714, enabling a bipolar current to flow when applied to the first body region and tuned by the first input signal 716.

[0064] A second embodiment 720 of the inverter driver includes a first dual mode transistor 722 and a second dual mode transistor 724. In a particular embodiment, the first dual mode transistor 722 and the second dual mode transistor 724 may each correspond to the dual mode transistor 100 of FIG. 1. Alternatively, or in addition, the first dual mode transistor 722 and the second dual mode transistor 724 may each correspond to any of the embodiments 310-340 of FIG. 3 and the corresponding embodiments 410-440 of FIG. 4.

[0065] In the second embodiment 720, a first body region of the first dual mode transistor 722 may be coupled to receive a first input signal 726. A first gate of the first dual mode transistor 722 may be coupled to a second gate of the second dual mode transistor 724. The first gate and the second gate may also be coupled to receive a second input signal 727. A second body region of the second dual mode transistor 724 may be coupled to receive a third input signal 728.

[0066] A first source (e.g., a first emitter) of the first dual mode transistor 722 may be coupled to receive a supply voltage (V_{dd}), and a second source (e.g., a second emitter) of the second dual mode transistor 724 may be coupled to ground (V_{ss}). A first drain (e.g., a first collector) of first dual mode transistor 722 may be coupled to a second drain (e.g., a second collector) of the second dual mode transistor 724. The first drain and the second drain may generate an output signal 729.

[0067] The first dual mode transistor 722 may be a PMOS (PNP) transistor, and the second dual mode transistor 724 may be an NMOS (NPN) transistor. The second embodiment 720 may invert the second input signal 727 and drive the inverted second input signal to an output. For example, when the second input signal 727 has a logic low voltage level, the first dual mode transistor 722 may be activated and a logic low voltage level signal (e.g., 727) is inverted from the second input signal 727 to the output signal 729 according to concurrent bipolar and unipolar operation, as described above. For example, the logic low voltage level of the second input signal 727 may enable a unipolar current (e.g., holes) to flow from the first source to the first drain and tuned by the second input signal 727. The first input signal 726 may have a logic low voltage level that is less than a negative

forward junction voltage (Vj) of the first dual mode transistor 722, enabling a bipolar current to flow when applied to the first body region and tuned by the first input signal 726.

[0068] Alternatively, when the second input signal 727 has a logic high voltage level, the second dual mode transistor 724 may be activated and a logic high voltage level signal (e.g., 727) is inverted from the second input signal 727 to the output signal 729 according to concurrent bipolar and unipolar operation, as described above. For example, the logic high voltage level of the second input signal 727 may enable a unipolar current (e.g., electrons) to flow from the second source to the second drain. The third input signal 728 may have a logic high voltage level that is greater than a forward junction voltage (V_j) of the second dual mode transistor 724, enabling a bipolar current to flow when applied to the first body region and tuned by the third input signal 728.

[0069] Referring to FIG. 8a, a particular illustrative embodiment of a PNP dual mode transistor 800a is shown. In a particular embodiment, the PNP dual mode transistor 800a may correspond to the dual mode transistor 100 of FIG. 1.

[0070] The PNP dual mode transistor 800a includes a first N- base region 807a and a second N- base region 808a. Each N- base region 807a, 808a may have a particular width (W). The first N- base region 807a and the second N- base region 808a may be coupled to (or include) an N- base well 809a. An N++ base contact 812a, 836a may also be coupled to the N- base regions 807a, 808a via the N- base well 809a. In a particular embodiment, the N++ base contact 812a, 836a may correspond to the first terminal 112 of FIG. 1. The PNP dual mode transistor 800a also includes an emitter region 806a, a first collector region 804a, and a second collector region 832a. The emitter region 806a, the first collector region 804a, and the second collector region 832a may each be doped with a P++ concentration. A first STI area 822a may prevent (or reduce) current leakage (from N++ base to P++ collector) from affecting the PNP dual mode transistor 800a. A second STI area 826a may prevent (or reduce) current leakage between the first collector region 804a and the N++ base contact 812a.

[0071] A first gate 801a may be coupled to the first N- base region 807a via a dielectric layer, and a second gate 802a may be coupled to the second N- base region 808a via a dielectric layer. A current gain of the PNP dual mode transistor 800a may be controlled by a gate voltage applied to the gates 801a, 802a. The PNP dual mode transistor 800a may also include a P- substrate 810a.

[0072] The PNP dual mode transistor 800a may operate in a digital MOS mode (e.g., a unipolar operation mode) and an analog gate control BJT mode (e.g., bipolar operation mode). For example, the gate voltages may be biased so that a gate-source-voltage enables formation of an inversion layer within the second N- base region 808a. A unipolar current (e.g., holes) may flow between the first collector region 804a, 832a and the emitter region 806a. The N++ base contact 812a, 836a may be biased such that an absolute value of a voltage difference between the N- base well 809a and the first collector region 804a, second collector region 832a is greater than a forward junction voltage (Vj) of the PNP dual mode transistor 800a. In a particular embodiment, the N++ base contact may be biased to a voltage that is less than a negative forward junction voltage (e.g., -0.7 V) of the PNP dual mode transistor 800a. Biasing the N++ base contact may enable the PNP dual mode transistor 800a to operate according to a PNP BJT (e.g., generate a bipolar current including holes and electrons).

[0073] Referring to FIG. 8b, a particular illustrative embodiment of a PNP dual mode transistor 800b is shown. In a particular embodiment, the PNP dual mode transistor 800b may correspond to the dual mode transistor 100 of FIG. 1.

[0074] The PNP dual mode transistor 800b includes a first N- base region 807b and a second N- base region 808b. Each N- base region 807b, 808b may have a particular width (W). The first N- base region 807b and the second N- base region 808b may be coupled to (or include) an N- base well 809b. An N++ base contact 812b, 836b may also be coupled to the N- base regions 807b, 808b via the N- base well 809b. In a particular embodiment, the N++ base contact 812b, 836b may correspond to the first terminal 112 of FIG. 1. The PNP dual mode transistor 800b also includes an emitter region 806b, a first collector region 804b, and a second collector region 832b. The emitter region 806b, the first collector region 804b, and the second collector region 832b may each be doped with a P++ concentration. A first STI area 822b may prevent (or reduce) current leakage (from other transistors) from affecting the PNP dual mode transistor 800b. A second STI area 826b may prevent (or reduce) current leakage from other transistors.

[0075] A first gate 801b may be coupled to the first N- base region 807b via a dielectric layer, and a second gate 802b may be coupled to the second N- base region 808b via a dielectric layer. Isolate gates 803b, 805b may be coupled to the third and fourth N- base region 811b, 835b via a dielectric layer. The isolate gates 803b, 805b may be used to isolate N++ base contact from P++ collector. A current gain of the PNP dual mode transistor 800b may be controlled by a gate voltage applied to the gates 801b, 802b. The PNP dual mode transistor 800b may also include a P- substrate 810b.

[0076] The PNP dual mode transistor 800b may operate in a digital MOS mode (e.g., a unipolar operation mode) and an analog gate control BJT mode (e.g., bipolar operation mode). For example, the gate voltages may be biased so that a gate-source-voltage enables formation of an inversion layer within the first and second N- base region 807b, 808b. A unipolar current (e.g., holes) may flow between the collector regions 804b, 832b and the emitter region 806b. The N++ base contact 812b, 836b may be biased such that an absolute value of a voltage difference between the N- base well 809b and the first

collector region 804b, second collector region 832b is greater than a forward junction voltage (Vj) of the PNP dual mode transistor 800b. In a particular embodiment, the N++ base contact may be biased to a voltage that is less than a negative forward junction voltage (e.g., -0.7 V) of the PNP dual mode transistor 800b. Biasing the N++ base contact may enable the PNP dual mode transistor 800b to operate according to a PNP BJT (e.g., generate a bipolar current including holes and electrons).

[0077] Referring to FIG. 9a, a particular illustrative embodiment of an NPN dual mode transistor 900a is shown. In a particular embodiment, the NPN dual mode transistor 900a may correspond to the dual mode transistor 100 of FIG. 1.

[0078] The NPN dual mode transistor 900a includes a first p- base region 907a and a second P- base region 908a. Each P- base region 907a, 908a may have a particular width (W). The first P- base region 907a and the second P- base region 908a may be coupled to (or include) a P- base well 909a. A P++ base contact 912a, 936a may also be coupled to the P- base regions 907a, 908a via the P- base well 909a. In a particular embodiment, the P++ base contact 912a, 936a may correspond to the first terminal 112 of FIG. 1. The NPN dual mode transistor 900a also includes an emitter region 906a, a first collector region 904a, and a second collector region 932a. The emitter region 906a, the first collector region 904a, and the second collector region 932a may each be doped with an N++ concentration. A first STI area 922a may prevent (or reduce) current leakage (from P++ base contact 936a). A second STI area 926a may prevent (or reduce) current leakage between the first collector region 904a and the P++ base contact 912a.

[0079] A first gate 901a may be coupled to the first P- base region 907a via a dielectric layer, and a second gate 902a may be coupled to the second P- base region 907a via a dielectric layer. A current gain of the NPN dual mode transistor 900a may be controlled by a gate voltage applied to the gates 901a, 902a. The NPN dual mode transistor 900a may also include a P- base well 910a and an N- base well 911a.

[0080] The NPN dual mode transistor 900a may operate in a digital MOS mode (e.g., a unipolar operation mode) and an analog gate control BJT mode (e.g., bipolar operation mode). For example, the gate voltages may be biased so that a gate-source-voltage enables formation of an inversion layer within the first and second N- base regions 907a and 908a. A unipolar current (e.g., electrons) may between the first and second collector region 932a, 904a and the emitter region 906a. The P++ base contact 912a and 936a may be biased such that an absolute value of a voltage difference between the P- base well 909a and the first and second collector regions 932a, 904a is greater than the junction voltage (V_j) of the NPN dual mode transistor 900a. Biasing the P++ base contact may enable the NPN dual mode transistor 900a to operate according to a NPN BJT (e.g., generate a bipolar current including holes and electrons).

[0081] Referring to FIG. 9b, a particular illustrative embodiment of an NPN dual mode transistor 900b is shown. In a particular embodiment, the NPN dual mode transistor 900b may correspond to the dual mode transistor 100 of FIG. 1.

[0082] The NPN dual mode transistor 900b includes a first p- base region 907b and a second P- base region 908b. Each P- base region 907b, 908b may have a particular width (W). The first P- base region 907b and the second P- base region 908b may be coupled to (or include) a P- base well 909b. A P++ base contact 912b and 936b may also be coupled to the P- base regions 907b, 908b via the P- base well 909b. In a particular embodiment, the P++ base contact 912b and 936b may correspond to the first terminal 112 of FIG. 1. The NPN dual mode transistor 900b also includes an emitter region 906b, a first collector region 904b, and a second collector region 932b. The emitter region 906b, the first collector region 904b, and the second collector region 932b may each be doped with an N++ concentration. A first STI area 922b may prevent (or reduce) current leakage (from P++ base contact 936b). A second STI area 926b may prevent (or reduce) current leakage between the first collector region 904b and the P++ base contact 912b.

[0083] A first gate 901b may be coupled to the first P- base region 907b via a dielectric layer, and a second gate 902b may be coupled to the second P- base region 907b via a dielectric layer. Isolate gates 903b, 905b may be coupled to the third and fourth N- base region 911b, 935b via a dielectric layer. The isolate gates 903b, 905b used to isolate N++ base contact from P++ collector. A current gain of the NPN dual mode transistor 900b may be controlled by a gate voltage applied to the gates 901b, 902b. The NPN dual mode transistor 900b may also include a P- base well 910b and an N- base well 911b.

[0084] The NPN dual mode transistor 900b may operate in a digital MOS mode (e.g., a unipolar operation mode) and an analog gate control BJT mode (e.g., bipolar operation mode). For example, the gate voltages may be biased so that a gate-source-voltage enables formation of an inversion layer within the first and second N- base regions 907b and 908b. A unipolar current (e.g., electrons) may between the first and second collector region 932b, 904b and the emitter region 906b. The P++ base contact 912b and 936b may be biased such that an absolute value of a voltage difference between the P- base well 909b and the first and second collector region 932b and 904b is greater than the junction voltage (V_j) of the NPN dual mode transistor 900b. Biasing the P++ base contact may enable the NPN dual mode transistor 900b to operate according to a NPN BJT (e.g., generate a bipolar current including holes and electrons).

[0085] Referring to FIG. 10a, a particular illustrative chart 1000-la depicting a change in drain current of a dual mode transistor based on biasing characteristics is shown. Values and results depicted in the chart 1000-la are provided for illustrative purposes and should not be construed as limiting. Values may vary based on external

conditions (e.g., temperature), gate widths of the dual mode transistor, gate lengths of the dual mode transistors, doping concentrations associated with the dual mode transistor, biasing voltages, etc.

[0086] The chart 1000-la illustrates operating results that correspond to an NPN-type configuration of the dual mode transistor 100 of FIG. 1. For example, the second voltage (V_2) applied to the first terminal 112 may correspond to the base voltage (V_B) depicted in the chart 1000. In addition, the first voltage (V_1) applied to the first gate region 102 of FIG. 1 may be approximately 1.5 V, as depicted in the chart 1000-la.

[0087] The chart 1000-la illustrates that a drain current (e.g., a collector current) may increase as the base voltage (V_B) increases for a particular drain voltage. As an illustrative example, the drain current may be approximately 540 uA/um when a 0.8 V signal is applied to the first terminal 112 and a 1.5 V signal is applied to the drain. However, when a 0.8 V signal is applied to the base and a 0.2 V signal is applied to the second terminal the drain current may be reduced to approximately 240 uA/um.

[0088] Thus, the drain current increases when both the unipolar operation (e.g., the FET operation) associated with unipolar current and the bipolar operation (e.g., the BJT operation) associated with the bipolar current are active as opposed to when only a single operation (e.g., unipolar or bipolar) is active. For example, when the base voltage (V_B) is 0.2 V (e.g., when the bipolar operation is inactive and the unipolar operation is active) the drain current is approximately 450 uA/um when a 1.5 voltage signal is applied to the drain. However, when the base voltage (V_B) is 1.2 V (e.g., when the bipolar operation and the unipolar operation are active), the drain current increases to approximately 650 uA/um when the 1.5 voltage signal is applied to the drain.

[0089] Another particular illustrative chart 1000-2a depicts the first gate region 102 controlling drain current at different the first terminal 112 (base) voltage of FIG.1. The base voltage between 0.6V~1.2V has higher NPN efficiency.

[0090] Referring to FIG. 10b, a particular illustrative chart 1000-lb depicting a change in current gain (beta) of a dual mode transistor based on biasing characteristics of the first gate region 102 and the first terminal 112 voltage of FIG.1 is shown. In an NPN activated region (e.g., where the first terminal voltage of FIG. 1 is 0.6V-1.2V), the current gain (beta) of the NPN is controlled by the first gate region voltage 102 and the first terminal region 112 voltage of FIG.1.

[0091] Another particular illustrative chart 1000-2b depicting a change in transconductance (gm) of a dual mode transistor based on biasing characteristics of the first gate region 102 and the first terminal 112 voltage of FIG.1 is shown. In an NPN activated region (e.g., where the first terminal voltage of FIG. 1 is 0.6V~1.2V), the transconductance (gm) of the NPN is controlled by the first gate region voltage 102 and the first terminal region 112 voltage of FIG.1.

[0092] Referring to FIG. 11, a particular illustrative embodiment of a silicon-on-insulator (SOI) PNP dual mode transistor 1100 is shown. In a particular embodiment, the SOI PNP dual mode transistor 1100 may correspond to the dual mode transistor 100 of FIG. 1. The SOI PNP dual mode transistor 1100 may include a similar configuration as the PNP dual mode transistor 800b of FIG. 8b; however, STIs 1122, 1126 may be extended through an Nwell base 1109 and may be coupled with an oxide substrate 1110. The oxide substrate 1110 may be different from the P- substrate 810b of FIG. 8b. For example, the SOI PNP dual mode transistor 1100 may have a PMOS/PNP silicon-on-insulator configuration and the PNP dual mode transistor 800b of FIG. 8b may have a PMOS/PNP bulk silicon configuration.

[0093] Referring to FIG. 12, a particular illustrative embodiment of a silicon-on-insulator (SOI) NPN dual mode transistor 1200 is shown. In a particular embodiment, the SOI NPN dual mode transistor 1200 may correspond to the dual mode transistor 100 of FIG. 1. The SOI NPN dual mode transistor 1200 may include a similar configuration as the NPN dual mode transistor 900b of FIG. 9b; however, STIs 1222, 1226 may be extended through a Pwell base 1209 and may be coupled with an oxide substrate 1210. The oxide substrate 1210 may be different from the P- base well 910b and the N- base well 911b. For example, the SOI NPN dual mode transistor 1200 may have a NMOS/NPN silicon-on-insulator configuration and the NPN dual mode transistor 900b of FIG. 9b may have a NMOS/NPN bulk silicon configuration.

[0094] Referring to FIG. 13 a flowchart of a particular embodiment of a method 1300 of biasing a dual mode transistor is shown. In an illustrative embodiment, the method 1300 may be performed with respect to the dual mode transistor 100 of FIG. 1, at least one of the embodiments 310-340 of the FET-type configurations of FIG. 3, at least one of the embodiments 410-440 of the BJT-type configurations of FIG. 4, at least one of the embodiments 510, 520 of the inverter mixer of FIG. 5, the differential mixer 600 of FIG. 6, at least one of the embodiments 710, 720 of the inverter driver of FIG. 7, the PNP dual mode transistors 800a, 800b of FIG. 8a and 8b, the NPN dual mode transistors 900a, 900b of FIG. 9a and 9b, the SOI PNP dual mode transistor 1100 of FIG. 11, the SOI NPN dual mode transistor 1200 of FIG. 12, or any combination thereof.

[0095] The method 1100 includes biasing a first gate voltage to enable unipolar current to flow from a first region of a transistor to a second region of the transistor according to a FET-type operation, at 1302. For example, in FIG. 1, the first gate voltage of the first gate region 102 may be biased to a first voltage (V_1). Biasing the first gate voltage may enable unipolar current to flow from the first region 104 to the second region 106 according to a FET-type operation. For example, the source voltage (V_s) may be applied to the first region 104. In a PNP configuration, the first gate region 102 may be biased such that the first voltage (V_1) is lower than the source voltage (V_s). For

example, the supply voltage (V_{dd}) may be applied to the first region 104 (e.g., the source), and the first voltage (V_1) may range from ground (e.g., zero volts) to the supply voltage (V_{dd}) such that the gate voltage is lower than the source voltage (V_s). Biasing the first gate region 102 with the first voltage (V_1) may enable channel formation (e.g., formation of an inversion layer) within the first body region 108 between the first region 104 and the second region 106. The unipolar current (e.g., holes) according to a PFET operation may flow from the first region 104 to the second region 106.

[0096] In an NPN configuration, the first gate region 102 may be biased such that the first voltage (V_1) is greater than a source voltage. For example, a ground voltage (e.g., zero volts) may be applied to the second region 106 (e.g., the source), and the first voltage (V_1) may range from ground to the supply voltage (V_{dd}) such that the first voltage (V_1) is greater than the source voltage. Biasing the first gate region 102 with the first voltage (V_1) may enable channel formation (e.g., formation of an inversion layer) within the first body region 108 between the first region 104 and the second region 106. The unipolar current (e.g., electrons) according to an NFET operation may flow from the first region 104 to the second region 106.

[0097] A body terminal may be biased to enable bipolar current to flow from the first region to the second region according to a BJT-type operation, at 1304. For example, in FIG. 1, the first terminal 112 (coupled to the first body region 108) may be biased to the second voltage (V_2). The first terminal 112 may be biased such that an absolute value of a body-to-source voltage (e.g., a voltage difference between the second voltage (V_2) and the source voltage (V_s)) is greater than a junction voltage (Vj) of the dual mode transistor 100. Biasing the first terminal 112 may enable bipolar current to flow between the first region 104 and the second region 106 concurrently with the unipolar current. In the PNP configuration, the second voltage (V_2) applied to the first terminal 112 (coupled to the first body region 108) may be biased to a voltage that is less than a negative forward junction voltage (e.g., -0.7 V) of the dual mode transistor 100. In the NPN configuration, the second voltage (V_2) applied to the first terminal 112 (coupled to the first body region 108) may be biased to a voltage that is greater than a forward junction voltage (e.g., 0.7 V) of the dual mode transistor 100. Thus, a bipolar current (including electrons and holes) according to a BJT-type operation may flow between the first region 104 and the second region 106 in response to biasing the first terminal 112 to the second voltage (V_2).

[0098] The method 1300 of FIG. 13 may enable a concurrent digital MOS operation mode (e.g., a unipolar operation mode corresponding to a unipolar current) and an analog gate control BJT operation mode (e.g., bipolar operation mode corresponding to a bipolar current). Thus, increased current, based on the unipolar and bipolar operation currents, may flow through the dual mode transistor 100 without increasing a supply voltage (V_{dd}) applied to the dual mode transistor 100. Increasing the current without increasing the supply voltage (V_{dd}) may yield increased operation efficiency. The dual mode transistor enables the gate control BJT operation and provides high performance BJT transistor in logic CMOS process.

[0099] Referring to FIG. 14, a block diagram of a wireless device 1400 including a component that is operable to bias a dual mode transistor is shown. The device 1400 includes a processor 1410, such as a digital signal processor (DSP), coupled to a memory 1432.

[0100] FIG. 14 also shows a display controller 1426 that is coupled to the processor 1410 and to a display 1428. A coder/decoder (CODEC) 1434 can also be coupled to the processor 1410. A speaker 1436 and a microphone 1438 can be coupled to the CODEC 1434. FIG. 14 also indicates that a wireless controller 1440 can be coupled to the processor 1410 and to an antenna 1442 via a radio-frequency (RF) interface 1490 disposed between the wireless controller 1440 and the antenna 1442. The RF interface 1490 may include a dual mode transistor device 1460 (or a component that includes one or more dual mode transistor devices). The dual mode transistor device 1460 may include, or correspond to, the dual mode transistor 100 of FIG. 1, at least one of the embodiments 310-340 of the FET-type configurations of FIG. 3, at least one of the embodiments 410-440 of the BJT-type configurations of FIG. 4, at least one of the embodiments 510, 520 of the inverter mixer of FIG. 5, the differential mixer 600 of FIG. 6, at least one of the embodiments 710, 720 of the inverter driver of FIG. 7, the PNP dual mode transistors 800a, 800b of FIG. 8a and 8b, the NPN dual mode transistors 900a, 900b of FIG. 9a and 9b, the SOI PNP dual mode transistor 1100 of FIG. 11, the SOI NPN dual mode transistor 1200 of FIG. 12, or any combination thereof.

[0101] A controller 1402 may also be coupled to the processor 1410 and to a dual mode transistor device 1450 (or a component that includes one or more dual mode transistor devices). The dual mode transistor device 1450 may include, or correspond to, the dual mode transistor 100 of FIG. 1, at least one of the embodiments 310-340 of the FET-type configurations of FIG. 3, at least one of the embodiments 410-440 of the BJT-type configurations of FIG. 4, at least one of the embodiments 510, 520 of the inverter mixer of FIG. 5, the differential mixer 600 of FIG. 6, at least one of the embodiments 710, 720 of the inverter driver of FIG. 7, the PNP dual mode transistor 800a, 800b of FIG. 8a and 8b, the NPN dual mode transistor 900a, 900b of FIG. 9a and 9b, the SOI PNP dual mode transistor 1100 of FIG. 11, the SOI NPN dual mode transistor 1200 of FIG. 12, or any combination thereof. In a particular embodiment, the controller 1402 may be a hardware controller, a firmware, or a combination thereof.

[0102] The memory 1432 may be a tangible non-transitory processor-readable storage medium that includes

executable instructions 1456. The instructions 1456 may be executed by a processor, such as the controller 1402, to perform the method 1300 of FIG. 13. For example, the instructions 1456 may be executable by the controller 1402 to bias the gate of the dual mode transistor device 1450 and/or the dual mode transistor device 1460. The instructions 1456 may also be executable by the controller 1402 to bias the terminal coupled to a body region of the dual mode transistor device 1450 and/or the dual mode transistor device 1460. The instructions 1456 may also be executable by an alternative processor (not shown) coupled to the processor 1410.

[0103] In a particular embodiment, the processor 1410, the display controller 1426, the memory 1432, the CODEC 1434, and the wireless controller 1440 are included in a system-in-package or system-on-chip device 1422. In a particular embodiment, an input device 1430 and a power supply 1444 are coupled to the system-on-chip device 1422. Moreover, in a particular embodiment, as illustrated in FIG. 14, the display 1428, the input device 1430, the speaker 1436, the microphone 1438, the antenna 1442, and the power supply 1444 are external to the system-on-chip device 1422. However, each of the display 1428, the input device 1430, the speaker 1436, the microphone 1438, the antenna 1442, and the power supply 1444 can be coupled to a component of the system-on-chip device 1422, such as an interface or a controller.

[0104] In conjunction with the described embodiments, an apparatus includes means for biasing a first gate voltage to enable unipolar current to flow from a first region of a transistor to a second region of the transistor according to a FET-type operation. For example, the means for biasing the first gate voltage may include the controller 1402 operable to execute the instructions 1462 of FIG. 14, one or more other devices, circuits, modules, or any combination thereof.

[0105] The apparatus may also include means for biasing a body terminal to enable bipolar current to flow from the first region to the second region according to a BJT-type operation. The unipolar current may flow concurrently with the bipolar current. For example, the means for biasing the body terminal may include the controller 1402 operable to execute the instructions 1462 of FIG. 14, one or more other devices, circuits, modules, or any combination thereof.

[0106] The foregoing disclosed devices and functionalities may be designed and configured into computer files (e.g. RTL, GDSII, GERBER, etc.) stored on computer readable media. Some or all such files may be provided to fabrication handlers who fabricate devices based on such files. Resulting products include semiconductor wafers that are then cut into semiconductor die and packaged into a semiconductor chip. The chips are then employed in devices described above. FIG. 13 depicts a particular illustrative embodiment of an electronic device manufacturing process 1300.

[0107] Physical device information 1302 is received at the manufacturing process 1300, such as at a research computer 1306. The physical device information 1302 may include design information representing at least one physical property of a semiconductor device, such as a device that includes the dual mode transistor 100 of FIG. 1, at least one of the embodiments 310-340 of the FET-type configurations of FIG. 3, at least one of the embodiments 410-440 of the BJT-type configurations of FIG. 4, at least one of the embodiments 510, 520 of the inverter mixer of FIG. 5, the differential mixer 600 of FIG. 6, at least one of the embodiments 710, 720 of the inverter driver of FIG. 7, the PNP dual mode transistor 800a, 800b of FIG. 8a and 8b, the NPN dual mode transistor 900a, 900b of FIG. 9a and 9b, the SOI PNP dual mode transistor 1100 of FIG. 11, the SOI NPN dual mode transistor 1200 of FIG. 12, the dual mode transistor device 1450 of FIG. 14, the dual mode transistor device 1460 of FIG. 14, or any combination thereof. For example, the physical device information 1502 may include physical parameters, material characteristics, and structure information that is entered via a user interface 1504 coupled to the research computer 1506. The research computer 1506 includes a processor 1508, such as one or more processing cores, coupled to a computer readable medium such as a memory 1510. The memory 1510 may store computer readable instructions that are executable to cause the processor 1508 to transform the physical device information 1502 to comply with a file format and to generate a library file 1512.

[0108] In a particular embodiment, the library file 1512 includes at least one data file including the transformed design information. For example, the library file 1512 may include a library of semiconductor devices including the dual mode transistor 100 of FIG. 1, at least one of the embodiments 310-340 of the FET-type configurations of FIG. 3, at least one of the embodiments 410-440 of the BJT-type configurations of FIG. 4, at least one of the embodiments 510, 520 of the inverter mixer of FIG. 5, the differential mixer 600 of FIG. 6, at least one of the embodiments 710, 720 of the inverter driver of FIG. 7, the PNP dual mode transistor 800a, 800b of FIG. 8a and 8b, the NPN dual mode transistor 900a, 900b of FIG. 9a and 9b, the SOI PNP dual mode transistor 1100 of FIG. 11, the SOI NPN dual mode transistor 1200 of FIG. 12, the dual mode transistor device 1450 of FIG. 14, the dual mode transistor device 1460 of FIG. 14, or any combination thereof, that is provided for use with an electronic design automation (EDA) tool 1520.

[0109] The library file 1512 may be used in conjunction with the EDA tool 1520 at a design computer 1514 including a processor 1516, such as one or more processing cores, coupled to a memory 1518. The EDA tool 1520 may be stored as processor executable instructions at the memory 1518 to enable a user of the design computer 1514 to design a device that includes the dual mode transistor 100 of FIG. 1, at least one of the embodiments 310-340 of the FET-type configurations of FIG. 3, at least one of the embodiments 410-440 of the BJT-type con-

figurations of FIG. 4, at least one of the embodiments 510, 520 of the inverter mixer of FIG. 5, the differential mixer 600 of FIG. 6, at least one of the embodiments 710, 720 of the inverter driver of FIG. 7, the PNP dual mode transistor 800 of FIG. 8, the NPN dual mode transistor 900 of FIG. 9, the dual mode transistor device 1250 of FIG. 12, the dual mode transistor device 1260 of FIG. 12, or any combination thereof. To illustrate, the circuit design property may include identification of particular circuits and relationships to other elements in a circuit design, positioning information, feature size information, interconnection information, or other information representing a physical property of a semiconductor device.

[0110] The design computer 1514 may be configured to transform the design information, including the circuit design information 1522, to comply with a file format. To illustrate, the file formation may include a database binary file format representing planar geometric shapes, text labels, and other information about a circuit layout in a hierarchical format, such as a Graphic Data System (GDSII) file format. The design computer 1514 may be configured to generate a data file including the transformed design information, such as a GDSII file 1526 that includes information describing a device that includes the dual mode transistor 100 of FIG. 1, at least one of the embodiments 310-340 of the FET-type configurations of FIG. 3, at least one of the embodiments 410-440 of the BJT-type configurations of FIG. 4, at least one of the embodiments 510, 520 of the inverter mixer of FIG. 5, the differential mixer 600 of FIG. 6, at least one of the embodiments 710, 720 of the inverter driver of FIG. 7, the PNP dual mode transistor 800a, 800b of FIG. 8a and 8b, the NPN dual mode transistor 900a, 900b of FIG. 9a and 9b, the SOI PNP dual mode transistor 1100 of FIG. 11, the SOI NPN dual mode transistor 1200 of FIG. 12, the dual mode transistor device 1450 of FIG. 14, the dual mode transistor device 1460 of FIG. 14, or any combination thereof, and that also includes additional electronic circuits and components within the SOC.

[0111] The GDSII file 1526 may be received at a fabrication process 1528 to manufacture a semiconductor device that includes the dual mode transistor 100 of FIG. 1, at least one of the embodiments 310-340 of the FET-type configurations of FIG. 3, at least one of the embodiments 410-440 of the BJT-type configurations of FIG. 4, at least one of the embodiments 510, 520 of the inverter mixer of FIG. 5, the differential mixer 600 of FIG. 6, at least one of the embodiments 710, 720 of the inverter driver of FIG. 7, the PNP dual mode transistor 800 of FIG. 8, the NPN dual mode transistor 900 of FIG. 9, the dual mode transistor device 1250 of FIG. 12, the dual mode transistor device 1260 of FIG. 12, or any combination thereof, according to transformed information in the GDSII file 1526. For example, a device manufacture process may include providing the GDSII file 1526 to a mask manufacturer 1530 to create one or more masks, such as masks to be used with photolithography processing, illustrated as a representative mask 1532. The mask 1532 may be used during the fabrication process to generate one or more wafers 1534, which may be tested and separated into dies, such as a representative die 1536. The die 1536 includes a circuit including the dual mode transistor 100 of FIG. 1, at least one of the embodiments 310-340 of the FET-type configurations of FIG. 3, at least one of the embodiments 410-440 of the BJT-type configurations of FIG. 4, at least one of the embodiments 510, 520 of the inverter mixer of FIG. 5, the differential mixer 600 of FIG. 6, at least one of the embodiments 710, 720 of the inverter driver of FIG. 7, the PNP dual mode transistor 800a, 800b of FIG. 8a and 8b, the NPN dual mode transistor 900a, 900b of FIG. 9a and 9b, the SOI PNP dual mode transistor 1100 of FIG. 11, the SOI NPN dual mode transistor 1200 of FIG. 12, the dual mode transistor device 1450 of FIG. 14, the dual mode transistor device 1460 of FIG. 14, or any combination thereof, or any combination thereof.

[0112] In a particular embodiment, the fabrication process 1428 may be initiated by or controlled by a processor 1434. The processor 1434 may access a memory 1435 that includes executable instructions 1437, such as computer-readable instructions or processor-readable instructions. The executable instructions may include one or more instructions that are executable by a computer, such as the processor 1434. The fabrication process 1428 may be implemented by a fabrication system that is fully automated or partially automated. For example, the fabrication process 1428 may be automated and may perform processing steps according to a schedule. The fabrication system may include fabrication equipment (e.g., processing tools) to perform one or more operations to form an electronic device.

[0113] The fabrication system may have a distributed architecture (e.g., a hierarchy). For example, the fabrication system may include one or more processors, such as the processor 1434, one or more memories, such as the memory 1435, and/or controllers that are distributed according to the distributed architecture. The distributed architecture may include a high-level processor that controls and/or initiates operations of one or more low-level systems. For example, a high-level portion of the fabrication process 1428 may include one or more processors, such as the processor 1434, and the low-level systems may each include or may be controlled by one or more corresponding controllers. A particular controller of a particular low-level system may receive one or more instructions (e.g., commands) from a high-level system, may issue sub-commands to subordinate modules or process tools, and may communicate status data back to the high-level system. Each of the one or more low-level systems may be associated with one or more corresponding pieces of fabrication equipment (e.g., processing tools). In a particular embodiment, the fabrication system may include multiple processors that are distributed in the fabrication system. For example, a controller of a low-level system component of the fabrication system may include a processor, such as the processor

1434.

[0114] Alternatively, the processor 1434 may be a part of a high-level system, subsystem, or component of the fabrication system. In another embodiment, the processor 1434 includes distributed processing at various levels and components of a fabrication system.

[0115] The die 1536 may be provided to a packaging process 1538 where the die 1536 is incorporated into a representative package 1540. For example, the package 1540 may include the single die 1536 or multiple dies, such as a system-in-package (SiP) arrangement. The package 1540 may be configured to conform to one or more standards or specifications, such as Joint Electron Device Engineering Council (JEDEC) standards.

[0116] Information regarding the package 1540 may be distributed to various product designers, such as via a component library stored at a computer 1546. The computer 1546 may include a processor 1548, such as one or more processing cores, coupled to a memory 1550. A printed circuit board (PCB) tool may be stored as processor executable instructions at the memory 1550 to process PCB design information 1542 received from a user of the computer 1546 via a user interface 1544. The PCB design information 1542 may include physical positioning information of a packaged semiconductor device on a circuit board, the packaged semiconductor device corresponding to the package 1540 including the a device that includes the dual mode transistor 100 of FIG. 1, at least one of the embodiments 310-340 of the FET-type configurations of FIG. 3, at least one of the embodiments 410-440 of the BJT-type configurations of FIG. 4, at least one of the embodiments 510, 520 of the inverter mixer of FIG. 5, the differential mixer 600 of FIG. 6, at least one of the embodiments 710, 720 of the inverter driver of FIG. 7, the PNP dual mode transistor 800a, 800b of FIG. 8a and 8b, the NPN dual mode transistor 900a, 900b of FIG. 9a and 9b, the SOI PNP dual mode transistor 1100 of FIG. 11, the SOI NPN dual mode transistor 1200 of FIG. 12, the dual mode transistor device 1450 of FIG. 14, the dual mode transistor device 1460 of FIG. 14, or any combination thereof.

[0117] The computer 1546 may be configured to transform the PCB design information 1542 to generate a data file, such as a GERBER file 1552 with data that includes physical positioning information of a packaged semiconductor device on a circuit board, as well as layout of electrical connections such as traces and vias, where the packaged semiconductor device corresponds to the package 1540 including the dual mode transistor 100 of FIG. 1, at least one of the embodiments 310-340 of the FET-type configurations of FIG. 3, at least one of the embodiments 410-440 of the BJT-type configurations of FIG. 4, at least one of the embodiments 510, 520 of the inverter mixer of FIG. 5, the differential mixer 600 of FIG. 6, at least one of the embodiments 710, 720 of the inverter driver of FIG. 7, the PNP dual mode transistor 800a, 800b of FIG. 8a and 8b, the NPN dual mode transistor 900a, 900b of FIG. 9a and 9b, the SOI PNP dual mode transistor 1100 of FIG. 11, the SOI NPN dual mode transistor 1200 of FIG. 12, the dual mode transistor device 1450 of FIG. 14, the dual mode transistor device 1460 of FIG. 14, or any combination thereof. In other embodiments, the data file generated by the transformed PCB design information may have a format other than a GERBER format.

[0118] The GERBER file 1552 may be received at a board assembly process 1554 and used to create PCBs, such as a representative PCB 1556, manufactured in accordance with the design information stored within the GERBER file 1552. For example, the GERBER file 1552 may be uploaded to one or more machines to perform various steps of a PCB production process. The PCB 1556 may be populated with electronic components including the package 1540 to form a representative printed circuit assembly (PCA) 1558.

[0119] The PCA 1558 may be received at a product manufacture process 1560 and integrated into one or more electronic devices, such as a first representative electronic device 1562 and a second representative electronic device 1564. As an illustrative, non-limiting example, the first representative electronic device 1562, the second representative electronic device 1564, or both, may be selected from the group of a set top box, a music player, a video player, an entertainment unit, a navigation device, a communications device, a personal digital assistant (PDA), a fixed location data unit, and a computer, into which the dual mode transistor 100 of FIG. 1, at least one of the embodiments 310-340 of the FET-type configurations of FIG. 3, at least one of the embodiments 410-440 of the BJT-type configurations of FIG. 4, at least one of the embodiments 510, 520 of the inverter mixer of FIG. 5, the differential mixer 600 of FIG. 6, at least one of the embodiments 710, 720 of the inverter driver of FIG. 7, the PNP dual mode transistor 800a, 800b of FIG. 8a and 8b, the NPN dual mode transistor 900a, 900b of FIG. 9a and 9b, the SOI PNP dual mode transistor 1100 of FIG. 11, the SOI NPN dual mode transistor 1200 of FIG. 12, the dual mode transistor device 1450 of FIG. 14, the dual mode transistor device 1460 of FIG. 14, or any combination thereof is integrated. As another illustrative, non-limiting example, one or more of the electronic devices 1562 and 1564 may be remote units such as mobile phones, hand-held personal communication systems (PCS) units, portable data units such as personal data assistants, global positioning system (GPS) enabled devices, navigation devices, fixed location data units such as meter reading equipment, or any other device that stores or retrieves data or computer instructions, or any combination thereof. In addition to remote units according to teachings of the disclosure, embodiments of the disclosure may be suitably employed in any device which includes active integrated circuitry including memory and on-chip circuitry.

[0120] A device that includes the dual mode transistor 100 of FIG. 1, at least one of the embodiments 310-340 of the FET-type configurations of FIG. 3, at least one of the embodiments 410-440 of the BJT-type configurations

of FIG. 4, at least one of the embodiments 510, 520 of the inverter mixer of FIG. 5, the differential mixer 600 of FIG. 6, at least one of the embodiments 710, 720 of the inverter driver of FIG. 7, the PNP dual mode transistor 800a, 800b of FIG. 8a and 8b, the NPN dual mode transistor 900a, 900b of FIG. 9a and 9b, the SOI PNP dual mode transistor 1100 of FIG. 11, the SOI NPN dual mode transistor 1200 of FIG. 12, the dual mode transistor device 1450 of FIG. 14, the dual mode transistor device 1460 of FIG. 14, or any combination thereof, may be fabricated, processed, and incorporated into an electronic device, as described in the illustrative process 1500. One or more aspects of the embodiments disclosed with respect to FIGS. 1-15 may be included at various processing stages, such as within the library file 1512, the GDSII file 1526, and the GERBER file 1552, as well as stored at the memory 1510 of the research computer 1506, the memory 1518 of the design computer 1514, the memory 1550 of the computer 1546, the memory of one or more other computers or processors (not shown) used at the various stages, such as at the board assembly process 1554, and also incorporated into one or more other physical embodiments such as the mask 1532, the die 1536, the package 1540, the PCA 1558, other products such as prototype circuits or devices (not shown), or any combination thereof. Although various representative stages of production from a physical device design to a final product are depicted, in other embodiments fewer stages may be used or additional stages may be included. Similarly, the process 1500 may be performed by a single entity or by one or more entities performing various stages of the process 1500.

[0121] Those of skill would further appreciate that the various illustrative logical blocks, configurations, modules, circuits, and algorithm steps described in connection with the embodiments disclosed herein may be implemented as electronic hardware, computer software executed by a processor, or combinations of both. Various illustrative components, blocks, configurations, modules, circuits, and steps have been described above generally in terms of their functionality. Whether such functionality is implemented as hardware or processor executable instructions depends upon the particular application and design constraints imposed on the overall system. Skilled artisans may implement the described functionality in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the present disclosure.

[0122] The steps of a method or algorithm described in connection with the embodiments disclosed herein may be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module may reside in random access memory (RAM), flash memory, read-only memory (ROM), programmable read-only memory (PROM), erasable programmable read-only memory (EPROM), electrically erasable programmable read-only memory (EEPROM), registers, hard disk, a removable disk, a compact disc read-only memory (CD-ROM), or any other form of non-transient storage medium known in the art. An exemplary storage medium is coupled to the processor such that the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium may be integral to the processor. The processor and the storage medium may reside in an application-specific integrated circuit (ASIC). The ASIC may reside in a computing device or a user terminal. In the alternative, the processor and the storage medium may reside as discrete components in a computing device or user terminal.

[0123] The previous description of the disclosed embodiments is provided to enable a person skilled in the art to make or use the disclosed embodiments. Various modifications to these embodiments will be readily apparent to those skilled in the art, and the principles defined herein may be applied to other embodiments without departing from the scope of the disclosure. Thus, the present disclosure is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope possible consistent with the principles and novel features as defined by the following claims.

Claims

1. A method comprising:

   biasing a first gate voltage to enable unipolar current to flow from a first region (104) of a transistor (100) to a second region (106) of the transistor (100) according to a field-effect transistor, FET,-type operation; and
   biasing a body terminal (112) to enable bipolar current to flow from the first region (104) to the second region (106), wherein the bipolar current is tuned by a body terminal current according to a bipolar junction transistor, BJT,-type operation;
   characterised in that the unipolar current flows concurrently with the bipolar current.

2. The method of claim 1, wherein the unipolar current is associated with a digital metal oxide semiconductor, MOS, mode, and wherein the bipolar current is associated with an analog gate control bipolar junction transistor mode.

3. The method of claim 1, wherein the first gate voltage controls a current gain of the transistor (100), a transconductance of the transistor (100), and a resistance of the transistor (100).

4. The method of claim 1, wherein the transistor (100) is an n-type metal oxide semiconductor, NMOS, and NPN-type device; or

wherein the transistor (100) is a p-type metal oxide semiconductor, PMOS, and PNP-type device; or
wherein the transistor (100) is a bulk complementary metal oxide semiconductor, CMOS, and BJT device; or
wherein the transistor (100) is a silicon-on-insulator, SOI, complementary metal oxide semiconductor, CMOS, and BJT device; or
wherein the transistor (100) is a planar complementary metal oxide semiconductor, CMOS, and a BJT device; or
wherein the transistor (100) is a three dimensional fin-type FET, 3D Finfet, complementary metal oxide semiconductor, CMOS, and a BJT device.

5. The method of claim 1, wherein biasing the first gate voltage forms an inversion layer to enable unipolar current; or
wherein biasing the first gate voltage and biasing the body terminal (112) coupled to a body region (108) are initiated by a processor integrated into an electronic device.

6. The method of claim 1, wherein the first region (104) of the transistor (100) corresponds to a source of the transistor (100), and wherein the second region (106) of the transistor (100) corresponds to a drain of the transistor (100).

7. An apparatus comprising:

a first gate region (102) of a transistor (100) that is biased via a first gate voltage
to enable a unipolar current to flow from a first region (104) of the transistor (100) to a second region (106) of the transistor (100) according to a field-effect transistor, FET,-type operation; and
a first body region (108) of the transistor (100) that is biased via a first body voltage to enable bipolar current to flow from the first region (104) of the transistor (100) to the second region (106) of the transistor (100) according to a bipolar junction transistor, BJT,-type operation;
characterised in that the unipolar current flows concurrently with the bipolar current.

8. The apparatus of claim 7, wherein the first region (104) corresponds to a source of the transistor (100); or
wherein the second region (106) corresponds to a drain of the transistor (100).

9. The apparatus of claim 7, wherein the transistor (100) operates in a unipolar operation mode and a bipolar operation mode, wherein the transistor (100) is an n-type transistor, and wherein the first body voltage is greater than a forward junction voltage.

10. The apparatus of claim 9, wherein the first gate voltage is equal to a supply voltage.

11. The apparatus of claim 7, wherein the transistor (100) operates in a unipolar operation mode and a bipolar operation mode, wherein the transistor (100) is a p-type transistor, and wherein the first body voltage is less than a negative forward junction voltage.

12. The apparatus of claim 11, wherein the first gate voltage is equal to zero volts.

13. The apparatus of claim 7, further comprising:

an inverter mixer circuit (510), wherein the inverter mixer circuit (510) comprises:

the transistor (512), wherein the first body voltage corresponds to a first input signal (516); and
a second transistor (514), wherein a second body region of the second transistor (514) is coupled to the first body region, wherein the second body region is biased via the first body voltage, wherein a second gate region of the second transistor (514) is coupled to the first gate region, wherein the second gate region is biased via the first gate voltage, wherein the first gate voltage corresponds to a second input signal (518), and wherein a second drain region of the second transistor (514) is coupled to a first drain region of the transistor (512);
or the apparatus of claim 7 further comprising

an inverter mixer circuit (520), wherein the inverter mixer circuit (520) comprises:

the transistor (522), wherein the first body voltage corresponds to a first input signal (526); and
a second transistor (524), wherein a second body region of the second transistor (524) is biased via a second body voltage that corresponds to a second input signal (527), wherein a second gate region of the second transistor (524) is coupled to the first gate region, wherein the second gate region is biased via the first gate voltage, wherein the first gate voltage corresponds to a third input signal (528), and wherein a second drain region of the second transistor (524) is coupled to a first drain region of the transistor (522);
or the apparatus of claim 7 further comprising

a differential mixer circuit (600), wherein the differential mixer circuit (600) comprises:

the transistor (602), wherein the first gate voltage corresponds to a first signal of a first differential input signal, wherein the first body voltage corresponds to a second signal of a second differential input signal; and a second transistor (604), wherein a second gate region of the second transistor is biased via a second gate voltage, wherein the second gate voltage corresponds to a second signal of the first differential input signal, wherein a second body region of the second transistor (604) is biased via a first signal of the second differential input signal, and wherein a first source region of the transistor (602) is coupled to a second source region of the second transistor (604);
or the apparatus of claim 7 further comprising

an inverter driver circuit (710), wherein the inverter driver circuit (710) comprises:

the transistor (712), wherein the first gate voltage and the first body voltage correspond to a first input signal (716); and
a second transistor (714), wherein a second gate region of the second transistor (714) is coupled to the first gate region, wherein a second body region of the second transistor (714) is coupled to the first body region, wherein the second body region is biased via the first body voltage, and wherein a second drain region of the second transistor (714) is coupled to a first drain region of the transistor (712);
or the apparatus of claim 7 further comprising

an inverter driver circuit (720), wherein the inverter driver circuit (720) comprises:

the transistor (722), wherein the first body voltage corresponds to a first input signal (726), and wherein the first gate voltage correspond to a second input signal (727); and a second transistor (724), wherein a second gate region of the second transistor (724) is coupled to the first gate region, wherein the second gate region is biased via the first gate voltage, wherein a second body region of the second transistor (724) is biased via a third input signal (728), and wherein a second drain region of the second transistor (724) is coupled to a first drain region of the transistor (722).

14. A non-transitory computer readable medium comprising instructions that, when executed by a processor, cause the processor to:

bias a first gate voltage of a gate of a transistor (100) to enable a unipolar current to flow from a first region (104) of the transistor (100) to a second region (106) of the transistor (100); and
bias a terminal (112) coupled to a body region (108) of the transistor to a second voltage such that an absolute value of a body-to-source voltage is greater than a junction voltage of the transistor (100), wherein biasing the terminal (112) enables a bipolar current to flow from the first region (104) of the transistor (100) to the second region (106) of the transistor (100);
wherein the unipolar current flows concurrently with the bipolar current.

15. The non-transitory computer readable medium of claim 14, wherein the unipolar current is associated with a digital metal oxide semiconductor, MOS, mode, and wherein the bipolar current is associated with an analog gate control bipolar junction transistor mode.

Patentansprüche

1. Ein Verfahren, aufweisend:

Vorspannen einer ersten Gate-Spannung, um einen Fluss eines unipolaren Stroms von einem ersten Bereich (104) eines Transistors (100) zu einem zweiten Bereich (106) des Transistors (100) gemäß einem Feldeffekttransistor bzw. FET-Typ-Betrieb zu ermöglichen, und
Vorspannen eines Körperanschlusses (112), um einen Fluss eines bipolaren Stroms von dem ersten Bereich (104) zu dem zweiten Bereich (106) zu ermöglichen, wobei der bipolare Strom durch einen Körperanschlussstrom gemäß einem Bipolartransistor bzw. BJT-Typ-Betrieb eingestellt wird,
dadurch gekennzeichnet, dass der unipolare Strom gleichzeitig mit dem bipolaren Strom fließt.

2. Verfahren nach Anspruch 1, wobei der unipolare Strom mit einem digitalen Metalloxidhalbleiter bzw. MOS-Modus assoziiert ist und wobei der bipolare Strom mit einem analogen Gatesteuerungs-Bipolartransistor-Modus assoziiert ist.

3. Verfahren nach Anspruch 1, wobei die erste Gate-Spannung eine Stromverstärkung des Transistors (100), eine Transkonduktanz des Transistors (100) und einen Widerstand des Transistors (100) steuert.

4. Verfahren nach Anspruch 1, wobei der Transistor (100) ein n-Typ-Metalloxidhalbleiter bzw. NMOS und NPN-Typ-Bauelement ist, oder
wobei der Transistor (100) ein p-Typ-Metalloxidhalbleiter bzw. PMOS und PNP-Typ-Bauelement ist, oder
wobei der Transistor (100) ein Bulk-Complementary Metalloxidhalbleiter bzw. CMOS und BJT-Bauelement ist, oder
wobei der Transistor (100) ein Silicon-on-Insulator bzw. SOI Complementary Metalloxidhalbeiter bzw. CMOS und BJT-Bauelement ist, oder
wobei der Transistor (100) ein planares Complementary Metalloxidhalbleiter bzw. CMOS und BJT-Bauelement ist, oder
wobei der Transistor (100) ein dreidimensionales Rippen-Typ FET, 3D Finfet Complementary Metalloxidhalbleiter bzw. CMOS und BJT-Bauelement ist.

5. Verfahren nach Anspruch 1, wobei das Vorspannen der ersten Gate-Spannung eine Inversionsschicht für das Ermöglichen eines unipolaren Stroms bildet, oder
wobei das Vorspannen der ersten Gate-Spannung und das Vorspannen des mit einem Körperbereich (108) gekoppelten Körperanschlusses (112) durch einen in ein elektronisches Bauelement integrierten Prozessor eingeleitet werden.

6. Verfahren nach Anspruch 1, wobei der erste Bereich (104) des Transistors (100) einer Source des Transistors (100) entspricht und wobei der zweite Bereich (106) des Transistors (100) einem Drain des Transistors (100) entspricht.

7. Eine Vorrichtung, die aufweist:

einen ersten Gate-Bereich (102) eines Transistors (100), der über eine erste Gate-Spannung vorgespannt wird, um einen Fluss eines unipolaren Stroms von einem ersten Bereich (104) des Transistors (100) zu einem zweiten Bereich (106) des Transistors (100) gemäß einem Feldeffekttransistor bzw. FET-Typ-Betrieb zu ermöglichen, und
einen ersten Körperbereich (108) des Transistors (100), der über eine erste Körperspannung vorgespannt wird, um einen Strom eines bipolaren Stroms von dem ersten Bereich (104) zu dem zweiten Bereich (106) des Transistors (100) gemäß einem Bipolartransistor bzw. BJT-Typ-Betrieb zu ermöglichen,
dadurch gekennzeichnet, dass der unipolare Strom gleichzeitig mit dem bipolaren Strom fließt.

8. Vorrichtung nach Anspruch 7, wobei der erste Bereich (104) einer Source des Transistors (100) entspricht, oder
wobei der zweite Bereich (106) einem Drain des Transistors (100) entspricht.

9. Vorrichtung nach Anspruch 7, wobei der Transistor (100) in einem unipolaren Betriebsmodus und einem bipolaren Betriebsmodus betrieben wird, wobei der Transistor (100) ein n-Typ-Transistor ist und wobei die erste Körperspannung größer als eine Vorwärtsübergangsspannung ist.

10. Vorrichtung nach Anspruch 9, wobei die erste Gate-Spannung gleich einer Versorgungsspannung ist.

11. Vorrichtung nach Anspruch 7, wobei der Transistor (100) in einem unipolaren Betriebsmodus und einem bipolaren Betriebsmodus betrieben wird, wobei der Transistor (100) ein p-Typ-Transistor ist und wobei die erste Körperspannung kleiner als eine negative Vorwärtsübergangsspannung ist.

12. Vorrichtung nach Anspruch 11, wobei die erste Gate-Spannung gleich null Volt ist.

13. Vorrichtung nach Anspruch 7, die weiterhin aufweist:

eine Wechselrichter-Mischerschaltung (510), wobei die Wechselrichter-Mischerschaltung (510) aufweist:

den Transistor (512), wobei die erste Körperspannung einem ersten Eingangssignal (516) entspricht, und
einen zweiten Transistor (514), wobei ein zweiter Körperbereich des zweiten Transistors (514) mit dem ersten Körperbereich gekoppelt ist, wobei der zweite Körperbereich über die erste Körperspannung vorgespannt ist, wobei ein zweiter Gate-Bereich des zweiten Transistors (514) mit dem ersten Gate-Bereich gekoppelt ist, wobei der zweite Gate-Bereich über die erste Gate-Spannung vorgespannt ist, wobei die erste Gate-Spannung einem zweiten Eingangssignal (518) entspricht und wobei ein zweiter Drain-Bereich des zweiten Transistors (514) mit einem ersten Drain-Bereich des Transistors (512) gekoppelt ist,

oder wobei die Vorrichtung von Anspruch 7 weiterhin aufweist:

eine Wechselrichter-Mischerschaltung (520), wobei die Wechselrichter-Mischerschaltung (520) aufweist:

den Transistor (522), wobei die erste Körperspannung einem ersten Ein-

gangssignal (526) entspricht, und
einen zweiten Transistor (524), wobei ein zweiter Körperbereich des zweiten Transistors (524) über eine zweite Körperspannung vorgespannt ist, die einem zweiten Eingangssignal (527) entspricht, wobei ein zweiter Gate-Bereich des zweiten Transistors (524) mit dem ersten Gate-Bereich gekoppelt ist, wobei der zweite Gate-Bereich über die erste Gate-Spannung vorgespannt ist, wobei die erste Gate-Spannung einem dritten Eingangssignal (528) entspricht und wobei ein zweiter Drain-Bereich des zweiten Transistors (524) mit einem ersten Drain-Bereich des Transistors (522) gekoppelt ist,

oder wobei die Vorrichtung von Anspruch 7 weiterhin aufweist:
eine Differentialmischerschaltung (600), wobei die Differentialmischerschaltung (600) aufweist:

den Transistor (602), wobei die erste Gate-Spannung einem ersten Signal eines ersten Differential-Eingangssignals entspricht, wobei die erste Körperspannung einem zweiten Signal eines zweiten Differential-Eingangssignals entspricht, und
einen zweiten Transistor (604), wobei ein zweiter Gate-Bereich des zweiten Transistors über eine zweite Gate-Spannung vorgespannt ist, wobei die zweite Gate-Spannung einem zweiten Signal des ersten Differential-Eingangssignals entspricht, wobei ein zweiter Körperbereich des zweiten Transistors (604) über ein erstes Signal des zweiten Differential-Eingangssignals vorgespannt ist und wobei ein erster Source-Bereich des Transistors (602) mit einem zweiten Source-Bereich des zweiten Transistors (604) gekoppelt ist,

oder wobei die Vorrichtung von Anspruch 7 weiterhin aufweist:

eine Wechselrichter-Treiberschaltung (710), wobei die Wechselrichter-Treiberschaltung (710) aufweist:

den Transistor (712), wobei die erste Gate-Spannung und die erste Körperspannung einem ersten Eingangssignal (716) entsprechen, und
einen zweiten Transistor (714), wobei ein zweiter Gate-Bereich des zweiten Transistors (714) mit dem ersten Gate-Bereich gekoppelt ist, wobei ein zweiter Körperbereich des zweiten Transistors (714) mit dem ersten Körperbereich gekoppelt ist, wobei der zweite Körperbereich über die erste Körperspannung vorgespannt ist, und wobei ein zweiter Drain-Bereich des zweiten Transistors (714) mit einem ersten Drain-Bereich des Transistors (712) gekoppelt ist,

oder wobei die Vorrichtung von Anspruch 7 weiterhin aufweist:

eine Wechselrichter-Treiberschaltung (720), wobei die Wechselrichter-Treiberschaltung (720) aufweist:

den Transistor (722), wobei die erste Körperspannung einem ersten Eingangssignal (726) entspricht und wobei die erste Gate-Spannung einem zweiten Eingangssignal (727) entspricht, und
einen zweiten Transistor (724), wobei ein zweiter Gate-Bereich des zweiten Transistors (724) mit dem ersten Gate-Bereich gekoppelt ist, wobei der zweite Gate-Bereich über die erste Gate-Spannung vorgespannt ist, wobei ein zweiter Körperbereich des zweiten Transistors (724) über ein drittes Eingangssignal (728) vorgespannt ist und wobei ein zweiter Drain-Bereich des zweiten Transistors (724) mit einem ersten Drain-Bereich des Transistors (722) gekoppelt ist.

14. Ein nicht-transitorisches, computerlesbares Medium, das Befehle aufweist, die bei einer Ausführung durch einen Prozessor den Prozessor veranlassen zum:

Vorspannen einer erste Gate-Spannung eines Gates eines Transistors (100), um einen Fluss eines unipolaren Stroms von einem ersten Bereich (104) des Transistors (100) zu einem zweiten Bereich (106) des Transistors (100) zu ermöglichen, und
Vorspannen eines mit einem Körperbereich (108) des Transistors gekoppelten Anschlusses (112) zu einer zweiten Spannung, sodass der absolute Wert einer Körper-zu-Source-Spannung größer als eine Übergangsspannung des Transistors (100) ist, wobei das Vorspannen des Anschlusses (112) einen Fluss eines bipolaren Stroms von dem ersten Bereich (104) des Transistors (100) zu dem zweiten Bereich (106) des Transistors (100) ermöglicht,
wobei der unipolare Strom gleichzeitig mit dem

bipolaren Strom fließt.

15. Nicht-transitorisches computerlesbares Medium nach Anspruch 14, wobei der unipolare Strom mit einem digitalen Metalloxidhalbleiter bzw. MOS-Modus assoziiert ist und wobei der bipolare Strom mit einem analogen Gatesteuerungs-Bipolartransistor-Modus assoziiert ist.

Revendications

1. Un procédé comprenant :

la polarisation d'une première tension de grille pour permettre à un courant unipolaire de s'écouler d'une première zone (104) d'un transistor (100) vers une deuxième zone (106) du transistor (100) en fonction d'un fonctionnement de type transistor à effet de champ, FET, et
la polarisation d'une borne de corps (112) pour permettre à un courant bipolaire de s'écouler de la première zone (104) vers la deuxième zone (106), où le courant bipolaire est accordé par un courant de borne de corps en fonction d'un fonctionnement de type transistor à jonctions bipolaires,
caractérisé en ce que le courant unipolaire s'écoule conjointement avec le courant bipolaire.

2. Le procédé selon la Revendication 1, où le courant unipolaire est associé à un mode à semiconducteur à oxyde métallique numérique, MOS, et où le courant bipolaire est associé à un mode à transistor à jonctions bipolaires de commande de grille analogique.

3. Le procédé selon la Revendication 1, où la première tension de grille commande un gain de courant du transistor (100), une transconductance du transistor (100) et une résistance du transistor (100).

4. Le procédé selon la Revendication 1, où le transistor (100) est un dispositif de type NPN et à semiconducteur d'oxyde métallique de type n, NMOS, ou
où le transistor (100) est un dispositif de type PNP et à semiconducteur d'oxyde métallique de type p, PMOS, ou
où le transistor (100) est un dispositif BJT et à semiconducteur d'oxyde métallique complémentaire, CMOS, en vrac, ou
où le transistor (100) est un dispositif BJT et à semiconducteur d'oxyde métallique complémentaire, CMOS, à silicium sur isolant, SOI, ou
où le transistor (100) est un dispositif BJT et à semiconducteur d'oxyde métallique complémentaire, CMOS, planaire, ou
où le transistor (100) est un dispositif BJT et à semiconducteur d'oxyde métallique complémentaire, CMOS, à FET de type à ailettes en trois dimensions, 3D Finfet.

5. Le procédé selon la Revendication 1, où la polarisation de la première tension de grille forme une couche d'inversion destinée à l'activation d'un courant unipolaire, ou
où la polarisation de la première tension de grille et la polarisation de la borne de corps (112) couplée à une zone de corps (108) sont lancées par un processeur intégré à un dispositif électronique.

6. Le procédé selon la Revendication 1, où la première zone (104) du transistor (100) correspond à une source du transistor (100), et où la deuxième zone (106) du transistor (100) correspond à un drain du transistor (100).

7. Un appareil comprenant :

une première zone de grille (102) d'un transistor (100) qui est polarisée par l'intermédiaire d'une première tension de grille pour permettre à un courant unipolaire de s'écouler d'une première zone (104) du transistor (100) vers une deuxième zone (106) du transistor (100) en fonction d'un fonctionnement de type transistor à effet de champ, FET, et
une première zone de corps (108) du transistor (100) qui est polarisée par l'intermédiaire d'une première tension de corps pour permettre à un courant bipolaire de s'écouler de la première zone (104) du transistor (100) vers la deuxième zone (106) du transistor (100) en fonction d'un fonctionnement de type transistor à jonctions bipolaires, BJT,
caractérisé en ce que le courant unipolaire s'écoule conjointement avec le courant bipolaire.

8. L'appareil selon la Revendication 7, où la première zone (104) correspond à une source du transistor (100), ou
où la deuxième zone (106) correspond à un drain du transistor (100).

9. L'appareil selon la Revendication 7, où le transistor (100) fonctionne dans un mode de fonctionnement unipolaire et un mode de fonctionnement bipolaire, où le transistor (100) est un transistor de type n et où la première tension de corps est supérieure à une tension de jonction directe.

10. L'appareil selon la Revendication 9, où la première tension de grille est égale à une tension d'alimentation.

11. L'appareil selon la Revendication 7, où le transistor (100) fonctionne dans un mode de fonctionnement unipolaire et un mode de fonctionnement bipolaire, où le transistor (100) est un transistor de type p et où la première tension de corps est inférieure à une tension de jonction directe négative.

12. L'appareil selon la Revendication 11, où la première tension de grille est égale à zéro volt.

13. L'appareil selon la Revendication 7, comprenant en outre :

un circuit mélangeur inverseur (510), où le circuit mélangeur inverseur (510) comprend :

le transistor (512), où la première tension de corps correspond à un premier signal en entrée (516), et
un deuxième transistor (514), où une deuxième zone de corps du deuxième transistor (514) est couplée à la première zone de corps, où la deuxième zone de corps est polarisée par l'intermédiaire de la première tension de corps, où une deuxième zone de grille du deuxième transistor (514) est couplée à la première zone de grille, où la deuxième zone de grille est polarisée par l'intermédiaire de la première tension de grille, où la première tension de grille correspond à un deuxième signal en entrée (518) et où une deuxième zone de drain du deuxième transistor (514) est couplée à une première zone de drain du transistor (512),

ou l'appareil selon la Revendication 7 comprenant en outre
un circuit mélangeur inverseur (520), où le circuit mélangeur inverseur (520) comprend :

le transistor (522), où la première tension de corps correspond à un premier signal en entrée (526), et
un deuxième transistor (524), où une deuxième zone de corps du deuxième transistor (524) est polarisée par l'intermédiaire d'une deuxième tension de corps qui correspond à un deuxième signal en entrée (527), où une deuxième zone de grille du deuxième transistor (524) est couplée à la première zone de grille, où la deuxième zone de grille est polarisée par l'intermédiaire de la première tension de grille, où la première tension de grille correspond à un troisième signal en entrée (528) et où une deuxième zone de drain du deuxième transistor (524) est couplée à une première zone de drain du transistor (522),

ou l'appareil selon la Revendication 7 comprenant en outre
un circuit mélangeur différentiel (600), où le circuit mélangeur différentiel (600) comprend :

le transistor (602), où la première tension de grille correspond à un premier signal d'un premier signal en entrée différentiel, où la première tension de corps correspond à un deuxième signal d'un deuxième signal en entrée différentiel, et
un deuxième transistor (604), où une deuxième zone de grille du deuxième transistor est polarisée par l'intermédiaire d'une deuxième tension de grille, où la deuxième tension de grille correspond à un deuxième signal du premier signal en entrée différentiel, où une deuxième zone de corps du deuxième transistor (604) est polarisée par l'intermédiaire d'un premier signal du deuxième signal en entrée différentiel, et où une première zone source du transistor (602) est couplée à une deuxième zone source du deuxième transistor (604),

ou l'appareil selon la Revendication 7 comprenant en outre
un circuit d'attaque inverseur (710), où le circuit d'attaque inverseur (710) comprend :

le transistor (712), où la première tension de grille et la première tension de corps correspondent à un premier signal en entrée (716), et
un deuxième transistor (714), où une deuxième zone de grille du deuxième transistor (714) est couplée à la première zone de grille, où une deuxième zone de corps du deuxième transistor (714) est couplée à la première zone de corps, où la deuxième zone de corps est polarisée par l'intermédiaire de la première tension de corps et où une deuxième zone de drain du deuxième transistor (714) est couplée à une première zone de drain du transistor (712),

ou l'appareil selon la Revendication 7 comprenant en outre
un circuit d'attaque inverseur (720), où le circuit d'attaque inverseur (720) comprend :

le transistor (722), où la première tension de corps correspond à un premier signal en entrée (726) et où la première tension de grille correspond à un deuxième signal en entrée (727), et
un deuxième transistor (724), où une deuxième zone de grille du deuxième tran-

sistor (724) est couplée à la première zone de grille, où la deuxième zone de grille est polarisée par l'intermédiaire de la première tension de grille, où une deuxième zone de corps du deuxième transistor (724) est polarisée par l'intermédiaire d'un troisième signal en entrée (728) et où une deuxième zone de drain du deuxième transistor (724) est couplée à une première zone de drain du transistor (722).

14. Un support lisible par ordinateur non transitoire contenant des instructions qui, lorsqu'elles sont exécutées par un processeur, amènent le processeur à :

polariser une première tension de grille d'une grille d'un transistor (100) de façon à permettre à un courant unipolaire de s'écouler d'une première zone (104) du transistor (100) vers une deuxième zone (106) du transistor (100), et
polariser une borne (112) couplée à une zone de corps (108) du transistor à une deuxième tension de sorte qu'une valeur absolue d'une tension corps à source soit supérieure à une tension de jonction du transistor (100), où la polarisation de la borne (112) permet à un courant bipolaire de s'écouler de la première zone (104) du transistor (100) vers la deuxième zone (106) du transistor (100),
où le courant unipolaire s'écoule conjointement avec le courant bipolaire.

15. Le support lisible par ordinateur non transitoire selon la Revendication 14, où le courant unipolaire est associé à un mode à semiconducteur à oxyde métallique numérique, MOS, et où le courant bipolaire est associé à un mode à transistor à jonctions bipolaires de commande de grille analogique.

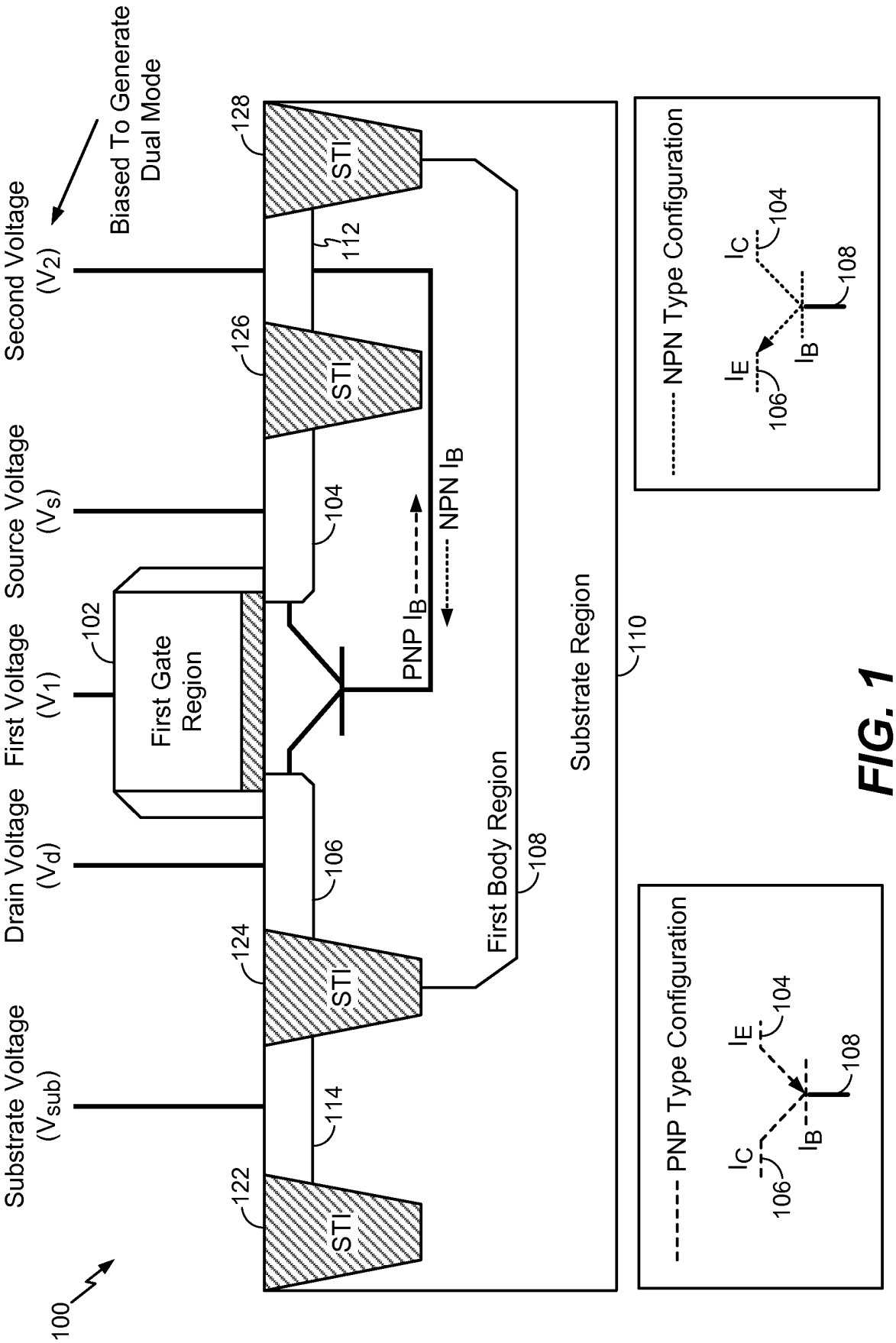

Biased To Generate Dual Mode
Second Voltage (V_2)
Source Voltage (V_s)
First Voltage (V_1)
Drain Voltage (V_d)
Substrate Voltage (V_{sub})
100
102
First Gate Region
104
106
108
First Body Region
110
Substrate Region
112
114
122
124
126
128
STI
PNP I_B
NPN I_B
NPN Type Configuration
I_C
I_E
I_B
PNP Type Configuration

FIG. 1

200

Gate Control PNP	
V_1	V_{GS}: 0 ~ V_{dd}
V_d	0
V_S	V_{dd}
V_2	$V_2 < -V_{forward\_pn}$
Operation	Bipolar + Unipolar

210

Gate Control NPN	
V_1	V_{GS}: V_{dd} ~ 0
V_d	V_{dd}
V_S	0
V_2	$V_2 > V_{forward\_pn}$
Operation	Bipolar + Unipolar

FIG. 2

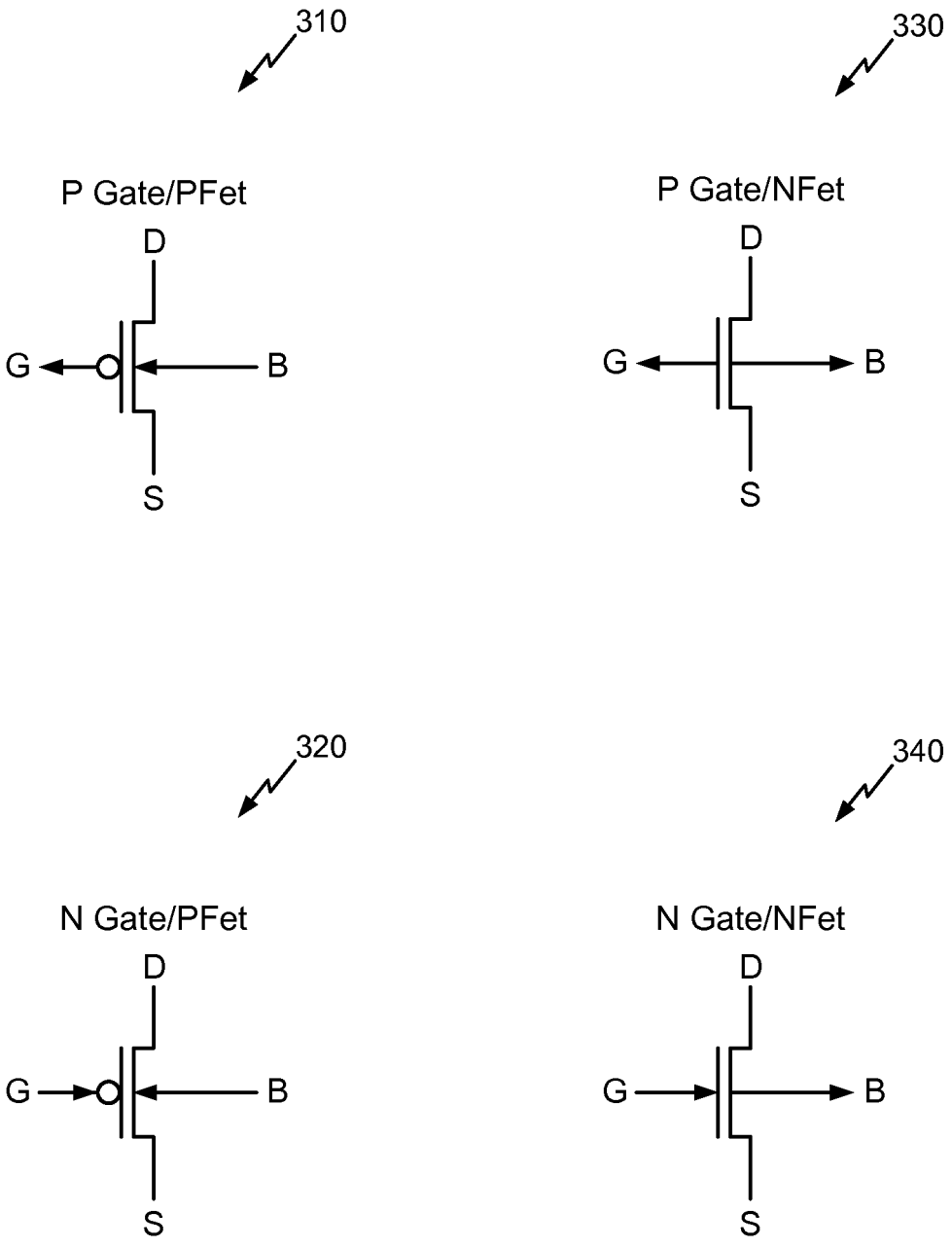

310
P Gate/PFet
D
G
B
S
330
P Gate/NFet
D
G
B
S
320
N Gate/PFet
D
G
B
S
340
N Gate/NFet
D
G
B
S

FIG. 3

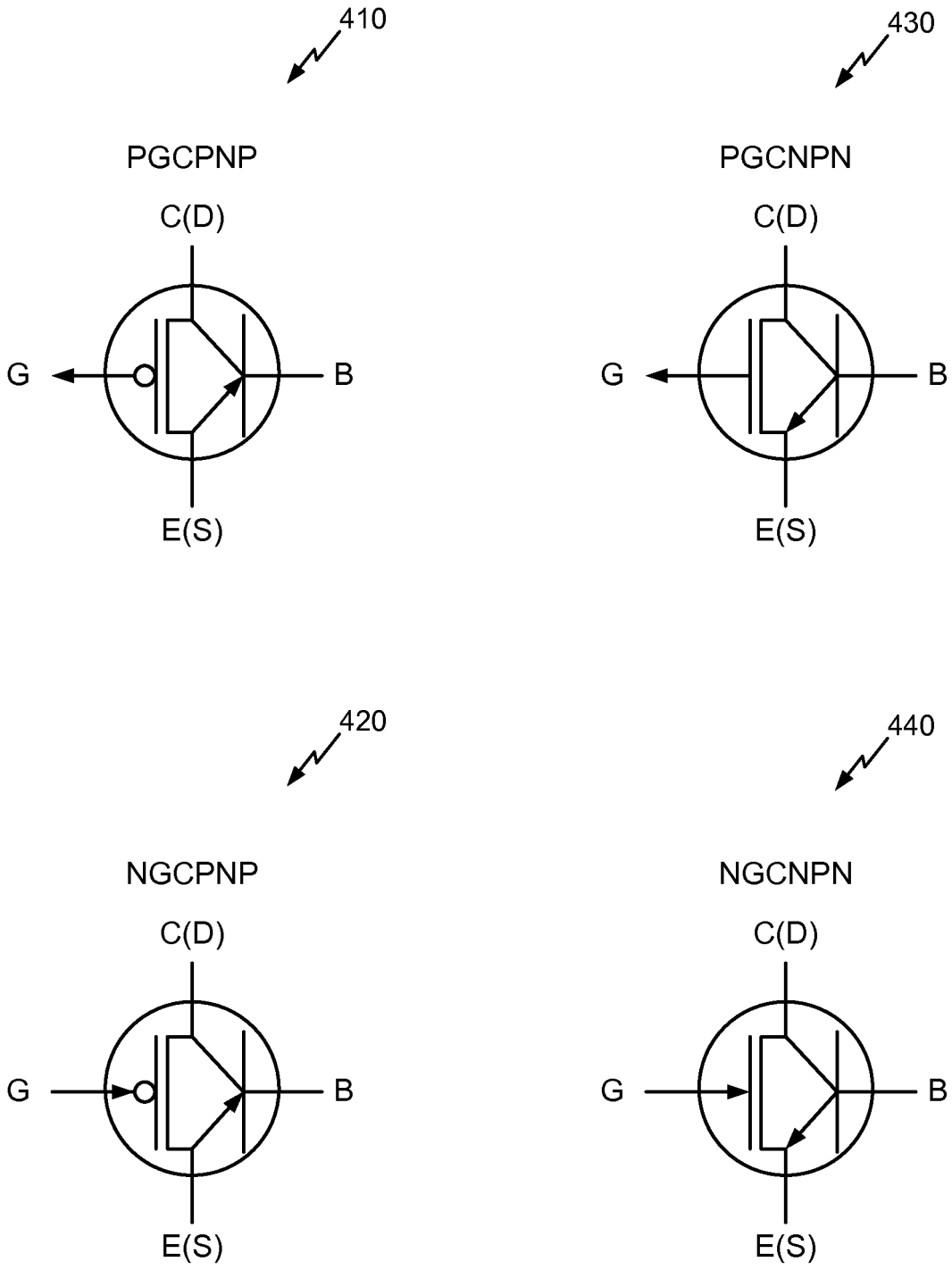

410
PGCPNP
C(D)
G
B
E(S)
430
PGCNPN
C(D)
G
B
E(S)
420
NGCPNP
C(D)
G
B
E(S)
440
NGCNPN
C(D)
G
B
E(S)

FIG. 4

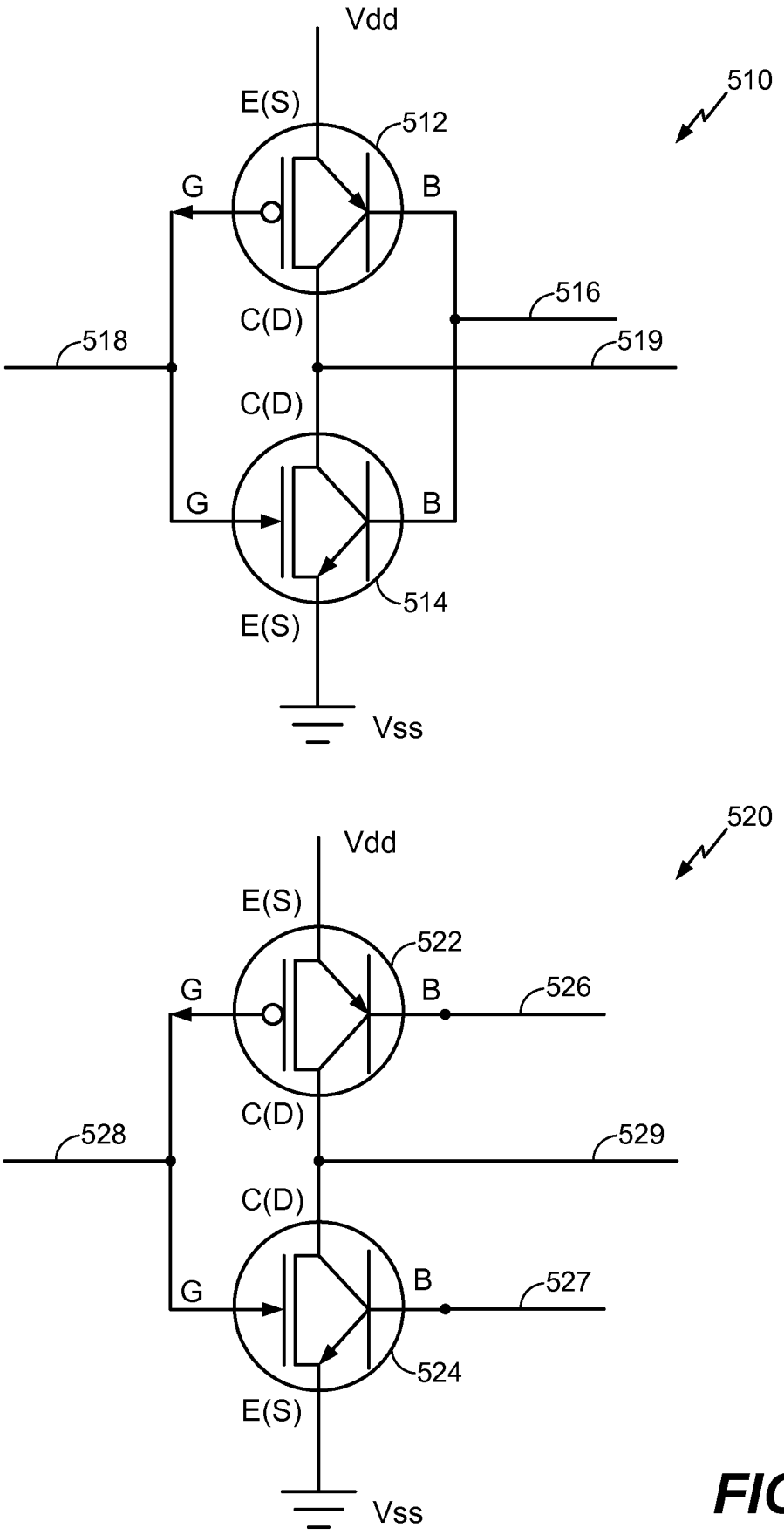

Vdd
510
E(S)
512
G
B
516
C(D)
518
519
C(D)
G
B
514
E(S)
Vss
520
Vdd
E(S)
522
G
B
526
C(D)
528
529
C(D)
G
B
527
524
E(S)
Vss

FIG. 5

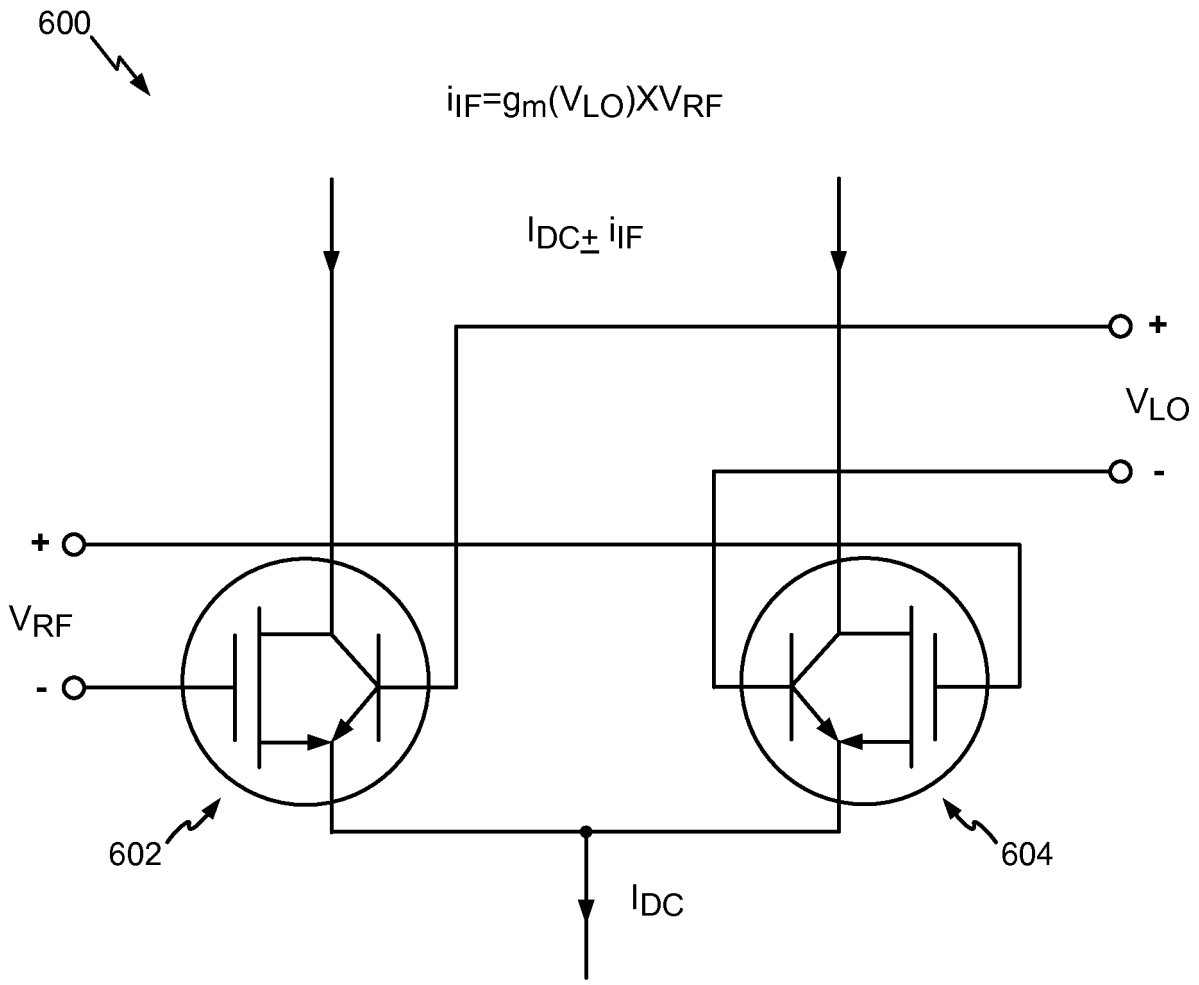


FIG. 6

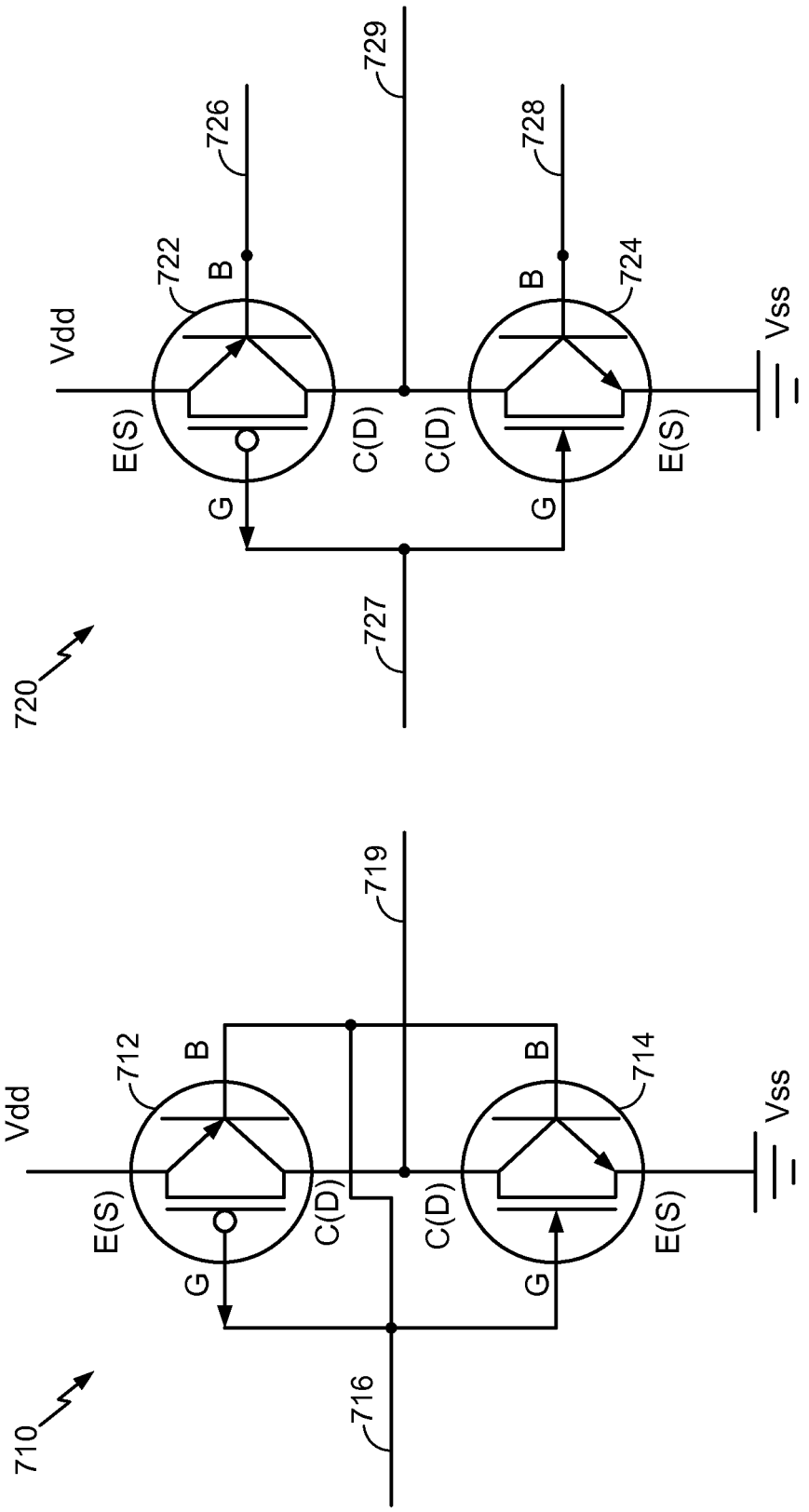


FIG. 7

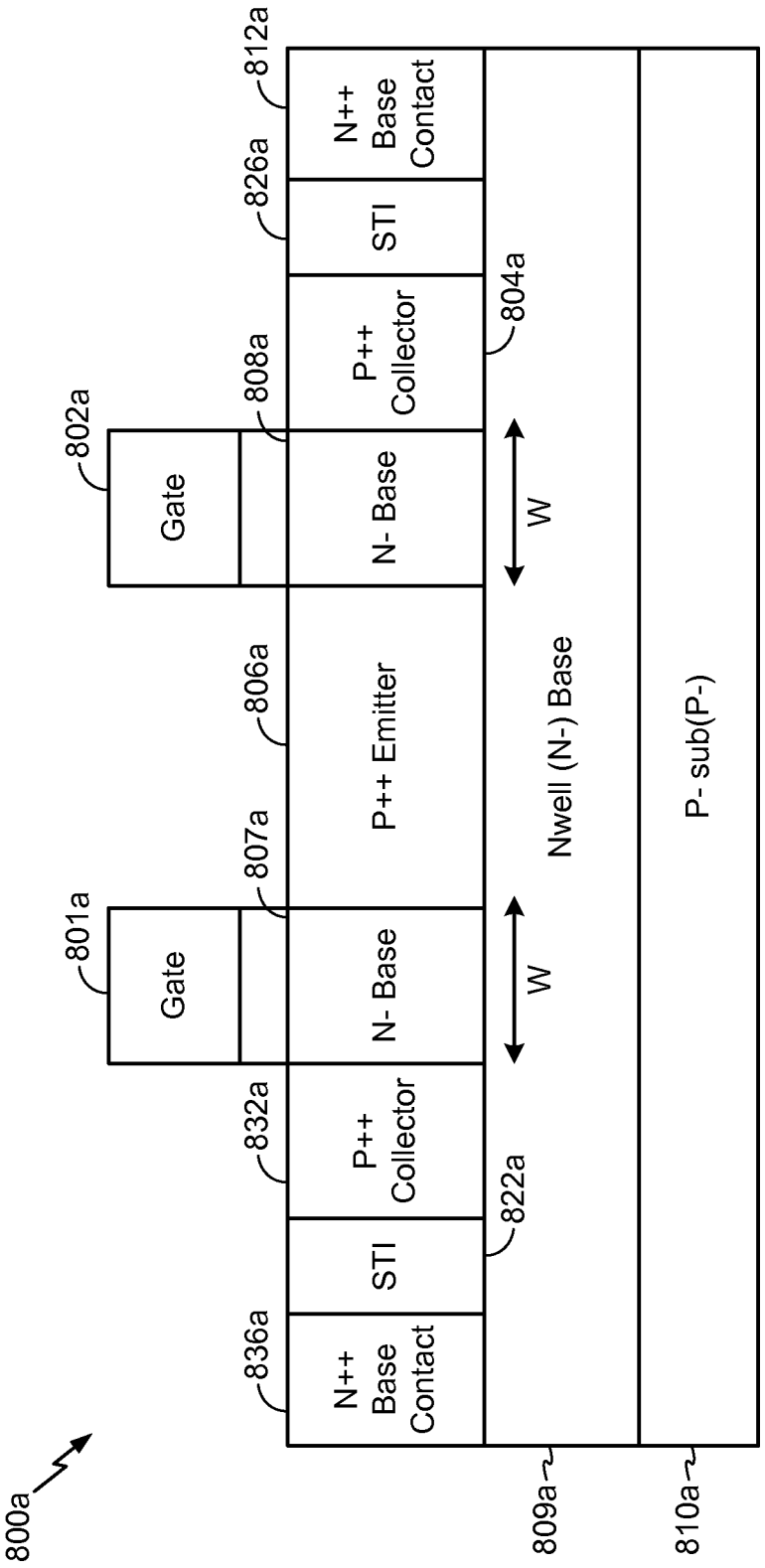

800a
801a
802a
806a
807a
808a
812a
826a
832a
836a
804a
822a
809a
810a
Gate
Gate
N- Base
N- Base
P++ Emitter
P++ Collector
P++ Collector
STI
STI
N++ Base Contact
N++ Base Contact
W
W
Nwell (N-) Base
P- sub(P-)

FIG. 8A

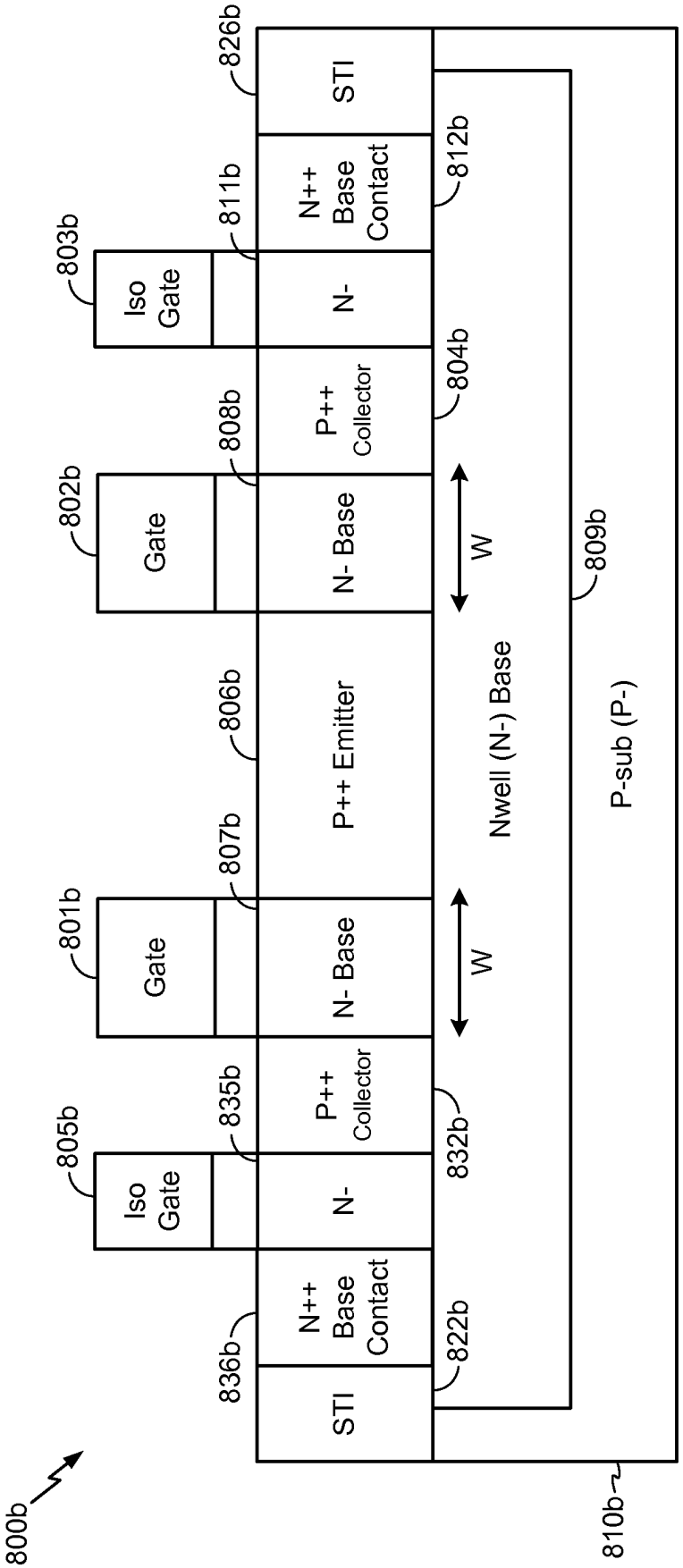

800b
836b
STI
N++ Base Contact
822b
805b
Iso Gate
835b
N-
P++ Collector
832b
801b
Gate
807b
N- Base
806b
P++ Emitter
802b
Gate
808b
N- Base
803b
Iso Gate
811b
N-
P++ Collector
804b
826b
STI
N++ Base Contact
812b
W
W
Nwell (N-) Base
P-sub (P-)
809b
810b

FIG. 8B

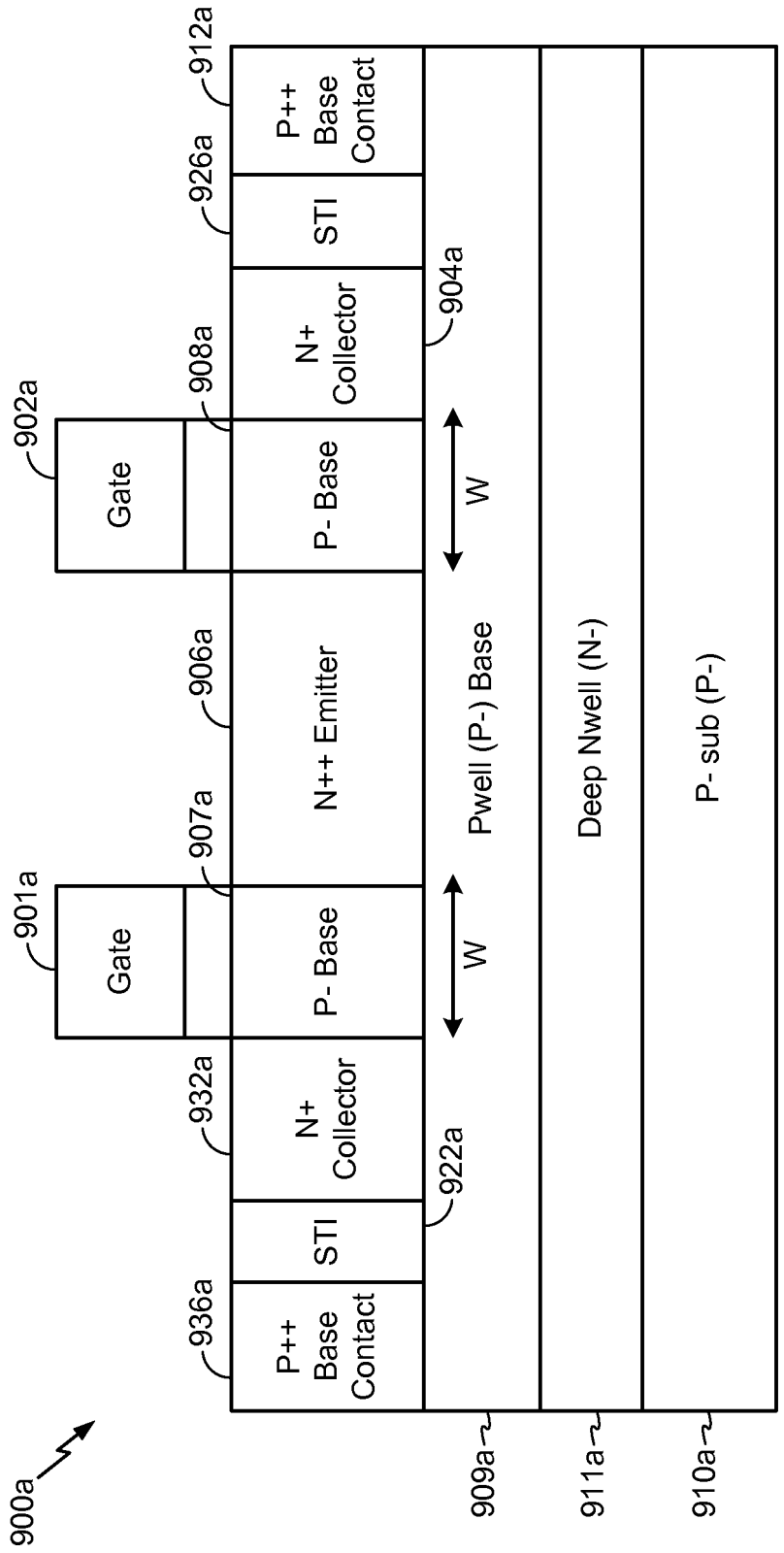

900a
936a
P++ Base Contact
STI
932a
N+ Collector
922a
901a
Gate
907a
P- Base
906a
N++ Emitter
902a
Gate
908a
P- Base
926a
STI
912a
P++ Base Contact
904a
N+ Collector
W
W
Pwell (P-) Base
Deep Nwell (N-)
P- sub (P-)
909a
911a
910a

FIG. 9A

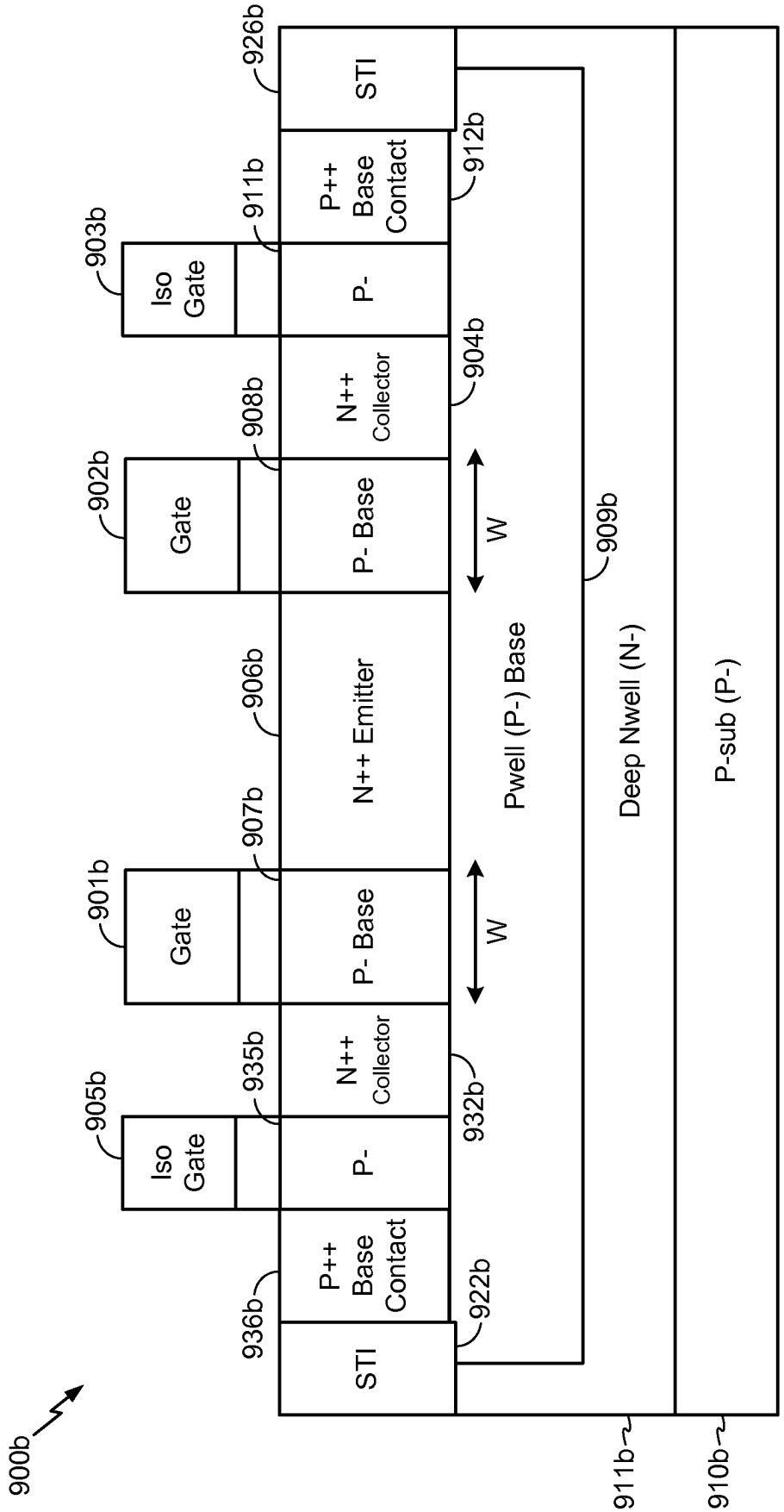
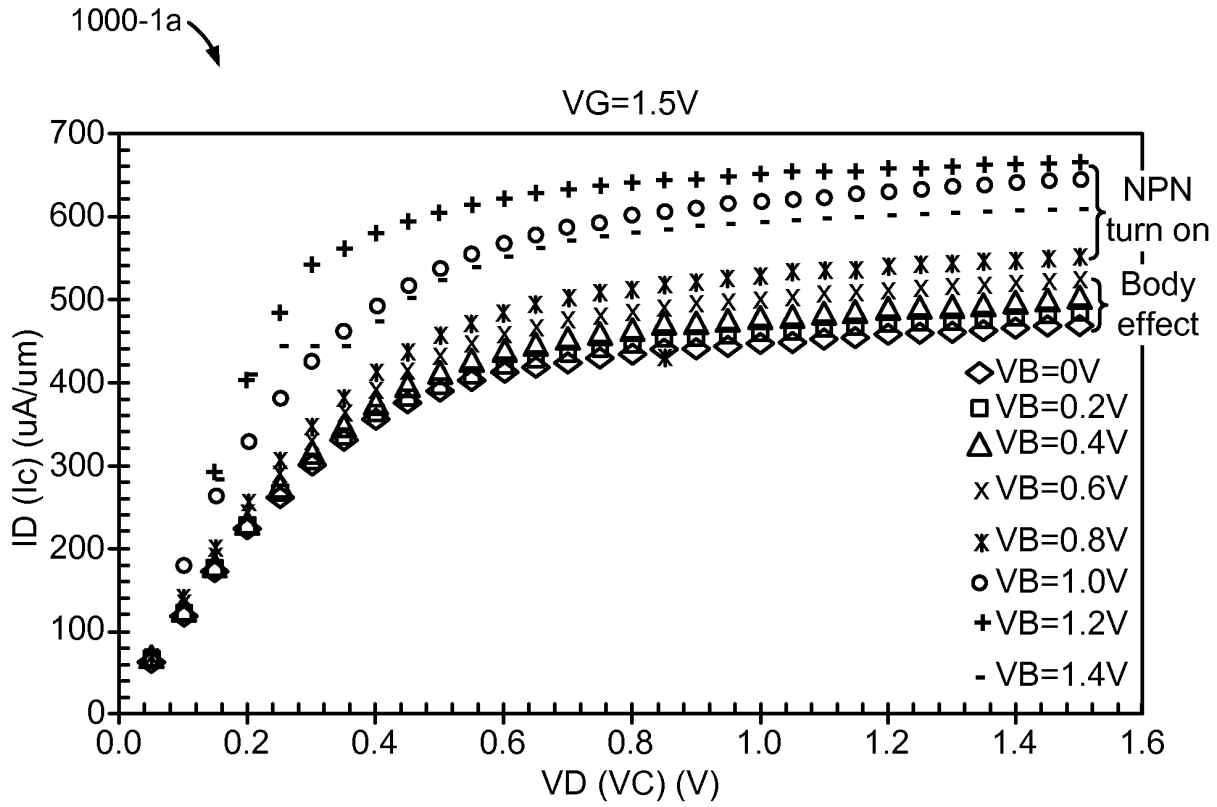

900b
911b
910b
STI
926b
P++ Base Contact
912b
911b
Iso Gate
903b
P-
N++ Collector
904b
908b
Gate
902b
P- Base
W
909b
N++ Emitter
906b
907b
Gate
901b
P- Base
W
Pwell (P-) Base
Deep Nwell (N-)
P-sub (P-)
Iso Gate
905b
P-
N++ Collector
935b
932b
P++ Base Contact
936b
922b
STI

FIG. 9B


1000-1a
VG=1.5V
ID (Ic) (uA/um)
VD (VC) (V)
NPN
turn on
Body
effect
VB=0V
VB=0.2V
VB=0.4V
VB=0.6V
VB=0.8V
VB=1.0V
VB=1.2V
VB=1.4V

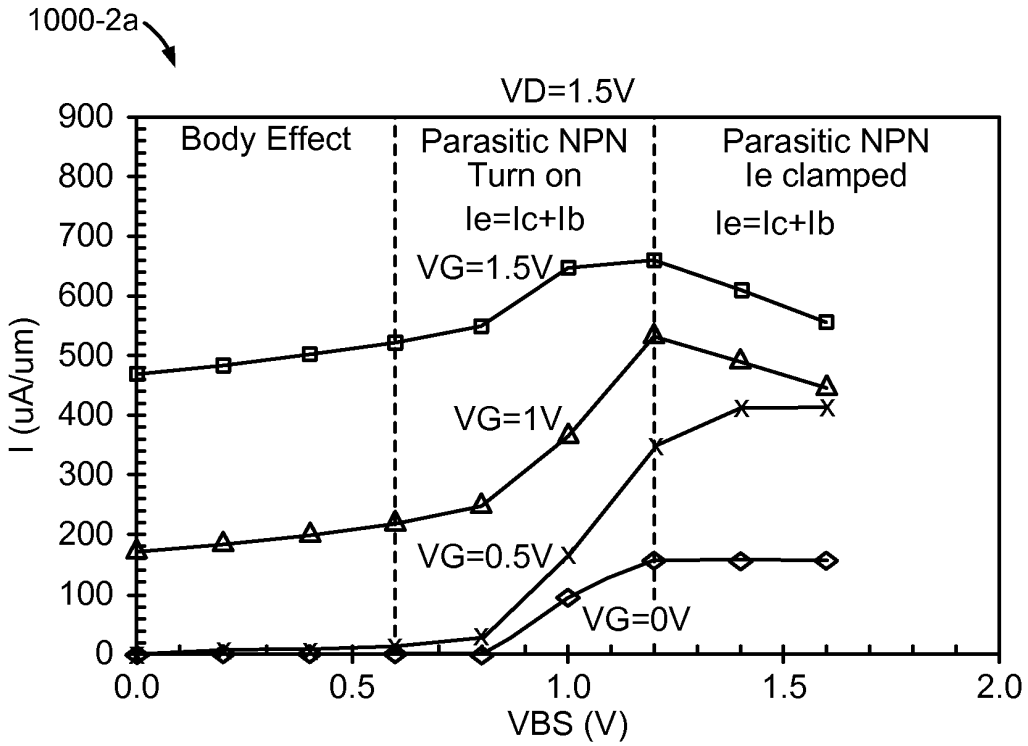

1000-2a
VD=1.5V
Body Effect
Parasitic NPN
Turn on
Ie=Ic+Ib
Parasitic NPN
Ie clamped
Ie=Ic+Ib
VG=1.5V
VG=1V
VG=0.5V
VG=0V
I (uA/um)
VBS (V)

FIG. 10A

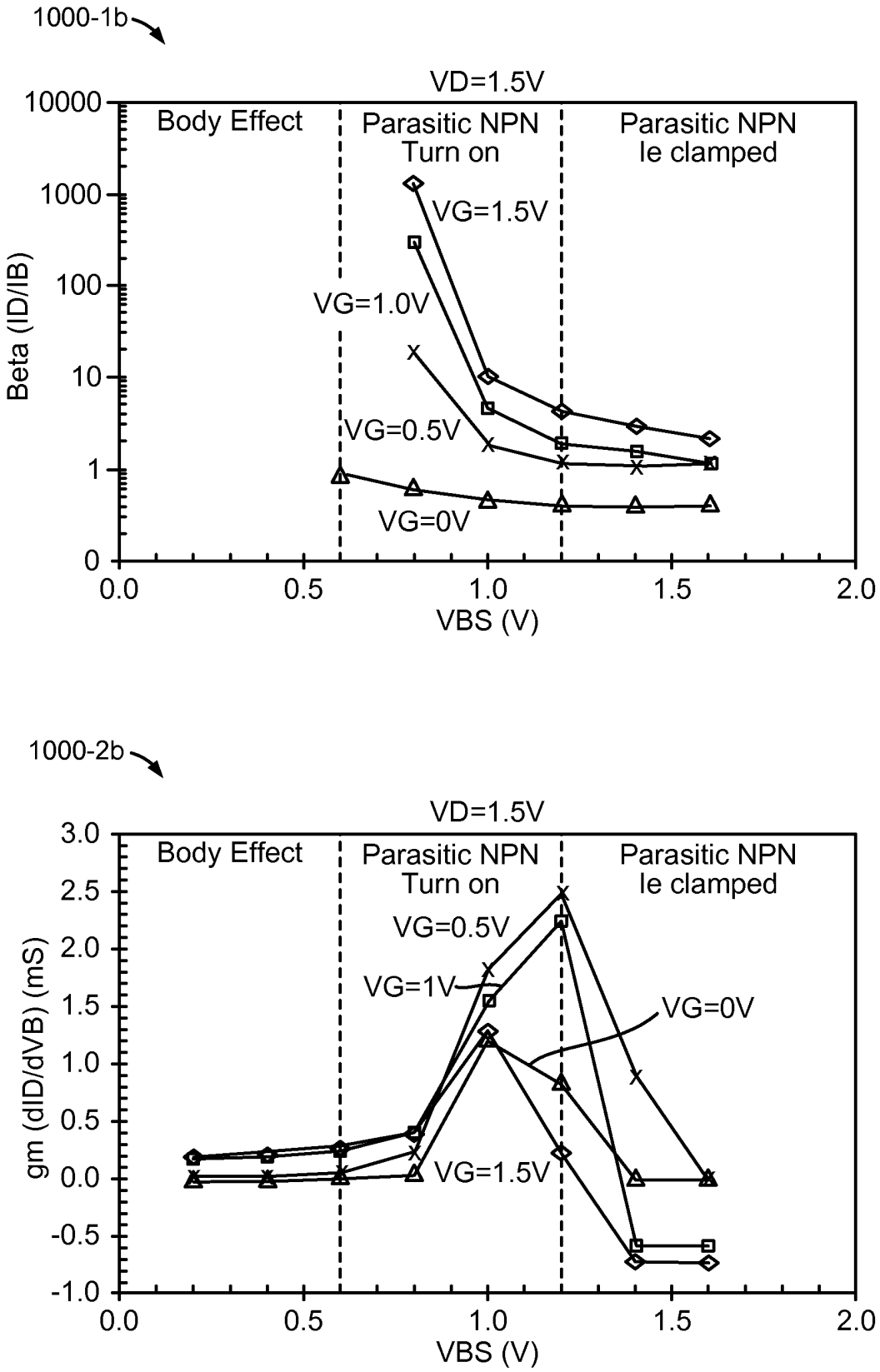

1000-1b
VD=1.5V
Body Effect
Parasitic NPN
Turn on
Parasitic NPN
le clamped
VG=1.5V
VG=1.0V
VG=0.5V
VG=0V
Beta (ID/IB)
10000
1000
100
10
1
0
0.0
0.5
1.0
1.5
2.0
VBS (V)
1000-2b
VD=1.5V
Body Effect
Parasitic NPN
Turn on
Parasitic NPN
le clamped
VG=0.5V
VG=1V
VG=0V
VG=1.5V
gm (dID/dVB) (mS)
3.0
2.5
2.0
1.5
1.0
0.5
0.0
-0.5
-1.0
0.0
0.5
1.0
1.5
2.0
VBS (V)

FIG. 10B

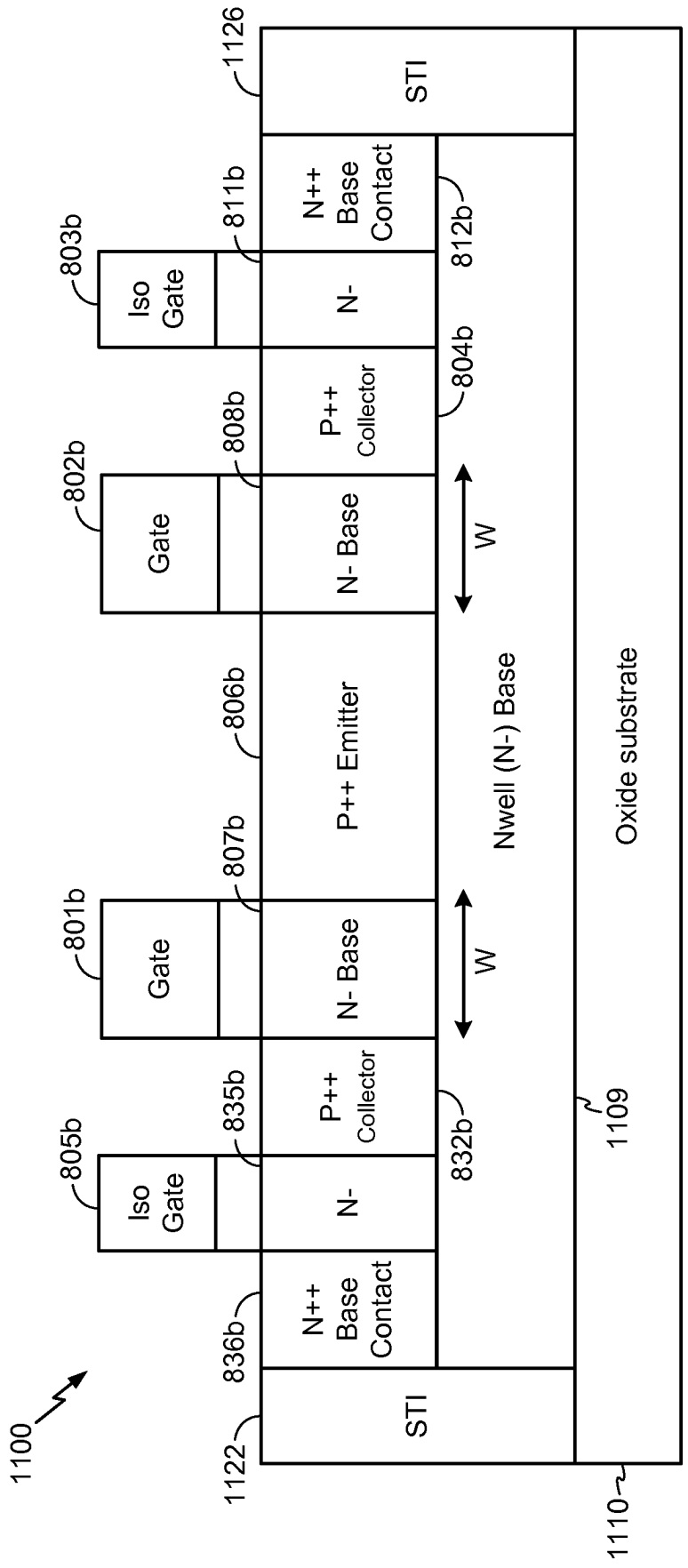

1100
1122
STI
836b
N++ Base Contact
805b
Iso Gate
835b
N-
P++ Collector
801b
Gate
807b
N- Base
806b
P++ Emitter
802b
Gate
808b
N- Base
803b
Iso Gate
811b
N-
P++ Collector
1126
STI
N++ Base Contact
812b
804b
W
W
832b
Nwell (N-) Base
1109
Oxide substrate
1110

FIG. 11

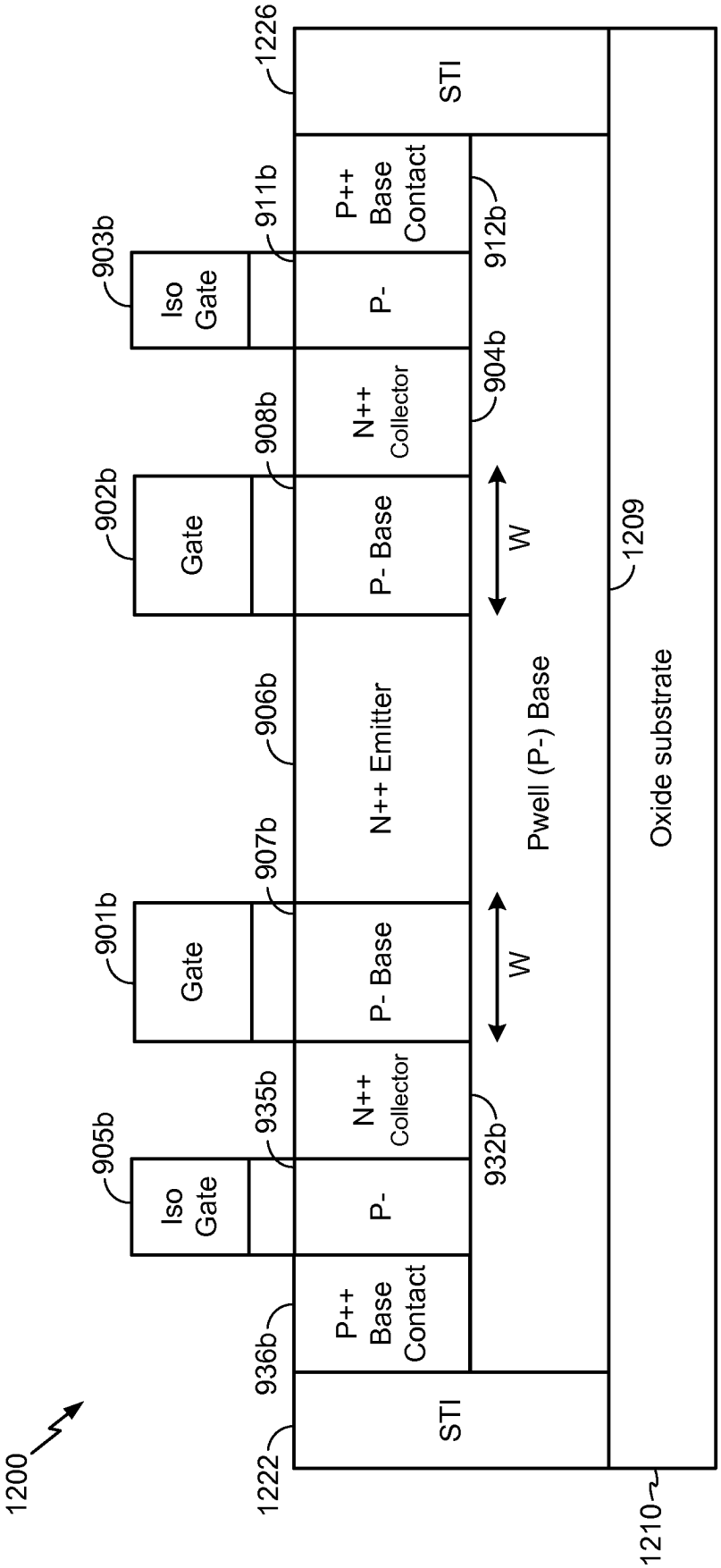

1200
1222
936b
905b
Iso Gate
935b
P-
N++ Collector
932b
901b
Gate
907b
P- Base
W
906b
N++ Emitter
902b
Gate
908b
P- Base
W
903b
Iso Gate
911b
P-
N++ Collector
904b
912b
P++ Base Contact
1226
STI
STI
P++ Base Contact
Pwell (P-) Base
1209
Oxide substrate
1210

FIG. 12

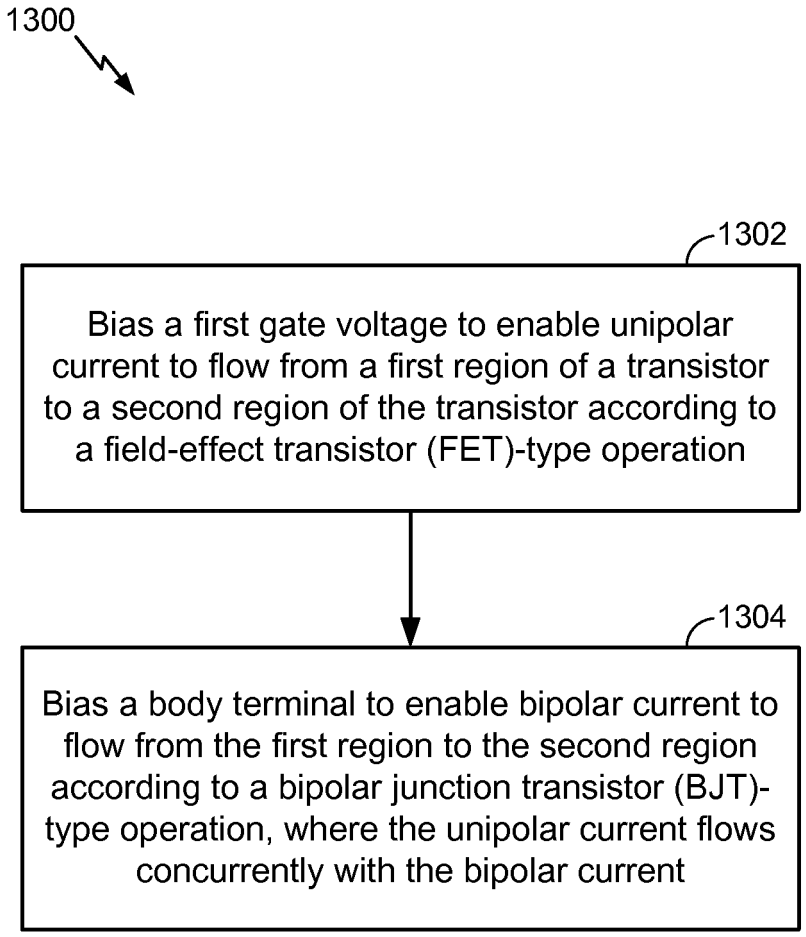

1300
1302
Bias a first gate voltage to enable unipolar current to flow from a first region of a transistor to a second region of the transistor according to a field-effect transistor (FET)-type operation
1304
Bias a body terminal to enable bipolar current to flow from the first region to the second region according to a bipolar junction transistor (BJT)-type operation, where the unipolar current flows concurrently with the bipolar current

FIG. 13

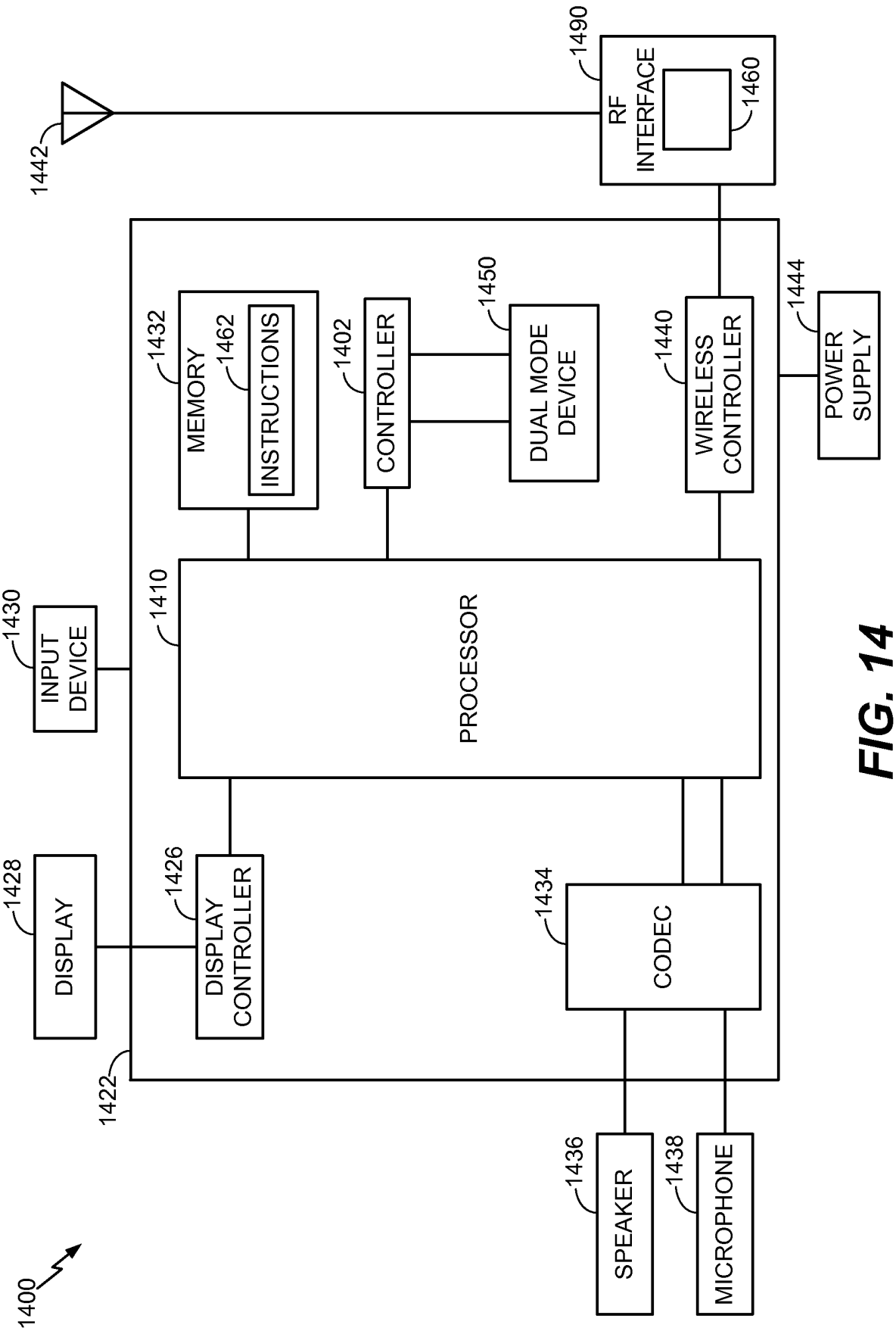

1400
1410
PROCESSOR
1422
1428
DISPLAY
1426
DISPLAY CONTROLLER
1430
INPUT DEVICE
1432
MEMORY
1462
INSTRUCTIONS
1434
CODEC
1436
SPEAKER
1438
MICROPHONE
1402
CONTROLLER
1450
DUAL MODE DEVICE
1440
WIRELESS CONTROLLER
1444
POWER SUPPLY
1442
1490
RF INTERFACE
1460

FIG. 14

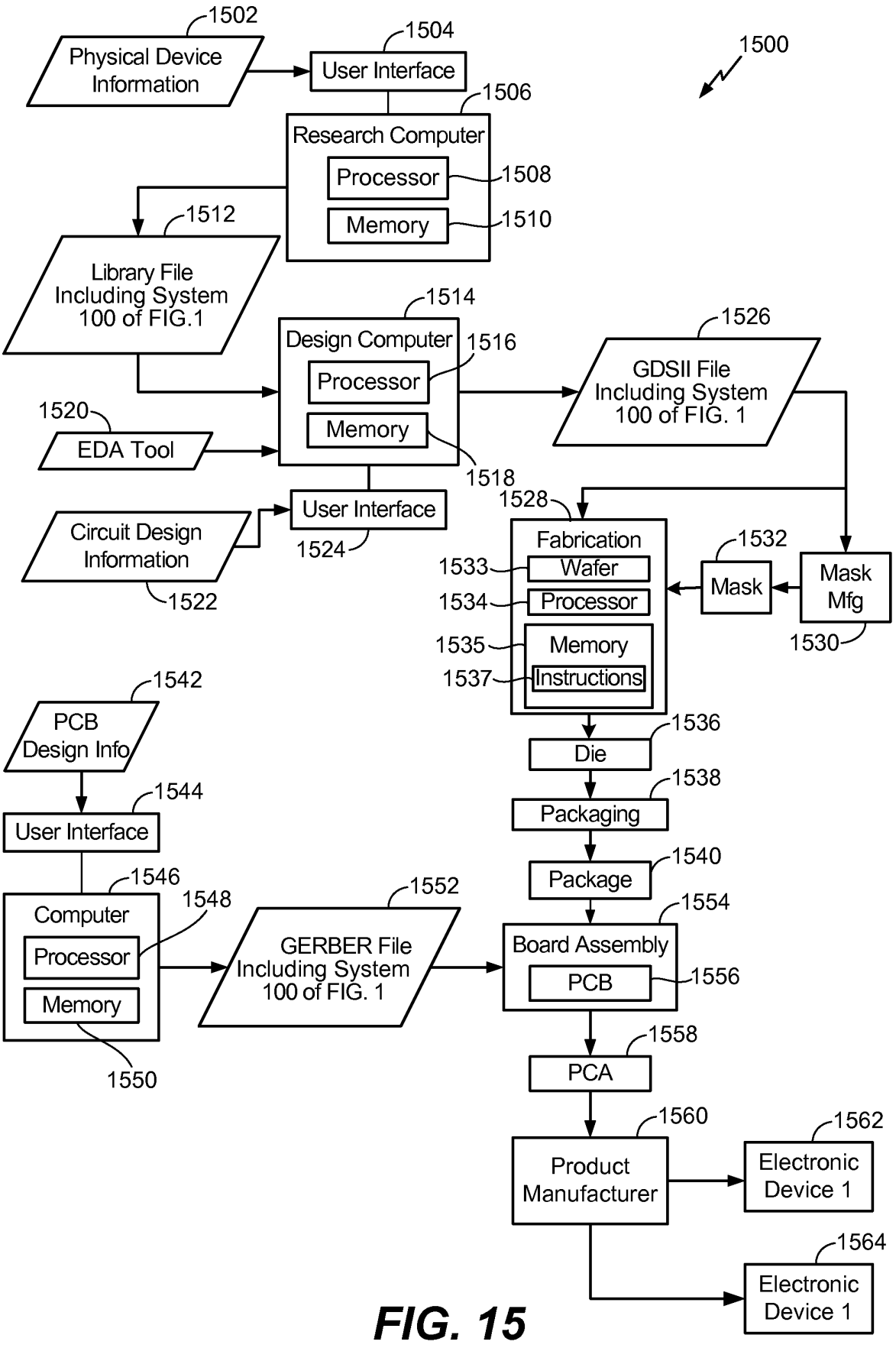

1500
1502
Physical Device Information
1504
User Interface
1506
Research Computer
Processor
1508
Memory
1510
1512
Library File Including System 100 of FIG.1
1514
Design Computer
Processor
1516
Memory
1518
1520
EDA Tool
User Interface
1524
Circuit Design Information
1522
1526
GDSII File Including System 100 of FIG. 1
1528
Fabrication
1533
Wafer
1534
Processor
1535
Memory
1537
Instructions
1532
Mask
Mask Mfg
1530
1542
PCB Design Info
1544
User Interface
1546
Computer
Processor
1548
Memory
1550
1552
GERBER File Including System 100 of FIG. 1
1536
Die
1538
Packaging
1540
Package
1554
Board Assembly
PCB
1556
1558
PCA
1560
Product Manufacturer
1562
Electronic Device 1
1564
Electronic Device 1

FIG. 15

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 5498885 A **[0004]**
- US 5717241 A **[0005]**
- US 2009256204 A1 **[0006]**