(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
18 December 2014 (18.12.2014)

WIPO | PCT

(10) International Publication Number
WO 2014/200663 A1

(51) International Patent Classification:
H01L 29/49 (2006.01)

(21) International Application Number:
PCT/US2014/038375

(22) International Filing Date:
16 May 2014 (16.05.2014)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
13/918,648 14 June 2013 (14.06.2013) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) Title: TRANSISTOR GATE AND PROCESS FOR MAKING TRANSISTOR GATE

(57) Abstract: A transistor gate is formed of a stack of layers including a polysilicon layer and a tungsten layer separated by a barrier layer. A titanium layer reduces interface resistance. A tungsten liner reduces sheet resistance. The tungsten liner, a tungsten nitride barrier layer, and the tungsten layer may be formed sequentially in the same chamber.

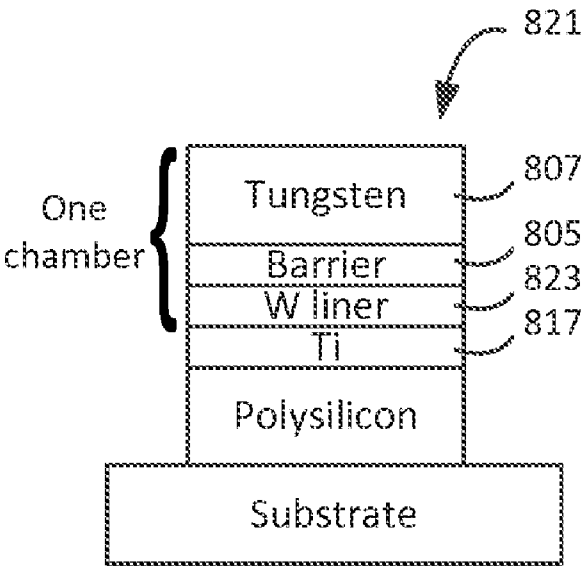

FIG. 8

WO 2014/200663 A1

TRANSISTOR GATE AND PROCESS FOR MAKING TRANSISTOR GATE

BACKGROUND OF THE INVENTION

[0001] This invention relates generally to semiconductor devices, their formation, structure and use, and specifically to methods of making transistor gates in nonvolatile memory integrated circuits.

[0002] Integrated circuits commonly include transistors. Many transistors have gates formed of a stack of materials that also form some wiring that connects the gates to other components. Examples of such arrangements are present in logic integrated circuits and in memory integrated circuits, including flash memory integrated circuits.

[0003] There are many commercially successful non-volatile memory products being used today, particularly in the form of small form factor cards, which use an array of flash EEPROM cells. An example of a flash memory system is shown in FIG. 1, in which a memory cell array 1 is formed on a memory chip 12, along with various peripheral circuits such as column control circuits 2, row control circuits 3, data input/output circuits 6, etc.

[0004] One popular flash EEPROM architecture utilizes a NAND array, wherein a large number of strings of memory cells are connected through one or more select transistors between individual bit lines and a reference potential. A portion of such an array is shown in plan view in Figure 2A. BL0 – BL4 represent diffused bit line connections to global vertical metal bit lines (not shown). Although four floating gate memory cells are shown in each string, the individual strings typically include 16, 32 or more memory cell charge storage elements, such as floating gates, in a column. Control gate (word) lines labeled WL0 – WL3 and string select lines DSL and SSL extend across multiple strings over rows of floating gates.

[0005] The top and bottom of the string connect to the bit line and a common source line respectively through select transistors (source select transistor and drain select transistor) as shown in FIG. 2B. Unlike memory cells, these transistors do not

generally include floating gates. The gates of select transistors are electrically driven from the periphery through select lines that may extend over significant distances so that resistance of such lines is a concern. Transistors in peripheral circuits are also formed without floating gates and may also be controlled using lines that have significant resistance. Accordingly, there is a need for a transistor gate structure that can provide low resistance and for methods of forming such transistor gate structures in an efficient manner.

SUMMARY OF THE INVENTION

[0006] A transistor gate stack includes a polysilicon layer and a tungsten layer separated by a barrier layer. A titanium (or other silicide metal) layer between the polysilicon layer and the barrier layer reduces interface resistance but increases sheet resistance. A tungsten liner between the titanium layer and the barrier layer allows the use of the titanium layer with little or no increase in sheet resistance. The tungsten liner, a tungsten nitride barrier layer, and the tungsten layer may be formed in the same Physical Vapor Deposition (PVD) chamber, for example by sputtering a tungsten target to form tungsten layers, and adding nitrogen gas during sputtering to form tungsten nitride.

[0007] An example of a transistor gate structure includes: a doped polysilicon layer; a silicide metal layer overlying the doped polysilicon layer; a first tungsten layer overlying the silicide metal layer; a barrier layer overlying the silicide metal layer; and a second tungsten layer overlying the barrier layer.

[0008] The silicide metal layer may comprise titanium. The silicide metal layer may comprise yttrium, or nickel. The barrier layer may comprise tungsten nitride. The barrier layer may comprise tungsten nitride deposited by Physical Vapor Deposition (PVD).

[0009] An example of a method of forming a transistor gate structure includes: depositing a doped polysilicon layer over a gate dielectric; depositing a silicide metal layer over the doped polysilicon layer; depositing a first tungsten layer over the silicide metal layer; depositing a barrier layer over the silicide metal layer; and depositing a second tungsten layer over the barrier layer.

[0010] Depositing the barrier layer may include depositing tungsten nitride or titanium nitride. The first tungsten layer, the barrier layer, and the second tungsten layer may be deposited in the same tool. The barrier layer may comprise tungsten nitride and the first tungsten layer, the barrier layer, and the second tungsten layer may be deposited in the same chamber of the same tool. The chamber may be a Physical Vapor Deposition (PVD) chamber and the first tungsten layer, the barrier layer, and the second tungsten layer may be deposited by sputtering. The first tungsten layer, the barrier layer, and the second tungsten layer may be deposited using a tungsten target, and nitrogen gas may be introduced into the chamber during the deposition of the barrier layer. The silicide metal layer may be deposited in the same tool. A patterned hard mask layer may subsequently be formed and subsequent etching may be performed with the hard mask layer in place to form individual gates.

[0011] An example of a method of forming a transistor gate structure includes: depositing a gate dielectric layer over a substrate surface; depositing a doped polysilicon layer over the gate dielectric layer; depositing a titanium layer overlying the doped polysilicon layer; depositing a first tungsten layer over the titanium layer by sputtering; depositing a metal nitride layer over the silicide metal layer by sputtering; and depositing a second tungsten layer over the metal nitride layer by sputtering.

[0012] The metal nitride may be tungsten nitride. The first tungsten layer, the metal nitride layer, and the second tungsten layer may be deposited sequentially by deposition in a sputtering chamber with a tungsten target. The titanium layer may be deposited in another chamber that is on the same tool as the sputtering chamber. The titanium layer may be deposited to a thickness of about one nanometer, the first tungsten layer may be deposited to a thickness of more than one nanometer, and the metal nitride layer may be deposited to a thickness of more than three nanometers.

[0013] Additional aspects, advantages and features of the present invention are included in the following description of examples thereof, which description should be taken in conjunction with the accompanying drawings. All patents, patent applications, articles, technical papers and other publications referenced herein are hereby incorporated herein in their entirety by this reference.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] FIG. 1 is a block diagram of a prior art memory system.

[0015] FIG. 2A is a plan view of a prior art NAND array.

[0016] FIG. 2B is a cross-sectional view of the prior art NAND array of FIG. 2A taken along the line A-A.

[0017] FIG. 3 shows a prior art gate stack.

[0018] FIG. 4 shows the prior art gate stack of FIG. 3 after patterning.

[0019] FIG. 5 illustrates interface resistance in a gate stack.

[0020] FIG. 6 shows an example of a gate stack that includes a titanium layer.

[0021] FIG. 7 illustrates wire resistance of a line formed from a gate stack.

[0022] FIG. 8 shows an example of a gate stack that includes a tungsten liner.

[0023] FIG. 9 shows a process for forming a gate stack.

[0024] FIG. 10 shows interface resistance as a function of titanium thickness for two gate stacks, one with, and one without a tungsten liner.

[0025] FIG. 11 shows wire resistance as a function of titanium thickness for two gate stacks, one with, and one without a tungsten liner.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

Memory System

[0026] An example of a prior art memory system, which may be modified to include various aspects of the present invention, is illustrated by the block diagram of FIG. 1. A memory cell array 1 including a plurality of memory cells M arranged in a matrix has peripheral circuits that allow access to the memory array. A column control circuit 2, a row control circuit 3, a c-source control circuit 4 and a c-p-well control circuit 5

are provided to supply appropriate voltages to access selected memory cells. The memory cell array 1 is, in this example, of the NAND type similar to that described above in the Background and in references incorporated therein by reference. A control circuit 2 is connected to bit lines (BL) of the memory cell array 1 for reading data stored in the memory cells (M), for determining a state of the memory cells (M) during a program operation, and for controlling potential levels of the bit lines (BL) to promote the programming or to inhibit the programming. The row control circuit 3 is connected to word lines (WL) to select one of the word lines (WL), to apply read voltages, to apply program voltages combined with the bit line potential levels controlled by the column control circuit 2, and to apply an erase voltage coupled with a voltage of a p-type region on which the memory cells (M) are formed. The c-source control circuit 4 controls a common source line (labeled as "c-source" in Figure 1) connected to the memory cells (M). The c-p-well control circuit 5 controls the c-p-well voltage.

[0027] The data stored in the memory cells (M) are read out by the column control circuit 2 and are output to external I/O lines via an I/O line and a data input/output buffer 6. Program data to be stored in the memory cells are input to the data input/output buffer 6 via the external I/O lines, and transferred to the column control circuit 2. The external I/O lines are connected to a controller 9. The controller 9 includes various types of registers and other memory including a volatile random-access-memory (RAM) 10.

[0028] The memory system of Figure 1 may be embedded as part of the host system, or may be included in a memory card, USB drive, or similar unit that is removably insertible into a mating socket of a host system. Such a card may include the entire memory system, or the controller and memory array, with associated peripheral circuits, may be provided in separate cards. Several card implementations are described, for example, in U.S. patent no. 5,887,145. The memory system of FIG. 1 may also be used in a Solid State Drive (SSD) or similar unit that provides mass data storage in a tablet, laptop computer, or similar device.

[0029] Memory chips such as memory chip 12 generally include many transistors with unitary gates (transistors that do not have floating gates). For example, select

gates at either end of a NAND string and transistors in peripheral circuits such as shown in FIG. 1 generally have unitary gates. Such gates may be formed of doped polysilicon, metal, metal silicide, or some combination of conductive layers. Transistors with unitary gates are used in a variety of other integrated circuits including memory controller chips and other logic chips.

[0030] FIG. 3 shows a prior art example of formation of a gate of such a transistor. A blanket layer of doped polysilicon 301 is deposited over a substrate 303 (an intervening gate dielectric layer, or layers, is omitted in FIG. 3). A barrier layer 305 overlies the polysilicon and separates it from a tungsten (W) layer 307. Barrier layer 305 between polysilicon layer 301 and tungsten layer 307 may be formed of tungsten nitride or titanium nitride for example. Tungsten nitride deposited by Physical Vapor Deposition "PVD" has been found to be an effective barrier. The barrier layer prevents silicidation of tungsten, i.e. the formation of tungsten silicide as a result of interaction with the silicon of the polysilicon layer.

[0031] A hard mask layer 309 overlies the tungsten layer 307 and a resist layer is formed (e.g. spun on) on the hard mask layer and is patterned (e.g. by photolithography) to form resist portions such as the resist portion 311 shown. Subsequently, the pattern of the resist portions is transferred to the hard mask layer thus forming corresponding hard mask portions. The hard mask portions are then used as an etch mask during an anisotropic etch step (e.g. using Reactive Ion Etch, or "RIE"). This results in the formation of a gate 413 as shown in FIG. 4. The series of layers that are deposited and etched to make such a gate form a stack that may be referred to as a "gate stack." Selecting appropriate materials for a gate stack has implications for efficient operation of the integrated circuit.

[0032] FIG. 5 illustrates one important characteristic of a gate stack, the resistance of the stack in the vertical direction, which contributes to power consumed by the transistor. An important contribution to the resistance of the stack is from interface resistance between materials (resistance of the tungsten, barrier, and polysilicon layers are relatively low in the vertical direction because of their large cross sectional area compared with their thickness). It has been found that the addition of a silicide metal such as titanium can significantly reduce interface resistance in such a stack.

[0033] FIG. 6 shows a cross section of a gate stack 615 that includes a titanium layer 617 between a polysilicon layer 601 and a barrier layer 605. In other examples a different silicide metal may be used instead of titanium, to reduce interface resistance, such as yttrium, nickel, or cobalt.

[0034] FIG. 7 illustrates another important characteristic of a gate stack, the resistance along a wire made from the gate stack, which depends on the geometry of such a wire and the sheet resistance of the gate stack. It has been found that a stack such as shown in FIG. 6 may have high sheet resistance as a result of including a titanium layer because tungsten grain size is affected by the titanium. For example, the addition of a titanium layer to a gate stack may result in sheet resistance that is two to three times higher than a gate stack that does not have such a titanium layer. The titanium layer appears to cause overlying tungsten to be formed with small grains and therefore high sheet resistance. Thus, although adding a titanium layer to a stack may improve interface resistance, this generally comes at the expense of increased sheet resistance.

[0035] FIG. 8 shows a cross section of a gate stack 821 that has both good interface resistance and good sheet resistance. In this example, a tungsten liner 823 is added between a titanium layer 817 and a barrier layer 805. The addition of a tungsten liner reduces or eliminates the effect of the titanium layer on grain size in the tungsten layer.

[0036] While various materials may be used for barrier layer 805, the use of tungsten nitride (WN) is convenient because this layer is formed between the tungsten liner layer 823 and the tungsten layer 807. In one example, all three of these layers (W liner layer 823, WN barrier 805, and W layer 807) may be formed sequentially in the same chamber, for example a PVD chamber. In one example, a sputtering chamber with a tungsten target may be used to sputter tungsten to form the tungsten liner. Then, sputtering may continue in the chamber with the addition of nitrogen into the sputtering chamber so that a tungsten nitride barrier layer is formed. Then, the flow of nitrogen is stopped and sputtering of tungsten forms the tungsten layer.

[0037] FIG. 9 illustrates the formation of a gate stack such as described above. A polysilicon layer is deposited 931 over a substrate that has a gate dielectric layer such

as a gate oxide. This may be done using a furnace or other conventional method. Then, a titanium layer is deposited 933 on the polysilicon to reduce interface resistance. Titanium may be deposited by PVD or otherwise (e.g. Chemical Vapor Deposition, CVD). Then, the substrate is sent to a tungsten sputtering chamber that is equipped with a controllable nitrogen supply. The tungsten liner is deposited 935, then the tungsten nitride barrier layer is deposited 937, and then the tungsten layer is deposited 939, in sequence, in the same chamber. In some cases, the titanium may be deposited in a separate chamber that is part of the same system. For example, a cluster tool may have a PVD chamber with a titanium target for depositing the titanium layer and another PVD chamber with a tungsten target and a nitrogen supply to deposit the liner, barrier, and tungsten layers. Substrates may be transferred between these chambers under vacuum so that no contamination is introduced between these layers and a high throughput is maintained. Subsequent to deposition of the tungsten layer 939, the substrate may be removed from the PVD deposition system and may be patterned 941 as before (e.g. using a hard mask layer followed by resist patterning).

[0038] FIG. 10 shows how interface resistance is somewhat lower with a tungsten liner than without. Interface resistance is shown on the vertical axis (in arbitrary units) and titanium thickness is shown along the horizontal axis. It can be seen that for a titanium layer thickness of 1.0nm, which is sufficient to reduce interface resistance by more than half (from over 1000 to less than 500), the addition of a 2nm thick tungsten liner reduces interface resistance by about another 25% compared with not using a tungsten liner.

[0039] FIG. 11 shows how sheet resistance is significantly lower with a tungsten liner than without. Wire resistance is shown on the vertical axis (in arbitrary units) and titanium thickness is again shown along the horizontal axis. It can be seen that as titanium thickness increases, the wire resistance increases significantly for the example without a tungsten liner (as tungsten grain size is negatively impacted by the titanium layer). In contrast, when a 2nm thick tungsten liner is provided, the wire resistance remains the same regardless of titanium thickness. Thus, the negative impact of the titanium layer on sheet resistance is overcome by the addition of a tungsten liner.

[0040] In general, any suitable layer thicknesses may be used. For example, the titanium layer may be 1nm, the tungsten liner layer may be greater than 1nm (e.g. 2nm), and the barrier tungsten nitride layer may be greater than 3nm (e.g. 5nm). While this form of gate stack may be used in nonvolatile memory integrated circuits, its use is not limited to nonvolatile memories or memories in general. Transistors may be formed in any integrated circuit so that they have gates as described above. Furthermore, other fabrication schemes may be used to produce the gate stack shown.

Conclusion

[0041] Although the various aspects of the present invention have been described with respect to exemplary embodiments thereof, it will be understood that the present invention is entitled to protection within the full scope of the appended claims. Furthermore, although the present invention teaches the method for implementation with respect to particular prior art structures, it will be understood that the present invention is entitled to protection when implemented in memory arrays with architectures than those described.

IT IS CLAIMED:

1. A transistor gate structure comprising:
a doped polysilicon layer;
a silicide metal layer overlying the doped polysilicon layer;
a first tungsten layer overlying the silicide metal layer;
a barrier layer overlying the silicide metal layer; and
a second tungsten layer overlying the barrier layer.

2. The transistor gate structure of claim 1 wherein the silicide metal layer comprises titanium.

3. The transistor gate structure of claim 1 wherein the silicide metal layer comprises yttrium, or nickel.

4. The transistor gate structure of claim 1 wherein the barrier layer comprises tungsten nitride.

5. The transistor gate structure of claim 4 wherein the barrier layer comprises tungsten nitride deposited by Physical Vapor Deposition (PVD).

6. A method of forming a transistor gate structure comprising:
depositing a doped polysilicon layer over a gate dielectric;
depositing a silicide metal layer over the doped polysilicon layer;
depositing a first tungsten layer over the silicide metal layer;
depositing a barrier layer over the silicide metal layer; and
depositing a second tungsten layer over the barrier layer.

7. The method of claim 6 wherein depositing the barrier layer comprises depositing tungsten nitride or titanium nitride.

8. The method of claim 7 wherein the first tungsten layer, the barrier layer, and the second tungsten layer are deposited in the same tool.

9. The method of claim 8 wherein barrier layer comprises tungsten nitride and the first tungsten layer, the barrier layer, and the second tungsten layer are deposited in the same chamber of the same tool.

10. The method of claim 9 wherein the chamber is a Physical Vapor Deposition (PVD) chamber and wherein the first tungsten layer, the barrier layer, and the second tungsten layer are deposited by sputtering.

11. The method of claim 10 wherein the first tungsten layer, the barrier layer, and the second tungsten layer are deposited using a tungsten target, and wherein nitrogen gas is introduced into the chamber during the deposition of the barrier layer.

12. The method of claim 8 further comprising depositing the silicide metal layer in the same tool.

13. The method of claim 6 further comprising subsequently forming a patterned hard mask layer and subsequently etching with the hard mask layer in place to form individual gates.

14. A method of forming a transistor gate structure comprising:

depositing gate dielectric layer over a substrate surface;

depositing a doped polysilicon layer over the gate dielectric layer;

depositing a titanium layer overlying the doped polysilicon layer;

depositing a first tungsten layer over the titanium layer by sputtering;

depositing a metal nitride layer over the silicide metal layer by sputtering; and

depositing a second tungsten layer over the metal nitride layer by sputtering.

15. The method of claim 14 wherein the metal nitride is tungsten nitride.

16. The method of claim 15 wherein the first tungsten layer, the metal nitride layer, and the second tungsten layer are deposited sequentially by deposition in a sputtering chamber with a tungsten target.

17. The method of claim 15 wherein the titanium layer is deposited in another chamber that is on the same tool as the sputtering chamber.

18. The method of claim 14 wherein the titanium layer is deposited to a thickness of about one nanometer, the first tungsten layer is deposited to a thickness of more than one nanometer, and the metal nitride layer is deposited to a thickness of more than three nanometers.

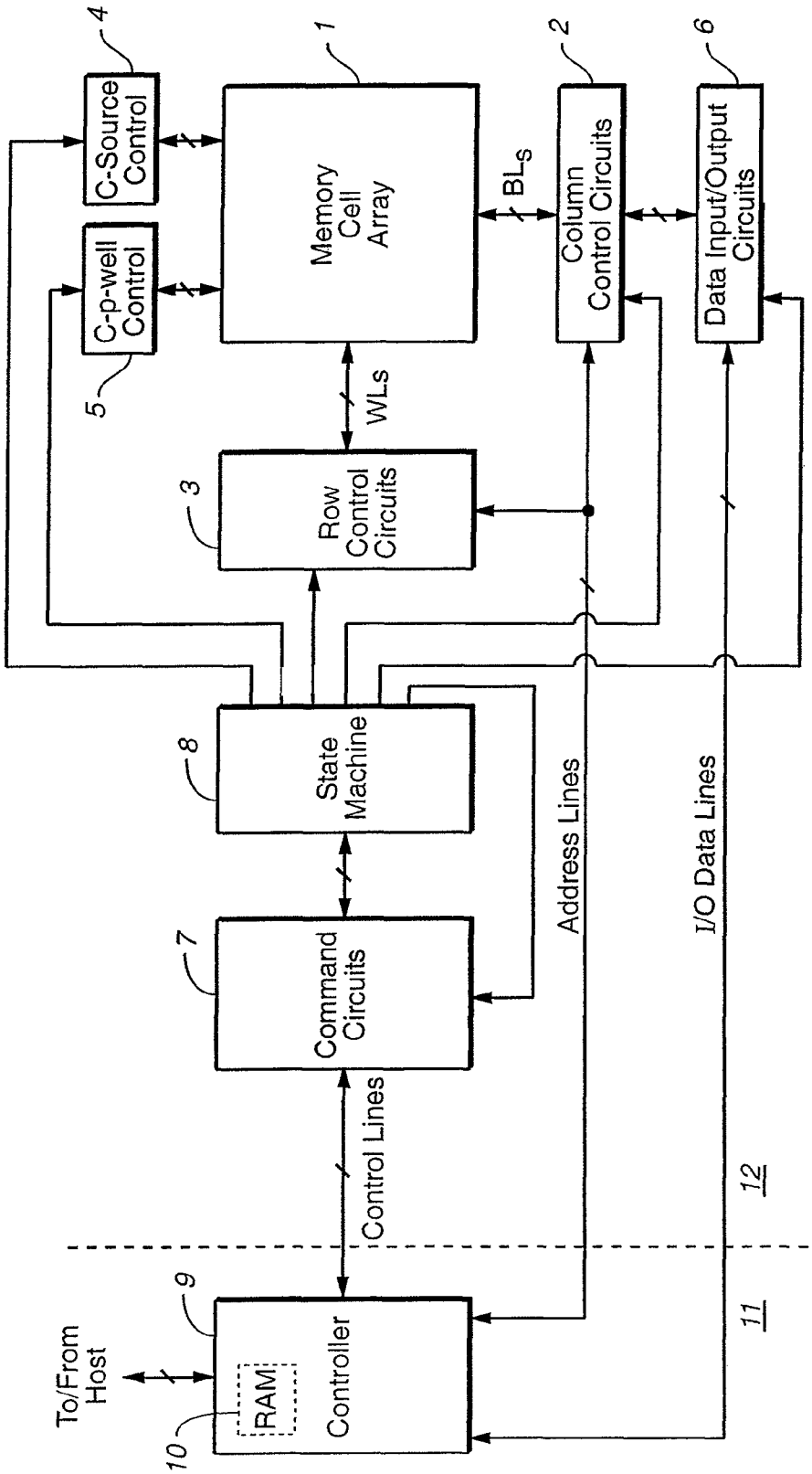

FIG._1
(Prior Art)

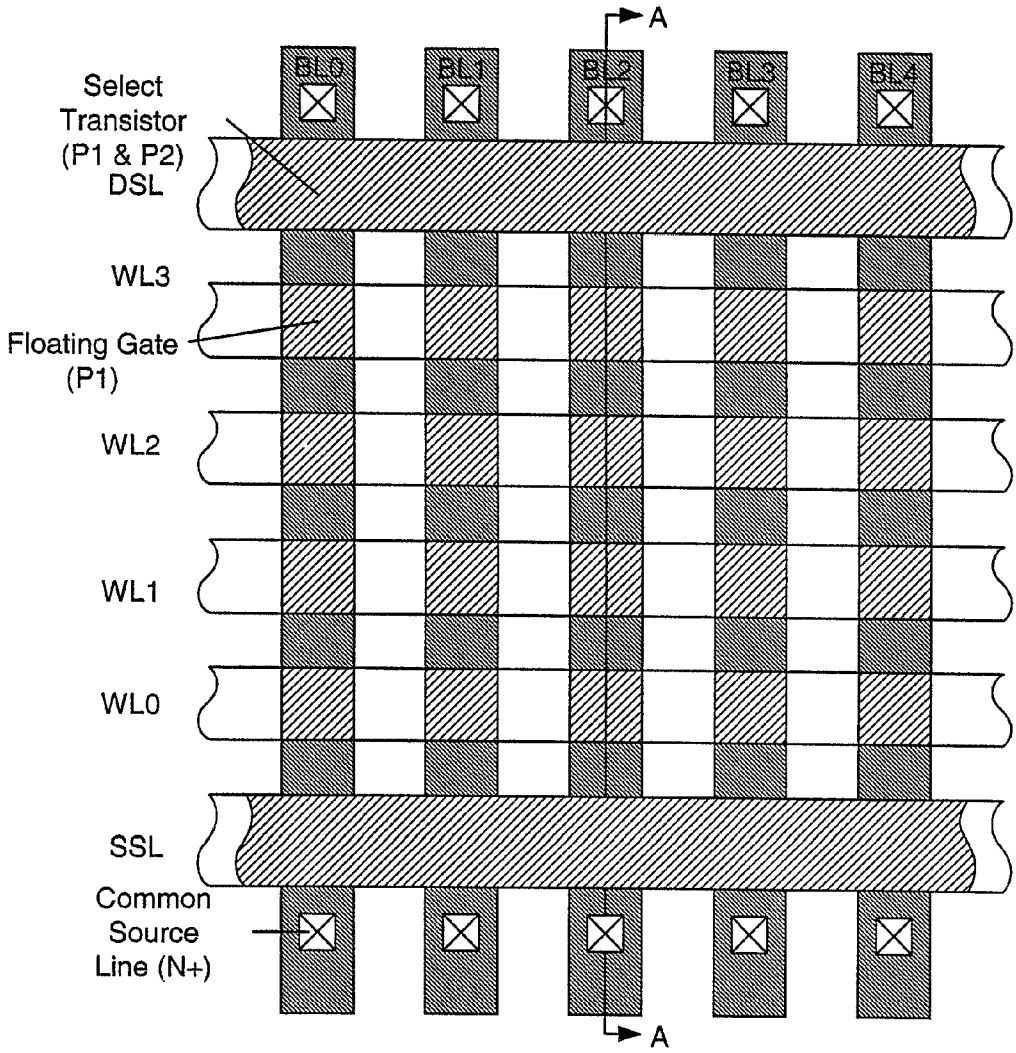

FIG._ 2A (PRIOR ART)

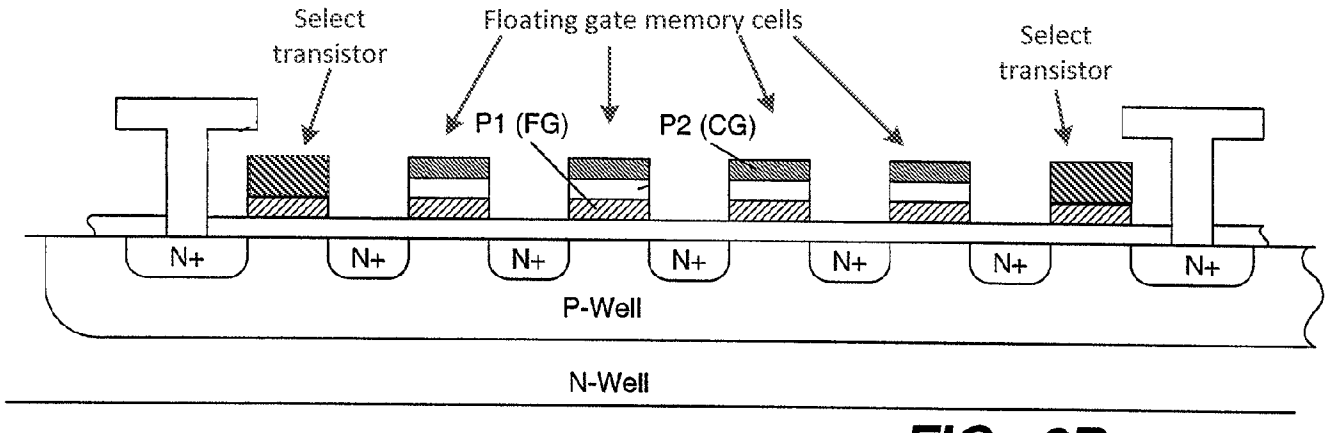

FIG._2B (PRIOR ART)
(Section A-A)

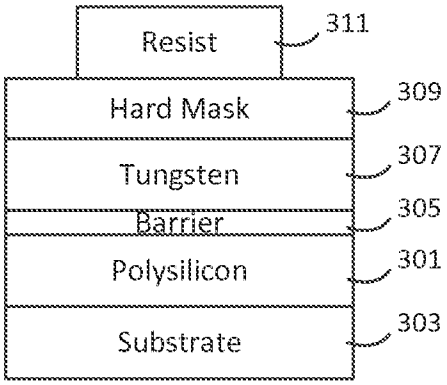

FIG. 3 (Prior art)

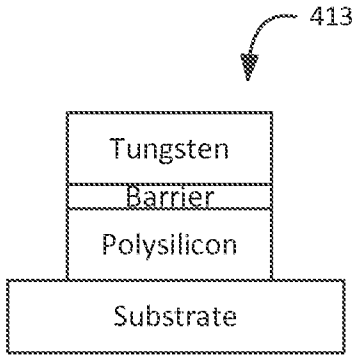

FIG. 4 (Prior art)

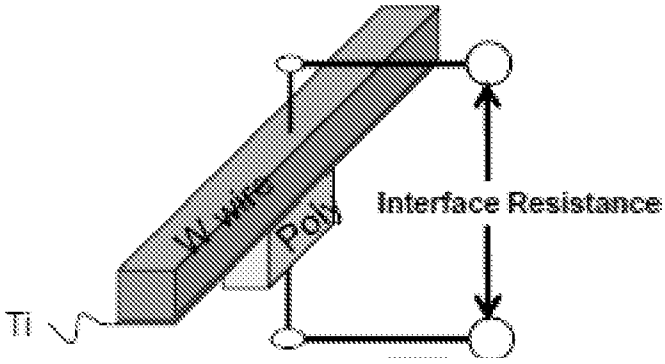

FIG. 5

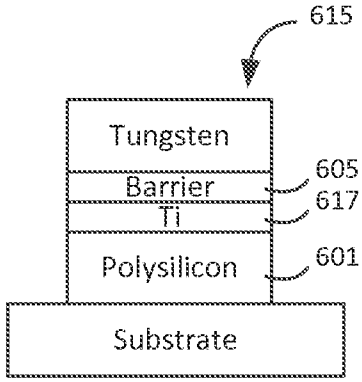

FIG. 6

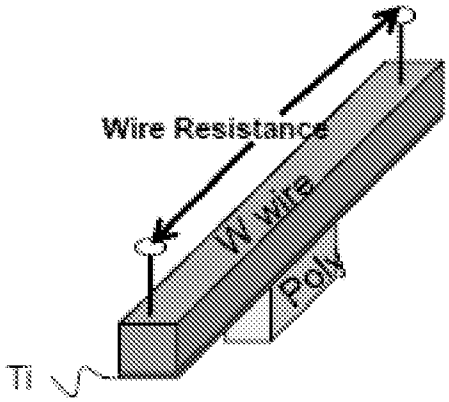

FIG. 7

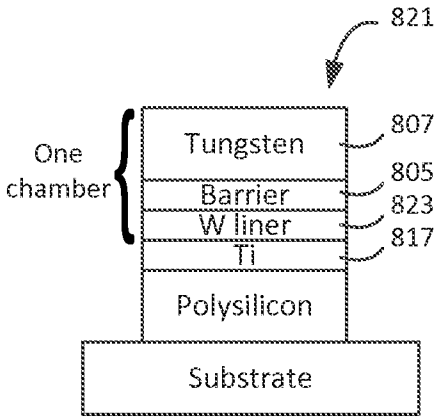

FIG. 8

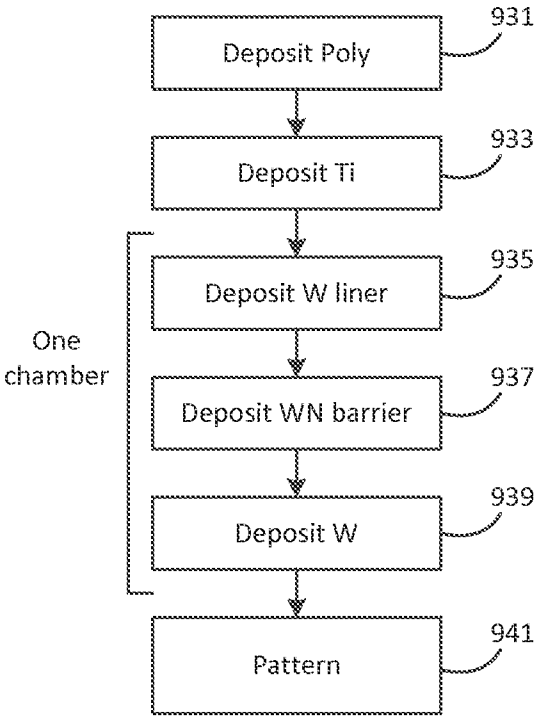

FIG. 9

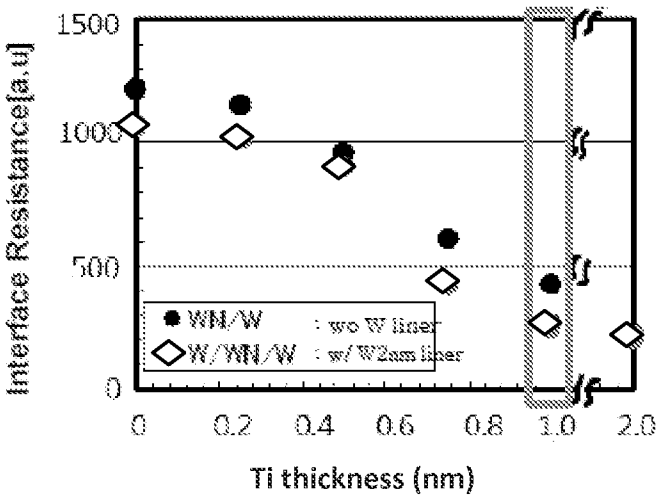

FIG. 10

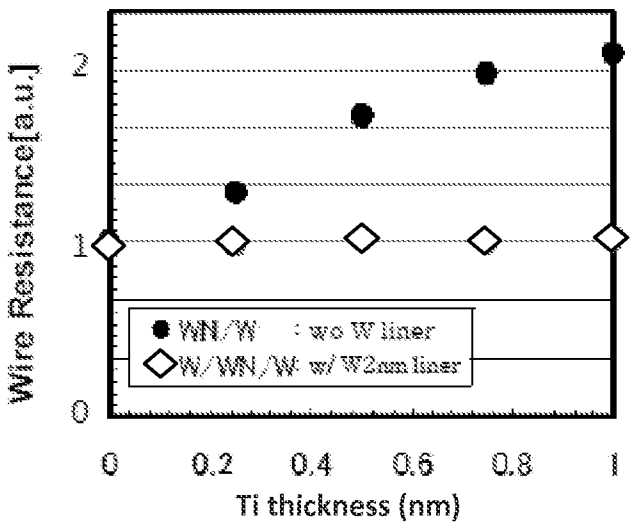

FIG. 11

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/038375

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L29/49
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2007/001246 A1 (LIM KWAN-YONG [KR] ET AL) 4 January 2007 (2007-01-04) paragraph [0028] - paragraph [0048]	1-7,13 8-12, 14-18
Y	US 6 271 590 B1 (AKRAM SALMAN [US] ET AL) 7 August 2001 (2001-08-07) column 3, line 9 - column 6, line 2	8-12, 14-18
Y	WO 2004/027824 A2 (INFINEON TECHNOLOGIES AG [DE]; IBM [US]; SCHUTZ RONALD J [DE]; ROBL WE) 1 April 2004 (2004-04-01) page 9, line 30 - page 18, line 11	8-12, 14-18

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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Date of the actual completion of the international search	Date of mailing of the international search report
5 August 2014	13/08/2014

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2014/038375

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