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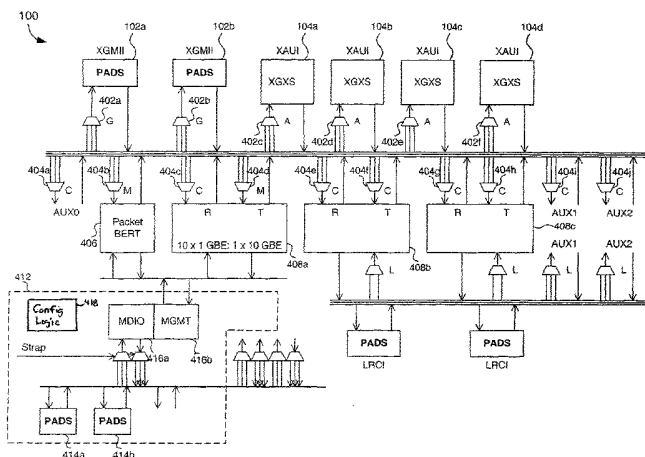
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(54) Title: A MULTI-RATE, MULTI-PORT, GIGABIT SERDES TRANSCIEVER



(57) Abstract: A multi-port Serdes transceiver (400) includes multiple parallel ports (102) and serial ports (104) and includes the flexibility to connect any one of the parallel ports to another parallel port or to a serial port, or both. Furthermore, the multi-port transceiver chip (400) can connect any one of serial ports (104) to another serial port or to one of the parallel ports (102). The substrate layout of the multi-port Serdes transceiver chip (400) is configured so that the parallel ports (102) and the serial ports (104) are on the outer perimeter of the substrate. A logic core is at the center of the substrate, where the logic core operates the serial and parallel data ports, and the bus that connects the data ports. The bus (106) can be described as a "ring" structure (or donut "structure") around the logic core, and is configured between the logic core and the data ports. The ring structure of the bus provides efficient communication between the logic core and the various data ports.

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INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER		
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B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols) U.S. : 710/20		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4,833,605 A (TERADA et al.) 23 MAY 1989, Col. 4, lines 35-36; Figs. 1 and 2; col. 5, lines 9-10; col 5, lines 15-21; col 5, lines 15-21; col 5, lines 42-49; col 6, lines 27-38	1-23
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.		
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