US 20070298526A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2007/0298526 A1**

Berry et al. (43) **Pub. Date: Dec. 27, 2007**

(54) **PROGRAMMABLE SEMICONDUCTOR DEVICE**

(76) Inventors: **Wayne S. Berry**, Essex Junction, VT (US); **John Atkinson Fifield**, Underhill, VT (US); **William H. Guthrie**, Essex Junction, VT (US); **Richard Steven Kontra**, Williston, VT (US); **William Robert Tonti**, Essex Junction, VT (US)

Correspondence Address:
IBM MICROELECTRONICS
INTELLECTUAL PROPERTY LAW
1000 RIVER STREET
972 E
ESSEX JUNCTION, VT 05452 (US)

(21) Appl. No.: **11/768,208**

(22) Filed: **Jun. 26, 2007**

Related U.S. Application Data

(63) Continuation-in-part of application No. 10/552,971, filed on Oct. 18, 2006, which is a continuation of application No. PCT/US03/13392, filed on Apr. 30, 2003.

(60) Provisional application No. 60/462,568, filed on Apr. 11, 2003.

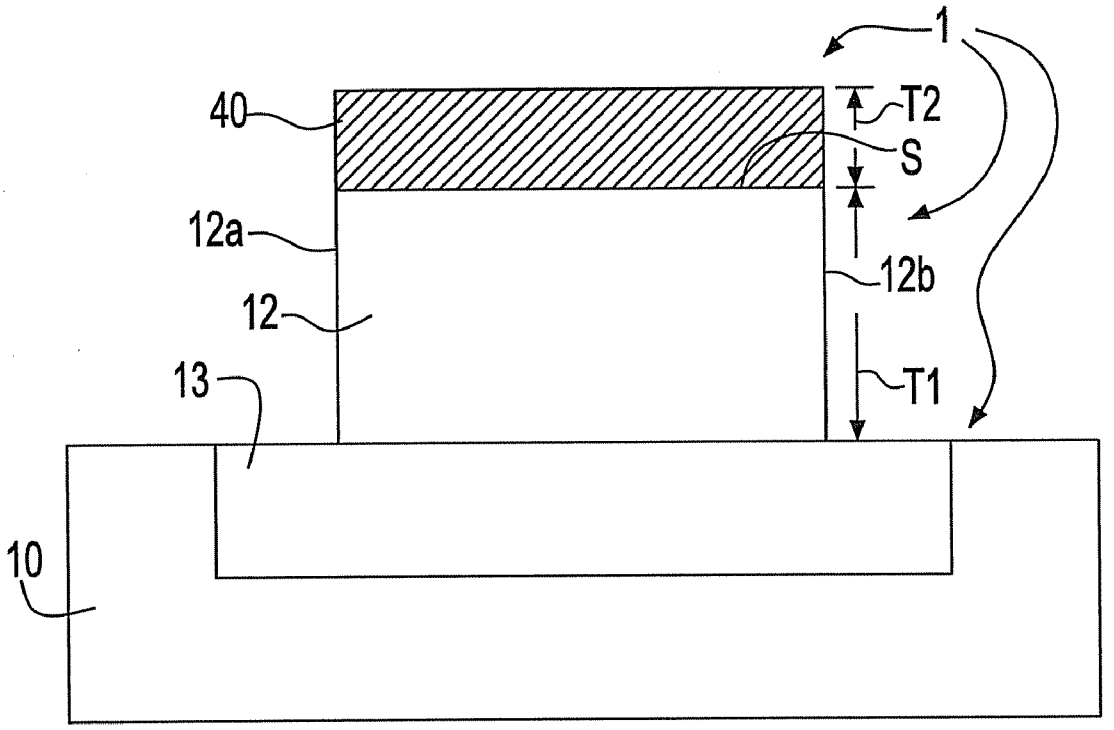
Publication Classification

(51) **Int. Cl.**
G01R 31/26 (2006.01)

(52) **U.S. Cl.** **438/14**; 257/E21

(57) **ABSTRACT**

A design structure for designing and manufacturing a programmable device. The design structure includes a substrate (**10**); an insulator (**13**) on the substrate; an elongated semiconductor material (**12**) on the insulator, the elongated semiconductor material having first and second ends, and an upper surface S; the first end (**12***a*) is substantially wider than the second end (**12***b*), and a metallic material is disposed on the upper surface; the metallic material being physically migratable along the upper surface responsive to an electrical current I flowable through the semiconductor material and the metallic material.



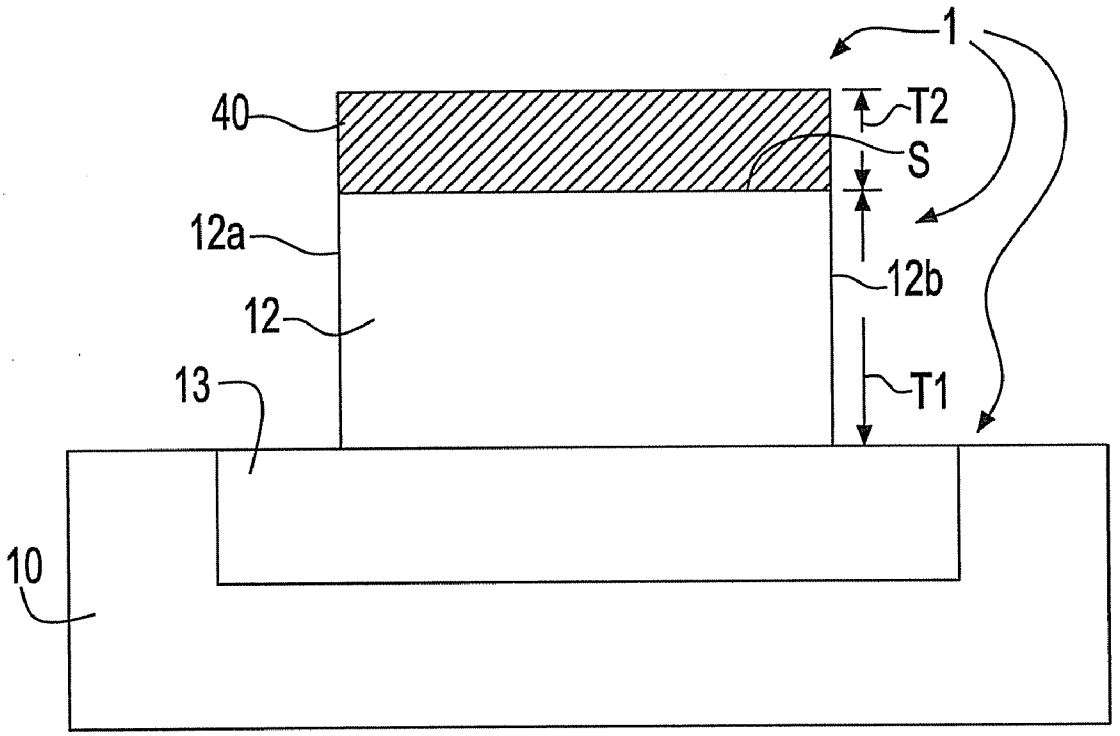


FIG. 1

FIG. 2

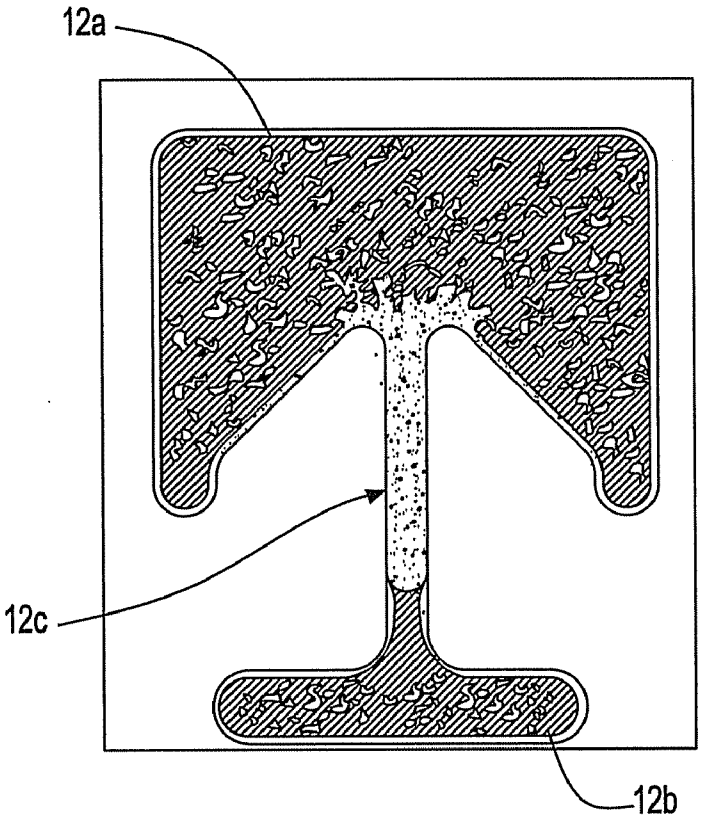
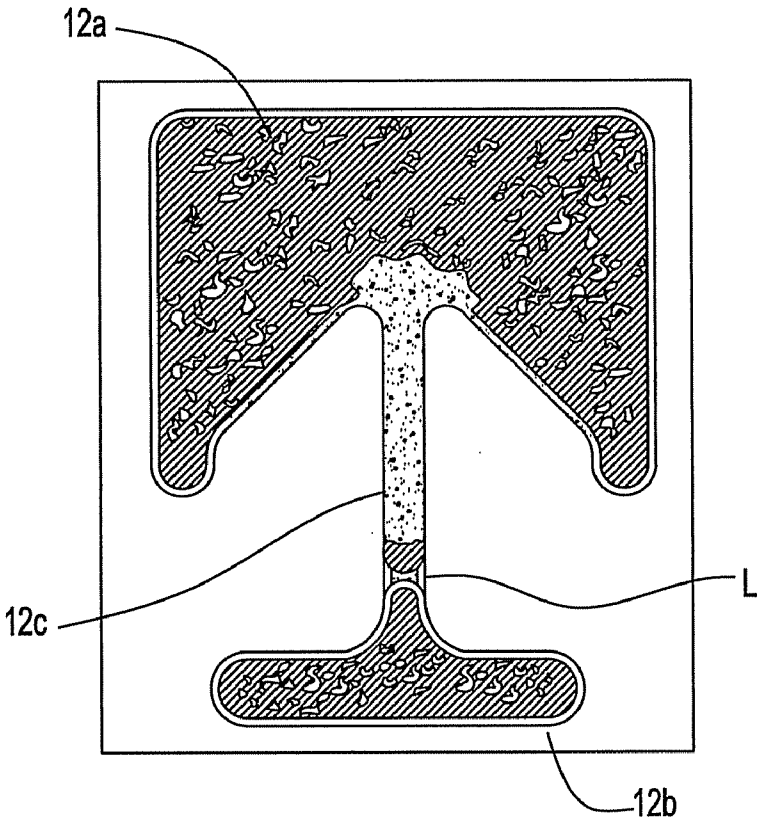


FIG. 3



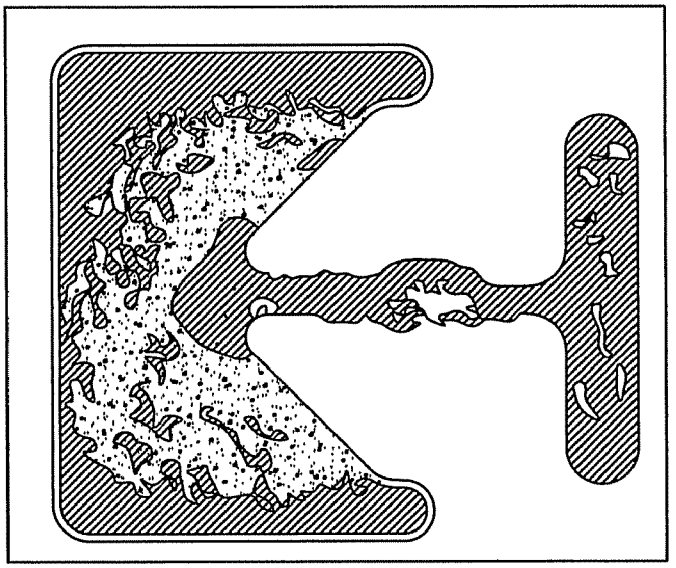


FIG. 4c

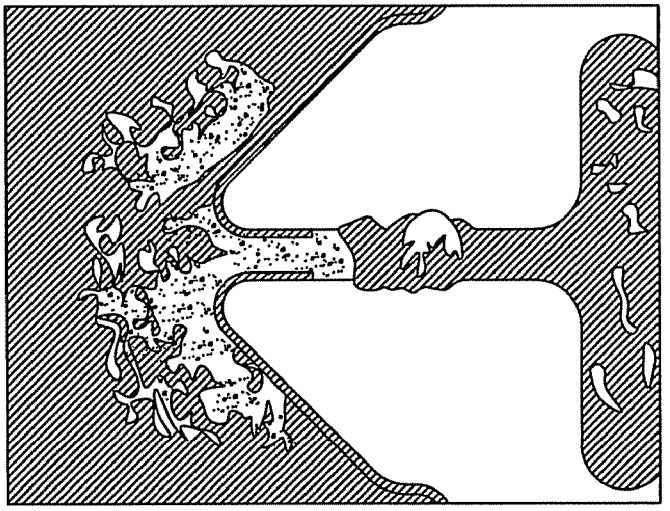


FIG. 4b

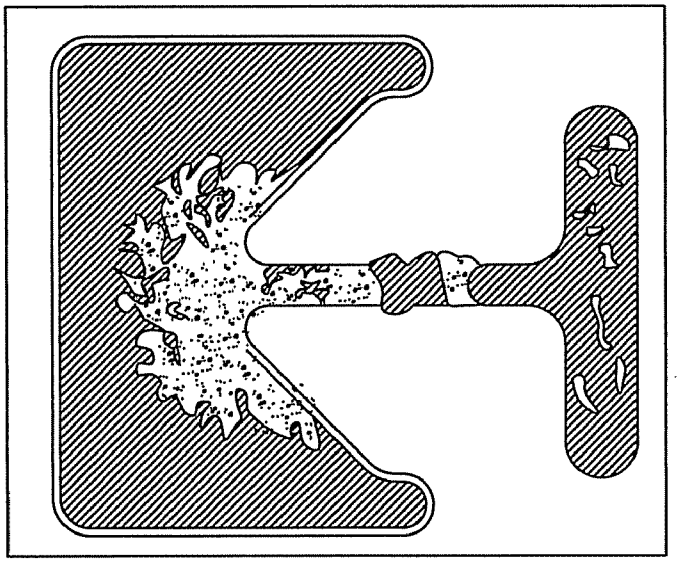


FIG. 4a

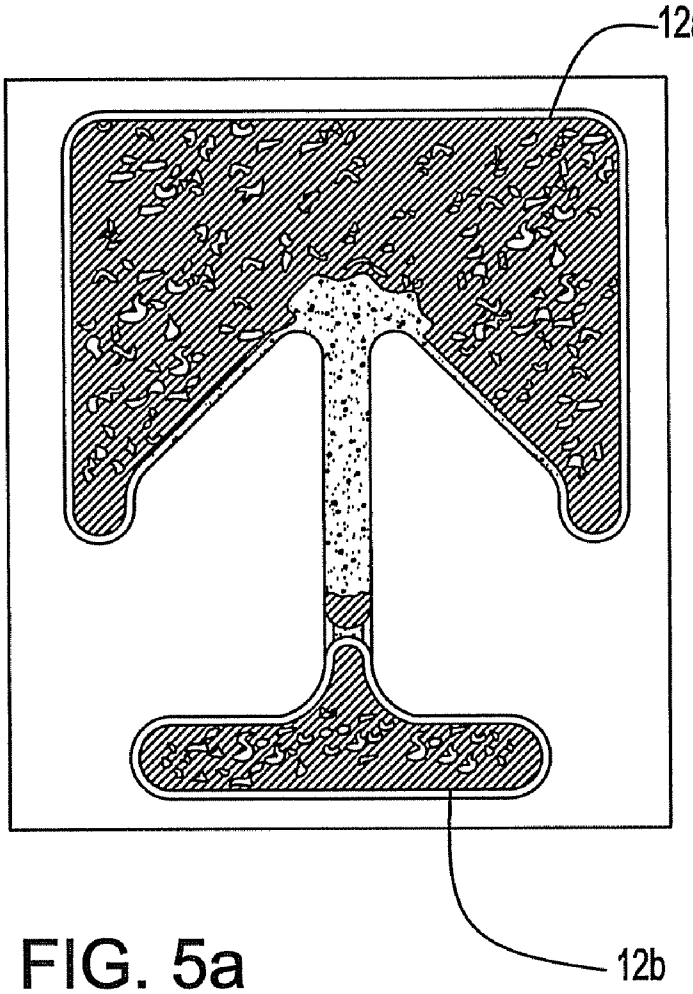


FIG. 5a

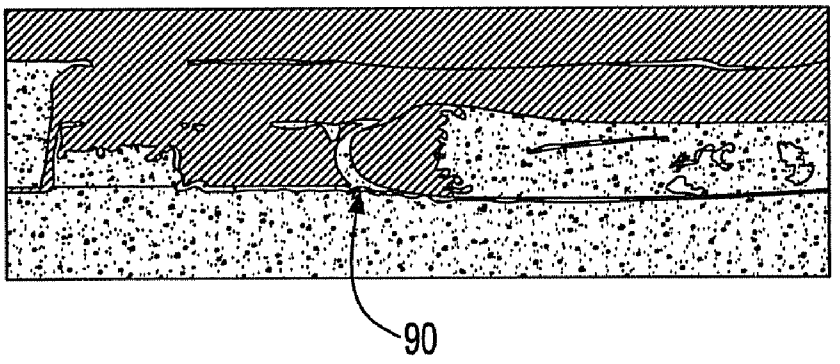


FIG. 5b

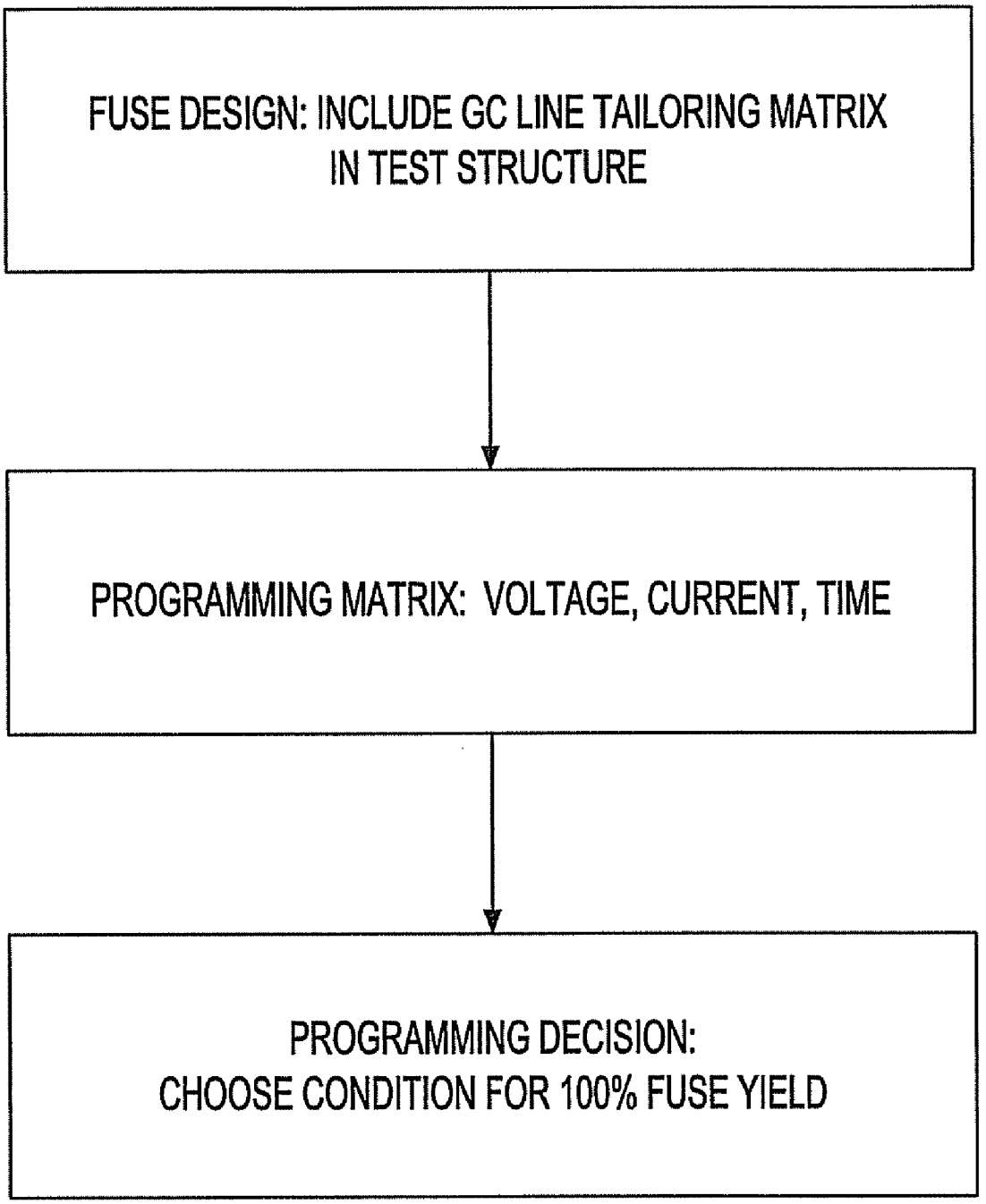

FUSE DESIGN: INCLUDE GC LINE TAILORING MATRIX IN TEST STRUCTURE
PROGRAMMING MATRIX: VOLTAGE, CURRENT, TIME
PROGRAMMING DECISION: CHOOSE CONDITION FOR 100% FUSE YIELD

FIG. 6

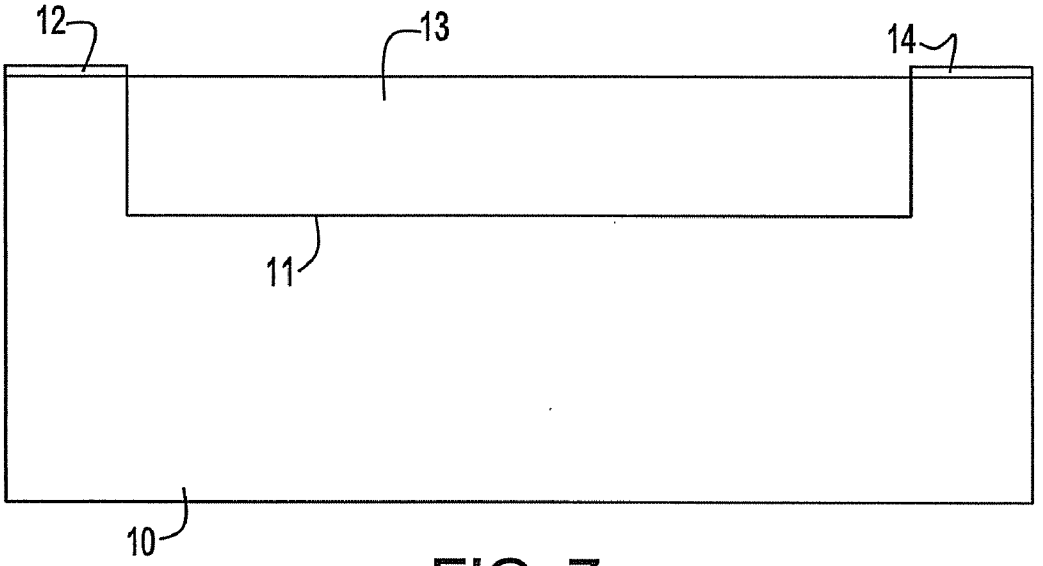


FIG. 7

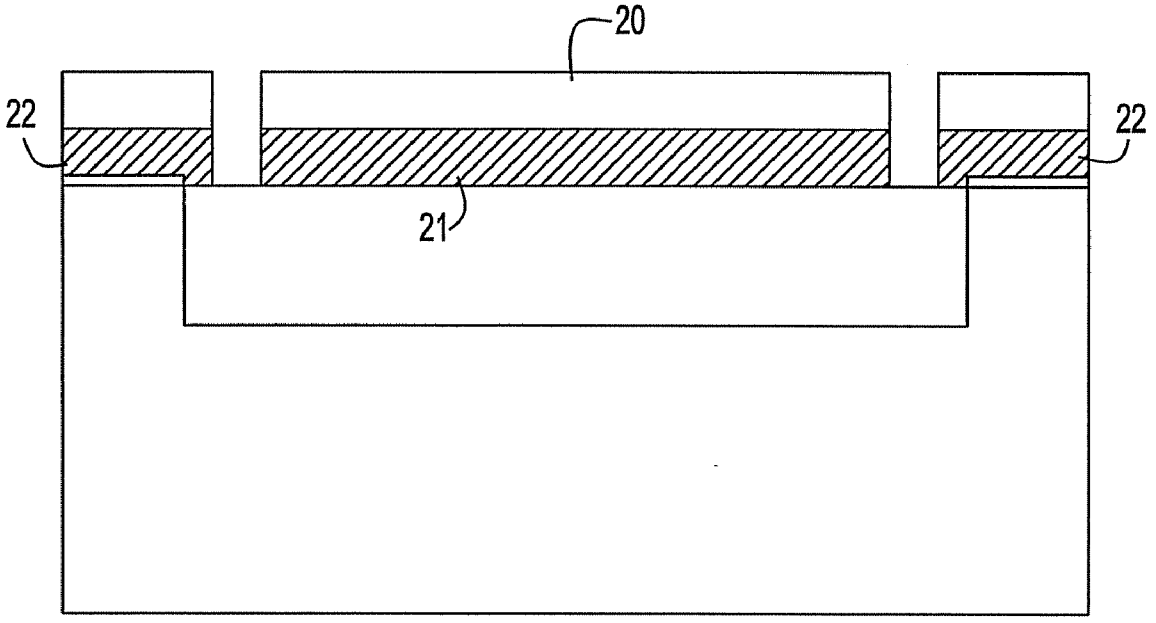


FIG. 8

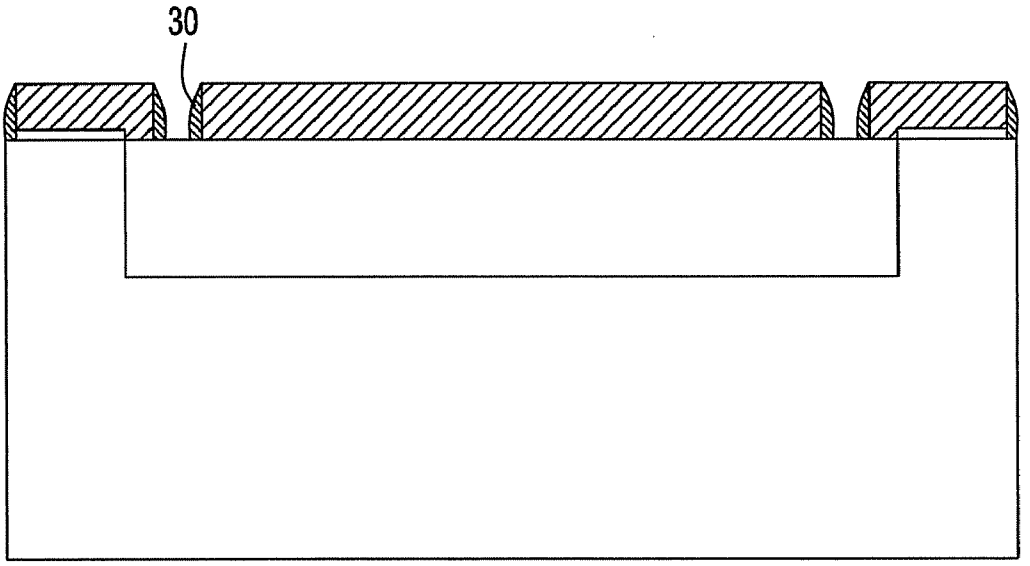


FIG. 9

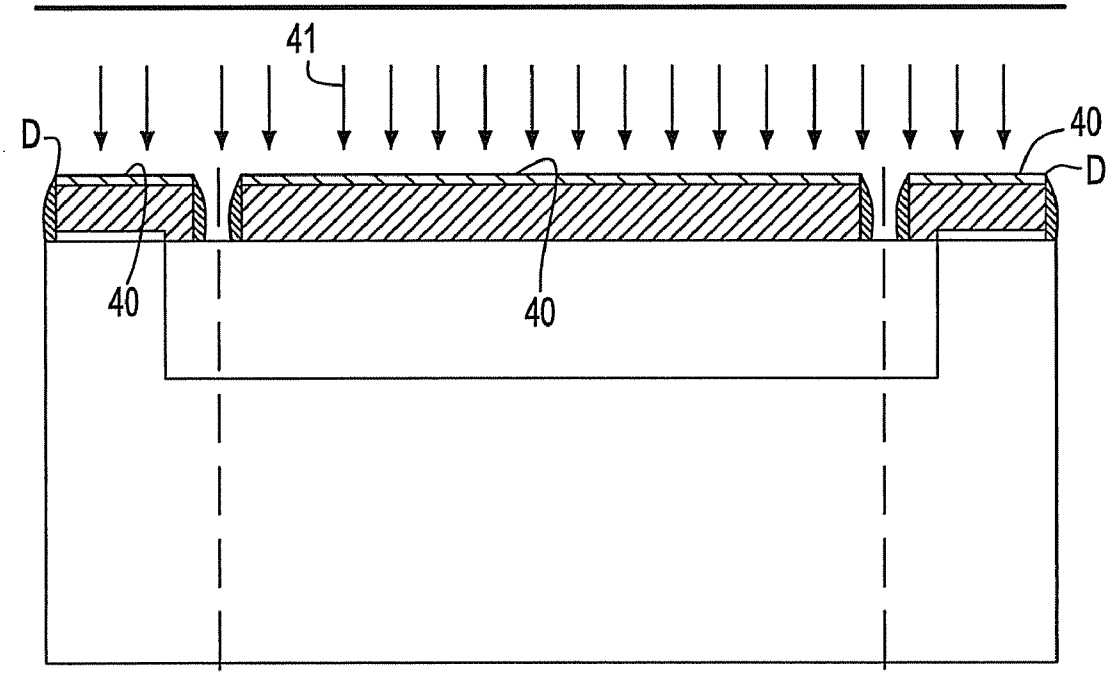


FIG. 10

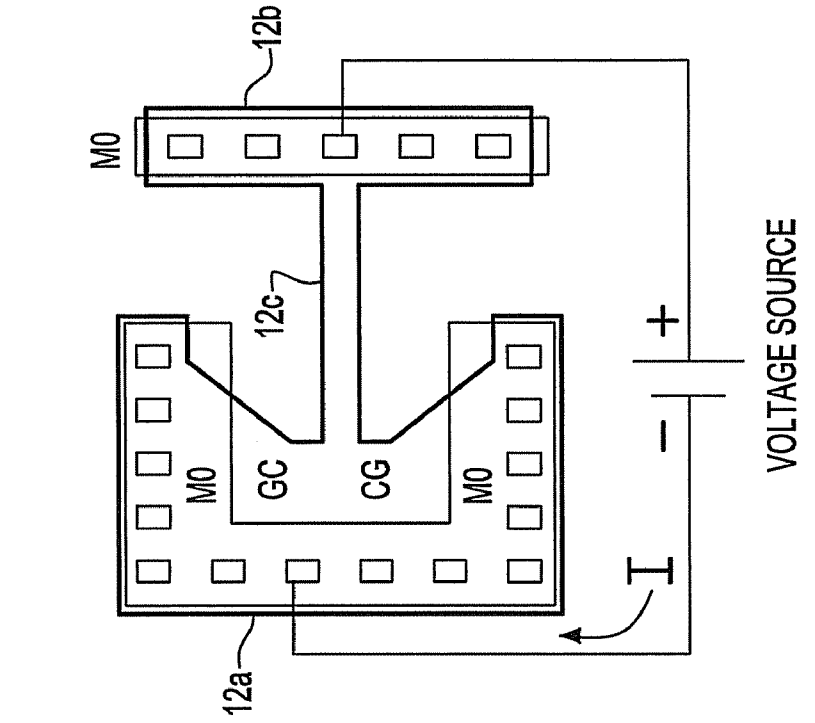


FIG. 11b

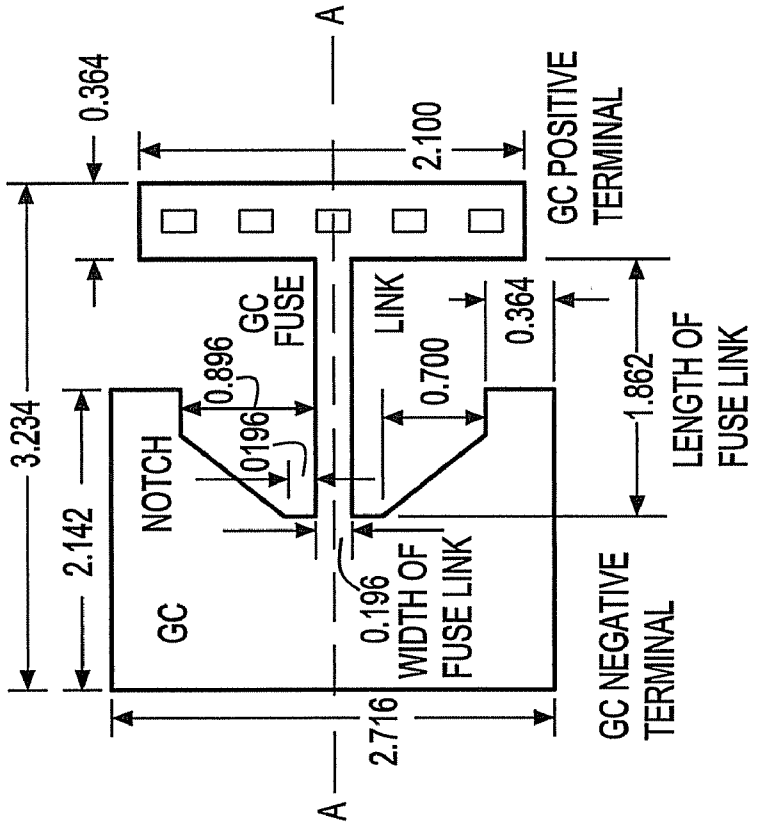


FIG. 11a

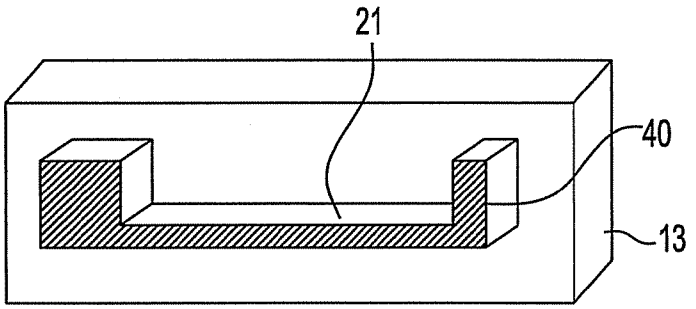


FIG. 12

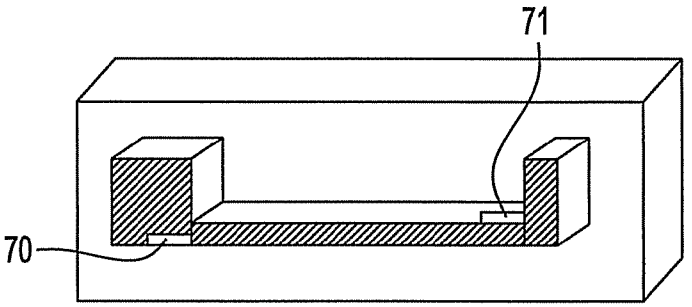


FIG. 13

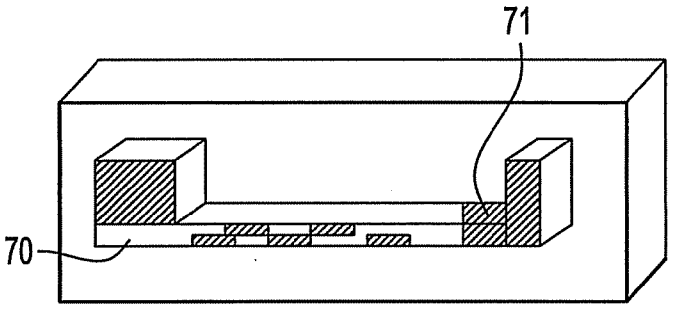


FIG. 14

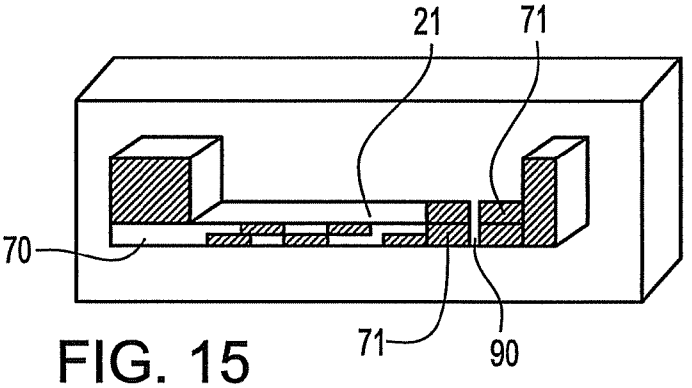


FIG. 15

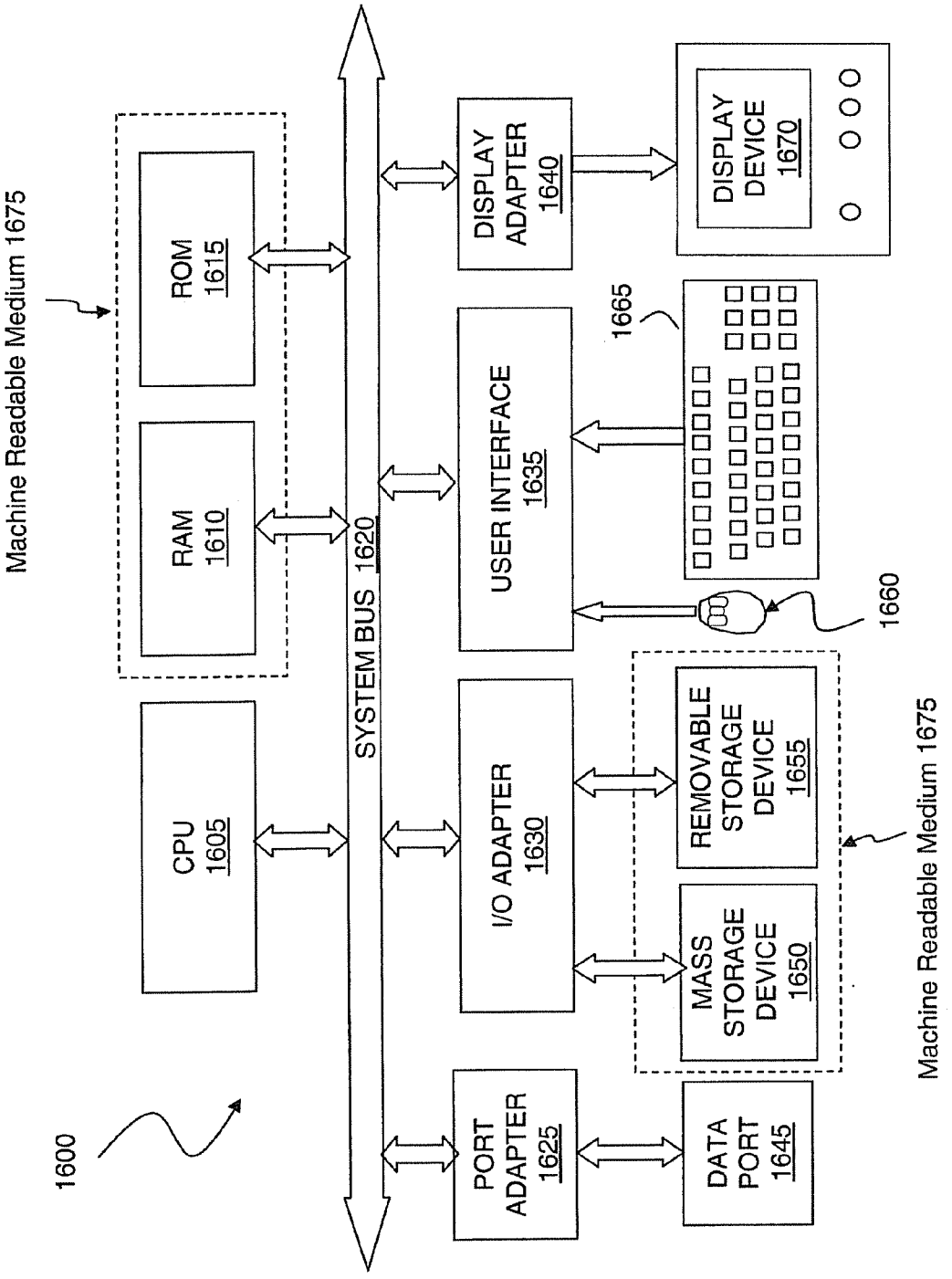

1600
CPU 1605
ROM 1615
RAM 1610
Machine Readable Medium 1675
SYSTEM BUS 1620
PORT ADAPTER 1625
I/O ADAPTER 1630
USER INTERFACE 1635
DISPLAY ADAPTER 1640
DATA PORT 1645
MASS STORAGE DEVICE 1650
REMOVABLE STORAGE DEVICE 1655
1660
1665
DISPLAY DEVICE 1670
Machine Readable Medium 1675

Fig. 16

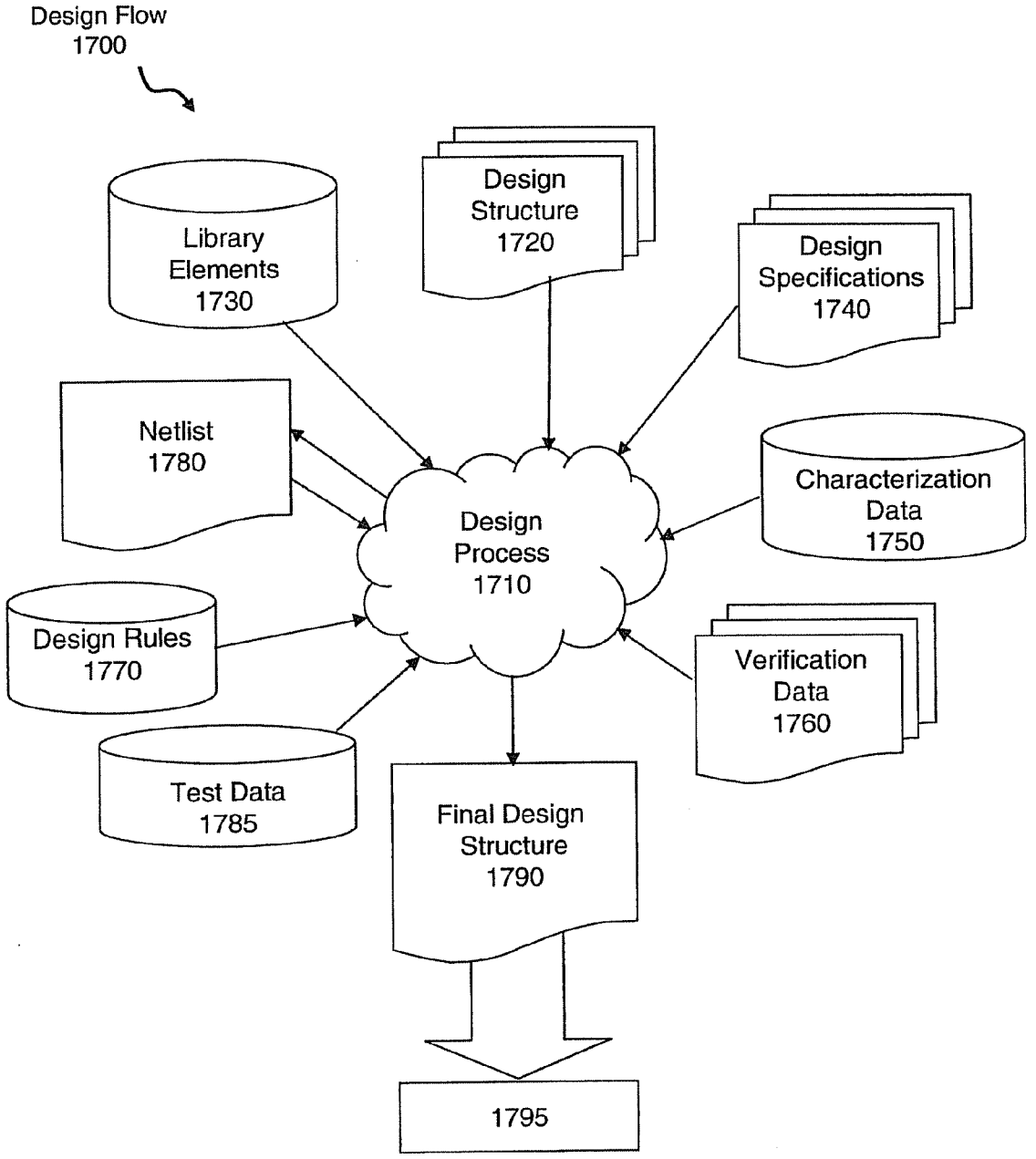

Design Flow
1700
Library
Elements
1730
Design
Structure
1720
Design
Specifications
1740
Netlist
1780
Characterization
Data
1750
Design
Process
1710
Design Rules
1770
Verification
Data
1760
Test Data
1785
Final Design
Structure
1790
1795

Fig. 17

PROGRAMMABLE SEMICONDUCTOR DEVICE

CROSS REFERENCE TO RELATED APPLICATION

[0001] This application is a continuation in part of pending U.S. application Ser. No. 10/552,971 filed Oct. 11, 2005, which is a continuation of PCT application serial no. PCT/U503/13392 filed 30 Apr. 2003, which claims priority of provisional application Ser. No. 60/462,568, filed 11 Apr. 2003; all assigned to the present assignee.

TECHNICAL FIELD

[0002] The present invention relates to programmable semiconductor devices and, more particularly, to design structures which comprise such devices usable as semiconductor electronic (E) fuses.

BACKGROUND

[0003] Semiconductor E-fuses in general are known. See, for example, U.S. Pat. No. 5,334,880, Low Voltage Programmable Storage Element, issued Aug. 2, 1994, by Abadeer et al., which is incorporated herein in its entirety.

[0004] However, known semiconductor E-fuses have not proven to be entirely satisfactory. Programming in silicon-based semiconductor devices (e.g., fuses) can result in post collateral damage of the neighboring structures. This result typically forces a fuse pitch, or fuse cavity, set of rules that do not scale well with the technology feature rules from one generation to the next. Thus, fuse density and effectiveness of fuse repair, replacement, or customization are limited. Typically, such damage is caused by particulates from fuse blow. In addition, standard electrical programming of a conductive fuse is to change its resistance, either from an unprogrammed state having a low resistance to a programmed state having a high resistance, or from an unprogrammed state having a high resistance to a programmed state having a low resistance. See, for example, U.S. Pat. No. 5,334,880. Such fuses contain an initial resistance, $R0 \pm \Delta R0$, and a programmed resistance, $Rp \pm \Delta Rp$. It is the $\pm \Delta Rp$ that causes fuse read instability because this parameter is statistical in nature. The variations that cause the R0 and Rp distributions to approach each other cause practical limitations in interrogating a programmed fuse through a standard CMOS latching circuit. To overcome these limitations, the prior art has included additional fuses as reference elements in order to discriminate between a programmed and unprogrammed fuse. Such practices result in unwanted growth in the fuse bank area.

SUMMARY OF THE INVENTION

[0005] The present invention overcomes this and other drawbacks by employing a device or fuse structure of a composite material that migrates during a programming event. The material that migrates (e.g., WSi_2) changes state, and does not cause collateral damage during its migration or material reformation, and has a programmed state where $\pm \Delta Rp$ is preferably equal to zero. This allows for individual fuses to discriminate among themselves and to eliminate unwanted reference fuse elements, as well as the circuitry used to bias and compare against the reference fuse elements.

[0006] According to the invention, a programmable device includes a substrate (**10**); an insulator (**13**) on the substrate; an elongated semiconductor material (**12**) on the insulator, the elongated semiconductor material having first and second ends, and an upper surface S; the first end (**12***a*) being substantially wider than the second end (**12***b*), and a metallic material (**40**) on the upper surface, said metallic material being physically migratable along the upper surfaces responsive to an electrical current I flowable through the elongated semiconductor material and the metallic material.

[0007] A method of programming a device includes flowing an electrical current I through a device having a semiconductor alloy (**40**) disposed on a doped semiconductor line (**12**), for a time period such that a portion of the semiconductor alloy migrates from a first end (**12***a*) of the device to a location L proximate to a second end (**12***b*) of the device.

[0008] A method of fabricating a programmed semiconductor device, includes providing a semiconductor substrate (**10**) having a thermal insulator (**13**); disposing an elongated semiconductor material (**12**) on the insulator, the semiconductor material having an upper surface S, a first resistivity, and two ends; disposing a metallic material (**40**) on the upper surface; the metallic material having a second resistivity much less than the first resistivity of the semiconductor material; flowing an electrical current I through the semiconductor material (**12**) and the metallic material (**40**) for a time period such that a portion of the metallic material migrates from one end (**12***a*) of the semiconductor material to the other end (**12***b*) and melts the semiconductor material to form an open circuit (**90**).

[0009] It is a principal object of the present invention to provide a programmable semiconductor device which does not cause collateral damage to adjacent devices or other elements during programming.

[0010] It is a further object of the present invention to provide a method of fabricating a programmable semiconductor device, which method is readily compatible with various standard MOS manufacturing processes.

[0011] It is an additional object of the present invention to provide a method of programming a programmable semiconductor device which reduces collateral damages to neighboring structures.

[0012] Further and still other objects of the present invention will become more readily apparent when the following detailed description is taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF DRAWINGS

[0013] FIG. **1** is a side schematic view of a programmable semiconductor device according to one embodiment of the present invention.

[0014] FIGS. **2-4** show top plan view photographs of devices according to the present invention when incompletely programmed (FIG. **2**), completely programmed (FIG. **3**) and overprogrammed (FIGS. **4***a*, **4***b*, **4***c*).

[0015] FIG. **5***a* shows a top plan view photograph and FIG. **5***b* a side sectional view photograph of a completely programmed device according to the invention.

[0016] FIG. **6** is a flow diagram of major steps to calibrate parameters for programming a device (**1**) of the invention.

[0017] FIGS. **7-10** show preferred salient process steps for fabricating an unprogrammed device according to the invention.

[0018] FIG. **11** a shows a top plan schematic views of the preferred embodiment of the device (**1**) according to the invention, and FIG. **11***b* shows the device (**1**) connected to an energy source for programming.

[0019] FIGS. **12-15** are top schematic cross-sectional conceptual views into the direction of line AA, but rotated approximately 90° for easier explanation.

[0020] FIG. **16** shows an example of a general-purpose computer system and machine readable medium for practicing the present invention.

[0021] FIG. **17** shows an example design flow process of instantiating a design structure comprising an embodiment of the present invention into an IC design to create a final design structure.

DETAILED DESCRIPTION OF THE INVENTION

[0022] FIG. **1** shows a preferred programmable (un-programmed) semiconductor device (**1**) (e.g. fuse) in cross section. The fuse (**1**) includes an elongated semiconductor material (**12**) having a metallic material (**40**) disposed on an upper surface S. The material (**12**) is disposed on/over an isolation region (**13**) in a silicon substrate (**10**). Preferably, the unprogrammed fuse includes N+ polysilicon (90 nm height/thickness T**1**) (**12**) and WSi_2 (55 nm height/thickness T**2**) (**40**). The region (**13**) is, for example, filled with an insulator such as an oxide. The region (**13**) is, for example, a known shallow trench isolation (STI) region. The device (**1**) includes a first end (**12***a*), a second end (**12***b*) and a central portion or link (**12***c*) connecting the first end (**12***a*) to the second end (**12***b*). Preferably, the link (**12***c*) and the second end (**12***b*), together, form a "T"-shaped member (FIG. **2**, and FIGS. **11***a*, **11***b*).

[0023] According to an important feature of the present invention, the resistivity of the metallic material (**40**) is much less than the resistivity of the semiconductor line (**12**). Preferably, the resistivity of the material (**40**) is in a range of approximately (±10%) 15 ohms per square to approximately 30 ohms per square, while the resistivity of the line (**12**) is in a range of approximately 100 ohms per square to approximately 200 ohms per square.

[0024] Preferably, the resistivity of the material (**40**) and the line (**12**) combined is approximately 17 ohms per square to approximately 25 ohms per square.

[0025] During programming, i.e., under suitable current, voltage and time conditions, the material (**40**) migrates from the first end (**12***a*) and the link (**12***c*), to a location "L" proximate to the second end (**12***b*), to accumulate and ultimately heat and melt the semiconductor material (**21**) at the location "L" to form an open circuit (**90**) (see FIG. **15**) within or at the location "L".

[0026] FIGS. **2** through **4** show an initial calibration used in determining the programming current and time required to rule out wafer level process variations when establishing the initial programming conditions. FIG. **2** shows an incomplete programming using 4.5V, 5 mA for 25 μS. FIG. **3** shows a typical preferred complete programming event at 4.5V, 5 mA for 250 μS. An open circuit (**90**) was formed at a location L proximate to the second end (**12***b*). The programming window was found to be compliant between 150 μS and 350 μS for this given technology. It was further determined that the fuse power and time scale with the technology feature, affording an electrical fuse that is reusable at nano scale technology nodes. FIGS. **4***a, b* and *c* indicate various results of overprogramming, and the effect of tungsten available volume.

[0027] These FIGS. **4***a, b, c* show the over programming at 4.7V, 5 mA from 1 mS, 2 S, 4 S. The tungsten silicide (**40**) continues to migrate until it is depleted. The polysilicon line (**12**) still melts at the hottest spot, similar to FIG. **3**, but in the case of overprogramming the tungsten silicide (**40**) forms a bridge over the program location, as well as causing stress and damage in the nearby isolation trench. Although the line resistivity has significantly changed due to the migration of the tungsten silicide, and the inventors believe also the dopant, this is not considered a realizable fuse. However, this places a design guideline for a volume of the fuse metallic silicide as compared to a volume of the fuse neck at the programming location to avoid this overprogramming situation. This guideline can be used to size the area of the migrating terminal pad so as to eliminate the condition of excess metallic silicide. These conditions are technology dependent, and can be established at the onset of technology manufacturing. This implies a fuse test and evaluation process flow is an additional feature of this invention. The process flow is self-explanatory and is shown in FIG. **6**.

[0028] FIGS. **5***a* and **5***b* show the result of program calibration on a random E-fuse of the invention. Programming occurs as a three stage event. Initially, as a current I is passed from the cathode to the anode terminals, the WSi_2 (**40**) migrates between the two terminals, and is heated to approximately (±10%) 2160° C. The local heating of the underlying polysilicon line (**12** or **21**) from the WSi_2 (**40**) and the subsequent opening (**90**) of the WSi_2 shunted path to the N+ polysilicon only path results in the N+ polysilicon line opening (**90**) as shown in FIG. **5***b* and FIG. **15**. Subsequent analysis of the E-fuse structure indicated the WSi_2 as designed transformed into pure W, and all material was conserved. Also, collateral damage is eliminated. The open circuit as shown in FIGS. **5***a* and **5***b* provides the correlated feedback required in the calibration programming previously described. It is important to have a shunted N+ polysilicon migratable fuse for two reasons: it allows for low current uniform heating of the entire polysilicon line, without the requirement of large programming devices; and the migration of a hot refractory metal assists in the final link opening and programming, without causing debris surrounding the fuse that might cause subsequent reliability failure.

[0029] For the preferred fuse dimensions referenced in FIG. **11***a*, the optimum fuse programming cycle is: Voltage Source=4.5V, I=5 mA, Time=250 μS±100 μS. The heating of the metallic silicide (**40**) is approximately (±10%) 2160 degrees C. Under an electron wind, the metallic silicide (**40**) migrates as depicted in the following FIGS. (**12-15**), resulting in the final fuse programming, i.e., the opening of polysilicon line (**21**) as physically shown in FIG. **15**. Noth-

ing happens to the surrounding isolation oxide (**13**). Locations **70**, **71** represent the proposed physical model of the redistribution of the metallic silicide (**40**) while it is heated and migrated by the voltage source (FIG. **11**) and current flow I.

[**0030**] GC=polysilicon,

[**0031**] CG=electrical contact to the polysilicon,

[**0032**] M0=metal zero (first metal to pad connections), and

[**0033**] Notch (optional)=notch in polysilicon pad.

[**0034**] FIGS. **7-10** show preferred process steps for fabricating the preferred embodiment of the fuse shown in FIG. **1**.

[**0035**] The process of fabricating the fuse of FIG. **1** will be well understood by those skilled in the art in view of the instant disclosure.

[**0036**] As shown in FIG. **7**, provide a substrate (**10**) which is bulk silicon, silicon-on-insulator or any other suitable substrate. Mask and etch shallow trench isolation region (**11**) (STI), fill trench (**11**) with an oxide (**13**), planarize (e.g., CMP) to a top silicon surface (**14**), grow gate oxide (**12**) for proposed active devices D which typically would be formed with the fuse (**1**). Devices D are, for example, MOS devices such as FETs.

[**0037**] In FIG. **8**, dispose (e.g., deposit) polysilicon (**22**, **21**) (doped N or P, or undoped). Pattern with a photoresist mask (**20**), etch and define active (**22**) and fuse (**21**) regions. See, for example, U.S. Pat. Nos. 4,229,502 and 4,309,224, which are incorporated herein by reference in their entireties.

[**0038**] In FIG. **9**, form sidewall spacers (**30**) with a conventional dielectric material.

[**0039**] In FIG. **10**, suitably implant (**41**) into proposed FETs D and into the polysilicon (**21**)—if not in-situ doped polysilicon. Form metallic silicide region (**40**) by conventional techniques such as deposition (thermal evaporation of WSi_2, sputter deposition, etc.). The metallic silicide (**40**) preferably is WSi_2, but can be $CoSi_2$, $TiSi_2$, $NiSi_2$, NiSi, PtSi, $PtSi_2$ and others with like electrical and thermal properties. The fuse region is shown between the vertical dashed lines of FIG. **10**. Suitable annealing steps can also be performed, and the spacers can be removed. See, for example, the book *VLSI Technology*, by Sze et al., (1988, 2nd edition, McGraw Hill) for discussions of various process steps, which book is hereby incorporated by reference.

[**0040**] FIG. **11** shows top views of the fuse, showing the fuse link width equal to 0.196 μm, and a fuse link (central portion) length of 1.862 μm. Of course, fuse link widths can be <<0.2 μm, i.e., 1 μm and below. It is important that all of the poly (**12**, **21**) sits over the isolation (**13**), such that a thermal path is directed towards heating the metallic silicide (**40**) during a programming event. Metallic silicide is migrated from the huge negative terminal source and flows to the positive source via an electron wind. The positive source area must be <<than the negative source area to allow the silicide to recrystallize within the underlying poly, and to heat the poly uniformly at the recrystalline point L so as to break (**90**) the line (**12**, **21**) through heating.

[**0041**] FIGS. **12-15** show top schematic conceptual views useful for understanding the programming process of the present invention. The silicide (**40**) is driven from the negative terminal and piles up at the positive terminal where the polysilicon is heated and subsequently forms an open circuit, where $\Delta Rp=0$. A cross section shows the recrystallization of the silicide near (proximate) the point of programming versus the original "skin" silicide layer (**40**) over the negative terminal. No damage of the surrounding oxide is evident. It is an important criterion that the resistivity of the metallic silicide (**40**) be <<than that of the underlying polysilicon (**12**, **21**). The materials described as examples meet this criterion.

[**0042**] Any metallic silicide ($NiSi_2$, $CoSi_2$ as examples) will react in the same manner as the tungsten silicide cladding layer we describe; i.e., we can drive a silicide along/down the line and force it to melt/annihilate the polysilicon layer (**12**, **21**) underneath it due to the increased temperature of the "piled" metallic layer (**71**).

[**0043**] FIG. **12** shows a top view in cross section through the fuse prior to programming, showing isolation oxide (**13**), doped polysilicon (**21**), and homogeneous silicide layer (**40**) as formed.

[**0044**] As shown in FIG. **13**, during programming, current I is driven through the fuse at a given voltage V. Current conducts primarily through the low resistance silicide layer, and the electron wind produced by the current migrates the silicide (**40**) towards the end of the link as shown by the absence of the silicide on one end of the line (**70**) and the buildup of the silicide at the far end of the line (**71**). The total volume of silicide is conserved within the line. Silicide continues to react with the polysilicon at the end of the line.

[**0045**] FIG. **14** shows, just prior to final programming, the migrated silicide (**71**) that consumes the entire end of the polysilicon line where the surrounding polysilicon is heated beyond its respective melting point. Current continues to flow, and silicide continues to migrate.

[**0046**] In FIG. **15**, programming is accomplished by removing the applied voltage and current, and the fuse link polysilicon (**12**, **12***c*) is pulled back into the migrated silicide (**71**), forming, in effect, an electrical open circuit (**90**).

[**0047**] To summarize: a low resistance layer (**40**) directly in contact, or chemically reacted with, a polysilicon layer (**21**) under a current I drive cathode to anode is used subsequently to melt a polysilicon line (**21**) at a location (**90**) and, thus, form/program a permanent antifuse.

[**0048**] FIG. **16** illustrates a block diagram of a general-purpose computer system which can be used to implement the system and method described herein. The system and method may be coded as a set of instructions on removable or hard media for use by general-purpose computer. FIG. **16** is a schematic block diagram of a general-purpose computer for practicing the present invention and includes computer system **1600**, which has at least one microprocessor or central processing unit (CPU) **1605**. CPU **1605** is interconnected via a system bus **1620** to machine readable media **1675**, which includes, for example, a random access memory (RAM) **1610**, a read-only memory (ROM) **1615**, a removable and/or program storage device **1655** and a mass data and/or program storage device **1650**. An input/output (I/O) adapter **1630** connects mass storage device **1650** and

removable storage device **1655** to system bus **1620**. A user interface **1635** connects a keyboard **1665** and a mouse **1660** to system bus **1620**, and a port adapter **1625** connects a data port **1645** to system bus **1620** and a display adapter **1640** connect a display device **1670**. ROM **1615** contains the basic operating system for computer system **1600**. Examples of removable data and/or program storage device **1655** include magnetic media such as floppy drives, tape drives, portable flash drives, zip drives, and optical media such as CD ROM or DVD drives. Examples of mass data and/or program storage device **1650** include hard disk drives and non-volatile memory such as flash memory. In addition to keyboard **1665** and mouse **1660**, other user input devices such as trackballs, writing tablets, pressure pads, microphones, light pens and position-sensing screen displays may be connected to user interface **1635**. Examples of display device **1670** include cathode-ray tubes (CRT) and liquid crystal displays (LCD).

[**0049**] A machine readable computer program may be created by one of skill in the art and stored in computer system **1600** or a data and/or any one or more of machine readable medium **1675** to simplify the practicing of this invention. In operation, information for the computer program created to run the present invention is loaded on the appropriate removable data and/or program storage device **1655**, fed through data port **1645** or entered using keyboard **1665**. A user controls the program by manipulating functions performed by the computer program and providing other data inputs via any of the above mentioned data input means. Display device **1670** provides a means for the user to accurately control the computer program and perform the desired tasks described herein.

[**0050**] FIG. **17** shows a block diagram of an example design flow **1700**. Design flow **1700** may vary depending on the type of IC being designed. For example, a design flow **1700** for building an application specific IC (ASIC) will differ from a design flow **1700** for designing a standard component. Design structure **1720** is an input to a design process **1710** and may come from an IP provider, a core developer, or other design company. Design structure **1720** comprises programmable device (**1**) in the form of schematics or HDL, a hardware-description language, (e.g., Verilog, VHDL, C, etc.). Design structure **1720** may be on one or more of machine readable medium **1675** as shown in FIG. **16**. For example, design structure **1720** may be a text file or a graphical representation of programmable device (**1**). Design process **1710** synthesizes (or translates) programmable device (**1**) into a netlist **1780**, where netlist **1780** is, for example, a list of transistors, devices, macros, etc. and describes the connections to other elements and circuits in an integrated circuit design and recorded on at least one of machine readable medium **1675**.

[**0051**] Design process **1710** includes using a variety of inputs; for example, inputs from library elements **1730** which may house a set of commonly used elements, circuits, and devices, including models, layouts, and symbolic representations, for a given manufacturing technology (e.g. different technology nodes, 32 nm, 45 nm, 90 nm, etc.), design specifications **1740**, characterization data **1750**, verification data **1760**, design rules **1770**, and test data files **1785**, which may include test patterns and other testing information. Design process **1710** further includes, for example, standard circuit design processes such as timing analysis, verification tools, design rule checkers, place and route tools, etc. One of ordinary skill in the art of integrated circuit design can appreciate the extent of possible electronic design automation tools and applications used in design process **1710** without deviating from the scope and spirit of the invention.

[**0052**] Ultimately design process **1710** translates programmable device (**1**), along with the rest of the integrated circuit design (if applicable), into a final design structure **1790** (e.g., information stored in a GDS storage medium). Final design structure **1790** may comprise information such as, for example, test data files, design content files, manufacturing data, layout parameters, wires, levels of metal, vias, shapes, test data, data for routing through the manufacturing line, and any other data required by a semiconductor manufacturer to produce programmable device (**1**). Final design structure **1790** may then proceed to a stage **1795** of design flow **1700**; where stage **1795** is, for example, where final design structure **1790**: proceeds to tape-out, is released to manufacturing, is sent to another design house or is sent back to the customer.

[**0053**] While there has been shown and described what is at present considered a preferred embodiment of the present invention, it will be readily understood by those skilled in the art that various changes and modification may be made therein without departing from the spirit and scope of the present invention which shall be limited only by the scope of the claims.

INDUSTRIAL APPLICABILITY

[**0054**] The present invention has applicability as design files containing E-fuses that may be employed during chip production, or within a deployed system to repair failing circuitry, or to customize a hardware or software application.

What is claimed is:

1. A design structure instantiated in a machine readable medium for designing, manufacturing, or testing a programmable device, the design structure comprising:

a substrate;

an insulator on said substrate;

an elongated semiconductor material on said insulator, said elongated semiconductor material having first and second ends, and an upper surface,

said first end being substantially wider than said second end and comprising a plurality of integral triangular-shaped portions forming openings which face generally toward said second end, and

a metallic material on said upper surface, said metallic material being physically migratable along said upper surface responsive to an electrical current flowable through said semiconductor material and through said metallic material.

2. The design structure as claimed in claim 1,

further comprising an energy source connected to said elongated semiconductor material, for causing an electrical current to flow through said elongated semiconductor material and through said metallic material, and for causing said metallic material to migrate along said upper surface.

3. The design structure as claimed in claim 1, wherein said elongated semiconductor material comprises a doped polysilicon.

4. The design structure as claimed in claim 1, wherein said metallic material comprises a metallic silicide.

5. The design structure as claimed in claim 1, wherein said metallic material is selected from the group consisting of WSi_2, $NiSi_2$, NiSi, PtSi, $PtSi_2$, and $CoSi_2$.

6. The design structure as claimed in claim 1, wherein said second end comprises an oblong-shaped portion.

7. The design structure as claimed in claim 1, wherein said metallic material is disposed on the entire upper surface of said elongated semiconductor material.

8. The design structure as claimed in claim 1, wherein said metallic material is a semiconductor alloy.

9. The design structure as claimed in claim 1, wherein said elongated semiconductor material is N+ polysilicon and said metallic material is WSi_2.

10. The design structure as claimed in claim 1, wherein said elongated semiconductor material includes a central portion connecting said first end to said second end.

11. The design structure as claimed in claim 10, wherein said central portion has a maximum substantially uniform width of less than approximately one micron.

12. The design structure as claimed in claim 10, wherein said central portion has a length of less than approximately two microns.

13. The design structure as claimed in claim 10, wherein said central portion and said second end form a T-shaped member.

14. A final design structure instantiated in a machine readable medium for designing, manufacturing or testing a programmable device,

the final design structure comprising:

a substrate;

an insulator on said substrate;

an elongated semiconductor material on said insulator, said elongated semiconductor material having first and second ends, and an upper surface,

said first end being substantially wider than said second end and comprising a plurality of integral triangular-shaped portions, and

a metallic material on said upper surface, said metallic material being physically migratable along said upper surface responsive to an electrical current flowable through said semiconductor material and through said metallic material.

15. The final design structure as claimed in claim 14, wherein the final design structure comprises a netlist which describes the programmable device.

16. The final design structure as claimed in claim 14, wherein the final design structure resides on a GDS storage medium.

17. The final design structure as claimed in claim 14, wherein the final design structure comprises programming information for the programmable device.

* * * * *