



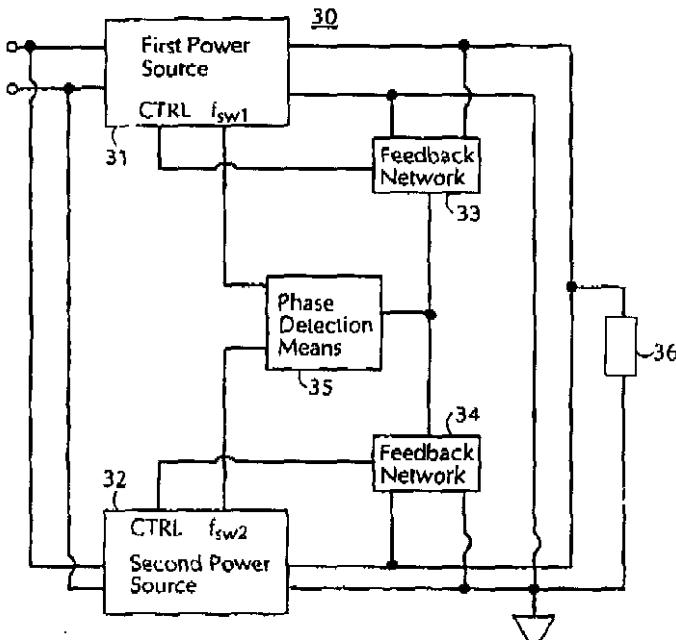
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(54) Title: SYSTEM AND METHOD FOR EQUALIZING POWER FROM TWO POWER SOURCES

(57) Abstract

A system (30) and a method may use variable-frequency power sources for supplying power to a load (36). The system and method use phase detection in order to automatically and substantially equalize the currents supplied to a load by each of the variable-frequency power sources, and to cancel a ripple component of the input current drawn by the system. First and second power sources (31, 32) supply power to the load. The power sources have a similar relationship between their respective variable switching frequencies of, respectively, the first and second power sources are locked to one another using phase detection to substantially equalize the power supplied to the load by each power source. The system and method are advantageously utilized to provide a power factor correction front-end for a switch-mode power supply. Power sources with non-linear and/or inverse relationships between power supplied and switching frequency can be used. In alternate embodiments power from series power sources is equalized by equalizing voltages supplied by each power source to a load.



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SYSTEM AND METHOD FOR EQUALIZING POWER FROM TWO POWER SOURCES

BACKGROUND OF THE INVENTION

1. Field of the Invention

5 The present invention relates generally to systems for supplying power to a load, and, in particular, to such systems that use plural power sources where the power supplied from the power sources is equalized.

2. Description of Background Art

10 It is known to couple two power sources together to supply power to a common load. FIGURE 1 shows a block diagram of a prior art system 10 for supplying power to a load. The system shown in FIGURE 1 includes first and second power sources 11 and 12 that are coupled to one another in parallel. The power sources 11 and 12 use first and second feedback networks 13 and 14 to regulate the voltages applied to the load 16 by the power sources 11 and 12. Each 15 power source 11 and 12 also includes a respective current sensing means 17 and 18 to monitor the current supplied to the load 16 by that power source. Each current sensing means 17 and 18 generates a voltage that is representative of the current supplied by the associated power source 11 and 12 to the load 16. The voltages generated by the current sensing means 17 and 18 are compared by the 20 amplifier 15, which provides an error voltage that is representative of the difference between the currents supplied to the load 16 by the power sources 11 and 12. This error voltage is applied to the feedback networks 13 and 14 to substantially equalize the currents supplied by each of the power sources 11 and 12 to the load 16. Accordingly, the power from the two power sources 11 and 12 25 is equalized.

FIGURE 2 shows a particular embodiment of the prior art system shown in FIGURE 1. The power sources 11 and 12 are coupled in parallel to one another for supplying power to the load 16. The output voltage of the power source 11 is compared to a first reference voltage VREF1 by the amplifier U1, and

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the resulting error voltage is applied to a control terminal of the first power source 11 to regulate its output voltage. Similarly, the output voltage of the power source 12 is compared to a second reference voltage VREF2 by the amplifier U2, and the resulting error voltage is applied to a control terminal of the second power source 5 12 to regulate its output voltage. A sense resistor R1 and its associated amplifier U3 provide a first current-sense voltage that is representative of the current supplied to the load 16 by the first power source 11, and a sense resistor R2 and its associated amplifier U4 provide a second current-sense voltage that is representative of the current supplied to the load 16 by the second power source 10 12. The first and second current sense voltages are compared by the amplifier U5, which provides an error voltage that is representative of the difference between the currents that are supplied to the load 16 by each of the power sources 11 and 12. The error voltage from the amplifier U5 is fed back to the feedback networks 13 15 and 14 to equalize the currents supplied to the load 6 by each of the power sources 11 and 12. The error voltage from the amplifier U5 is inverted by the inverter N1 prior to being fed back to the feedback network 14.

The prior art system 10 illustrated in FIGURES 1 and 2 works well to equalize the currents (and hence the power) supplied to the load 16 by each of the power sources 11 and 12. However, using the sense resistors R1 and R2 and their 20 associated circuitry to sense the currents supplied to the load 16 is disadvantageous because it increases the parts count (i.e., the number of parts) as well as size of the system and decreases the efficiency of the system.

It is known to cancel the input ripple current drawn by a system in order to power a load. It is known in the art to effect input ripple current 25 cancellation by coupling two power sources in parallel and by providing the two power sources with switching frequencies that are 180° out of phase. The prior art system 20 illustrated in FIGURE 3 provides for the cancellation of input ripple current in this manner. The system 20 includes a first boost-type power converter 21 (a first power source), which comprises a PWM controller 22, a FET power 30 switch M1, an inductance L1, a rectifier D1, and a filter capacitor C1. The power

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converter 21 operates in a manner that is well-known, and will not be described further herein. The power supplied to the load 26 by the first power converter 21 is regulated by the feedback network 27 and the PWM controller 22, the output of which is coupled to the gate electrode of the FET power switch M1. A voltage 5 divider formed by the resistors R3 and R4 of feedback network 27 divides the output voltage of the first power converter 21 and compares the divided output voltage against a reference voltage V_{REF3} in the amplifier U6. The output voltage from the amplifier U6 is then coupled to the control input of the PWM controller 22 to regulate the ON time of the power switch M1.

10 The system 20 further includes a second boost-type power converter 23 (a second power source), which comprises a PWM controller 24, a FET power switch M2, an inductance L2, a rectifier D2, and a filter capacitor C2. The power converter 23 operates in a manner that is well-known, and will not be described further herein. The power supplied to the load 26 by the second power converter 15 23 is also regulated by the feedback network 27 and by the PWM controller 24, the output of which is coupled to the gate electrode of the FET power switch M2. The output voltage from the amplifier U6 is also coupled to the control input of the PWM controller 24 to regulate the ON time of the power switch M2.

As is well-known, the currents flowing through the inductors L1 and 20 L2 in, respectively, the power converters 21 and 23 have triangular waveforms. A fixed-frequency oscillator 25 is directly coupled to the clock input of the PWM controller 22 and is coupled to the clock input of the PWM controller 24 through the inverter N2 to provide the PWM controllers 22 and 24 with clock waveforms that are 180° out of phase. As a result, the triangular current waveforms for the 25 inductors L1 and L2 will be 180° out of phase. Therefore, the triangular component of the input current is cancelled, leaving only the DC component of the input current. The circuit of FIGURE 3 does not address the problem of current or power equalization to the load 26.

U.S. Patent 4,779,184 to White, issued on October 18, 1988 and 30 entitled SWITCH MODE POWER SUPPLY WITH REDUCED NOISE ("the '184

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Patent") discloses a phase-locked loop for controlling the phase and duty cycle of two switch-mode power supplies that supply power to a common load to produce an output voltage which is substantially free of harmonics. The phase-locked loop maintains a desired phase shift between the drive signals of the two power supplies. A drive signal for one of the power supplies is provided by an oscillator which oscillates at a fixed frequency. The drive signal for the other power supply is provided by a voltage-controlled oscillator which oscillates at the frequency of the fixed oscillator. The power supplies disclosed in the '184 Patent are fixed frequency power supplies. The '184 Patent is not directed to substantially equalizing the load currents or power supplied by the power supplies or cancelling a ripple component of the input current drawn by the system.

U.S. Patent 5,079,686 to Vinciarelli, issued on January 7, 1992 and entitled ENHANCEMENT-MODEZERO-CURRENTSWITCHING CONVERTER ("the '686 Patent"), discloses a system of enhancement-mode power converters that have their outputs coupled together to deliver power to a load. Each power converter has an associated setpoint voltage, and the power converters synchronize to the operating frequency of the power converter that has the highest setpoint voltage, and hence, the highest power output. Synchronizing information is delivered to the power converters by a synchronizing bus. The '686 Patent discloses a complex system of setpoint voltages delivered through a bus to achieve frequency synchronization and, hence, power equalization, of its power converters. There is no disclosure of phase detection. The '686 Patent does not address cancellation of an input ripple component of the input current drawn by the system. The power converters that can be used in the system disclosed in the '686 Patent are unfortunately limited to those power converters that have a linear relationship between their switching frequency and the power that they deliver to a load.

SUMMARY

The present invention relates to a system and a method with plural power sources for powering a load where the power supplied from the plural power sources is equalized. The power source may be connected in parallel, in

which case the current from the power source is equalized or the power sources may be connected in series, in which case the voltages of the power sources are equalized.

The present invention may employ variable frequency power sources 5 and may employ power sources which the relationship between the power supplied by each power source and the switching frequency of that power source is either linear or non-linear and either direct or inverse.

The present invention contemplates the use of phase detection for locking the switching frequencies of the power sources to avoid the use of bulky 10 and inefficient components, such as sense resistors, used in current detection.

In certain applications, for example in power factor correction front-ends for switch-mode power supplies, there is a need to provide a system for supplying power to a load with the following features: variable frequency operation of the power sources in the good current sharing over the entire range 15 of the input voltage waveform, and good input current ripple cancellation.

It is desirable to have a system for supplying power to the load that utilizes variable-frequency power sources that provide power over a range of switching frequencies. In order to provide such a system with minimum complexity and minimum cost, it is desirable that such a system use phase detection to lock 20 together the switching frequencies of the variable-frequency power sources in order to automatically and substantially equalize the currents (and hence power) supplied by the power sources to the load, and to cancel the ripple component of the input current drawn by the system.

The present invention is directed to a system and a method that use 25 variable-frequency power sources for supplying power to a load. The system and method use phase detection in order to automatically and substantially equalize the currents supplied to a load by each of the variable-frequency power sources, and to cancel a ripple component of the input current drawn by the system.

According to a feature of the present invention, a system for 30 supplying power to a load comprises first and second power sources for supplying

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power to the load. The power sources have a similar relationship between their respective variable switching frequencies and the power that they supply to the load. A phase detection means locks the first and second switching frequencies of, respectively, the first and second power sources to one another to substantially 5 equalize the power supplied to the load by each power source.

According to another feature of the present invention, a system for providing power factor correction to a power supply comprises first and second power sources for supplying input power to the power supply. Each of the power sources has a relationship between the power it supplies and its switching 10 frequency. That relationship can be either linear or non-linear and either direct or inverse, and the first and second power sources have a similar such relationship. A phase detection means locks the first and second switching frequencies of, respectively, the first and second power sources to one another to substantially equalize the input power supplied to the power supply by each of the power 15 sources.

According to yet another feature of the present invention, power is supplied to a load by selecting first and second power sources that have a similar relationship between their respective variable switching frequencies and the power that they supply to the load. The first and second switching frequencies of, 20 respectively, the first and second power sources are varied. The switching frequencies are locked to one another using phase detection to substantially equalize the power supplied to the load by each of the power sources.

According to a further feature of the present invention, power factor correction is provided to a power supply by selecting first and second power 25 sources to have a similar relationship between their respective variable switching frequencies and the input power that they supply to the power supply. One of the first or second switching frequencies of, respectively, the first or second power sources is set. The switching frequency of each of the power sources has a relationship to the power supplied by that power source that can be either linear 30 or non-linear and either direct or inverse. The switching frequencies are locked to

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one another using phase detection to substantially equalize the input power supplied to the power supply by each of the power sources.

The above, and other features, aspects, and advantages of the present invention will become apparent from the following description read in conjunction with the accompanying drawings, in which like reference numerals designate the same elements.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGURE 1 is a block diagram of a prior art system for supplying power to a load.

10 FIGURE 2 is a schematic diagram of the prior art system shown in FIGURE 1.

FIGURE 3 is a block diagram of another prior art system for supplying power to a load.

15 FIGURES 4 and 5 are block diagrams that illustrate a system for supplying power to a load according to a feature of the present invention.

FIGURES 6 and 7 are schematic diagrams illustrating the inventive system shown in FIGURE 4.

FIGURE 8 is a diagram, in block and schematic form, that illustrates a feature of the inventive system described herein.

20 FIGURE 9 is a diagram, in block and schematic form, of a preferred embodiment of the inventive system described herein.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIGURE 4 shows a block diagram that illustrates a system 30 for supplying power to the load 6 according to the present invention. The system 30 includes first and second power sources 31 and 32 which are coupled together at their input terminals and supply power to the same load 36. Each of the power sources 31 and 32 is a variable-frequency power source that has a relationship between its switching frequency and the power that it supplies to a load. For example, each power source 31 and 32 can have a relationship between its switching frequency and the power that it supplies to a load that is either linear or

non-linear. At the same time, each power supply can also have a relationship between its switching frequency and the power that it supplies to the load that is direct, so that power and switching frequency increase or decrease in the same direction, or inverse, so that power and switching frequency change in opposite directions. The power sources 31 and 32 of the system 30 have similar relationships between their switching frequencies and the power that they supply to the load 36. The first and second power sources 31 and 32 can be coupled to one another in parallel, as shown in FIGURE 4, or in series, as shown in FIGURE 5. For the sake of simplicity, the description of the present invention will be made primarily with reference to the parallel embodiment shown in FIGURE 4.

Referring to FIGURE 4, the system further includes feedback networks 33 and 34 associated with, respectively, the first and second power sources 31 and 32. The first feedback network 33 couples a portion of the output voltage of the first power source 31 to a control terminal CTRL of the first power source 31 to vary the first switching frequency f_{sw1} of the first power source 31, thereby regulating the power supplied by the first power source 31 to the load 36. Similarly, the second feedback network 34 couples a portion of the output voltage of the second power source 32 to a control terminal CTRL of the second power source 32 to vary the second switching frequency f_{sw2} of the second power source 32, thereby regulating the power supplied by the second power source 32 to the load 36.

According to a feature of the present invention, a phase detection means 35, which may be any conventional phase detector, provides an error signal that is representative of the difference between the first switching frequency f_{sw1} of the first power source 31 and the second switching frequency f_{sw2} of the second power source 32. The first switching frequency f_{sw1} is coupled from a terminal of the first power source 31 and is applied to an input terminal of the phase detection means 35. Similarly, the second switching frequency f_{sw2} is coupled from a terminal of the second power source 32 and is applied to the other input terminal of the phase detection means 35. The error signal provided by the phase detection

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means 35 is coupled to the feedback networks 33 and 34. The result is that the first and second switching frequencies f_{sw1} and f_{sw2} are locked to one another.

Furthermore, because the first and second power sources 31 and 32 have similar relationships between their switching frequencies and the power that 5 they supply to a load, the power supplied to the load 36 by the first power source 31 is substantially equal to the power supplied to the load 36 by the second power source 32. In the embodiment of the present invention illustrated in FIGURE 4, the substantial equalization of the power supplied to the load 36 by the first and second power sources 31 and 32 means that the currents supplied to the load 36 10 by each of the power sources 31 and 32 are substantially equalized, because the power sources 31 and 32 are coupled to one another in parallel and, thus, apply the same voltage to the load 36. In the embodiment of the present invention illustrated in FIGURE 5, the substantial equalization of the power supplied to the load 36 by the first and second power sources 31 and 32 means that the voltages 15 supplied to the load 36 by each of the power sources 31 and 32 are substantially equalized, because the power sources 31 and 32 are coupled to one another in series and thus provide the same current to the load 36.

A schematic illustration of the inventive system 30 of FIGURE 4 is shown in FIGURE 6, where the power sources are power converters. The system 20 30 includes first and second variable-frequency power converters 37 and 38, the amplifiers U7 and U8, the phase detector 35, and the inverter N3. The power converters 37 and 38 are coupled to one another in parallel to provide DC power to the load 36. The amplifier U7 provides a feedback voltage that is representative 25 of the difference between the output voltage provided by the first power converter 37 and a reference voltage V_{REF4} to regulate the voltage applied to the load by the first power converter 37. The feedback voltage provided by the amplifier U7 is applied to a voltage-controlled oscillator at the VCO-IN terminal of the first power converter 37 to control the switching frequency of, and hence the power supplied by, the first power converter 37. The phase detection means 35 and the voltage-controlled oscillator of the first power converter 37 together comprise a phase- 30

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locked loop. The bandwidth of this phase-locked loop is greater than or equal to the bandwidth of the feedback loop provided from the output of the first power converter 37 to its VCO-IN terminal by the amplifier U7.

Similarly, the amplifier U8 provides a feedback voltage that is 5 representative of the difference between the output voltage provided by the second power converter 38 and a reference voltage V_{REFS} to regulate the voltage applied to the load by the second power converter 38. The feedback voltage provided by the amplifier U8 is applied to a voltage-controlled oscillator at the VCO-IN terminal of the second power converter 38 to control the switching frequency of, and hence the 10 power supplied by, the second power converter 38. The phase detection means 35 and the voltage-controlled oscillator of the second power converter 38 together comprise a phase-locked loop. The bandwidth of this phase-locked loop is greater than or equal to the bandwidth of the feedback loop provided from the output of the second power converter 38 to its VCO-IN terminal by the amplifier U8.

15 The first and second switching frequencies f_{sw1} and f_{sw2} of, respectively, the first and second power converters 37 and 38 are made available at a terminal VCO-OUT of the respective power converters 37 and 38, and are coupled as inputs to the phase detection means 35. Any difference in the output power supplied to the load 6 by the power converters 36 and 37 will result in a 20 difference in the first and second switching frequencies f_{sw1} and f_{sw2} , which will cause a continuously changing phase shift between the first and second switching frequencies f_{sw1} and f_{sw2} at the inputs to the phase detection means 35. The phase detection means 35 provides an error voltage that is a function of the phase difference of the signals at its inputs. Thus, the phase detection means 35 detects 25 the difference between the first and second switching frequencies f_{sw1} and f_{sw2} at its input terminals, and provides an error voltage that is summed with the voltages provided by the amplifiers U7 and U8 to lock together the first and second switching frequencies f_{sw1} and f_{sw2} of the first and second power converters 37 and 38, thereby substantially equalizing the power supplied to the load 6 by each of the 30 power converters 37 and 38. The error voltage from the phase detection means 35

is inverted by the inverter N3 before being summed with the output voltage of the amplifier U8. Again, because the power converters 37 and 38 are coupled together in parallel and have a similar relationship between their respective switching frequencies and the power that they supply to the load 36, the currents provided 5 to the load 36 by each of the power converters 37 and 38 are substantially equalized by the operation of the phase detection means 35.

In an alternative embodiment of the inventive system 30 described herein, and shown in FIGURE 7, the error signal generated by the phase detection means 35 is applied to only the first power converter 37. The error voltage from 10 the phase detection means 35 is coupled to the non-inverting input of the amplifier U9 through a resistor R5. As a result, the first switching frequency f_{sw1} of the first power converter 37 is locked to the second switching frequency f_{sw2} of the second power converter 38. The first power converter 37 thus has a "slave" relationship with respect to the "master" second power converter 38. It will be apparent to 15 those having ordinary skill in the art that the second switching frequency f_{sw2} of the second power converter 38 can, alternatively, be locked to the first switching frequency f_{sw1} of the first power converter 37 so that the second power converter 38 has a "slave" relationship with respect to the "master" first power converter 37.

FIGURE 8 illustrates, in block and schematic form, a further feature 20 of the inventive system described herein. A system 40 for delivering power to the load 46 includes a first power source 41, which includes a variable-frequency controller 42 and its associated first power stage 48. The power supplied to the load 46 by the first power source 41 is regulated by the feedback network 47 and the first variable-frequency controller 42. The system 40 further includes a second 25 power source 43, which includes a variable-frequency controller 44 and its associated second power stage 49. The second power source 43 is coupled in parallel to the first power source 41. The power supplied to the load 46 by the second power source 43 is also regulated by the feedback network 47 and a second variable-frequency controller 44.

Each of the power sources 41 and 43 is a variable-frequency power source that has a relationship between its switching frequency and the power that it supplies to a load. For example, each power source 41 and 43 can have a relationship between its switching frequency and the power that it supplies to a load that is either linear or non-linear. At the same time, each power source can also have a relationship between its switching frequency and the power that it supplies to the load that is direct, so that power and switching frequency increase or decrease in the same direction, or inverse, so that power and switching frequency change in opposite directions. The power sources 41 and 43 of the system 40 have similar relationships between their respective switching frequencies and the power that they supply to the load 46.

According to a feature of the present invention, the drive waveform provided by the first variable frequency controller 42 in the first power source 41 is also provided to an input terminal of the phase detection means 45. The drive waveform provided by the second variable frequency controller 44 in the second power source 43 is inverted by the inverter N4 before being provided to another input terminal of the phase detection means 45. The error signal provided by the phase detection means 45, which represents the phase difference between the drive waveform of the first variable-frequency controller 42 and the inverted drive waveform of the second variable-frequency controller 44, is summed with the feedback voltage V_f provided by the feedback network 47 to lock together the frequencies f_1 and f_2 of the drive waveforms provided by the variable frequency controllers 42 and 44, while maintaining the two drive waveforms substantially 180° out of phase with respect to one another.

Once the frequencies f_1 and f_2 of the two drive waveforms are locked together, the power supplied to the load 46 by each of the power sources 41 and 43 will be substantially equal because the power sources 41 and 43 have similar relationships between their respective switching frequencies and the power that they supply to the load 46. The currents supplied to the load 46 by the power sources 41 and 43 will be substantially equal because the power sources 41 and 43

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are coupled together in parallel. As a result of the phase difference between the two drive waveforms, the triangular component of the input current I drawn by the system will be cancelled, leaving only the DC component of the input current.

In a presently preferred embodiment, the system 40 of FIGURE 8 is advantageously utilized to provide a power factor correction (PFC) front-end for a switch-mode power supply. FIGURE 9 shows an embodiment of the system of FIGURE 8 used for power factor correction. The purpose of a power factor correction front-end is to achieve an input current for a switch-mode power supply that is proportional to the AC input voltage V_{MAINS} . For example, if the AC input voltage V_{MAINS} has the waveform of a sine wave, then the power factor correction front-end draws an input current that also has the waveform of a sine wave.

In the presently preferred embodiment shown in FIGURE 9, the load 56 represents a switch-mode power supply. An AC input voltage V_{MAINS} is rectified by the bridge rectifier VR1 to provide a DC input voltage to the first and second power converters 51 and 53. In the system 50, as in all power factor correction front-ends, the frequency of the AC input voltage V_{MAINS} is lower than the switching frequencies of the first and second power converters 51 and 53. The first and second power converters 51 and 53 each utilize a boost-type DC-DC power converter, which has a relationship between its switching frequency and the power it supplies to a load that is both non-linear and inverse. The first power converter 51 includes a variable-frequency PFC controller 52, the inductor L3, the FET power switch M3, the rectifier D3, and the filter capacitor C3. The second power converter 53 includes a variable-frequency PFC controller 54, the inductor L4, the FET power switch M4, the rectifier D4, and the filter capacitor C4. In the presently preferred embodiment, the boost-type power converters 51 and 53 operate at the edge of the continuous and discontinuous modes of conduction, which necessitates that the power converters 51 and 53 be of the variable-frequency type. The operation of the boost-type power converters 51 and 53 is well-known to those having ordinary skill in the art, and will not be described further herein.

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The variable frequency PFC controllers 52 and 54, which provide the drive waveforms with frequencies f_1 and f_2 to, respectively, the first and second power converters 51 and 53, will change the frequencies f_1 and f_2 of their respective drive waveforms as a function of the momentary input voltage V_{MAINS} to 5 maintain the input current to the switch-mode power supply proportional to the AC input voltage V_{MAINS} , which is coupled to the load 56 by the first and second power converters 51 and 53. The DC output voltage of the power converters 51 and 53 is divided by the voltage divider formed by the resistors R9 and R10, and the divided voltage is compared by the amplifier U12 against a reference voltage V_{REF} , 10 to provide a feedback voltage that is coupled to the first and second variable-frequency PFC controllers 52 and 54.

The drive waveforms with frequencies f_1 and f_2 of the variable frequency PFC controllers 52 and 54 are also applied to the input terminals of the phase detection means 55. The phase detection means 55 provides an error signal 15 that is representative of the frequency and phase difference between the drive waveforms with frequencies f_1 and f_2 . The loop filter 58 shapes the frequency response of the feedback network 58 to provide a desired frequency response for the feedback network 58. The error signal is summed with the feedback voltage provided by the feedback network 57 and coupled to the first and second variable 20 frequency PFC controllers 52 and 54. The phase detector 55 thus forms a separate phase-locked loop with each of the variable frequency PFC controllers 52 and 54. The bandwidths of these phase-locked loops are significantly greater than the frequency of the AC input voltage V_{MAINS} .

The drive waveforms of the variable frequency PFC controllers 52 and 25 54 are locked to the same frequency by the operation of the phase detection means 55. As a result, the power supplied to the switch-mode power supply by each of the boost-type power converters 51 and 53 is substantially equalized because both power converters 51 and 53 have a similar relationship between their respective switching frequencies and the power that they deliver to the load 56. The currents 30 supplied by the power converters 51 and 52 are substantially equalized because the

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power converters are coupled together in parallel. The ripple component of the input current I drawn by the system is then substantially cancelled because the phase detection means 55 regulates the drive waveforms provided by the variable frequency controllers 52 and 54 to be substantially 180° out of phase.

5 Having described preferred embodiments of the invention with reference to the accompanying drawings, it is to be understood that the invention is not limited to those precise embodiments, and that various changes and modifications may be effected therein by one having ordinary skill in the art without departing from the scope or spirit of the invention as defined in the
10 appended claims.

WHAT IS CLAIMED IS:

1. A system for supplying power to a load, said system comprising:

5 first and second power sources for supplying power to said load, said power sources having a similar relationship between a variable switching frequency of said power source and the power supplied by said power source to said load; and,

10 phase detection means for locking first and second switching frequencies of, respectively, said first and second power sources to one another to substantially equalize the power supplied to said load by each power source.

2. The system of Claim 1, wherein an error signal generated by said phase detection means is coupled to one of said first and second power sources.

3. The system of Claim 2, wherein the phase detection means 15 locks the switching frequency of said one of said first and second power sources to the switching frequency of the other one of said first and second power sources.

4. The system of Claim 2, wherein said error signal is also inverted and coupled to the other one of said first and second power sources.

5. The system of Claim 1, wherein said first and second power 20 sources are coupled to one another in parallel.

6. The system of Claim 5, wherein said phase detection means locks said first and second frequencies to one another to substantially equalize the currents supplied by each of said first and second power sources to said load.

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7. The system of Claim 6, wherein said first and second switching frequencies are substantially 180° out of phase.

8. The system of Claim 7, wherein a ripple current component of an input current supplied to said first and second power sources is substantially 5 cancelled.

9. The system of Claim 1, wherein said first and second power sources are coupled to one another in series.

10. The system of Claim 9, wherein said phase detection means locks said first and second frequencies to one another to substantially equalize the 10 voltages supplied by each of said first and second power sources to said load.

11. The system of Claim 1, further comprising:
a feedback loop for each of said first and second power sources for regulating an output voltage supplied by said power sources; and,
a voltage-controlled oscillator coupled to said phase detection means 15 to provide a phase-locked loop, the bandwidth of said phase-locked loop being greater than or equal to the bandwidth of said feedback loop.

12. A system for providing power factor correction to a power supply, said system comprising:

first and second power sources for supplying input power to said 20 power supply, where each of said power sources has a relationship between the power supplied by said power source and a switching frequency of said power source that can be either linear or non-linear and either direct or inverse, said first and second power sources having a similar such relationship; and,

phase detection means for locking first and second switching 25 frequencies of, respectively, said first and second power sources to one another to

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substantially equalize the input power supplied to said power supply by each of said power sources.

13. The system of Claim 12, further comprising a voltage-controlled oscillator coupled to said phase detection means for providing a phase-locked loop, wherein the bandwidth of said phase-locked loop is significantly greater than the frequency of an input signal to said first and second power sources.

14. The system according to Claim 13, wherein each of said power sources has a relationship between the power supplied by said power source and a switching frequency of said power source that is non-linear.

15. The system according to Claim 14, wherein each of said power sources has a relationship between the power supplied by said power source and a switching frequency of said power source that is inverse.

16. The system according to Claim 15, wherein each of said power sources comprises a boost converter.

17. A method for supplying power to a load, said method comprising the steps of:

selecting first and second power sources having a similar relationship between a variable switching frequency of said power source and the power supplied by said power source to said load;

varying at least one of first and second switching frequencies of, respectively, said first and second power sources; and,

locking said switching frequencies to one another using phase detection to substantially equalize the power supplied to said load by each of said power sources.

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18. The method of Claim 17, wherein said locking step comprises the steps of:

generating an error signal; and,
coupling said error signal to one of said first and second power
5 sources.

19. The method of Claim 18, further comprising the step of locking the switching frequency of said one of said first and second power sources to the switching frequency of the other one of the first and second power sources.

20. The method of Claim 18, further comprising the step of
10 inverting and coupling said error signal to the other one of said first and second power sources.

21. The method of Claim 17, further comprising the step of coupling said first and second power sources in parallel.

22. The method of Claim 21, wherein said locking step comprises
15 locking said first and second frequencies to one another to substantially equalize the currents supplied by said first and second power sources to said load.

23. The method of Claim 22, further comprising the step of setting said first and second switching frequencies to be substantially 180° out of phase with one another.

20 24. The method of Claim 23, further comprising the step of substantially cancelling a ripple current component of an input current supplied to said first and second power sources.

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25. The method of Claim 17, further comprising the step of coupling said first and second power sources in series.

26. The method of Claim 25, wherein said locking step comprises locking said first and second frequencies to one another to substantially equalize 5 the voltages supplied by said first and second power sources to said load.

27. The method of Claim 17, further comprising the steps of: generating an error signal; coupling said error signal to a variable-frequency controller of at least one of said first and second power sources to provide a phase-locked loop; and, 10 regulating the output voltages supplied by said power sources using a feedback loop which has a bandwidth which is less than or equal to the bandwidth of said phase-locked loop.

28. A method for providing power factor correction to a power supply, said method comprising the steps of:

15 selecting first and second power sources to have a similar relationship between a switching frequency of said power source and the input power supplied by said power source to said power supply;

20 have a relationship to the power supplied by their respective power source that can be either linear or non-linear and either direct or inverse; and,

locking said switching frequencies to one another using phase detection to substantially equalize the input power supplied to said power supply by each of said power sources.

25 29. The method of Claim 28, wherein said locking step comprises the steps of:

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- generating an error signal;
- coupling said error signal to a variable-frequency controller to provide a phase-locked loop; and
- setting the bandwidth of said phase-locked loop to be significantly
- 5 greater than the frequency of an input signal to said first and second power sources.

30. The method of Claim 29, wherein said setting step is performed according to said relationship being non-linear.

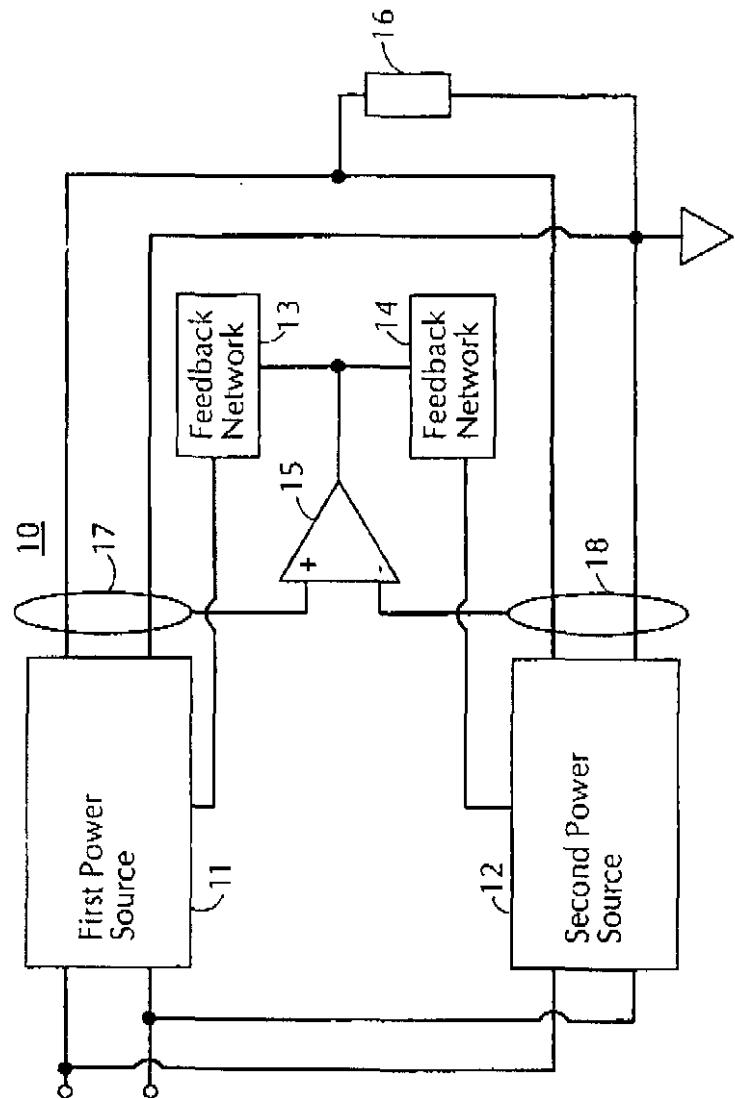
31. The method of Claim 30, wherein said setting step is

10 performed according to said relationship being inverse.

32. The method of Claim 31, wherein said selecting step comprises selecting first and second boost converters.

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FIG. 1
Prior Art

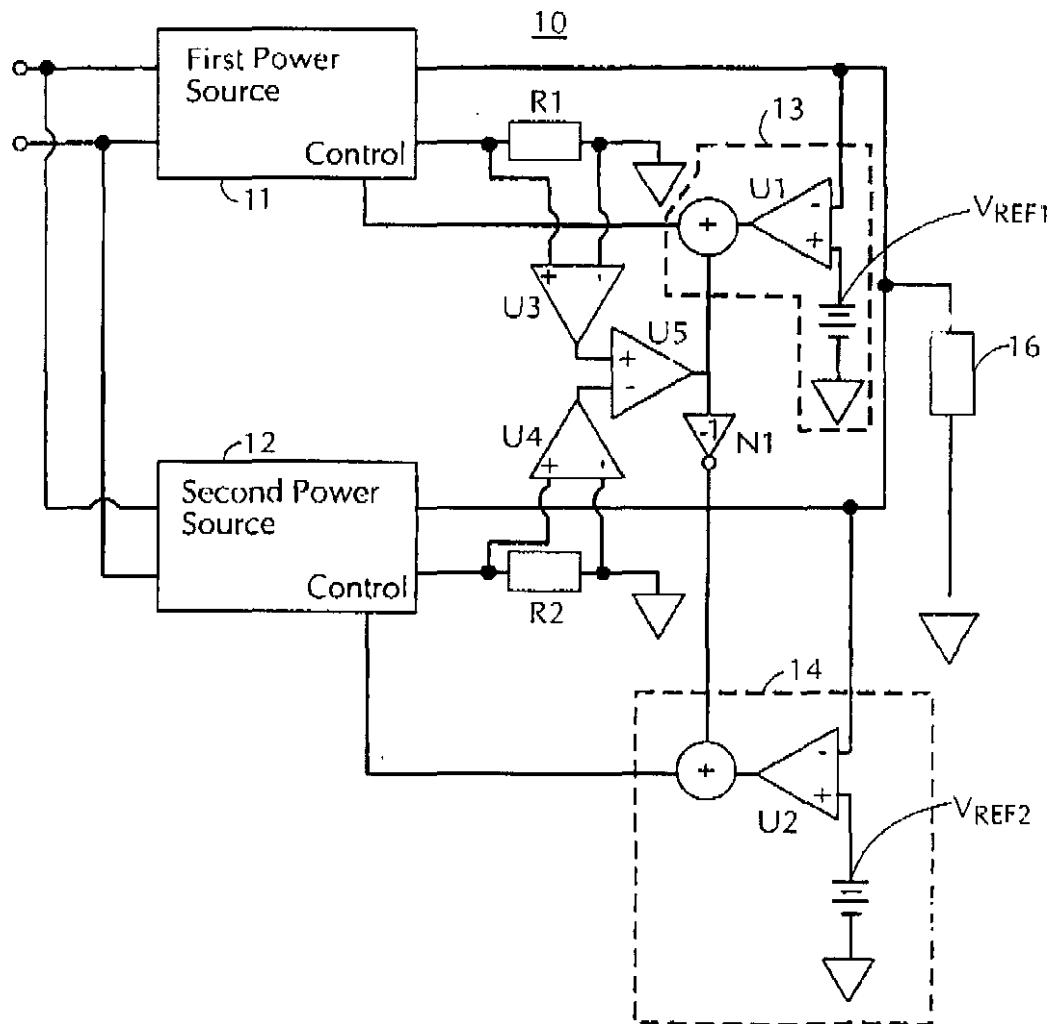


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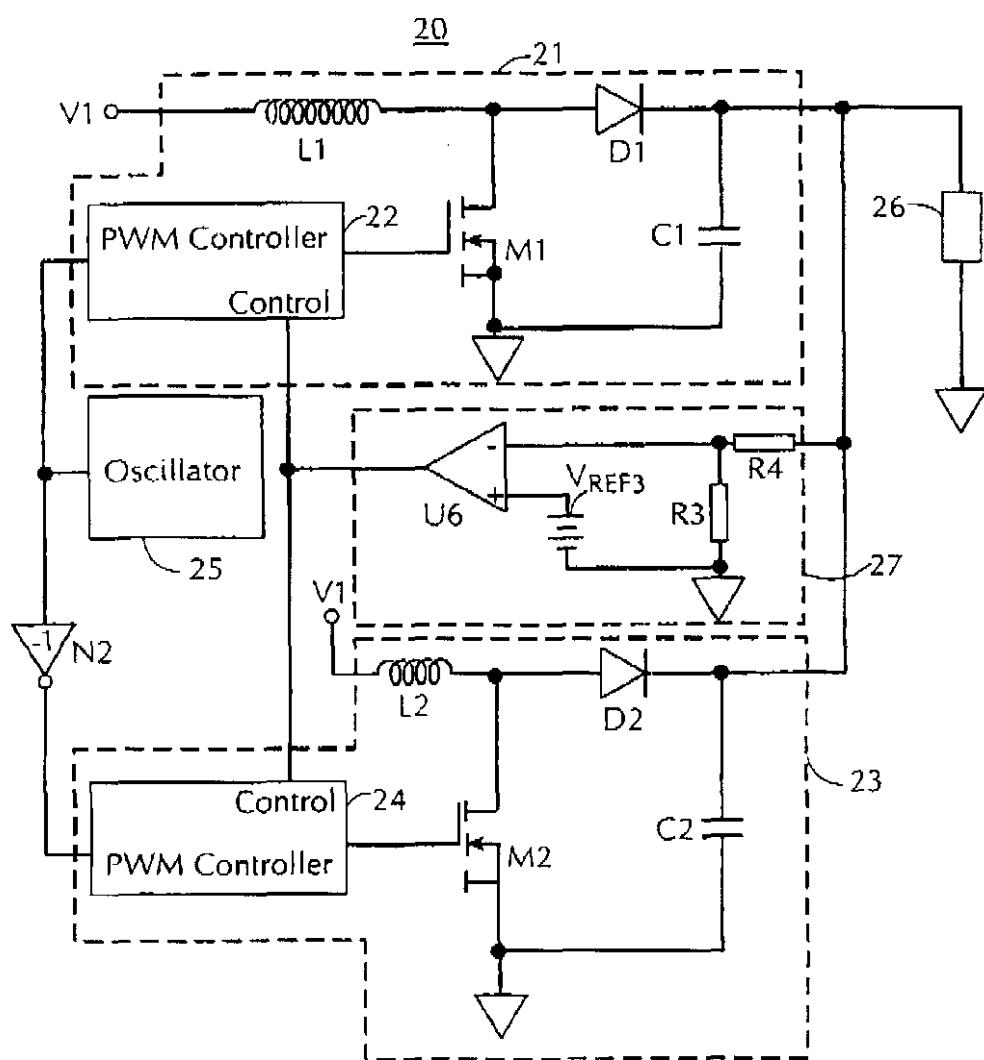
FIG. 2

Prior Art



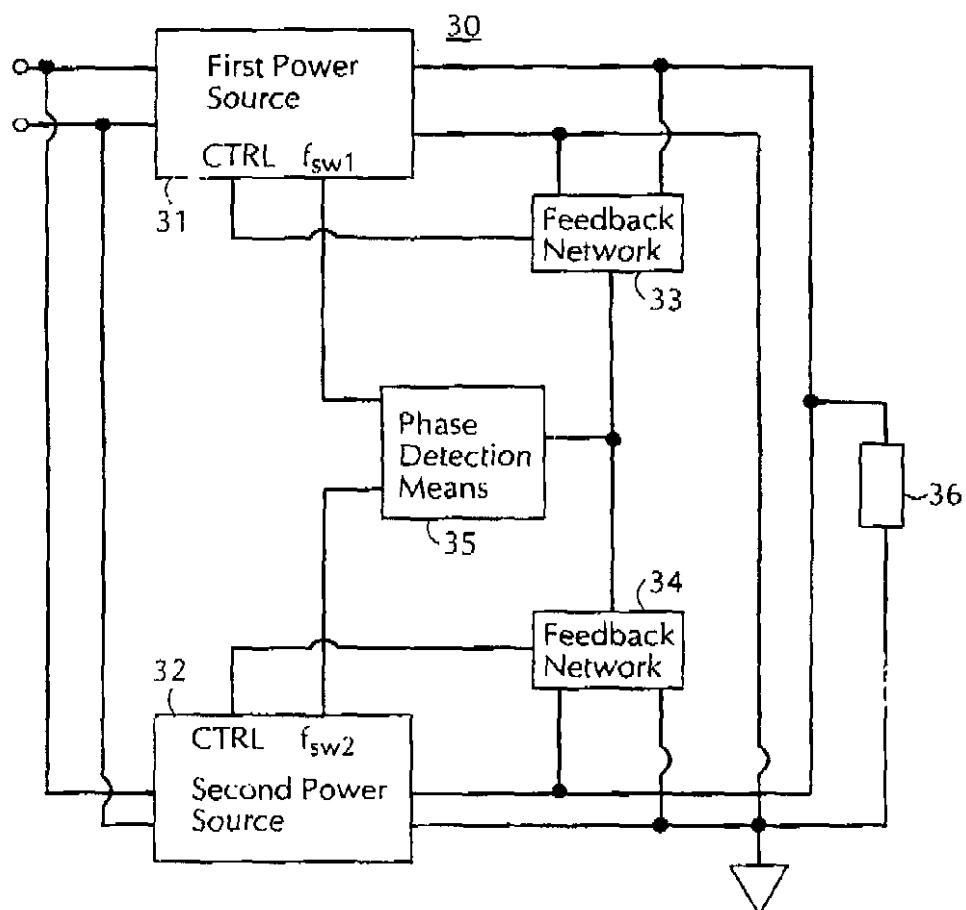
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FIG. 3Prior Art**SUBSTITUTE SHEET (RULE 26)**

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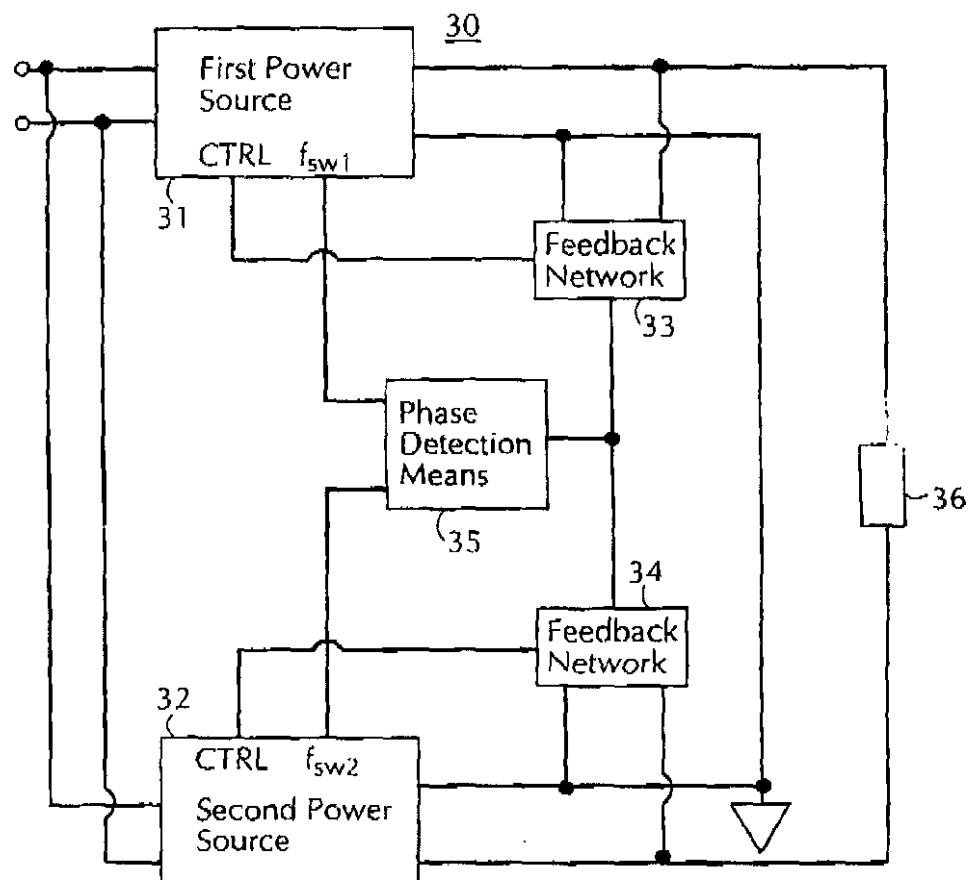
FIG. 4



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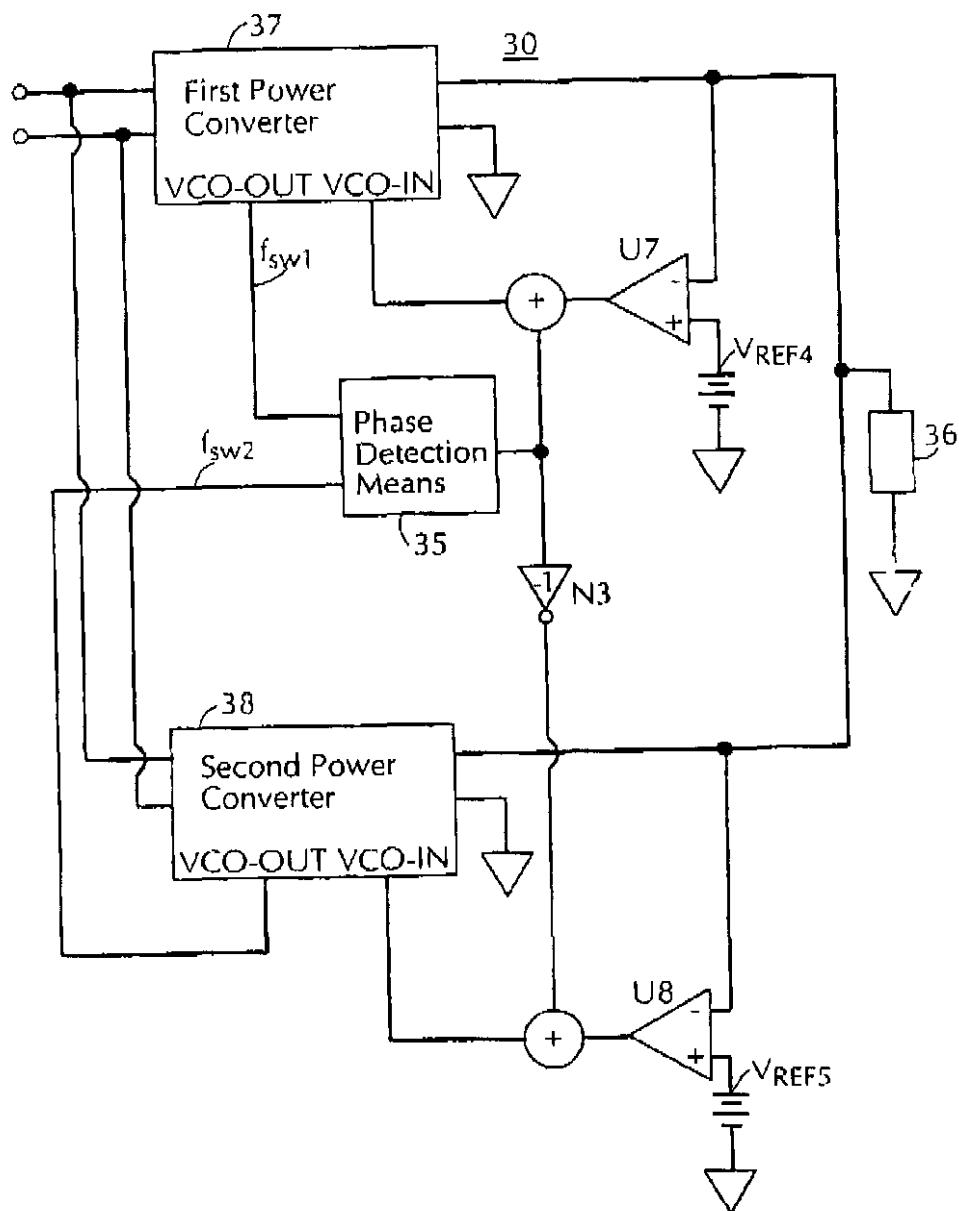
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FIG. 5



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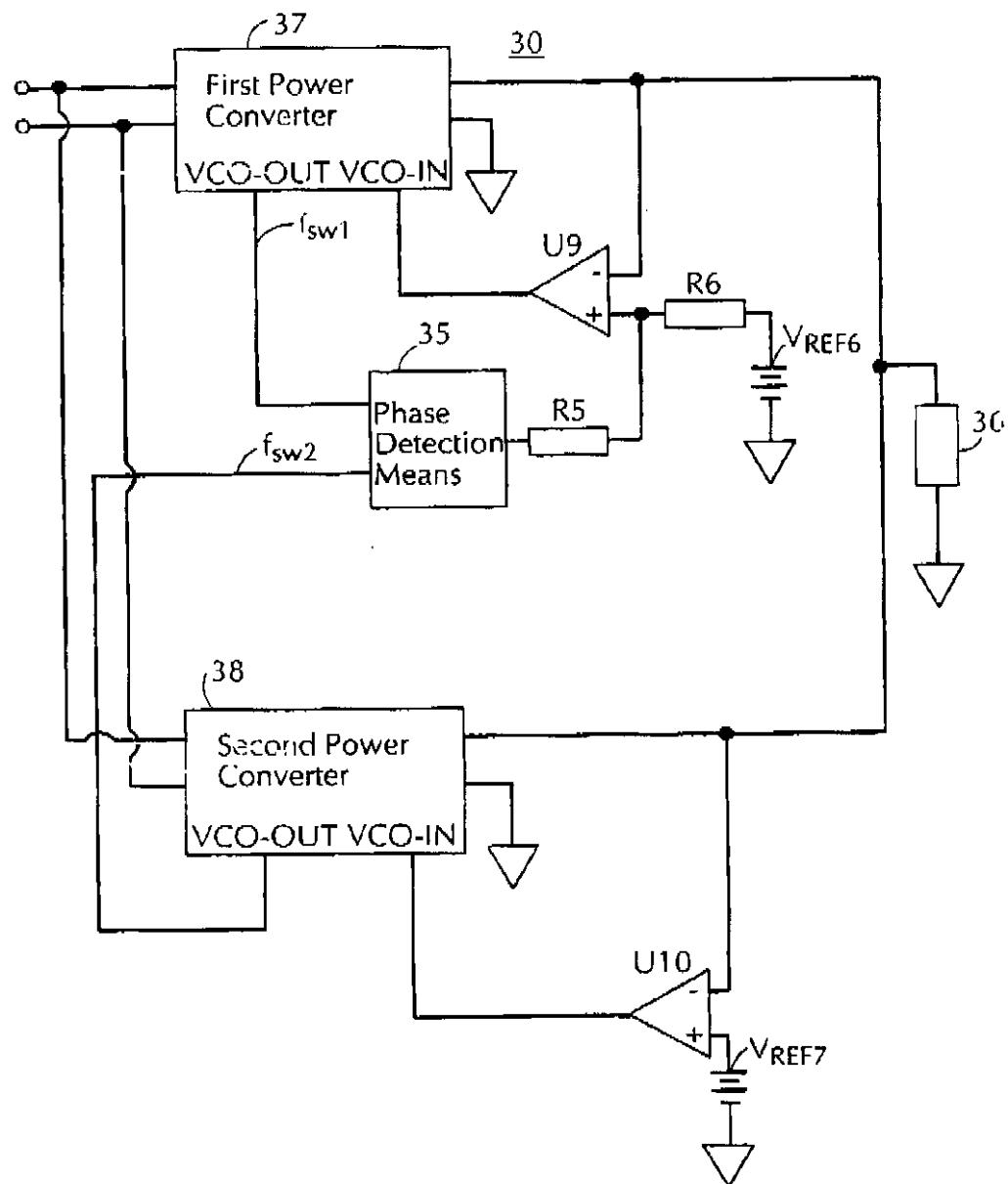
FIG. 6



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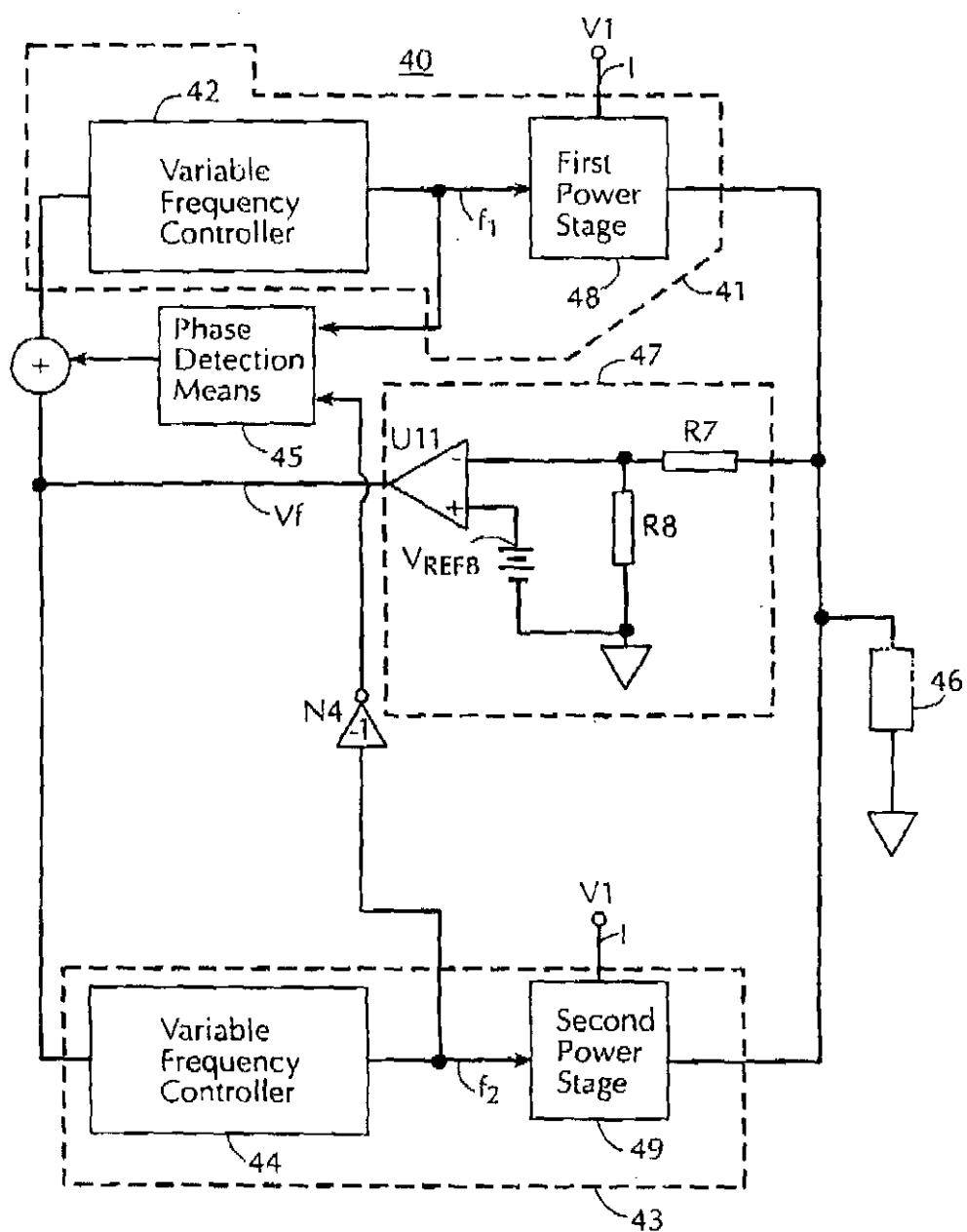
FIG. 7



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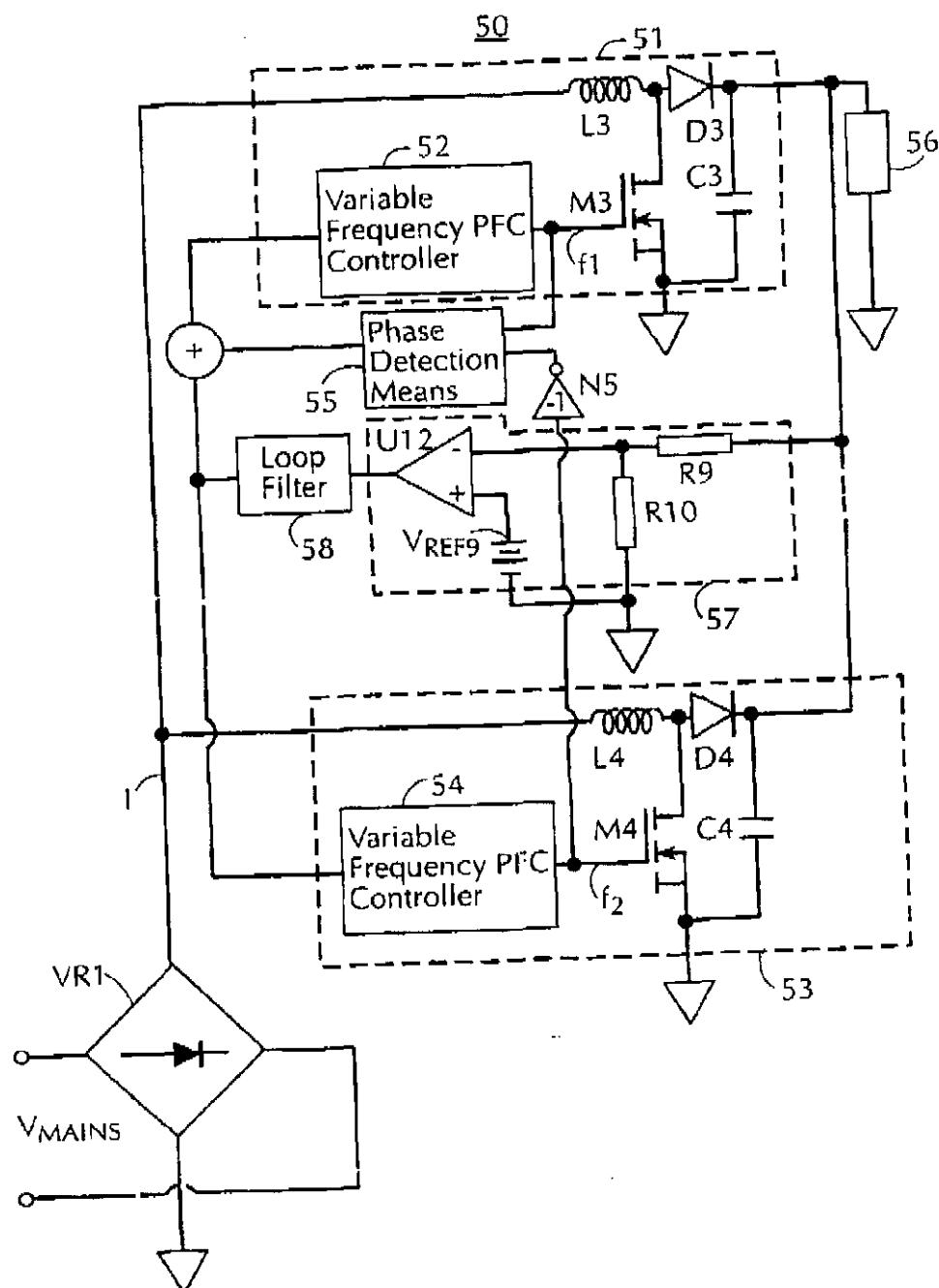
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FIG. 8



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FIG. 9



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INTERNATIONAL SEARCH REPORT

Intern. application No.

PCT/US00/06305

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H02M 3/28, 3/335, 7/00

US CL : 363/65, 67, 71

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 363/65, 67, 71

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,079,686 A [VINCIARELLI] 07 January 1992, (17/01/92) col. 7, line 3 to col. 8, line 67	1-32
X	US 5,309,344 A [SMITH] 03 May 1994, (03/05/94) col. 27 line 65 to col. 28, line 60.	1-32

 Further documents are listed in the continuation of Box C. See patent family annex.

Special categories of cited documents:	
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O	document referring to an oral disclosure, use, exhibition or other means
P	document published prior to the international filing date but later than the priority date claimed
T	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
V	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
W	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
E	document member of the same patent family

Date of the actual completion of the international search

01 MAY 2000

Date of mailing of the international search report

30 MAY 2000

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Form PCT/ISA/210 (second sheet) (July 1998) *

PCT Patent Pub. No.: WO 00/54397

Our Ref: YCT/PT-102/2002/II (2895.58824)

發明名稱： 等化來自二個電源之電源之系統及方法 /

發明摘要： 本發明揭示一種使用變頻電源以供應電源至一負載(36)之系統(30)及方法。該系統及方法使用相位偵測以自動及實質地等化每一來自變頻電源且供應至負載之電流，及消除由系統汲取之輸入電流之諧波成分。第一及第二電源(31，32)提供電源至負載。電源在各別之可變交換頻率間有類似之關係。第一及第二電源係使用相位偵測互鎖以實質等化各電源所供應至負載之電源。該系統及方法可被有效的使用以提供交換式電源供應器之功率因數修正前端。具有非線性及/或電源供應與交換頻率間之反向關係之電源可被使用。在另一實施例中，來自串聯電源之電源係被各電源所供應至負載之等化電壓等化。