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- (71) **Applicant:** CIRRUS LOGIC INTERNATIONAL SEMICONDUCTOR LIMITED [GB/GB]; 7B Nightingale Way, Quartermile, Edinburgh EH3 9EG (GB).
- (72) **Inventor:** KHARE, Rupesh; 31 Cleveland Grove, Newbury, Berkshire RG14 1XF (GB).
- (74) **Agent:** DAVIES, Philip; Redcliff Quay, 120 Redcliff Street, Bristol, Bristol BS1 6HU (GB).
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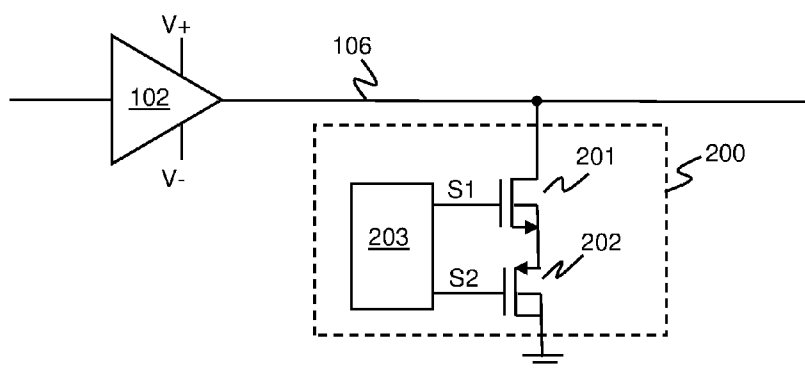
(54) **Title:** CLAMPING CIRCUIT FOR AUDIO SIGNALS

Figure 2

(57) **Abstract:** This application describes methods and apparatus for selectively clamping a signal path (106) for an analogue audio signal to a clamp voltage, e.g. ground. Voltage clamping circuitry (200) is disclosed having a first switching device (201) in series with a second switching device (202) between a node of the signal path and the clamp voltage. The clamping circuitry is configured to be operable in: a first state where the first and second switching devices are both on to electrically connect the signal path to the clamp voltage; and also a second state to electrically disconnect the signal path from the clamp voltage. In the second state one of the first and second switching devices is configured to block conduction when the voltage at said node of the signal path is positive and the other switching device is configured to block conduction when the voltage at said node of the signal path is negative.

CLAMPING CIRCUIT FOR AUDIO SIGNALS

This application relates to methods and apparatus for audio output circuits and especially for voltage clamping of an audio signal path, and in particular for clamping of
5 an audio signal path for outputting an audio signal to an audio accessory such as a set of headphones.

Many electronic devices include an audio output circuit for outputting an analogue audio signal to an accessory or peripheral apparatus that can be removably connected
10 to the electrical device in use. For example, for many portable electronics devices a set of headphones or similar audio accessory may be removably connected to the device, to be driven by an analogue audio signal output from that device. **Figure 1** illustrates an electronic device 100, which will be referred to as the host device, that in use can be connected to an accessory audio apparatus 101, such as a headset, e.g.
15 headphones or earbuds or the like. In use the accessory apparatus 101 may be removably connected to the host device 100 via a suitable connector, e.g. a mating connector such as plug and receptacle arrangement. One well known connector for audio accessories is a 3.5mm jack plug and jack socket arrangement, whether a four pole (TRRS) or three pole (TRS) connector, but other connectors are known, such as
20 USB type connectors, and may be used for analogue audio signals.

The host device 100 includes an audio output stage 102 for driving an audio load, such as a speaker 103, of an accessory apparatus 101 when connected. The audio output stage 102 may thus be connected to a contact or pole 104 of a connector of the host
25 device 101, e.g. a jack socket, which is arranged to make electrical contact with a corresponding contact or pole 105 of a connector, e.g. jack plug, of a suitable accessory apparatus when connected. There is thus an audio signal path 106 between the output stage 102 and contact 104 of the connector.

30 Typically when not being used, e.g. without a suitable audio accessory apparatus connected, the audio output stage 102 is inoperative and typically the audio signal path 106 between the output stage 102 and contact 104 is clamped to ground. Switch 107 is thus provided so as to clamp the audio signal path to ground when closed and opened in use when driving an audio output signal to a connected accessory
35 apparatus.

Embodiments of the present disclosure relate to methods and apparatus for voltage clamping of an audio signal path when not use.

According to an aspect of the present invention there is provided a voltage clamp for an
5 analogue audio signal path comprising:

an n-channel transistor in series with a p-channel transistor between a node of the signal path and a clamp voltage;

the n-channel transistor being configured such that when driven by a positive gate drive voltage above a first threshold the n-channel transistor substantially blocks
10 conduction when the node of the signal path is at a positive voltage;

the p-channel transistor being configured such that when driven by a negative gate drive voltage with a magnitude above a second threshold the p-channel transistor substantially blocks conduction when the node of the signal path is at a negative voltage.

15

The n-channel transistor may comprise a drain terminal connected to the node of the signal path, a source terminal connected to the p-channel transistor and a bulk terminal connected to the source terminal of the n-channel transistor. The p-channel transistor may comprise a drain terminal connected to the clamp voltage, a source terminal
20 connected to the n-channel transistor and a bulk terminal connected to the drain terminal of the p-channel transistor.

Alternatively the p-channel transistor may comprise a drain terminal connected to the node of the signal path, a source terminal connected to the n-channel transistor and a
25 bulk terminal connected to the source terminal of the p-channel transistor. The n-channel transistor may comprise a drain terminal connected to the clamp voltage, a source terminal connected to the p-channel transistor and a bulk terminal connected to the drain terminal of the n-channel transistor.

30 The circuitry may be configured to be operable in: a first state where the n-channel transistor and p-channel transistor are both on to electrically connect the signal path to the clamp voltage; and also a second state electrically disconnect the signal path from the clamp voltage wherein in the second state the n-channel transistor is configured to block conduction when the voltage at said node of the signal path is positive and the p-
35 channel transistor is configured to block conduction when the voltage at said node of the signal path is negative. The first state may be enabled when the gate drive voltage

for the n-channel transistor is positive with a magnitude greater than said first threshold and the gate drive voltage for the p-channel transistor is negative with a magnitude greater than said second threshold. The second state may be enabled when the gate drive voltages for the n-channel transistor and the p-channel transistor are each
5 substantially at ground. The circuit may comprise a controller for generating the gate drive voltages for the n-channel transistor and the p-channel transistor.

According to another aspect of the present invention there is provided voltage clamping circuitry for selectively clamping a signal path for an analogue audio signal to a clamp
10 voltage comprising:

a first switching device in series with a second switching device between a node of the signal path and the clamp voltage;

the clamping circuitry being configured to be operable in:

a first state where the first and second switching devices are both on to
15 electrically connect the signal path to the clamp voltage; and also

a second state electrically disconnect the signal path from the clamp voltage wherein in the second state the first switching device is configured to block conduction when the voltage at said node of the signal path is positive and the second switching device is configured to block conduction when the voltage at said node of the signal
20 path is negative.

The first switching device may comprise a first transistor. The first transistor may comprise a drain terminal connected to the node of the signal path and a source terminal connected to the second switching device. A bulk terminal of the first
25 transistor may be connected to the source terminal of the first transistor.

The second switching device may comprise a second transistor. The second transistor may comprise a drain terminal connected to the clamp voltage and a source terminal connected to the first switching device. A bulk terminal of the second transistor may be
30 connected to the drain terminal of the second transistor.

One of the first and second switching devices may comprise a p-channel transistor and the other of the first and second switching devices may comprise an n-channel transistor. In one embodiment the first switching device is an n-channel transistor and
35 the second switching device is a p-channel transistor. In another embodiment the first

switching device is a p-channel transistor and the second switching device is an n-channel transistor

5 The first and second switching devices may be configured to be controlled by first and second switch control signals respectively. The first state may be enabled when the first switch control signal is positive with a magnitude greater than a first threshold value and the second switch control signal is negative with a magnitude greater than a second threshold value. The second state may be enabled when the first and second switch control signals are each substantially at ground. The circuitry may comprise a
10 controller for generating said first and second switch control signals.

In some embodiments the clamp voltage may be ground, e.g. substantially zero volts.

15 The audio signal path may be a signal path for outputting an audio signal, in use, to an accessory apparatus that may be removably connected to the signal path. The audio signal path may be connected to a contact of a connector of a host device. The audio signal path may be connected to an audio output stage.

20 In some embodiments the peak-to-peak voltage swing of the audio signal path, in use, is greater than the voltage rating of at least one of the first and second switching devices.

Embodiments also provide voltage clamping circuitry for selectively clamping a signal path for an analogue audio signal to a clamp voltage comprising:

25 an n-channel transistor in series with a p-channel transistor between a node of the signal path and the clamp voltage;
wherein a source terminal of the n-channel transistor is connected to a source terminal of the p-channel transistor;
wherein a bulk terminal of the n-channel transistor is connected to its source
30 terminal; and
wherein a bulk terminal of the p-channel transistor is connected to its drain terminal.

35 In one embodiment the drain of the n-channel transistor is connected to the node of the signal path and the drain of the p-channel transistor is connected to the clamp voltage. In another embodiment the drain of the p-channel transistor is connected to the node of

the signal path and the drain of the n-channel transistor is connected to the clamp voltage.

In a further aspect there is provided a voltage clamp for an analogue audio signal path comprising:

an n-channel transistor coupled to a node of the audio signal path; and
a p-channel transistor coupled between the n-channel transistor and a clamp voltage node;

wherein a bulk terminal of the n-channel transistor is electrically connected to the midpoint of series connection with p-channel transistor; and
wherein a bulk terminal of the p-channel transistor is electrically connected to the clamp voltage node.

In a further aspect there is provided a voltage clamp for an analogue audio signal path comprising:

a p-channel transistor coupled to a node of the audio signal path; and
an n-channel transistor coupled between the p-channel transistor and a clamp voltage node;

wherein a bulk terminal of the p-channel transistor is electrically connected to the midpoint of series connection with n-channel transistor; and

wherein a bulk terminal of the n-channel transistor is electrically connected to the clamp voltage node.

The invention will now be described by way of example only with reference to the accompanying drawings, of which:

Figure 1 illustrates an audio output stage for driving an audio load of a connected
5 accessory apparatus;

Figure 2 illustrates voltage clamping circuitry according to an embodiment of the invention; and

10 Figure 3 illustrates voltage clamping circuitry according to another embodiment of the invention.

As discussed above figure 1 illustrates a conventional arrangement for a host device 100 for outputting an analogue audio signal to an accessory apparatus 101 when
15 connected, via a contact 104 of the host device. A switch 107, such an NMOS transistor, is provided to clamp signal path 106, and hence the contact 104, to a desired voltage, usually ground, when not in use, e.g. when no accessory apparatus 101 is connected. Switch 107 is thus closed when the signal path 106 is to be disabled and opened when the signal path 106 is used to output an analogue audio signal.

20 When outputting an audio signal the switch 107 is open (or off). One side of the switch 107 is connected to the audio signal path 106 and thus swings in voltage with the analogue audio signal. The other side of the switch 107 is connected to the desired voltage, i.e. ground. The voltage across the switch thus varies with the output signal, which for a ground referenced audio signal, may vary between peak positive and peak
25 negative values. Conventionally, for driving headphones and the like, the peak-to-peak voltage swing for an audio signal output via such a signal path 106 is relatively low and a standard transistor such as an NMOS transistor may be used for switch 107. By peak-to-peak is meant the variation between the maximum positive signal and
30 maximum negative signal.

It has been appreciated that in some instances however it may be desirable to be able to output audio signals with a greater peak-to-peak voltage swing, say of the order of several volts. In one example the positive and negative supplies, $V+$ and $V-$, for the
35 output stage 102 may be of the order of +3.3V and -3.3V. This can provide a relatively high peak-to-peak voltage swing for the audio signal.

Additionally there is a general desire to reduce the size of integrated circuit components as much as possible, especially for portable devices, and thus increasingly processing technologies that allow for smaller feature sizes, i.e. process nodes of smaller size, are being used for fabrication. Smaller transistors however generally may have a lower voltage rating, i.e. a rating with regard to the voltage stress the device is designed to be able to handle.

As noted above in conventional arrangements the switch 107 may be implemented by an NMOS transistor, as illustrated in figure 1, with its source terminal connected to ground and its bulk terminal coupled to the source terminal, so also at ground. When the switch 107 is off the gate voltage may be held at or near ground. In such an arrangement if the audio signal goes to a relatively large negative value, say around -3V, the voltage between the bulk and drain may be sufficient to forward bias a body diode of the transistor between the p-type bulk and n-type drain, allowing for unwanted leakage from ground.

This could in theory be prevented by biasing the bulk of the transistor to be at or near the negative supply voltage V_- but in such a case when the audio signal swings to a high positive value the voltage difference between the drain terminal and bulk terminal will be relatively high. For instance if the peak positive signal value is of the order of 3V and the bulk is biased to -3.3V then there may, at times, be greater than 6V across the transistor. Equally if the gate voltage is driven to around the positive supply voltage V_+ when the switch 107 is on then voltage between the gate terminal and the bulk terminal will be relatively high.

It has therefore been recognised that there may be situations where it is wished to clamp an audio signal path to a desired voltage, when not in use, where the audio signal path is for, in use, output of an analogue audio signal with a relatively high peak-to-peak voltage swing and/or is implemented in a circuit fabricated using a relatively small process node and a conventional clamp switch may not be adequate.

Embodiments of the present disclosure thus relate to methods and apparatus for clamping an audio signal path to a desired voltage, e.g. ground, and especially where the audio signal path is a signal path for outputting a ground referenced analogue

audio signal to an accessory apparatus, e.g. a signal path for driving headphones or the like.

Embodiments of the present invention relate to voltage clamping circuitry that

5 comprises first and second switching devices in series between a node of the signal path and the clamp voltage. The first and second switching devices are active switching devices, i.e. devices such as transistors where the device can be controllably varied between different switching states, e.g. in response to a signal at a control

10 terminal. The switching devices may, for example, be MOS transistors or the like where a control applied to one terminal, e.g. a gate terminal, may controllably allow current flow between two other terminals. One of the first switching devices comprises an n-channel device and the other switching devices comprises an p-channel device. The source of the first switching device may be connected to the source of the second switching device. The drain of the first switching device may be coupled to the signal

15 path node with the drain of the second switching device coupled to the clamp voltage. The bulk terminal of the first switching device may be coupled to its source terminal, i.e. to the mid-point of the series connection. The bulk terminal of the second switching device is coupled to its drain, i.e. to the clamp voltage.

20 When voltage clamping is required both switching devices may be controlled to an on state so as to clamp the node of the signal path to ground. When the signal path is not to be clamped both devices can be controlled to an off state and at least one of the switching devices will block conduction at relatively high positive voltages at the signal node and at least the other switching device will block conduction at relatively high

25 negative voltages at the signal node.

Figure 2 illustrates one embodiment of voltage clamping circuitry 200 for clamping the signal path 106. The voltage clamping circuitry 200 comprises a first switching device 201 in series with a second switching device 202. The first switching device is

30 electrically connected to the signal path 106 and the second switching device is connected to the desired clamp voltage, in this example ground (zero volts).

The voltage clamping circuitry 200 may be operable in a first state, which may be seen as an on-state, to clamp the signal path to the desired clamp voltage. In this first (on)

35 state both the first and second switching devices 201 and 202 are on, i.e. conductive, simultaneously. The voltage clamping circuitry 200 is also operable in a second state,

which may be seen as an off-state, to disconnect the signal path 106 from clamp voltage. As will be described in more detail below in the second (off) state the first switching device 201 may effectively block conduction through the clamping circuitry 200 during any period of positive voltage of the signal path 106 and the second
5 switching device 202 may effectively block conduction through the clamping circuitry 200 during any period of positive voltage of the signal path 106. This combination thus prevents any substantial current flow through the voltage clamping circuitry 200 and means that the voltage across the first and second switching devices in the second state are no greater than the magnitude of the positive and negative signal voltages
10 respectively.

In this example the first switching device 201 is an n-channel transistor, such as an NMOS, and the second switch 202 is a p-channel transistor, such as a PMOS. In this example the drain of the NMOS 201 is connected to the signal path 106 and the source
15 of NMOS 201 is coupled to the second switching device 202. The bulk terminal of the NMOS 201 is connected to the source terminal.

The source terminal of PMOS 202 is connected to the first switching device 201 and the drain of PMOS 202 is coupled to the clamp voltage, in this case ground. The bulk
20 terminal of PMOS 202 is connected to the drain terminal, and hence in this example connected to ground.

The gate of NMOS 201 is driven by a first switch control signal S1 and the gate of PMOS 202 is driven by a second switch control signal S2. The switch control signals
25 S1 and S2 may be generated by a controller 203 which controls the state of the switch control signals S1 and S2 in accordance with the required state of the voltage clamping circuitry 200.

When the clamping circuitry 200 is operated in the first (on) state to clamp the signal
30 path 106 to the clamp voltage, e.g. ground, the first and second gate control signals are driven to relatively high positive and negative voltages respectively. For instance the first switch control signal S1 may be set to a value +V1 and the second switch control signal S2 may be set to a negative value -V1. In some examples the values +V1 and -V1 may be set to be equal to the positive and negative supply voltages provides to the
35 output stage 102.

The gate voltage of the PMOS 202 is thus sufficiently low for PMOS conduction and the gate voltage of the NMOS 201 is thus sufficiently high for NMOS conduction. Both switching elements are thus on and conductive and the signal path 106 is thus clamped to ground.

5

When the clamping circuitry 200 is operated in the second (off) state to disconnect the signal path 106 from the reference voltage the first and second switch control signals S1 and S2 may be set to be substantially equal to zero volts, i.e. ground. This prevents substantial conduction through the voltage clamping circuitry 200.

10

As noted above in use the signal path voltage will vary depending on the audio signal being output and may vary between being positive and negative within a certain peak-to-peak range. When the audio signal is positive the gate-source voltage of the first switching device, NMOS 201 will be below the relevant threshold voltage and thus the NMOS will block conduction. The PMOS 202 can be seen as effectively being on and thus the bulk of NMOS 201 will be at ground. The maximum voltage across the NMOS 201 will thus be equal to the magnitude of the peak positive audio signal voltage across the drain and source/bulk terminals.

15

When the audio signal is negative the NMOS 201 may be seen as effectively being on but the gate-source voltage of PMOS 202 will be above the relevant threshold such that the PMOS 202 is off and blocks conduction. The maximum voltage across the PMOS 202 will thus be equal to the magnitude of the peak negative audio signal voltage across the source – drain/bulk terminals or equal to the magnitude of the voltage of the second switch control signal between the gate terminal and bulk.

25

In this way the series combination of the first and second switching devices 201 and 202 of the clamping circuitry 200 collectively block any substantial current flow whether the audio signal is positive or negative. As noted the first switching device 201 acts to prevent any current flow when the audio signal is positive and the second switching device 202 acts to prevent any current flow when the audio signal is negative. The maximum voltage across the first switching device is defined by the magnitude of the peak positive audio signal and the maximum voltage across the second switching device is defined by the magnitude of the peak negative audio signal.

30

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Thus, for example if the positive and negative supply voltages for the output stage 102 were of the order of +3.3V and -3.3V and the audio signal had a peak-to-peak voltage swing of around 6V, each of the first and second switching devices 201 and 202 could have an individual voltage rating of about 3.3V and the voltage clamping circuitry 200
5 would operate to clamp the signal path 106 to ground when required but also to prevent substantial conduction through the clamping circuitry 200 when the signal path 106 is in use, without undue voltage stress on the switching devices.

The discussion above in relation to figure 2 refers to an NMOS transistor 201 as the
10 first switching device in series with a PMOS transistor 202 as the second switching device. It will be appreciated that each switching device may, in practice be implemented by a number of individual elements in parallel. As used herein the term the term switching device may thus refer to a switching arrangement or switching circuit, although in some embodiments there may be a single transistor. It will also be
15 appreciated that other types of transistor could be used. Other combinations of switching elements could be arranged to provide the same functionality.

Figure 3 illustrates another example of voltage clamping circuitry 300 for clamping the signal path 106. Again the clamping circuitry has a first and switching devices in
20 series, e.g. first and second transistors 301 and 302, with the sources of the two switching transistors coupled together and the drain of the first transistor 301 coupled to the signal path and the drain of the second transistor 302 coupled to the clamp voltage. The bulk terminal of first transistor 301 is coupled to its source terminal to be tied to the midpoint voltage and the bulk of the second transistor 302 is coupled to its
25 drain terminal to be tied to the clamp voltage. In this example the first switching device 301 is a PMOS transistor and the second switching device 302 is an NMOS transistor. The first and second transistors 301 and 302 are again controlled by a controller 303 that generates gate control signals S1' and S2' in the same manner as described above with respect to figure 2, except in this instance the relative values of the gate
30 control signals are swapped. That is the control signal S1' for the first switching device, i.e. PMOS 301, will have the same value as described above the control signal S2 for PMOS 302 and the control signal S2' for the second switching device, i.e. NMOS 302, will have the same value as described above the control signal S1 for NMOS 301. The embodiment of figure 3 operates in the same way as that described for figure 2, just
35 with the positions of the PMOS and NMOS swapped and the gate control signals swapped accordingly.

The discussion in relation to figures 2 and 3 refers to clamping the signal path to ground, where the signal path is for a ground referenced analogue audio signal, i.e. where the midpoint, quiescent voltage is ground. In some embodiments a different clamping voltage could be used if required, for instance if the signal path were used for a signal of one polarity only, with a quiescent midpoint voltage is equal to a defined value V_{mid} , it may be wished to clamp the signal path to V_{mid} when not in use. In which case the clamp voltage may be equal to V_{mid} and reference to positive and negative in the foregoing discussion should be interpreted with regard to being above or below the midpoint voltage V_{mid} .

Embodiments are particularly applicable to audio signal paths of a host device for outputting an analogue audio signal to a connector of the host device to drive an audio load of a connected accessory. In particular the voltage clamping circuitry may be implemented for voltage clamping of a headphone amplifier of a host device and/or a contact or pole of a connector that, in use, may be used for analogue audio output. The principles however are applicable to any signal path and embodiments may be implemented on a signal path between an audio output stage and an audio load of the host device.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. The word "comprising" does not exclude the presence of elements or steps other than those listed in a claim, "a" or "an" does not exclude a plurality, and a single feature or other unit may fulfil the functions of several units recited in the claims. Any reference numerals or labels in the claims shall not be construed so as to limit their scope. Terms such as amplify or gain include possibly applying a scaling factor of less than unity to a signal.

CLAIMS

1. A voltage clamp for an analogue audio signal path comprising:
an n-channel transistor in series with a p-channel transistor between a node of
5 the signal path and a clamp voltage;
the n-channel transistor being configured such that when driven by a positive
gate drive voltage above a first threshold the n-channel transistor
substantially blocks conduction when the node of the signal path is at a
positive voltage;
10 the p-channel transistor being configured such that when driven by a negative
gate drive voltage with a magnitude above a second threshold the p-
channel transistor substantially blocks conduction when the node of the
signal path is at a negative voltage.
- 15 2. Voltage clamping circuitry as claimed in claim 1 wherein the n-channel transistor
comprises a drain terminal connected to the node of the signal path, a source
terminal connected to the p-channel transistor and a bulk terminal connected to
the source terminal of the n-channel transistor.
- 20 3. Voltage clamping circuitry as claimed in claim 1 or claim 2 wherein the p-channel
transistor comprises a drain terminal connected to the clamp voltage, a source
terminal connected to the n-channel transistor and a bulk terminal connected to
the drain terminal of the p-channel transistor.
- 25 4. Voltage clamping circuitry as claimed in claim 1 wherein the p-channel transistor
comprises a drain terminal connected to the node of the signal path, a source
terminal connected to the n-channel transistor and a bulk terminal connected to
the source terminal of the p-channel transistor.
- 30 5. Voltage clamping circuitry as claimed in claim 1 or claim 4 wherein the n-channel
transistor comprises a drain terminal connected to the clamp voltage, a source
terminal connected to the p-channel transistor and a bulk terminal connected to
the drain terminal of the n-channel transistor.
- 35 6. Voltage clamping circuitry as claimed in any preceding claim, wherein the circuitry
is configured to be operable in:

a first state where the n-channel transistor and p-channel transistor are both on to electrically connect the signal path to the clamp voltage; and also a second state electrically disconnect the signal path from the clamp voltage wherein in the second state the n-channel transistor is configured to block conduction when the voltage at said node of the signal path is positive and the p-channel transistor is configured to block conduction when the voltage at said node of the signal path is negative.

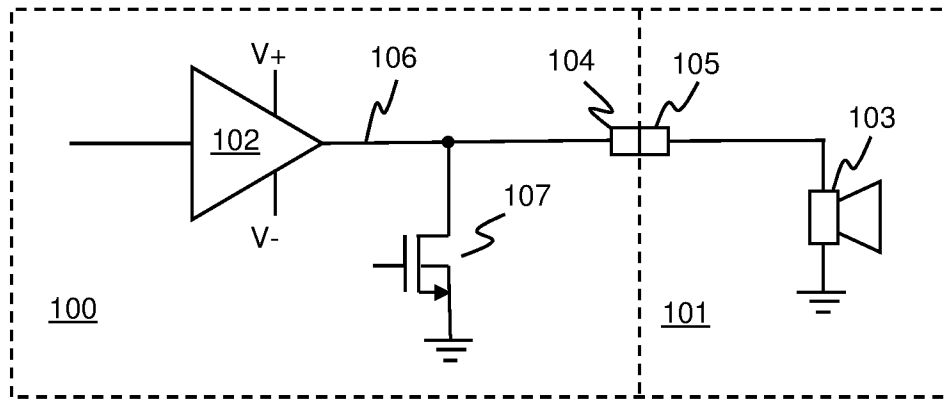
7. Voltage clamping circuitry as claimed in claim 6 wherein said first state is enabled when the gate drive voltage for the n-channel transistor is positive with a magnitude greater than said first threshold and the gate drive voltage for the p-channel transistor is negative with a magnitude greater than said second threshold.
8. Voltage clamping circuitry as claimed in claim 6 or claim 7 wherein said second state is enabled when the gate drive voltages for the n-channel transistor and the p-channel transistor are each substantially at ground.
9. Voltage clamping circuitry as claimed in any of claims 6 to 8 comprising a controller for generating said gate drive voltages for the n-channel transistor and the p-channel transistor.
10. Voltage clamping circuitry as claimed in any preceding claim wherein said clamp voltage is ground.
11. Voltage clamping circuitry as claimed in any preceding claim wherein said audio signal path is a signal path for outputting an audio signal, in use, to an accessory apparatus that may be removably connected to the signal path.
12. Voltage clamping circuitry as claimed in any preceding claim wherein said audio signal path is connected to a contact of a connector of a host device.
13. Voltage clamping circuitry as claimed in any preceding claim wherein said audio signal path is connected to an audio output stage.

14. Voltage clamping circuitry as claimed in any preceding claim wherein a peak-to-peak voltage swing of the audio signal path in use is greater than the voltage rating of at least one of the n-channel transistor and the p-channel transistor.
- 5 15. Voltage clamping circuitry for selectively clamping a signal path for an analogue audio signal to a clamp voltage comprising:
an n-channel transistor in series with a p-channel transistor between a node of
the signal path and the clamp voltage;
wherein a source terminal of the n-channel transistor is connected to a source
10 terminal of the p-channel transistor;
wherein a bulk terminal of the n-channel transistor is connected to its source
terminal; and
wherein a bulk terminal of the p-channel transistor is connected to its drain
terminal.
- 15 16. Voltage clamping circuitry for selectively clamping a signal path for an analogue audio signal to a clamp voltage comprising:
a first switching device in series with a second switching device between a node
of the signal path and the clamp voltage;
20 the clamping circuitry being configured to be operable in:
a first state where the first and second switching devices are both on to
electrically connect the signal path to the clamp voltage; and also
a second state electrically disconnect the signal path from the clamp voltage
wherein in the second state the first switching device is configured to block
25 conduction when the voltage at said node of the signal path is positive and
the second switching device is configured to block conduction when the
voltage at said node of the signal path is negative.
- 30 17. Voltage clamping circuitry for selectively clamping a signal path for an analogue audio signal to a clamp voltage comprising:
a first transistor in series with a second transistor between a node of the signal
path and the clamp voltage;
the clamping circuitry being configured to be operable in:
a first state where the first and second transistors are both on to electrically
35 connect the signal path to the clamp voltage; and also

a second state electrically disconnect the signal path from the clamp voltage wherein in the second state at least one of the first and second transistors is configured to block conduction when the voltage at said node of the signal path is positive and at least the other of the first and second transistors is configured to block conduction when the voltage at said node of the signal path is negative.

18. A voltage clamp for an analogue audio signal path comprising:
an n-channel transistor coupled to a node of the audio signal path; and
a p-channel transistor coupled between the n-channel transistor and a clamp voltage node;
wherein a bulk terminal of the n-channel transistor is electrically connected to the midpoint of series connection with p-channel transistor; and
wherein a bulk terminal of the p-channel transistor is electrically connected to the clamp voltage node.

19. A voltage clamp for an analogue audio signal path comprising:
a p-channel transistor coupled to a node of the audio signal path; and
an n-channel transistor coupled between the p-channel transistor and a clamp voltage node;
wherein a bulk terminal of the p-channel transistor is electrically connected to the midpoint of series connection with n-channel transistor; and
wherein a bulk terminal of the n-channel transistor is electrically connected to the clamp voltage node.



PRIOR ART
Figure 1

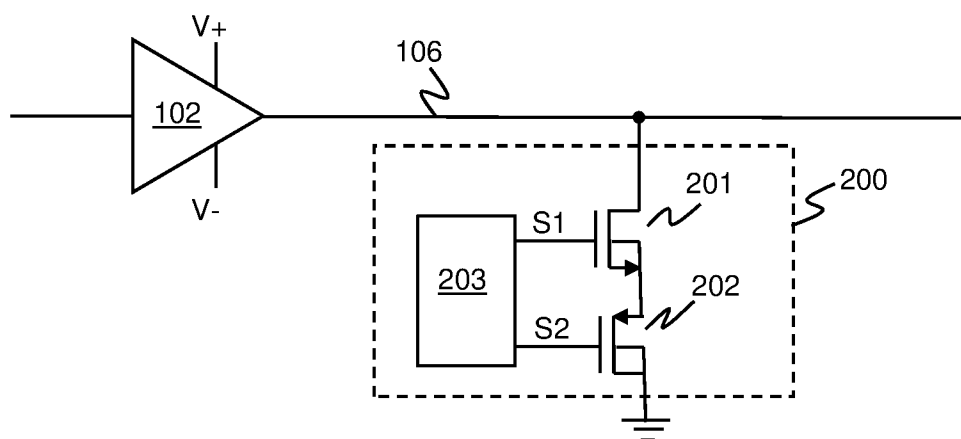


Figure 2

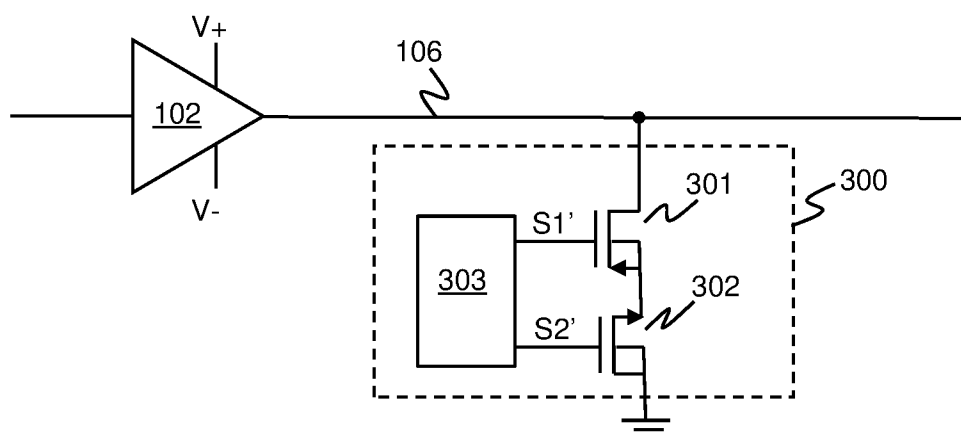


Figure 3

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2017/050478

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04R3/00 H03K19/0185
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04R H03K H03G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 7 321 238 B1 (REID DAVID [AU]) 22 January 2008 (2008-01-22) figure 3	1-19
X	----- EP 0 453 651 A1 (SIEMENS AG [DE]) 30 October 1991 (1991-10-30) figure 3	1-19
X	----- US 9 088 274 B1 (CHAUDHRY NIDHI [IN] ET AL) 21 July 2015 (2015-07-21) figure 1	1-19



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

7 April 2017

Date of mailing of the international search report

19/04/2017

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Rogala, Tomasz

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/GB2017/050478

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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			EP 0453651 A1 30-10-1991
			IE 911333 A1 23-10-1991
			JP H07122991 A 12-05-1995

US 9088274	B1	21-07-2015	NONE
