(12) UK Patent Application (19) GB (11) 2 291 295 (13) A

(43) Date of A Publication 17.01.1996

(21) Application No 9514270.9

(22) Date of Filing 13.07.1995

(30) Priority Data
(31) 9416974 (32) 14.07.1994 (33) KR

(71) Applicant(s)
Hyundai Electronics Industries Co. Ltd.

(Incorporated in the Republic of Korea)

San 136-1,Ami-Ri, Bubal-eub, Ichon-Kun, Kyoungki-Do 467-860, Republic of Korea

(72) Inventor(s)
Young Nam Oh

(74) Agent and/or Address for Service
W H Beck, Greener & Co
7 Stone Buildings, Lincoln's Inn, LONDON, WC2A 3SZ, United Kingdom

(51) INT CL^6
H03K 19/003 19/0185

(52) UK CL (Edition O)
H3P PHFC
H3T T2B6 T2T3F T4D T5E
U1S S2088 S2121

(56) Documents Cited
US 5157282 A US 5149991 A US 5144161 A

(58) Field of Search
UK CL (Edition N) H3P PHFC PHFX
INT CL^6 H03K 19/003

(54) Low-noise CMOS output driver

(57) An NMOS transistor Q3 is inserted between the pull-down transistor Q2 and the negative supply Vss to reduce the impulsive current transient which occurs when the output node N3 is driven low after being high. The series transistor Q3 is initially diode-connected via Q4, but is then turned fully on by Q5 when signal N4, which is delayed with respect to N2 by the inverter chain G7, G8, goes low. Transistor Q3 may be permanently enabled, dependent on the supply voltage (figure 5).

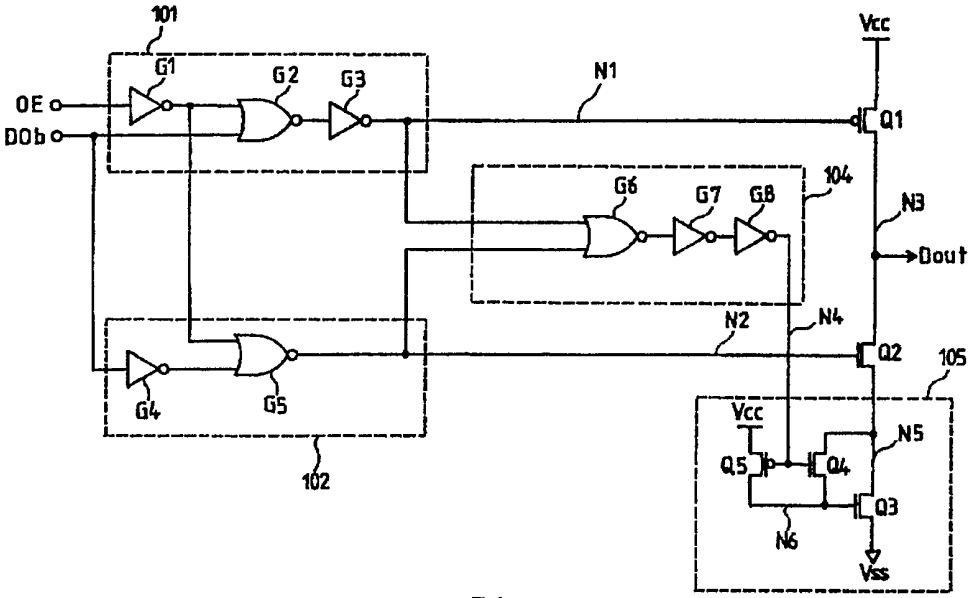

Fig.3

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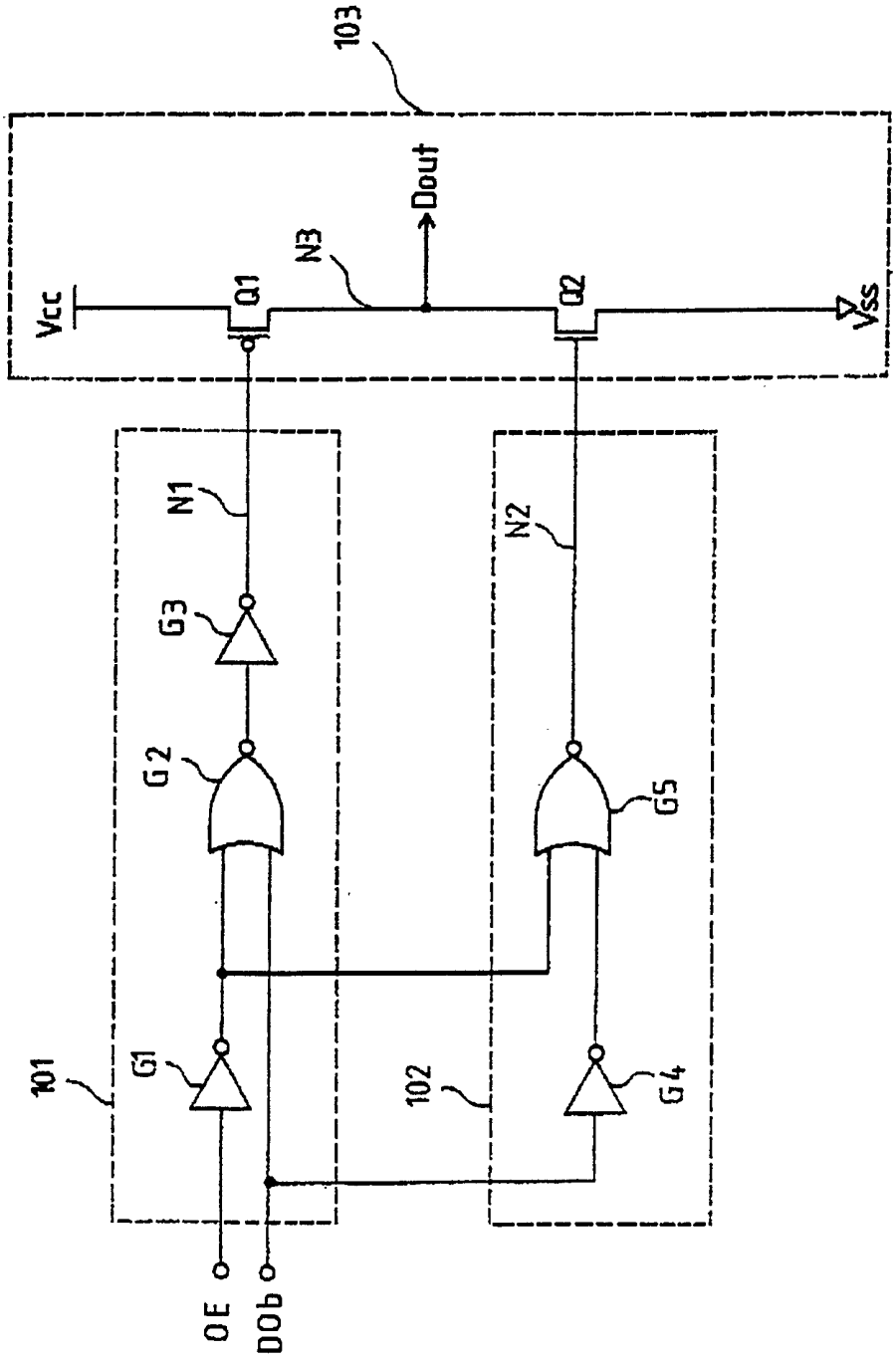
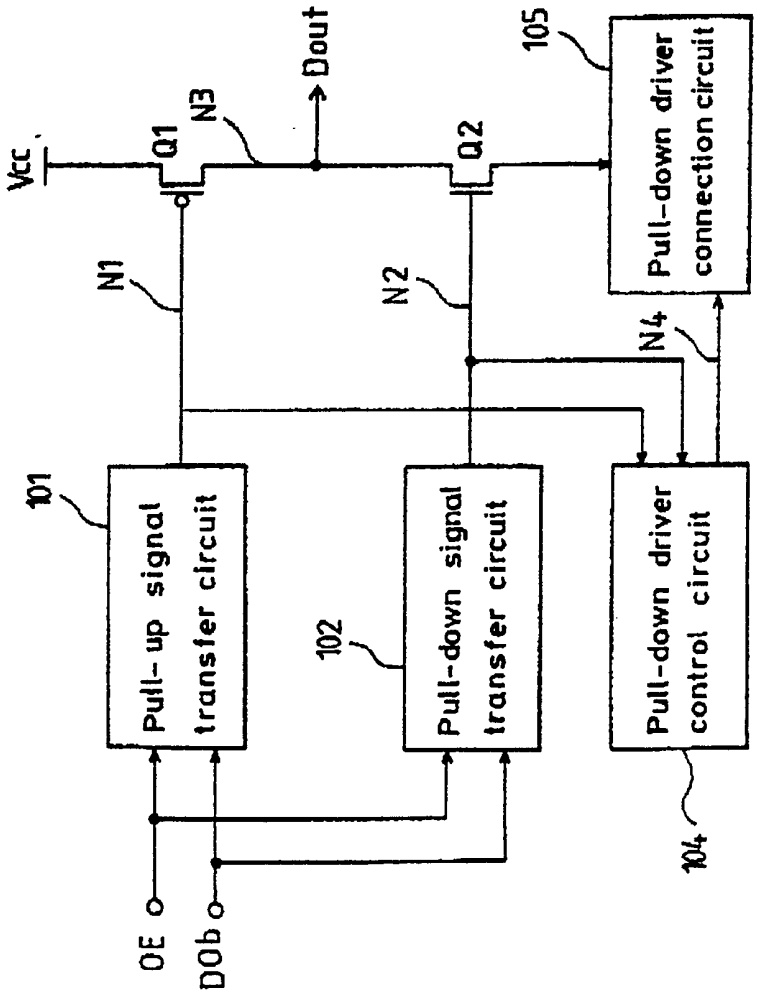


Fig . 1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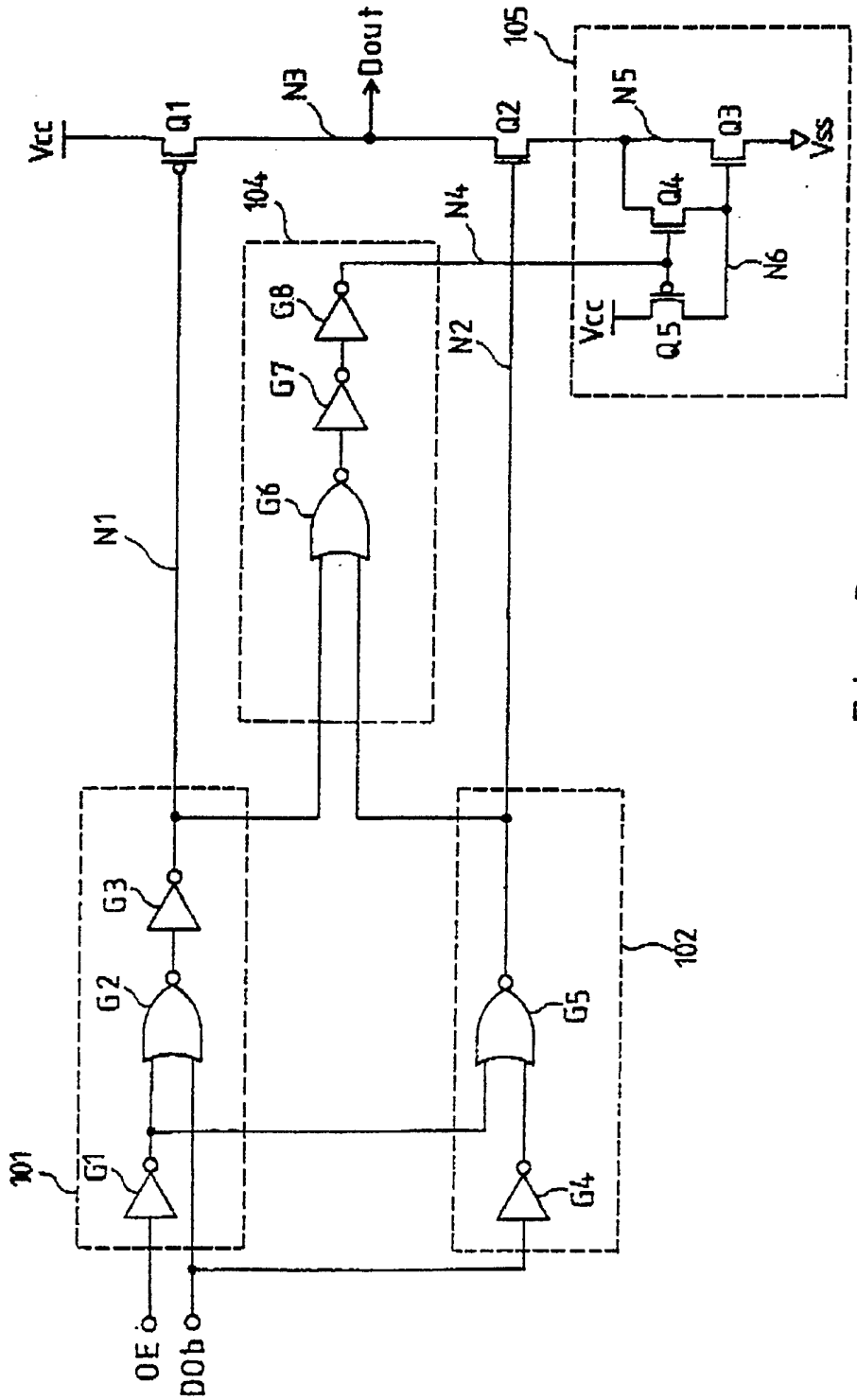
Q1
N3
Dout
Q2
105
Pull-down driver connection circuit
N1
N2
N4
101
Pull-up signal transfer circuit
102
Pull-down signal transfer circuit
Pull-down driver control circuit
104
OE
DOb

Fig. 2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G6
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Vcc
Q5
N1
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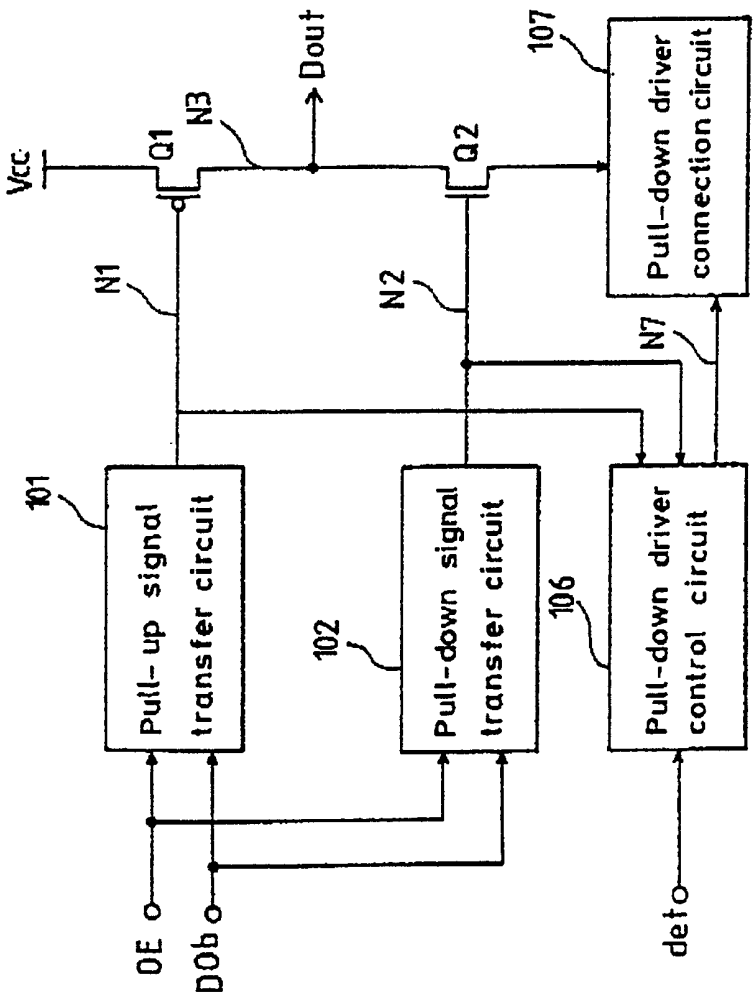
G2
G5
102
101
G1
G4
OE
DOb

Fig.3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Dout
Q2
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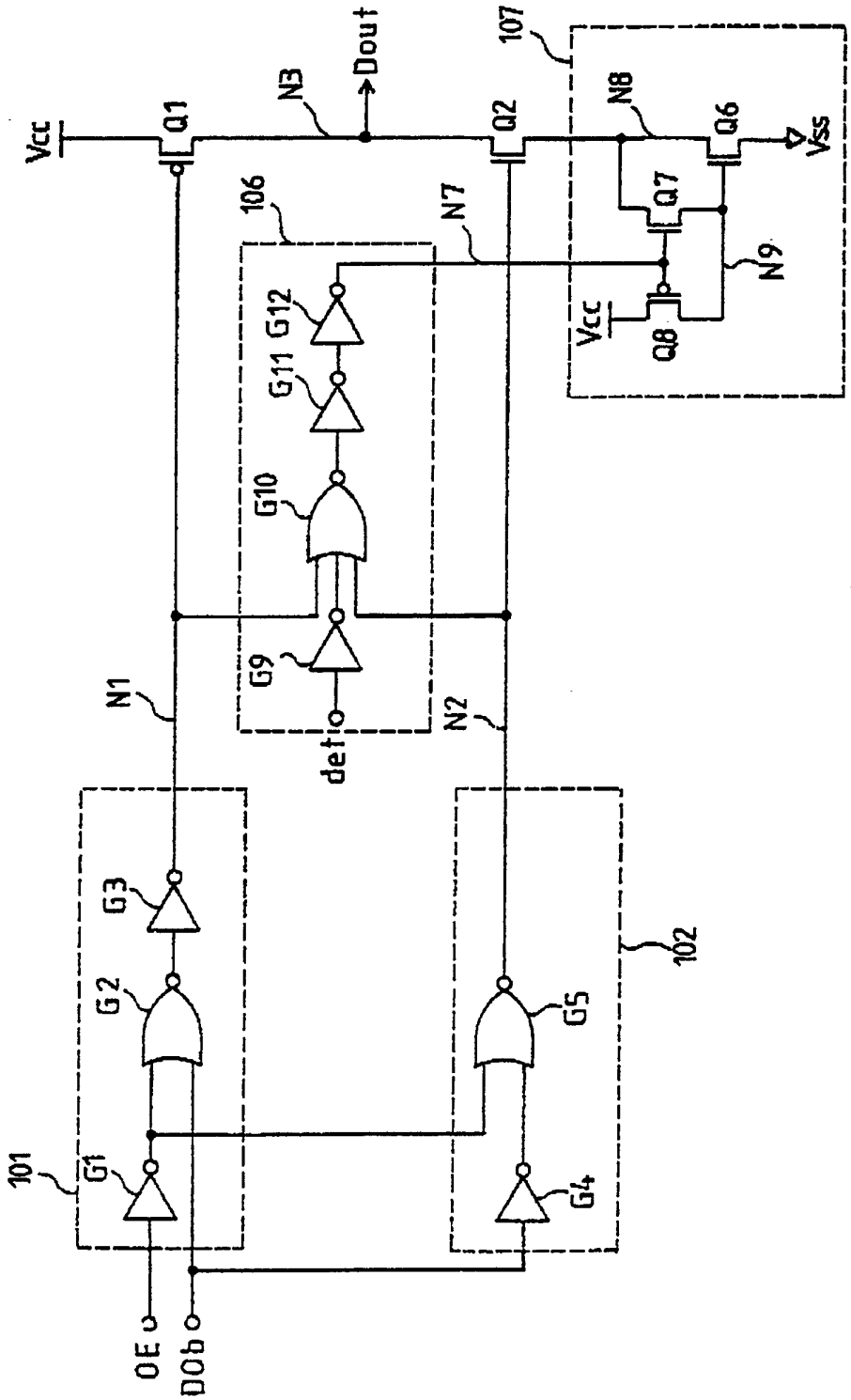
Pull-down driver connection circuit
N1
N2
N7
101
Pull-up signal transfer circuit
102
Pull-down signal transfer circuit
106
Pull-down driver control circuit
OE
DOb
det

Fig. 4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Q7
N9
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N7
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G11
G10
G9
Vcc
Q8
det
N1
N2
G3
G2
G1
101
G5
G4
102
OE
DOb

Fig. 5

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DATA OUTPUT BUFFER

The present invention relates to a data output buffer. For example, a data output buffer of the invention may be used in a semiconductor memory device.

The present invention seeks to provide a data output buffer in which impulse noise components on the data output line are reduced.

According to a first aspect of the present invention there is provided a data output buffer comprising:

a pull-up driver coupled between a first voltage source and a data output line;

a pull-down driver coupled between a second voltage source and said data output line;

a pull-down driver connection circuit coupled between said pull-down driver and said second voltage source; and

a pull-down driver control circuit generating a control signal in dependence upon the value of an input data signal.

A data output buffer of an embodiment of the invention is able to control the amount of current flowing through the pull-down driver in a multi-step manner which can be applied to all highly integrated circuits.

The present invention also extends to a data output buffer comprising:

a pull-down driver for amplifying a second logic value of an input data signal;

a pull-down connection circuit for varying the impedance of said pull-down driver; and

a pull-down driver control circuit for detecting whether the input data signal has its second logic value

and controlling the pull-down connection circuit in dependence upon the logic value detected.

In an embodiment, the data output buffer further comprises a pull-up driver for amplifying a first logic value of said input data signal.

An embodiment of a data output buffer of the invention is arranged to control an instantaneous current amount di/dt flowing through the pull-down driver to minimize an impulse noise component in output data on the data output line.

According to a further aspect of the invention there is provided a data output buffer comprising:

a pull-up driver connected between a first voltage source and a data output line, for amplifying a first logic value of an input data signal;

a pull-down driver connected between a second voltage source and said data output line, for amplifying a second logic value of said input data signal;

a pull-down driver connection circuit connected between said pull-down driver and said second voltage source, for varying an impedance of said pull-down driver; and

a pull-down driver control circuit for detecting whether said input data signal has its second logic value and generating a control signal in accordance with the detected result to control the operation of said pull-down driver connection circuit.

In an embodiment, said first logic value of said input data signal is low and said second logic value of said input data signal is high.

Preferably, said first voltage source generates a high

voltage and said second voltage source generates a low voltage.

In a preferred embodiment, said pull-down driver connection circuit comprises:

a first NMOS transistor coupled between a first node and said second voltage source, said first node being connected to said pull-down driver;

a second NMOS transistor coupled between said first node and a second node, said second node being connected to a gate of said first NMOS transistor; and

a PMOS transistor coupled between said first voltage source and said second node, said PMOS transistor being driven complementarily to said second NMOS transistor in response to an output signal from said pull-down driver control circuit.

The pull-down driver control circuit may comprise an inverter chain for inverting said first or second logic value of said input data signal and delaying the resultant signal for a predetermined time period. For example, said pull-down driver control circuit further comprises a switch for switching said input data signal to said inverter chain in response to an output enable signal. Preferably, said inverter chain includes an even number of inverters and said switch is a NOR gate.

In an embodiment, said pull-down driver control circuit receives a voltage detect signal, said voltage detect signal having a logic value depending on a difference between voltages from said first and second voltage sources, said pull-down driver control circuit selectively driving said pull-down driver connection circuit in response to the logic values of said voltage detect signal and said input data signal.

For example, said pull-down driver control circuit comprises:

a NOR gate for NORing said input data signal and said voltage detect signal; and

an inverter chain for delaying an output signal from said NOR gate for a predetermined time period and transferring the delayed signal to said pull-down driver connection circuit.

Embodiments of the present invention will hereinafter be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a circuit diagram of a substantially conventional data output buffer;

Figure 2 is a block diagram of a data output buffer of an embodiment of the present invention;

Figure 3 is a circuit diagram of the data output buffer of Figure 2;

Figure 4 is a block diagram of a data output buffer of a further embodiment of the present invention; and

Figure 5 is a circuit diagram of the data output buffer of Figure 4.

Figure 1 shows an example of a substantially conventional data output buffer. In the case where output data on a data output line N3 is low in logic, a difference between a voltage on a node N2 and a ground voltage from a ground voltage source Vss becomes large, thereby causing a pull-down transistor Q2 to be turned on. As the pull-down transistor Q2 is turned on, a voltage on the data output line N3 is transferred to the ground voltage source Vss. At this time, an amount of current flowing through the pull-down transistor Q2 to the ground voltage source Vss instantaneously varies abruptly, resulting in the generation of a very high impulse noise component in the low logic output data on the data output line N3.

On the other hand, in the case where a control signal OE is high on logic and an input data signal DOb on a data input line is low in logic, a pull-up transistor Q1 is turned on, thereby causing the data output line N3 to maintain a high voltage corresponding to a supply voltage. When the input data signal DOb on the data input line goes from low to high in logic, the current flowing through the pull-down transistor Q2 is abruptly increased in amount because of the high voltage on the data output line N3. Namely, the noise component included in the output data on the data output line N3 varies more abruptly as the supply voltage is increased.

Figure 2 shows a block diagram of a data output buffer of an embodiment of the present invention. Some parts in this drawing are the same as those in Figure 1, and like reference numerals designate similar or like parts. As shown in Figure 2, the data output buffer comprises a pull-down driver connection circuit 105 and a pull-down driver control circuit 104 in addition to the construction of the conventional data output buffer in Figure 1. The pull-down driver control circuit 104 is arranged to control the pull-down driver connection circuit 105.

The pull-down driver connection circuit 105 is connected between the pull-down transistor Q2 and the ground voltage source Vss to make variations in the current amount through the pull-down transistor Q2 gentle. The pull-down driver control circuit 104 is arranged to control the pull-down driver connection circuit 105 in response to logic states of the control signal OE and the input data signal DOb.

Figure 3 shows a circuit diagram of the data output buffer of Figure 2. The operation of the data output

buffer with the above-described construction in accordance with an embodiment of the invention will hereinafter be described with reference to Figures 2 and 3.

When the control signal OE is high in logic and the input data signal DOb from a memory cell (not shown) is low in logic, a pull-up signal transfer circuit 101 generates a low logic signal on a node N1. To this end, the pull-up signal transfer circuit 101 includes an inverter G1 for inverting the control signal OE, a NOR gate G2 for NORing an output signal from the inverter G1 and the input data signal DOb, and an inverter G3 for inverting an output signal from the NOR gate G2. The pull-up transistor Q1 is turned on in response to the low logic signal on the node N1 to generate high logic output data Dout on the data output line N3.

A pull-down signal transfer circuit 102 includes an inverter G4 for inverting the input data signal DOb, and a NOR gate G5 for NORing an output signal from the inverter G4 and the output signal from the inverter G1 in the pull-up signal transfer circuit 101. When the control signal OE is high in logic and the input data signal DOb is high in logic, the pull-down signal transfer circuit 102 generates a high logic signal on the node N2. The pull-down transistor Q2 is turned on in response to the high logic signal on the node N2 to generate low logic output data Dout on the data output line N3.

The pull-down driver control circuit 104 includes a NOR gate G6 for NORing the logic signals on the nodes N1 and N2, and an inverter series circuit for delaying an output signal from the NOR gate G6 for a predetermined time period and supplying the delayed signal to the pull-down driver connection circuit 105 through a node N4. The inverter series circuit is provided with two inverters G7

and G8. Under the condition that the control signal OE remains at its high logic state, the pull-down driver control circuit 104 generates a logic signal on the node N4 by delaying the input data signal DOb by propagation delay times of the NOR gate G6 and two inverters G7 and G8 and inverting the delayed signal in logic.

The pull-down driver connection circuit 105 includes an NMOS transistor Q4 and a PMOS transistor Q5 being driven complementarily to each other in response to the logic signal on the node N4. In a standby mode in which the control signal OE is low in logic, the logic signal on the node N4 becomes low in logic because the logic signals on the nodes N1 and N2 have their different logic states. In this case, the PMOS transistor Q5 is turned on in response to the low logic signal on the node N4 to transfer a supply voltage from a supply voltage source Vcc to a gate of an NMOS transistor Q3 connected between the pull-down transistor Q2 and the ground voltage source Vss. As a result, the NMOS transistor Q3 is driven in response to the supply voltage from the supply voltage source Vcc to allow a large amount of current to be passed to the ground voltage source Vss through the pull-down transistor Q2 and a node N5.

In an active mode in which the control signal OE is high in logic, the logic signal on the node N4 has the opposite logic state to that of the input data signal DOb and a waveform which is delayed by a predetermined time period from the input data signal DOb. Namely, when the input data signal DOb is changed from high to low in logic, the logic signal on the node N4 is changed from low to high in logic after the lapse of the predetermined time period from a falling edge of the input data signal DOb. When the input data signal DOb is changed from low to high in logic, the logic signal on the node N4 is changed from high to low

in logic after the lapse of the predetermined time period from a rising edge of the input data signal DOb.

As described above, the pull-down driver connection circuit 105 includes the NMOS transistors Q3 and Q4 and the PMOS transistor Q5. The NMOS transistor Q3 is connected between the node N5 and the ground voltage source Vss. The NMOS transistor Q4 is connected between the node N5 and a node N6 which is connected to the gate of the NMOS transistor Q3. The PMOS transistor Q5 is connected between the supply voltage source Vcc and the gate of the NMOS transistor Q3. When the logic signal on the node N4 is high in logic, the NMOS transistor Q4 is turned on to supply a varying voltage Vss + Vtn from the node N5 to the node N6. Noticeably, the NMOS transistor Q4 is turned off after the lapse of a predetermined time period from the turning-on of the pull-down transistor Q2. At this time, the varying voltage Vss + Vtn on the node N5 has a linear characteristic in that it is increased from the ground voltage Vss to a predetermined voltage (for example, supply voltage Vcc/2) and then reduced to the ground voltage Vss.

In the case where the logic signal on the node N4 is low in logic, the PMOS transistor Q5 is turned on to transfer the supply voltage from the supply voltage source Vcc to the node N6. Noticeably, the PMOS transistor Q5 is turned on after the lapse of the predetermined time period from the turning-on of the pull-down transistor Q2.

For example in the case where the output data on the data output line N3 is low in logic, the logic signal on the node N4 remains at its high logic state in response to the previous input data signal DOb. Also, the NMOS transistor Q4 remains at its ON state, whereas the PMOS transistor Q5 remains at its OFF state. The pull-down transistor Q2 is turned on in response to the logic signal

on the node N2 being high in logic, thereby causing current from the data output line N3 to abruptly flow to the node N5. At this time, the varying voltage Vss + Vtn on the node N5 begins to be increased from the ground voltage Vss. It should be noted that the high logic signal on the node N2 results from the present input data signal DOb. The varying voltage Vss + Vtn on the node N5 is transferred to the gate of the NMOS transistor Q3 through the NMOS transistor Q4 and the node N6. In response to the varying voltage Vss + Vtn on the node N5, the NMOS transistor Q3 allows an amount of current flowing from the node N5 to the ground voltage source Vss to be slowly increased. As a result, an amount of current flowing from the data output line N3 to the ground voltage source Vss and the varying voltage Vss + Vtn on the node N5 are gently increased and then slowly reduced. In result, the voltage on the data output line N3 is discharged at a gradually increasing speed and then at a gradually decreasing speed.

When the logic signal on the node N4 is changed from high to low in logic in response to the present input data signal DOb, the NMOS transistor Q4 is turned off, whereas the PMOS transistor Q5 is turned on. As being turned on, the PMOS transistor Q5 transfers the supply voltage from the supply voltage source Vcc to the gate of the NMOS transistor Q3 through the node N6. At this time, the NMOS transistor Q3 is driven in response to the supply voltage from the supply voltage source Vcc to make a current path from the node N5 to the ground voltage source Vss large, so that the remaining voltage on the data output line N3 can be fully discharged. In this manner, a minimized impulse noise component can be present in the low logic output data on the data output line N3.

Figure 4 shows a block diagram of a further embodiment of a data output buffer of the invention. The construction

of the embodiment shown in Figure 4 is substantially the same as that of the embodiment shown in Figure 2, with the exception that a voltage detect signal det from a voltage detector (not shown) is additionally supplied to a pull-down driver control circuit 106.

The operation of the data output buffer of the further embodiment of the invention will now be described with reference to Figure 5 which shows a circuit diagram of the data output buffer of Figure 4.

In the case where the supply voltage is low, the voltage on the data output line N3 is slowly discharged through the sequential steps in the same manner as that in Figure 3, resulting in a reduction in the data output speed. In order to prevent such a reduction in the data output speed, the voltage detect signal det from the voltage detector remains at its low logic state.

In this case, the pull-down driver control circuit 106 generates a low logic signal and supplies the generated low logic signal to a pull-down driver connection circuit 107 through a node N7. To this end, the pull-down driver control circuit 106 includes an inverter G9 for inverting the voltage detect signal det from the voltage detector, a NOR gate G10 for NORing the logic signal on the node N1 which is the output signal from the pull-up signal transfer circuit 101, the logic signal on the node N2 which is the output signal from the pull-down signal transfer circuit 102 and an output signal from the inverter G9, and an inverter series circuit for delaying an output signal from the NOR gate G10 for a predetermined time period and supplying the delayed signal to the pull-down driver connection circuit 107 through the node N7. The inverter series circuit is provided with two inverters G11 and G12.

When the logic signal on the node N7 is low in logic, the pull-down driver connection circuit 107 makes a current path between the data output line N3 and the ground voltage source Vss large to the maximum. Namely, an impedance between the data output line N3 and the ground voltage source Vss becomes the minimum. For this reason, the voltage on the data output line N3 is rapidly discharged to the ground voltage source Vss. To this end, the pull-down driver connection circuit 107 includes an NMOS transistor Q6 connected between a node N8, which is connected to the pull-down transistor Q2, and the ground voltage source Vss, an NMOS transistor Q7 connected between the node N8 and a node N9 connected to a gate of the NMOS transistor Q6, and a PMOS transistor Q8 connected between the supply voltage source Vcc and the gate of the NMOS transistor Q6.

In the case where the logic signal on the node N7 is low in logic, the NMOS transistor Q7 is turned off, whereas the PMOS transistor Q8 is turned on. As being turned on, the PMOS transistor Q8 transfers the supply voltage from the supply voltage source Vcc to the gate of the NMOS transistor Q6 through the node N9. At this time, the NMOS transistor Q6 is driven in response to the supply voltage from the supply voltage source Vcc in such a manner that the voltage on the data output line N3 can be rapidly discharged to the ground voltage source Vss through the pull-down transistor Q2 and the node N8.

The embodiments of the data output buffer disclosed and illustrated can control the amount of current flowing through the pull-down transistor to the ground voltage source in a multi-step manner to minimize the impulse noise component in the low logic output data. Also, the embodiments of the data output buffer described can control the amount of current flowing through the pull-down transistor to the ground voltage source in response to the

supply voltage. Therefore, data output buffers of the invention have the effect of performing the high-speed operation even when the supply voltage is low.

Although the preferred embodiments of the present invention have been disclosed for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope of the invention as defined in the accompanying claims.

CLAIMS

1. A data output buffer comprising:

a pull-up driver coupled between a first voltage source and a data output line;

a pull-down driver coupled between a second voltage source and said data output line;

a pull-down driver connection circuit coupled between said pull-down driver and said second voltage source; and

a pull-down driver control circuit generating a control signal in dependence upon the value of an input data signal.

2. A data output buffer comprising:

a pull-down driver for amplifying a second logic value of an input data signal;

a pull-down connection circuit for varying the impedance of said pull-down driver; and

a pull-down driver control circuit for detecting whether the input data signal has its second logic value and controlling the pull-down connection circuit in dependence upon the logic value detected.

3. A data output buffer as claimed in Claim 2, further comprising a pull-up driver for amplifying a first logic value of said input data signal.

4. A data output buffer comprising:

a pull-up driver connected between a first voltage source and a data output line, for amplifying a first logic value of an input data signal;

a pull-down driver connected between a second voltage source and said data output line, for amplifying a second logic value of said input data signal;

a pull-down driver connection circuit connected between said pull-down driver and said second voltage

source, for varying an impedance of said pull-down driver; and

a pull-down driver control circuit for detecting whether said input data signal has its second logic value and generating a control signal in accordance with the detected result to control the operation of said pull-down driver connection circuit.

5. A data output buffer as claimed in Claim 4, wherein said first logic value of said input data signal is low and said second logic value of said input data signal is high.

6. A data output buffer as claimed in Claim 4 or Claim 5, wherein said first voltage source generates a high voltage and said second voltage source generates a low voltage.

7. A data output buffer as claimed in any preceding claim, wherein said pull-down driver connection circuit comprises:

a first NMOS transistor coupled between a first node and said second voltage source, said first node being connected to said pull-down driver;

a second NMOS transistor coupled between said first node and a second node, said second node being connected to a gate of said first NMOS transistor; and

a PMOS transistor coupled between said first voltage source and said second node, said PMOS transistor being driven complementarily to said second NMOS transistor in response to an output signal from said pull-down driver control circuit.

8. A data output buffer as claimed in any preceding claim, wherein said pull-down driver control circuit comprises an inverter chain for inverting said first or second logic value of said input data signal and delaying the resultant signal for a predetermined time period.

9. A data output buffer as claimed in Claim 8, wherein said pull-down driver control circuit further comprises a switch for switching said input data signal to said inverter chain in response to an output enable signal.

10. A data output buffer as claimed in Claim 9, wherein said inverter chain includes an even number of inverters and said switch is a NOR gate.

11. A data output buffer as claimed in any preceding claim, wherein said pull-down driver control circuit receives a voltage detect signal, said voltage detect signal having a logic value depending on a difference between voltages from said first and second voltage sources, said pull-down driver control circuit selectively driving said pull-down driver connection circuit in response to the logic values of said voltage detect signal and said input data signal.

12. A data output buffer as claimed in Claim 11, wherein said pull-down driver control circuit comprises:

a NOR gate for NORing said input data signal and said voltage detect signal; and

an inverter chain for delaying an output signal from said NOR gate for a predetermined time period and transferring the delayed signal to said pull-down driver connection circuit.

13. A data output buffer substantially as hereinbefore described with reference to Figures 2 to 5 of the accompanying drawings.

Patents Act 1977
E· ıiner's report to the Comptroller under Section 17
(The Search report)

Application number
GB 9514270.9

Relevant Technical Fields

(i) UK Cl (Ed.N) H3P (PHFC, PHFX)

(ii) Int Cl (Ed.6) H03K (19/003)

Search Examiner
K SYLVAN

Date of completion of Search
10 OCTOBER 1995

Databases (see below)
(i) UK Patent Office collections of GB, EP, WO and US patent specifications.

(ii)

Documents considered relevant following a search in respect of Claims :-
1-13

Categories of documents

X: Document indicating lack of novelty or of inventive step.

Y: Document indicating lack of inventive step if combined with one or more other documents of the same category.

A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

&: Member of the same patent family; corresponding document.

Category	Identity of document and relevant passages		Relevant to claim(s)
X	US 5157282	(CYPRESS) see Figure 4	1 at least
X	US 5149991	(N.S.) see Figure 6	1 at least
X	US 5144161	(OKI)	1 at least

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