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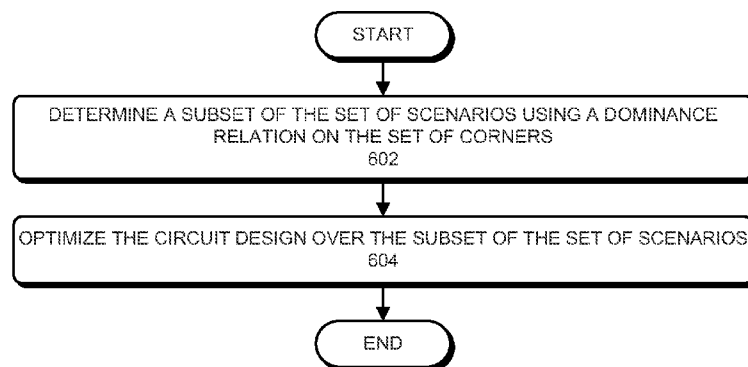


FIG. 6

(57) Abstract: Some embodiments of the present invention provide techniques and systems for performing scenario reduction using a dominance relation on a set of corners. During operation, the system can receive a design library which specifies gate characteristics at each corner in a set of corners. Next, the system can use the design library to determine a dominance relation on the set of corners for each gate type. The dominance relations can be stored with the design library. The system can then receive a set of scenarios over which a circuit design is to be optimized. Next, the system can determine a subset of the set of scenarios using one or more dominance relations on the set of corners. The system can then optimize the circuit design over the subset of the set of scenarios.



PERFORMING SCENARIO REDUCTION USING A DOMINANCE RELATION ON A SET OF CORNERS

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Technical Field

10 [0001] This disclosure relates to electronic design automation (EDA). More specifically, this disclosure relates to methods and apparatuses for performing scenario reduction using a dominance relation on a set of corners.

BACKGROUND

15 Related Art

 [0001] The relentless miniaturization and increasing complexity of integrated circuits have been key driving forces behind the rapid advances in computer technology.

 [0002] The advance to smaller semiconductor geometries has increased the variability in process and operating conditions of integrated circuits. A process corner is a particular set of
20 process conditions under which the circuit design may be manufactured. An operating corner is a particular set of operating conditions (e.g., temperature, voltage) under which the circuit design may operate. The term “corner” can refer to a process corner, an operating corner, or a combination thereof.

 [0003] One reason for the increase in complexity of circuit designs is the introduction of
25 a large number of operational modes (e.g., stand-by, mission, test, etc.). Different operational modes (or “modes” for short) can have drastically different voltages and clock speeds. In fact, some parts of the circuit design may be completely switched off in certain modes.

 [0004] Note that modes are different from corners. Specifically, modes are design dependent, i.e., the circuit design dictates the different modes in which a circuit design can
30 operate. For example, typical modes for a circuit design include, but are not limited to, a normal mode, a sleep mode, a stand-by mode, and a test mode. On the other hand, a corner depends on the ambient conditions that are expected to occur during manufacturing and/or operation. For example, if a chip is expected to be used over a temperature range of -40° C to 80° C, then the circuit designer may define multiple corners that are associated with different operating
35 temperatures.

[0005] An important goal is to ensure that a circuit design meets the functional and performance requirements under all conditions that are expected to occur. The term “Multi-Corner/Multi-Mode (MCMM) scenario,” or “scenario” for short, refers to a combination of a corner and a mode.

5 [0006] Circuit optimization is a complex task that can consume a significant portion of the circuit design time. Therefore, the task of optimizing a circuit design across multiple scenarios can easily become computationally intensive if the number of scenarios is large.

[0007] Unfortunately, the number of scenarios over which circuit designs are desired to be optimized is increasing rapidly as semiconductor geometries become smaller and circuit
10 designs become more complex.

SUMMARY

[0008] Some embodiments of the present invention provide techniques and systems for
15 reducing the number of scenarios over which a circuit design is optimized. During optimization, the circuit design is modified so that one or more design constraints are met over a set of scenarios, wherein each scenario in the set of scenarios can be associated with a corner and a mode. A corner can be associated with an operating temperature and a power supply voltage. The set of modes can include, but is not limited to, a normal mode, a sleep mode, a standby
20 mode, and a test mode.

[0009] In some embodiments, the system can receive a set of scenarios over which the circuit design is to be optimized. Next, the system can determine a subset of the set of scenarios using a dominance relation on the set of corners such that if the circuit design meets a set of design constraints in each scenario in the subset of the set of scenarios, the circuit design is
25 expected to meet the set of design constraints in each scenario in the set of scenarios. The system can then optimize the circuit design over the subset of the set of scenarios. In some embodiments, the system can update circuit information only in the subset of the set of scenarios whenever a gate is changed in the circuit design during optimization, thereby substantially reducing the amount of computation required to optimize the circuit design. Note that a subset of
30 a set can include all or a portion of the set.

[0010] In some embodiments, the system can determine the subset of the set of scenarios by removing a first scenario from the set of scenarios if the first scenario and a second scenario in the set of scenarios are associated with the same mode and a first corner associated with the first scenario is dominated by a second corner associated with the second scenario. Note that the
35 second corner dominates the first corner if the delay and output transition time values in the

second corner are greater than or equal to the corresponding delay and output transition time values in the first corner over different sized implementations of a gate type, input transition times, and capacitive load values.

The term “gate type” can refer to a family of gates that performs a particular logical function (e.g., AND, OR, NAND, etc.). A library typically includes different sized implementations of each gate type. Each cell in the target technology library that is being used to optimize the circuit design is typically an implementation of a gate type.

[0011] In some embodiments, the system can determine the dominance relation on the set of corners as follows. The system can represent the set of corners by a set of points in an n-dimensional space, wherein each corner in the set of corners is associated with a point in the set of points, and wherein each coordinate of a point is associated with the value of a parameter in the corresponding corner. Next, the system can formulate a direct dominance problem on the set of points. The system can then determine the dominance relation on the set of corners by solving the direct dominance problem.

BRIEF DESCRIPTION OF THE FIGURES

[0012] FIG. 1 illustrates various steps in the design and fabrication of an integrated circuit.

[0013] FIG. 2 illustrates delay curves for different corners in accordance with some embodiments of the present invention.

[0014] FIG. 3A illustrates a dominance relation on a set of corners in accordance with some embodiments of the present invention.

[0015] FIG. 3B illustrates a dominance relation on a set of corners in accordance with some embodiments of the present invention.

[0016] FIG. 4 illustrates how a dominance relation on a set of corners can be used to perform scenario reduction in accordance with some embodiments of the present invention.

[0017] FIG. 5 presents a flowchart that illustrates a process for using library analysis to determine a dominance relation on a set of corners in accordance with some embodiments of the present invention.

[0018] FIG. 6 presents a flowchart that illustrates a process for optimizing a circuit design over a set of scenarios in accordance with some embodiments of the present invention.

[0019] FIG. 7 illustrates a computer system in accordance with some embodiments of the present invention.

[0020] FIG. 8 illustrates an apparatus in accordance with some embodiments of the present invention.

DETAILED DESCRIPTION

[0021] The following description is presented to enable any person skilled in the art to make and use the invention, and is provided in the context of a particular application and its requirements. Various modifications to the disclosed embodiments will be readily apparent to those skilled in the art, and the general principles defined herein may be applied to other embodiments and applications without departing from the spirit and scope of the present invention. Thus, the present invention is not limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features disclosed herein.

[0022] FIG. 1 illustrates various steps in the design and fabrication of an integrated circuit. The process starts with a product idea 100, which is realized using Electronic Design Automation (EDA) software 110. Chips 170 can be produced from the finalized design by performing fabrication 150 and packaging and assembly 160 steps.

[0023] A design flow that uses EDA software 110 is described below. Note that the design flow description is for illustration purposes only, and is not intended to limit the present invention. For example, an actual integrated circuit design may require a designer to perform the design flow steps in a different sequence than the sequence described below.

[0024] In the system design step 112, the designers can describe the functionality to implement. They can also perform what-if planning to refine the functionality and to check costs. Further, hardware-software architecture partitioning can occur at this step. In the logic design and functional verification step 114, a Hardware Description Language (HDL) design can be created and checked for functional accuracy.

[0025] In the synthesis and design step 116, the HDL code can be translated to a netlist, which can be optimized for the target technology. Further, tests can be designed and implemented to check the finished chips. In the netlist verification step 118, the netlist can be checked for compliance with timing constraints and for correspondence with the HDL code.

[0026] In the design planning step 120, an overall floor plan for the chip can be constructed and analyzed for timing and top-level routing. Next, in the physical implementation step 122, placement and routing can be performed.

[0027] In the analysis and extraction step 124, the circuit functionality can be verified at a transistor level. In the physical verification step 126, the design can be checked to correct any functional, manufacturing, electrical, or lithographic issues.

[0028] In the resolution enhancement step 128, geometric manipulations can be performed on the layout to improve manufacturability of the design. Finally, in the mask data

preparation step 130, the design can be taped-out for production of masks to produce finished chips.

[0029] A circuit optimization technique that optimizes a circuit design over a set of scenarios must meet the functional and performance goals (timing, power, area, electrical design rules, etc.) for the circuit design for all the scenarios. Note that, as used in this disclosure, the terms “optimize,” “optimizing,” “optimization,” etc., relate to a process that tries to improve one or more metrics associated with the circuit design. These terms are not intended to imply that a local or a global optimum value is being determined. The metrics could include electrical design rules (e.g., maximum capacitance, maximum transition, maximum fanout), leakage power, area, and timing-related metrics (e.g., Worst Negative Slack (WNS) and Total Negative Slack (TNS)).

[0030] Each scenario can be associated with a corner and a mode. For example, a scenario may be associated with a positive defocus process corner and a normal operating mode. If there are no design requirement violations in this scenario, the chip is expected to behave as desired in its normal operating mode, even if the chip was manufactured using a photolithography process that is positively defocused.

[0031] Traditional approaches optimize each scenario independently and sequentially. These approaches suffer from poor quality of results and long run-times in converging on an optimal solution for all scenarios. Very often, these techniques fail to converge on an optimal solution because of “ping-pong” effects. For example, if an optimizing transformation performed in one scenario cancels the effects of an optimizing transformation performed in another scenario, the technique may “ping-pong” between these two scenarios, thereby preventing the solution from converging.

[0032] Some approaches model all of the scenarios concurrently and construct optimal solutions under the constraints of all scenarios. For example, these approaches evaluate the timing of the circuit by performing static timing analysis for all scenarios, and update timing information for all scenarios when an optimization transformation is applied to a gate. Note that the term “gate” as used in this disclosure can generally refer to any portion of the circuit design that performs a logical function and that may have one or more inputs and one or more outputs. In these approaches, the system optimizes the circuit design based on the slack/timing, leakage power, and DRC information over all scenarios. Although these approaches are superior to approaches that optimize one scenario at a time, they incur additional run-time and memory overhead. This is because, in these approaches, whenever timing, power, and DRC information (e.g., electrical design rules) are updated, they have to be updated across all scenarios. Note that the run-time and memory overhead increase with the number of scenarios. Since the number of

scenarios is rapidly increasing as semiconductor geometries become smaller and circuit designs become more complex, these approaches are quickly becoming computationally impractical.

[0033] Some embodiments of the present invention overcome the run-time and memory overhead of approaches that concurrently analyze and optimize a circuit design over a set of scenarios by identifying a subset of scenarios that is sufficient for achieving optimal implementation results. Once the subset of scenarios has been identified, the analysis and optimization is performed only over the subset of scenarios. Specifically, timing, power, and DRC analyses are performed only on the subset of scenarios. All other scenarios that do not belong to the subset are not considered during analysis and optimization, thereby reducing the run-time and memory requirements.

[0034] A circuit design is typically optimized for a number of constraints or optimization criteria (e.g., timing, power, electrical design rules, etc.) in each of the scenarios for each relevant object (e.g., timing end-point, net, cell, design, etc.) in the design. The system typically uses a design library which provides the optimization process a set of implementations for each gate type. During optimization the system can change the circuit design by replacing an implementation of a gate type in the circuit design with another implementation that is selected from the design library. Each gate type implementation in the design library can have different characteristics. Further, the characteristics of a gate type implementation can vary from one corner to another.

[0035] FIG. 2 illustrates delay curves for different corners in accordance with some embodiments of the present invention. Each delay curve represents the variation of the gate delay against the capacitive load for a given implementation of a gate type, input transition value, and corner.

[0036] Plot 202 illustrates four delay curves that correspond to corners C1, C2, C3, and C4. Note that these delay curves are for a particular input transition value and a particular gate size (i.e., a particular implementation of a gate type in a technology library). Similar delay curves can be created for other input transition values and implementations of the gate type.

[0037] In plot 202, the gate delay in corner C1 is greater than the gate delays in corners C2, C3, and C4 across all capacitive load values. In other words, corner C1 dominates corners C2, C3, and C4. Consider a circuit design that consists of a single gate whose delay characteristics are given by plot 202. If this circuit design meets timing requirements in corner C1, then we can conclude that the circuit design will meet timing requirements in corners C2, C3, and C4. Thus, instead of optimizing this circuit design over all four corners, we only need to optimize the circuit design over corner C1.

[0038] Plot 204 illustrates delay curves for a different input transition value and/or a different implementation of the gate type in the same technology library. Specifically, in plot 204, the gate delays in corners C1 and C2 are greater than the gate delays in corners C3 and C4 across all capacitive load values. However, depending on the capacitive load, the gate delay in corner C1 may or may not be greater than the gate delay in corner C2 (the delay curve for corner C2 has been shown as a dotted line to clearly distinguish it from the delay curve for corner C1). In other words, corners C1 and C2 dominate corners C3 and C4. Thus, in this situation, we need to optimize the single gate circuit design in corners C1 and C2 to ensure that the circuit design will meet timing requirements across all corners.

[0039] Corner C_i can be said to dominate corner C_j if the gate delay in corner C_i is greater than or equal to the gate delay in corner C_j across all implementations of a gate type, input transitions, and capacitive loads. Similarly, corner C_i can be said to dominate C_j if leakage power values (or electrical design rule values) in C_i are greater than or equal to corresponding leakage power values (or electrical design rule values) in C_j over a set of gate implementations of a gate type.

[0040] The notion of dominance can be extended to multiple parameter values (e.g., gate delay, leakage power, electrical design rules, etc.). Specifically, corner C_i can be said to dominate corner C_j if, for each parameter in a set of parameters, the parameter value in corner C_i is greater than or equal to the parameter value in corner C_j across the entire optimization space. A dominance relation D can be defined on a set of corners such that $C_i D C_j$ if and only if corner C_i dominates corner C_j .

[0041] FIG. 3A illustrates a dominance relation on a set of corners in accordance with some embodiments of the present invention.

[0042] The dominance relation shown in FIG. 3A corresponds to the gate delays shown in plots 202 and 204. In FIG. 3A, the dominance relation is represented as a set of corner tuples, wherein the corner tuple (C_i, C_j) indicates that corner C_i dominates corner C_j . Note that corner C1 would have dominated corner C2 if we had only considered the implementation of the gate type in plot 202. However, since in plot 204 (which corresponds to a different implementation of the gate type) the gate delay in corner C1 is less than the gate delay in corner C2 for at least one data point, corner C1 does not dominate corner C2.

[0043] FIG. 3B illustrates a dominance relation on a set of corners in accordance with some embodiments of the present invention.

[0044] The dominance relation shown in FIG. 3B corresponds to the gate delays shown in plots 202 and 204. In FIG. 3B, the dominance relation is represented visually as a directed graph, wherein a directed edge (C_i, C_j) indicates that corner C_i dominates corner C_j . The

representations in FIGs. 3A and 3B are not intended to be exhaustive or to limit the present invention to the forms disclosed. Accordingly, many different representations of a dominance relation will be apparent to practitioners skilled in the art.

[0045] FIG. 4 illustrates how a dominance relation on a set of corners can be used to perform scenario reduction in accordance with some embodiments of the present invention.

[0046] Suppose a circuit design needs to be optimized over the set of scenarios {S1, S2, S3, S4, S5, S6, S7}. As shown in FIG. 4, each scenario is a combination of a mode from the set of modes {M1, M2, M3}, and a corner from the set of corners {C1, C2, C3, C4}. Let us assume that the dominance relation on the set of corners {C1, C2, C3, C4} is the same as those illustrated in FIGs. 3A or 3B.

[0047] The dominance relation on the set of corners can be used to perform scenario reduction as follows. First, the system can group the scenarios based on the associated modes. For example, as shown in FIG. 4, the system can create three scenario groups G1, G2, and G3 by grouping the scenarios based on the associated modes. Next, the system can use the dominance relation on the set of corners to reduce the number of scenarios in each group. For example, since corner C4 is dominated by corners C1 and C2, the system can remove scenario S3 from group G1. Similarly, scenarios S5 and S7 can be removed from groups G2 and G3, respectively. The resulting subset of the set of scenarios consists of scenarios S1, S2, S4, and S6. Note that scenario reduction based on a dominance relation on the set of corners must be performed on a per-mode basis because different modes can have vastly different supply voltages, design constraints, and clock speeds.

[0048] The scenario reduction process illustrated in FIG. 4 is for illustration purposes only and is not intended to limit the scope of the present invention. Accordingly, many modifications and variations will be apparent to practitioners skilled in the art. For example, in some embodiments, the system can use the dominance relation on the set of corners to determine a dominance relation on the set of scenarios. Specifically, scenario S_i dominates scenario S_j if both S_i and S_j are associated with the same mode, and the corner associated with scenario S_i dominates the corner associated with scenario S_j . Once a dominance relation on the set of scenarios is determined, the system can determine a dominant subset of scenarios. Let Σ be the set of scenarios. A dominant subset of scenarios, Δ , is a subset of Σ such that every scenario in the set $\Sigma - \Delta$ is dominated by at least one scenario in Δ .

[0049] FIG. 5 presents a flowchart that illustrates a process for using library analysis to determine a dominance relation on a set of corners in accordance with some embodiments of the present invention.

[0050] The process can begin by receiving a design library which specifies gate characteristics at each corner in a set of corners (step 502). The system can then use the design library to determine a dominance relation on the set of corners (step 504). Specifically, in some embodiments, the system can represent the set of corners by a set of points in an n-dimensional space, wherein each corner in the set of corners is associated with a point in the set of points, and wherein each coordinate of a point is associated with the value of a parameter in the corresponding corner. Next, the system can formulate a direct dominance problem on the set of points, and determine the dominance relation on the set of corners by solving the direct dominance problem. Note that a dominance relation on the set of corners can be determined at any level of granularity. Specifically, a dominance relation can be determined for each gate type and/or for the entire design library. A dominance relation can be used to determine a dominant subset of corners. Specifically, let Σ be the set of corners. A dominant subset of corners, Δ , is a subset of Σ such that every corner in the set $\Sigma - \Delta$ is dominated by at least one corner in Δ .

[0051] Next, the system can store the dominance relation in a non-transitory computer-readable storage medium (step 506). In some embodiments, the dominance relation can be stored with the design library.

[0052] FIG. 6 presents a flowchart that illustrates a process for performing scenario reduction using a dominance relation on a set of corners in accordance with some embodiments of the present invention.

[0053] The process can begin by determining a subset of the set of scenarios using a dominance relation on the set of corners (step 602). Note that, if the circuit design meets a set of design constraints in each scenario in the subset of the set of scenarios, the circuit design is expected to meet the set of design constraints in each scenario in the set of scenarios. Specifically, the system can determine a subset of the set of scenarios by removing a first scenario from the set of scenarios if the first scenario and a second scenario in the set of scenarios are associated with the same mode and a first corner associated with the first scenario is dominated by a second corner associated with the second scenario.

[0054] The system can then optimize the circuit design over the subset of the set of scenarios (step 604). Specifically, the system can update circuit information only in the subset of the set of scenarios whenever a gate is changed in the circuit design during optimization, thereby substantially reducing the amount of computation required to optimize the circuit design over the set of scenarios.

[0055] Note that a design library can include a large number of gate types. As explained above, the system can determine a dominant subset of corners for each gate type in the design library. In some embodiments, the system can consider dominant subsets of corners associated

with all gate types regardless of which gate types are expected to be used during optimization. Alternatively, the system can first identify the gate types that are expected to be used during optimization, and then use only those dominant subsets of corners that are associated with the identified gate types.

5 **[0056]** FIG. 7 illustrates a computer system in accordance with some embodiments of the present invention.

[0057] Computer system 702 can include processor 704, memory 706, and storage device 708. Computer system 702 can be coupled to display device 714, keyboard 710, and pointing device 712. Storage device 708 can store operating system 718, applications 716, and data 720.

10 **[0058]** Applications 716 can include instructions which, when executed by computer system 702, can cause computer system 702 to perform processes which are inherently or explicitly described in this disclosure. Data 720 can include any data that is required as input or that is generated as output by processes which are inherently or explicitly described in this disclosure.

15 **[0059]** FIG. 8 illustrates an apparatus in accordance with some embodiments of the present invention.

[0060] Apparatus 802 can comprise a plurality of mechanisms which may communicate with one another via a wired or wireless communication channel. Apparatus 802 may be realized using one or more integrated circuits, and apparatus 802 may include fewer or more mechanisms
20 than those shown in FIG. 8. Further, apparatus 802 may be integrated in a computer system, or it may be realized as a separate device which is capable of communicating with other computer systems and/or devices.

[0061] Apparatus 802 can include one or more mechanisms which are configured to perform operations which are inherently or explicitly described in this disclosure. Specifically,
25 apparatus 802 can include receiving mechanism 804, determining mechanism 806, optimizing mechanism 808, and storing mechanism 810.

[0062] In some embodiments, receiving mechanism 804 can be configured to receive a set of scenarios, wherein each scenario is a combination of a mode from a set of modes and a corner from a set of corners. Determining mechanism 806 can be configured to determine a
30 subset of the set of scenarios using a dominance relation on the set of corners. Optimizing mechanism 808 can be configured to optimize a circuit design over the subset of the set of scenarios.

[0063] In some embodiments, receiving mechanism 804 can be configured to receive a design library that specifies circuit characteristics over a set of corners, determining mechanism
35 806 can be configured to determine a dominance relation on the set of corners, and storing

mechanism 810 can be configured to store the dominance relation on the set of corners in a non-transitory computer-readable storage medium.

CONCLUSION

5 **[0064]** The above description is presented to enable any person skilled in the art to make and use the embodiments. Various modifications to the disclosed embodiments will be readily apparent to those skilled in the art, and the general principles defined herein are applicable to other embodiments and applications without departing from the spirit and scope of the present disclosure. Thus, the present invention is not limited to the embodiments shown, but is to be
10 accorded the widest scope consistent with the principles and features disclosed herein.

[0065] The data structures and code described in this disclosure can be partially or fully stored on a computer-readable storage medium and/or a hardware module and/or hardware apparatus. A computer-readable storage medium includes, but is not limited to, volatile memory, non-volatile memory, magnetic and optical storage devices such as disk drives, magnetic tape,
15 CDs (compact discs), DVDs (digital versatile discs or digital video discs), or other media, now known or later developed, that are capable of storing code and/or data. Hardware modules or apparatuses described in this disclosure include, but are not limited to, application-specific integrated circuits (ASICs), field-programmable gate arrays (FPGAs), dedicated or shared processors, and/or other hardware modules or apparatuses now known or later developed.

20 **[0066]** The methods and processes described in this disclosure can be partially or fully embodied as code and/or data stored in a computer-readable storage medium or device, so that when a computer system reads and executes the code and/or data, the computer system performs the associated methods and processes. The methods and processes can also be partially or fully embodied in hardware modules or apparatuses, so that when the hardware modules or
25 apparatuses are activated, they perform the associated methods and processes. Note that the methods and processes can be embodied using a combination of code, data, and hardware modules or apparatuses.

[0067] The foregoing descriptions of embodiments of the present invention have been presented only for purposes of illustration and description. They are not intended to be
30 exhaustive or to limit the present invention to the forms disclosed. Accordingly, many modifications and variations will be apparent to practitioners skilled in the art. Additionally, the above disclosure is not intended to limit the present invention. The scope of the present invention is defined by the appended claims.

1. A method for optimizing a circuit design over a set of scenarios, wherein each scenario is associated with a corner from a set of corners and a mode from a set of modes, the method comprising:

determining a subset of the set of scenarios using a dominance relation on the set of corners such that if the circuit design meets a set of design constraints in each scenario in the subset of the set of scenarios, the circuit design is expected to meet the set of design constraints in each scenario in the set of scenarios; and

optimizing the circuit design over the subset of the set of scenarios.

2. The method of claim 1, wherein determining the subset of the set of scenarios using the dominance relation on the set of corners includes removing a first scenario from the set of scenarios if the first scenario and a second scenario in the set of scenarios are associated with the same mode and a first corner associated with the first scenario is dominated by a second corner associated with the second scenario.

3. The method of claim 1, wherein a second corner dominates a first corner if delay and output transition time values in the second corner are greater than or equal to corresponding delay and output transition time values in the first corner over a set of implementations of a gate type, input transition times, and capacitive load values.

4. The method of claim 1, wherein a second corner dominates a first corner if leakage power values in the second corner are greater than or equal to corresponding leakage power values in the first corner over a set of gate implementations of a gate type.

5. The method of claim 1, wherein a second corner dominates a first corner if electrical design rule values in the second corner are greater than or equal to corresponding electrical design rule values in the first corner over a set of gate implementations of a gate type.

6. The method of claim 1, further comprising:

representing the set of corners by a set of points in an n-dimensional space, wherein each corner in the set of corners is associated with a point in the set of points, and wherein each coordinate of a point is associated with the value of a parameter in the corresponding corner;

formulating a direct dominance problem on the set of points; and

determining the dominance relation on the set of corners by solving the direct dominance problem.

7. The method of claim 1, wherein circuit information is updated only in the subset of the set of scenarios whenever a gate is changed in the circuit design during optimization.

8. The method of claim 1, wherein the subset of the set of scenarios is determined using dominant subsets of corners associated with gate types in a library.

9. The method of claim 1, wherein determining the subset of the set of scenarios using the dominance relation on the set of corners includes:

determining gate types that are expected to be used during optimization; and

determining the subset of the set of scenarios using dominant subsets of corners associated with the gate types.

10. A non-transitory computer-readable storage medium storing instructions that when executed by a computer cause the computer to perform a method for optimizing a circuit design over a set of scenarios, wherein each scenario is associated with a corner from a set of corners and a mode from a set of modes, the method comprising:

determining a subset of the set of scenarios using a dominance relation on the set of corners such that if the circuit design meets a set of design constraints in each scenario in the subset of the set of scenarios, the circuit design is expected to meet the set of design constraints in each scenario in the set of scenarios; and

optimizing the circuit design over the subset of the set of scenarios.

11. The non-transitory computer-readable storage medium of claim 10, wherein determining the subset of the set of scenarios using the dominance relation on the set of corners includes removing a first scenario from the set of scenarios if the first scenario and a second scenario in the set of scenarios are associated with the same mode and a first corner associated with the first scenario is dominated by a second corner associated with the second scenario.

12. The non-transitory computer-readable storage medium of claim 10, wherein a second corner dominates a first corner if the delay and output transition time values in the second corner are greater than or equal to the corresponding delay and output transition time values in

the first corner over a set of implementations of a gate type, input transition times, and capacitive load values.

13. The non-transitory computer-readable storage medium of claim 10, wherein a
5 second corner dominates a first corner if leakage power values in the second corner are greater than or equal to corresponding leakage power values in the first corner over a set of gate implementations of a gate type.

14. The non-transitory computer-readable storage medium of claim 10, wherein a
10 second corner dominates a first corner if electrical design rule values in the second corner are greater than or equal to corresponding electrical design rule values in the first corner over a set of gate implementations of a gate type.

15. The non-transitory computer-readable storage medium of claim 10, further
15 comprising:

representing the set of corners by a set of points in an n-dimensional space, wherein each corner in the set of corners is associated with a point in the set of points, and wherein each coordinate of a point is associated with the value of a parameter in the corresponding corner;
formulating a direct dominance problem on the set of points; and
20 determining the dominance relation on the set of corners by solving the direct dominance problem.

16. The non-transitory computer-readable storage medium of claim 10, wherein
25 circuit information is updated only in the subset of the set of scenarios whenever a gate is changed in the circuit design during optimization.

17. The non-transitory computer-readable storage medium of claim 10, wherein the
subset of the set of scenarios is determined using dominant subsets of corners associated with gate types in a library.

18. The non-transitory computer-readable storage medium of claim 10, wherein
30 determining the subset of the set of scenarios using the dominance relation on the set of corners includes:

determining gate types that are expected to be used during optimization; and

determining the subset of the set of scenarios using dominant subsets of corners associated with the gate types.

19. An apparatus for optimizing a circuit design over a set of scenarios, the apparatus comprising:

a determining mechanism configured to determine a subset of the set of scenarios using a dominance relation on the set of corners such that if the circuit design meets a set of design constraints in each scenario in the subset of the set of scenarios, the circuit design is expected to meet the set of design constraints in each scenario in the set of scenarios; and

an optimizing mechanism configured to optimize the circuit design over the subset of the set of scenarios.

20. The apparatus of claim 19, wherein the determining mechanism is configured to remove a first scenario from the set of scenarios if the first scenario and a second scenario in the set of scenarios are associated with the same mode and a first corner associated with the first scenario is dominated by a second corner associated with the second scenario.

21. The apparatus of claim 19, wherein a second corner dominates a first corner if delay and output transition time values in the second corner are greater than or equal to corresponding delay and output transition time values in the first corner over a set of implementations of a gate type, input transition times, and capacitive load values.

22. The apparatus of claim 19, wherein a second corner dominates a first corner if leakage power values in the second corner are greater than or equal to corresponding leakage power values in the first corner over a set of gate implementations of a gate type.

23. The apparatus of claim 19, wherein a second corner dominates a first corner if electrical design rule values in the second corner are greater than or equal to corresponding electrical design rule values in the first corner over a set of gate implementations of a gate type.

24. The apparatus of claim 19, further comprising:

a representing mechanism configured to represent the set of corners by a set of points in an n-dimensional space, wherein each corner in the set of corners is associated with a point in the set of points, and wherein each coordinate of a point is associated with the value of a parameter in the corresponding corner;

a formulating mechanism configured to formulate a direct dominance problem on the set of points; and

a second determining mechanism configured to determine the dominance relation on the set of corners by solving the direct dominance problem.

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25. The apparatus of claim 19, wherein the optimizing mechanism is configured to update circuit information only in the subset of the set of scenarios whenever a gate is changed in the circuit design during optimization.

10

26. The apparatus of claim 19, wherein the determining mechanism is configured to determine the subset of the set of scenarios using dominant subsets of corners associated with gate types in a library.

15

27. The apparatus of claim 19, wherein the determining mechanism is configured to:
determine gate types that are expected to be used during optimization; and
determine the subset of the set of scenarios using dominant subsets of corners associated with the gate types.

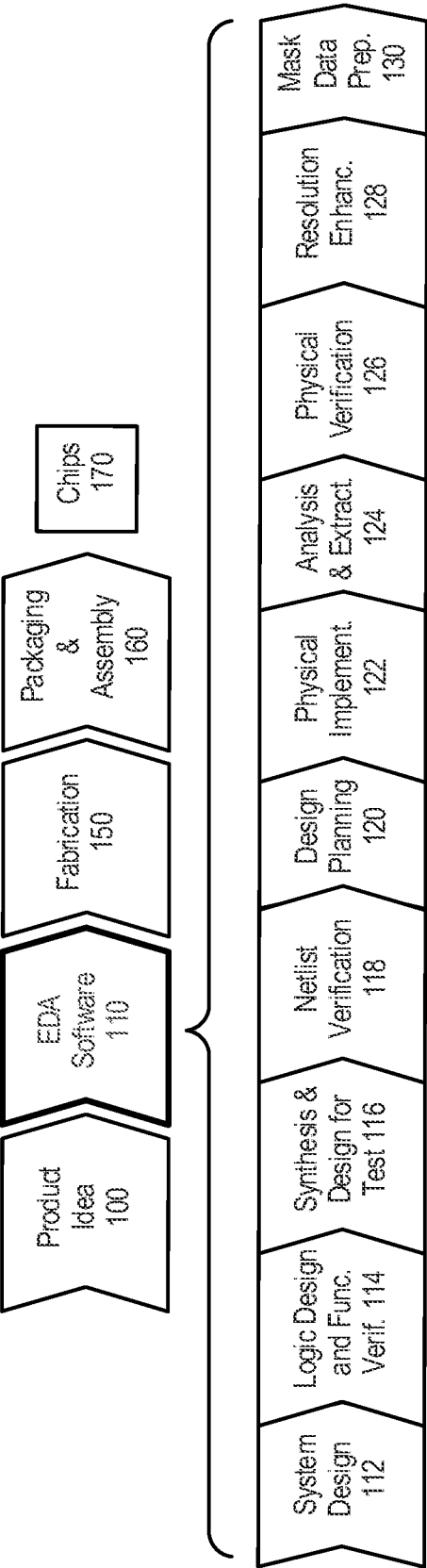


FIG. 1

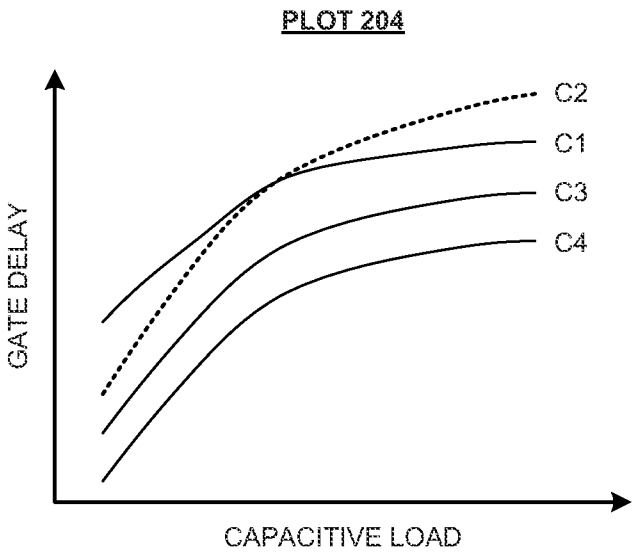
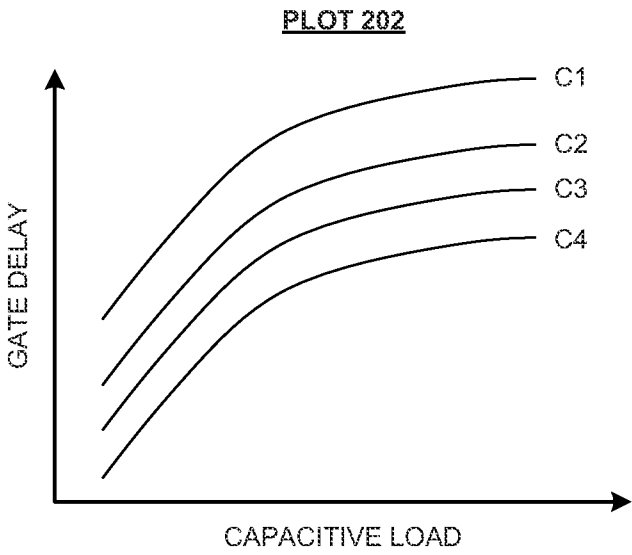
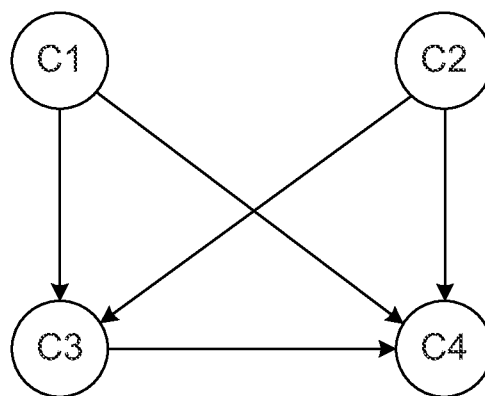
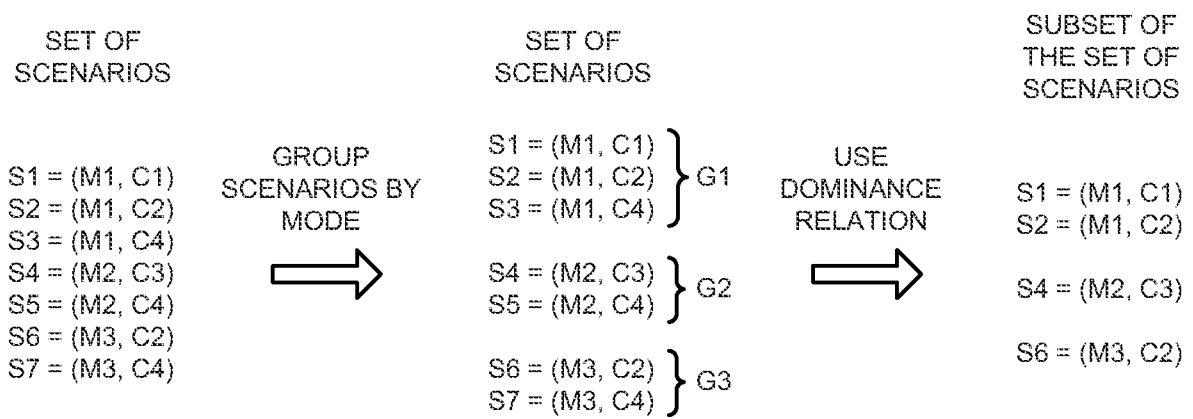
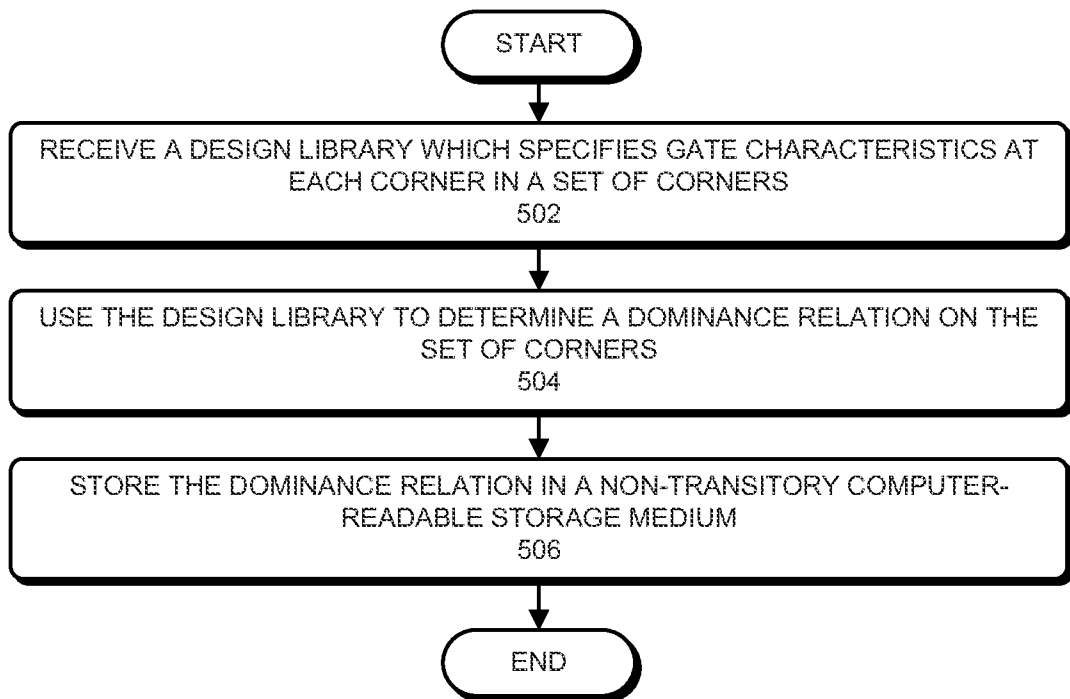
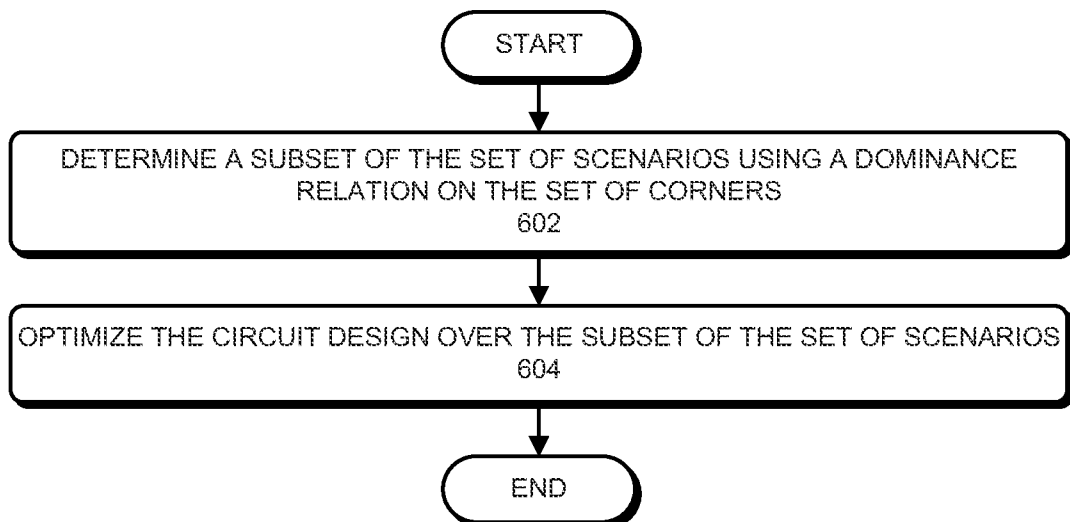


FIG. 2

$$\{ (C1, C3), (C1, C4), (C2, C3), (C2, C4), (C3, C4) \}$$
FIG. 3A**FIG. 3B****FIG. 4**

**FIG. 5****FIG. 6**

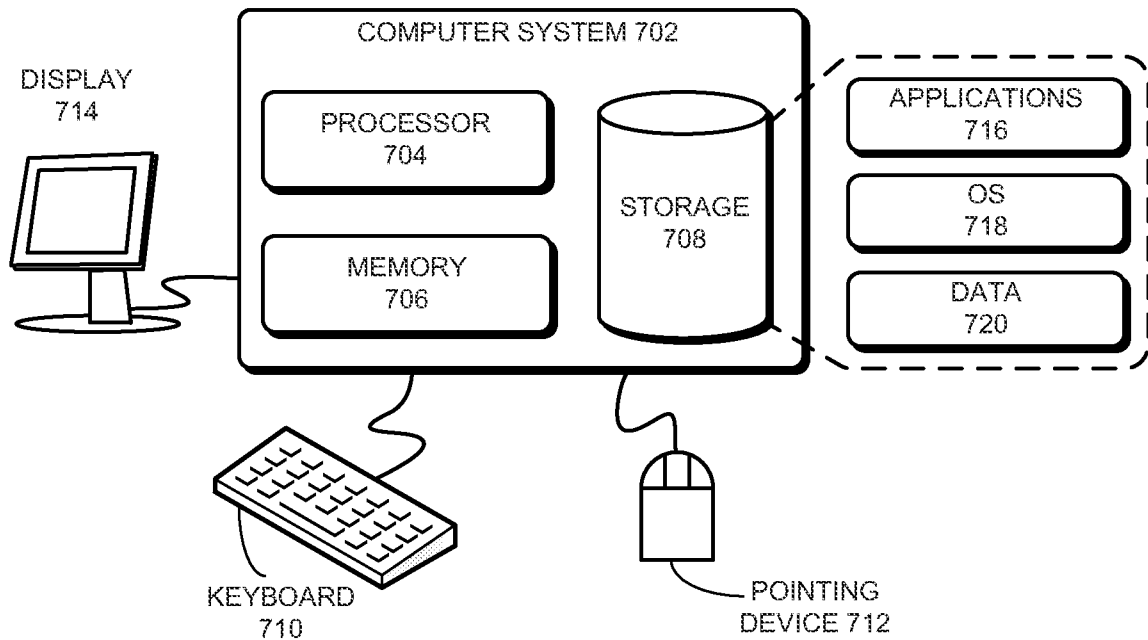


FIG. 7

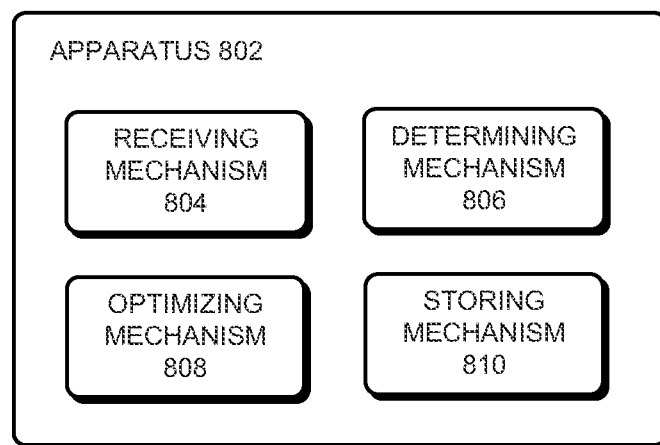


FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/044982**A. CLASSIFICATION OF SUBJECT MATTER****G06F 17/50(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 9: G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: circuit, design, scenarios, constraints

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2008-0244476 A1 (FOTAKIS et al.) 02 October 2008 See the abstract, figure 3, and claim 1.	1-27
A	US 2006-0026544 A1 (ENGEL et al.) 02 February 2006 See the abstract, figure 4, and claims 1, 8.	1-27
A	US 2009-0100385 A1 (BAUMGARTNER et al.) 16 April 2009 See the abstract, figure 1, and claim 1.	1-27



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

03 JANUARY 2012 (03.01.2012)

Date of mailing of the international search report

04 JANUARY 2012 (04.01.2012)

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Telephone No. 82-42-481-5973



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2011/044982

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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US 2006-0026544 A1	02.02.2006	US 2007-0089078 A1 US 7174523 B2	19.04.2007 06.02.2007
US 2009-0100385 A1	16.04.2009	US 7913208 B2	22.03.2011