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(54) **Title:** METHOD OF FORMING A SEMICONDUCTOR DEVICE WITH AIR GAPS FOR LOW CAPACITANCE INTERCONNECTS

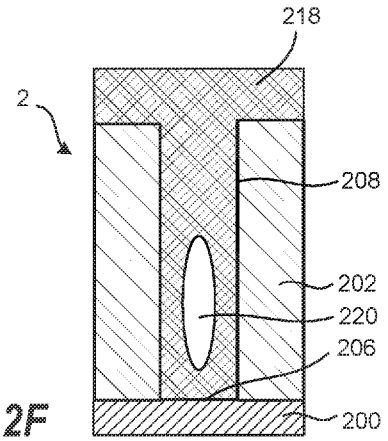

FIG. 2F

(57) **Abstract:** A substrate processing method comprises providing a substrate containing raised features with top areas and sidewalls, and bottom areas between the raised features and exposing the substrate to a gas pulse sequence to deposit a material that forms an air gap between the raised features, wherein the gas pulse sequence includes, in any order: a) sequentially first, exposing the substrate to a first precursor gas to non-conformally form a first precursor layer on the top area and on the upper parts of the sidewalls, and second exposing the substrate to a second precursor gas that reacts with the first precursor layer to form a first layer of the material on the substrate, and b) sequentially first, exposing the substrate to the first precursor gas to conformally form a second precursor layer on the top areas, on the sidewalls, and on the bottom areas, and second, exposing the substrate to the second precursor gas that reacts with the second precursor layer to form a second layer of the material on the substrate.

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METHOD OF FORMING A SEMICONDUCTOR DEVICE WITH AIR GAPS FOR LOW CAPACITANCE INTERCONNECTS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is related to and claims priority to United States Provisional Patent Application serial no. 62/654,760 filed on April 9, 2018, the entire contents of which are herein incorporated by reference.

FIELD OF INVENTION

[0002] The present invention relates to the field of semiconductor manufacturing and semiconductor devices, and more particularly, to a method of forming a semiconductor device with air gaps for low capacitance interconnects.

BACKGROUND OF THE INVENTION

[0003] As device feature size is scaled, interconnects are becoming a significant problem in performance improvement. This is in part due to an increase in electrical resistivity (Rs) with ever decreasing device feature sizes and detrimental capacitance between adjacent features. One way of reducing capacitance is using ultra low-k dielectric materials, but air gaps offer the lowest dielectric constant (k) value of approximately 1. As a result, device manufacturers are adding air gaps to critical layers in advanced metallization schemes.

SUMMARY OF THE INVENTION

[0004] This disclosure describes a novel method of fabricating air gaps in advanced semiconductor devices. According to one embodiment, the method includes providing a substrate containing raised features with top areas and sidewalls, and bottom areas between the raised features, and exposing the substrate to a gas pulse sequence to deposit a material that forms an air gap between the raised features, where the gas pulse sequence includes, in any order: a) sequentially first, exposing the substrate to a first precursor gas to non-conformally form a first precursor layer on the top areas and on the upper parts of the sidewalls, but not on the lower parts of the sidewalls and the bottom areas, and second, exposing the substrate to a second precursor gas that reacts with the first precursor layer to form a layer of the material on the substrate, and b) sequentially first, exposing the substrate to the first precursor gas to conformally form a second precursor layer on the top areas, on the sidewalls, and on the bottom

areas, and second, exposing the substrate to the second precursor gas that reacts with the second precursor layer to form a second layer of the material on the substrate. The steps a), b), or a) and b), may be repeated at least once until the air gap is formed.

[0005] According to another embodiment, the method includes providing a substrate containing raised features with top areas and sidewalls, and bottom areas between the raised features, and exposing the substrate to a gas pulse sequence to deposit a material that forms an air gap between the raised features, where the gas pulse sequence includes, in any order: a) sequentially first, exposing the substrate to a first precursor gas to conformally form a first precursor layer on the top areas, on the sidewalls, and on the bottom areas, second, exposing the substrate to a plasma-excited halogen-containing gas to deactivate or at least partially remove the first precursor layer in the top areas and the bottom areas, and third, exposing the substrate to the second precursor gas that reacts with the first precursor layer to form a layer of the material on the sidewalls, and b) sequentially first, exposing the substrate to the first precursor gas to conformally form a second precursor layer on the top areas, on the sidewalls, and on the bottom areas, and second, exposing the substrate to the second precursor gas that reacts with the second precursor layer to form a second layer of the material on the substrate. The steps a), b), or a) and b), may be repeated at least once until the air gap is formed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] A more complete appreciation of the invention and many of the attendant advantages thereof will be readily obtained as the same becomes better understood by reference to the following detailed description when considered in connection with the accompanying drawings, wherein:

[0007] FIG. 1 is a process flow diagram for processing a substrate according to an embodiment of the invention;

[0008] FIGS. 2A-2F schematically show through cross-sectional views a method of processing a substrate according to an embodiment of the invention;

[0009] FIG. 3 is a process flow diagram for processing a substrate according to an embodiment of the invention;

[0010] FIGS. 4A-4G schematically show through cross-sectional views a method of processing a substrate according to an embodiment of the invention; and

[0011] FIG. 5 shows a cross-sectional scanning electron micrograph (SEM) image of air gaps formed in a SiO_2 material according to an embodiment of the invention.

DETAILED DESCRIPTION OF SEVERAL EMBODIMENTS

[0012] A method of fabricating air gaps in advanced semiconductor devices is described. FIG. 1 is a process flow diagram for processing a substrate according to an embodiment of the invention, and FIGS. 2A-2F schematically show through cross-sectional views a method of processing a substrate according to an embodiment of the invention.

[0013] The process flow 1 in FIG. 1 includes in 100, providing a substrate 2 containing a base film 200 and raised features 202 with top areas 201 and sidewalls 208, and bottom areas 206 between the raised features 202. The raised features 202 define a recessed feature 204 between the raised features 202. The recessed feature 204 can, for example, have a width 207 that is less than 200nm, less than 100nm, less than 50nm, less than 25nm, less than 20nm, or less than 10nm. In other examples, the recessed feature 204 can have a width 207 that is between 5nm and 10nm, between 10nm and 20nm, between 20nm and 50nm, between 50nm and 100nm, between 100nm and 200nm, between 10nm and 50nm, or between 10nm and 100nm. The width 207 can also be referred to as a critical dimension (CD). The recessed feature 204 can, for example, have a depth of 25nm, 50nm, 100nm, 200nm, or greater.

[0014] In some examples, the base film 200 and the raised features 202 may contain or consist of the same material. In one example, the base film 200 and the raised features 202 may contain or consist of Si. In some examples, the raised features 202 may contain a dielectric material, for example SiO_2, SiON, SiN, a high-k material, a low-k material, or an ultra-low-k material. The recessed feature 204 may be formed using well-known lithography and etching processes.

[0015] The process flow 1 further includes exposing the substrate 2 to a gas pulse sequence to deposit a material that forms an air gap on the substrate 2, where the gas pulse sequence includes, in any order: in 102, sequentially first, exposing the substrate to a first precursor gas to non-conformally form a first precursor layer on the top areas and on the upper parts of the sidewalls, but not on the lower parts of the sidewalls and the bottom areas (FIG. 2B), and second, exposing the substrate to a second precursor gas that reacts with the first precursor layer to form a first layer of the material on the substrate (FIG. 2C), and in 104, sequentially first, exposing the substrate to the first precursor gas to conformally form a second precursor layer on the top areas, on the sidewalls, and on the bottom areas (FIG. 2D), and second, exposing the substrate to the second precursor gas that reacts with the second precursor layer form a second layer of the material on the substrate (FIG. 2E).

[0016] FIG. 2B schematically shows a first precursor layer 210 that is non-conformally formed on the top areas 201 and on the upper parts of the sidewalls 208, but not on the lower parts of the sidewalls 208 and the bottom areas 206. According to embodiments of the invention, the first

precursor layer 210 may be deposited or formed by various methods including a) controlling the saturation regime at the substrate using an undersaturated exposure of the first precursor gas that results in depletion of the first precursor gas in the recessed feature 204, b) pressure control at the substrate to limit the diffusion of the first precursor gas to the bottom areas 206, c) spatial rapid horizontal movement of a rotating substrate below a gas inlet dispensing the first precursor gas during an atomic layer deposition (ALD) process, or d) plasma densification of a conformal precursor layer on the top areas 201 and on the upper parts of the sidewalls 208, followed by etching of the conformal precursor layer the lower parts of the sidewalls 208 and the bottom areas 206.

[0017] FIG. 2C shows the formation of a first layer of material 212 from exposure of the second precursor gas that reacts with the first precursor layer 210 in FIG. 2B.

[0018] FIG. 2D shows a second precursor layer 214 that is conformally formed on the top areas 201, on the sidewalls 208, and on the bottom areas 206. The second precursor layer 214 may be deposited using a saturated exposure of the first precursor gas that reaches and saturates the bottom areas 206 between the raised features 202.

[0019] FIG. 2E shows the formation of a second layer of material 216 from exposure of the second precursor gas that reacts with the second precursor layer 214 in FIG. 2D.

[0020] Steps 102, 104, or both 102 and 104, may be repeated at least once until an air gap is formed on the substrate 2. Steps 102 and 104 may be performed in any order, i.e., step 102 before step 104, or step 104 before step 102. FIG. 2F shows the formation of an air gap 220 in the material 218 following deposition of additional material until the recessed feature 204 is pinched off near the top. The material 218 containing the air gap 220 includes the first layer of material 212, the second layer of material 216, and any further materials needed to close the opening near the top of the recessed feature 204.

[0021] In one example, the first precursor gas can include a metal-containing precursor and the first and second precursor layers 210 and 214 can form an adsorbed layer of the first precursor that is approximately one atomic layer thick.

[0022] In some examples, the metal-containing precursor contains aluminum, titanium, or a combination thereof. Examples of metal-containing precursor include aluminum (Al), titanium (Ti), or both aluminum and titanium. According to one embodiment, the first and second precursor layers 210 and 214 are selected from the group consisting of Al, Al_2O_3, AlN, AlON, an Al-containing precursor, Al-alloys, CuAl, TiAlN, TaAlN, Ti, TiAlC, TiO_2, TiON, TiN, a Ti-containing precursor, Ti-alloys, and combinations thereof.

[0023] Embodiments of the invention may utilize a wide variety of Al-containing precursors. For example, many aluminum precursors have the formula: $AlL_1L_2L_3D_x$ where L_1, L_2, L_3 are individual anionic ligands, and D is a neutral donor ligand where x can be 0, 1, or 2. Each L_1, L_2, L_3 ligand may be individually selected from the groups of alkoxides, halides, aryloxides, amides, cyclopentadienyls, alkyls, silyls, amidinates, β-diketonates, ketoiminates, silanoates, and carboxylates. D ligands may be selected from groups of ethers, furans, pyridines, pyroles, pyrolidines, amines, crown ethers, glymes, and nitriles.

[0024] Other examples of aluminum precursors include: $AlMe_3$, $AlEt_3$, $AlMe_2H$, $[Al(O^sBu)_3]_4$, $Al(CH_3COCHCOCH_3)_3$, $AlCl_3$, $AlBr_3$, AlI_3, $Al(O^iPr)_3$, $[Al(NMe_2)_3]_2$, $Al(^iBu)_2Cl$, $Al(^iBu)_3$, $Al(^iBu)_2H$, $AlEt_2Cl$, $Et_3Al_2(O^sBu)_3$, and $Al(THD)_3$.

[0025] Embodiments of the invention may utilize a wide variety of Ti-containing precursors. Examples include Ti-containing precursors having "Ti-N" intra-molecular bonds include $Ti(NEt_2)_4$ (TDEAT), $Ti(NMeEt)_4$ (TEMAT), $Ti(NMe_2)_4$ (TDMAT). Other examples include Ti-containing precursors containing "Ti-C" intra-molecular bonds include $Ti(COCH_3)(\eta5\text{-}C_5H_5)_2Cl$, $Ti(\eta5\text{-}C_5H_5)Cl_2$, $Ti(\eta5\text{-}C_5H_5)Cl_3$, $Ti(\eta5\text{-}C_5H_5)_2Cl_2$, $Ti(\eta5\text{-}C_5(CH_3)_5)Cl_3$, $Ti(CH_3)(\eta5\text{-}C_5H_5)_2Cl$, $Ti(\eta5\text{-}C_9H_7)_2Cl_2$, $Ti((\eta5\text{-}C_5(CH_3)_5)_2Cl$, $Ti((\eta5\text{-}C_5(CH_3)_5)_2Cl_2$, $Ti(\eta5\text{-}C_5H_5)_2(\mu\text{-}Cl)_2$, $Ti(\eta5\text{-}C_5H_5)_2(CO)_2$, $Ti(CH_3)_3(\eta5\text{-}C_5H_5)$, $Ti(CH_3)_2(\eta5\text{-}C_5H_5)_2$, $Ti(CH_3)_4$, $Ti(\eta5\text{-}C_5H_5)(\eta7\text{-}C_7H_7)$, $Ti(\eta5\text{-}C_5H_5)(\eta8\text{-}C_8H_8)$, $Ti(C_5H_5)_2(\eta5\text{-}C_5H_5)_2$, $Ti((C_5H_5)_2)_2(\eta\text{-}H)_2$, $Ti(\eta5\text{-}C_5(CH_3)_5)_2$, $Ti(\eta5\text{-}C_5(CH_3)_5)_2(H)_2$, and $Ti(CH_3)_2(\eta5\text{-}C_5(CH_3)_5)_2$. $TiCl_4$ is an example of a titanium halide precursor containing a "Ti-halogen" bond.

[0026] According to some embodiments, the second precursor gas may include a silanol gas and the material deposited on the substrate can include SiO_2. In some examples, the silanol gas may be selected from the group consisting of tris(tert-pentoxy) silanol (TPSOL), tris(tert-butoxy) silanol, and bis(tert-butoxy)(isopropoxy) silanol.

[0027] In the absence of any oxidizing and hydrolyzing agent, the substrate may be exposed, at a substrate temperature of approximately 150°C or less, to a process gas containing a silanol gas to deposit a SiO_2 film. The thickness of the SiO_2 film is controlled by self-limiting adsorption of the silanol gas on the precursor layer. This catalytic effect has been observed until the SiO_2 films were about 3nm thick, thereafter the SiO_2 deposition stopped. In another embodiment, the substrate temperature may be approximately 120°C or less. In yet another embodiment, the substrate temperature may be approximately 100°C or less.

[0028] FIG. 5 shows a cross-sectional scanning electron micrograph (SEM) image of air gaps 502 formed in a SiO_2 material 500 according to an embodiment of the invention. The SiO_2 material 500 was deposited over raised features according to the embodiment described in FIGS.

1 and 2A-2F. The first precursor contained $AlMe_3$ and the second precursor contained tris(tert-pentoxy) silanol.

[0029] FIG. 3 is a process flow diagram for processing a substrate according to an embodiment of the invention, and FIGS. 4A-4G schematically show through cross-sectional views a method of processing a substrate according to an embodiment of the invention.

[0030] The process flow 3 includes, in 300, providing a substrate 4 containing a base film 400 and raised features 402 with top areas 401 and sidewalls 408, and bottom areas 406 between the raised features 402. As shown in FIG. 4A, the raised features 402 define a recessed feature 404 having a width 407 between the raised features 402.

[0031] The process flow 3 further includes exposing the substrate 4 to a gas pulse sequence to deposit a material that forms an air gap on the substrate 4, where the gas pulse sequence includes, in any order: in 302, sequentially first, exposing the substrate to a first precursor gas to conformally form a first precursor layer on the top areas, on the sidewalls, and on the bottom areas (FIG. 4B), second, exposing the substrate to a plasma-excited halogen-containing gas to deactivate or at least partially remove the first precursor layer in the top areas and the bottom areas (FIG. 4C), and third, exposing the substrate to the second precursor gas that reacts with the precursor layer to form a first layer of the material on the sidewalls (FIG. 4D), and in 304, sequentially first, exposing the substrate to a first precursor gas to conformally form a second precursor layer on the top areas, on the sidewalls, and on the bottom areas (FIG. 4E), and second, exposing the substrate to the second precursor gas that reacts with the second precursor layer to form an additional layer of the material on the substrate (FIG. 4F). Steps a), b) or a) and b), may be repeated at least once to increase a thickness of the first and second material layers.

[0032] FIG. 4B shows the first precursor layer 410 that is conformally formed on the top areas 401, on the sidewalls 408, and on the bottom areas 406. According to one embodiment, the first precursor layer 410 may be deposited using a saturated exposure of the first precursor gas.

[0033] FIG. 4C shows the first precursor layer 410 following exposing the substrate 4 to a plasma-excited halogen-containing gas. The exposure to the plasma-excited halogen-containing gas removes the first precursor layer 410 from the top areas 401 and the bottom areas 406. Non-limiting examples of the halogen-containing gas contain Cl_2, BCl_3, CCl_4, HCl, HBr, $TiCl_4$, or a combination thereof. The halogen-containing gas can further include an inert gas such as Argon (Ar). In some examples, the plasma-excitation may be performed using a high density plasma source, for example an inductively coupled plasma (ICP) source or a microwave plasma source. The substrate 4 may be biased through a substrate holder to further enhance the anisotropic characteristics of the plasma exposure. Further, processing conditions such as substrate

temperature, gas pressure, and plasma power, may be selected to control the removal of the first precursor layer 410 and to minimize the damage to the substrate 4.

[0034] FIG. 4D shows the formation of a second layer of material 412 from exposure of the second precursor gas that reacts with the first precursor layer 410 in FIG. 4C on the sidewalls 408.

[0035] FIG. 4E shows the second precursor layer 414 that is conformally formed on the top areas 401, on the sidewalls 408, and on the bottom areas 406. The second precursor layer 414 may be deposited using a saturated exposure of the first precursor gas that reaches and saturates the bottom areas 406 between the raised features 402.

[0036] FIG. 4F shows the formation of a second layer of material 416 from exposure of the second precursor gas that reacts with the second precursor layer 414 in FIG. 4E.

[0037] Steps 302, 304, or both 302 and 304, may be repeated at least once until an air gap is formed on the substrate 4. Steps 302 and 304 may be performed in any order, i.e., step 302 before step 304, or step 304 before step 302. FIG. 4G shows the formation of an air gap 420 in the material 418 following deposition of additional material until the recessed feature 404 is pinched off near the top. The material 418 containing the air gap 420 includes the layer of material 412, the additional layer of material 216, and any further materials needed to close the opening near the top of the recessed feature 204.

[0038] A plurality of embodiments for a method of fabricating air gaps in advanced semiconductor devices have been described. The foregoing description of the embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. This description and the claims following include terms that are used for descriptive purposes only and are not to be construed as limiting. Persons skilled in the relevant art can appreciate that many modifications and variations are possible in light of the above teaching. Persons skilled in the art will recognize various equivalent combinations and substitutions for various components shown in the Figures. It is therefore intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

WHAT IS CLAIMED IS:

1. A substrate processing method, comprising:

providing a substrate containing raised features with top areas and sidewalls, and bottom areas between the raised features; and

exposing the substrate to a gas pulse sequence to deposit a material that forms an air gap between the raised features, wherein the gas pulse sequence includes, in any order:

a) sequentially first, exposing the substrate to a first precursor gas to non-conformally form a first precursor layer on the top areas and on the upper parts of the sidewalls, but not on the lower parts of the sidewalls and the bottom areas, and second, exposing the substrate to a second precursor gas that reacts with the first precursor layer to form a first layer of the material on the substrate, and

b) sequentially first, exposing the substrate to the first precursor gas to conformally form a second precursor layer on the top areas, on the sidewalls, and on the bottom areas, and second, exposing the substrate to the second precursor gas that reacts with the second precursor layer to form a second layer of the material on the substrate.

2. The method of claim 1, further comprising

repeating steps a), b), or a) and b), at least once until the air gap is formed.

3. The method of claim 1, wherein the first precursor gas contains a metal-containing precursor.

4. The method of claim 1, wherein the first precursor contains aluminum, titanium, or a combination thereof.

5. The method of claim 3, wherein the precursor layers are selected from the group consisting of Al, Al_2O_3, AlN, AlON, an Al-containing precursor, Al-alloys, CuAl, TiAlN, TaAlN, Ti, TiAlC, TiO_2, TiON, TiN, a Ti-containing precursor, Ti-alloys, and combinations thereof.

6. The method of claim 1, wherein the first and second layers of the material contain SiO_2.

7. The method of claim 1, wherein the second precursor gas includes a silanol gas.

8. The method of claim 7, wherein the silanol gas is selected from the group consisting of tris(tert-pentoxy) silanol, tris(tert-butoxy) silanol, and bis(tert-butoxy)(isopropoxy) silanol.

9. The method of claim 1, wherein first precursor contains $AlMe_3$ and the second precursor contains tris(tert-pentoxy) silanol.

10. The method of claim 1, wherein the exposing the substrate to the second precursor gas includes:

in the absence of any oxidizing and hydrolyzing agent, exposing the substrate at a substrate temperature of approximately 150°C or less, to a process gas containing a silanol.

11. A substrate processing method, comprising:

providing a substrate containing raised features with top areas and sidewalls, and bottom areas between the raised features; and

exposing the substrate to a gas pulse sequence to deposit a material that forms an air gap between the raised features, wherein the gas pulse sequence includes, in any order:

a) sequentially first, exposing the substrate to a first precursor gas to conformally form a first precursor layer on the top areas, on the sidewalls, and on the bottom areas, second, exposing the substrate to a plasma-excited halogen-containing gas to deactivate or at least partially remove the first precursor layer in the top areas and the bottom areas, and third, exposing the substrate to the second precursor gas that reacts with the precursor layer to form a first layer of the material on the sidewalls, and

b) sequentially first, exposing the substrate to the first precursor gas to conformally form a second precursor layer on the top areas, on the sidewalls, and on the bottom areas, and second, exposing the substrate to the second precursor gas that reacts with the second precursor layer form a second layer of the material on the substrate.

12. The method of claim 11, further comprising

repeating steps a), b), or a) and b), at least once until the air gap is formed.

13. The method of claim 11, wherein the first precursor gas contains a metal-containing precursor.

14. The method of claim 11, wherein the first precursor contains aluminum, titanium, or a combination thereof.

15. The method of claim 14, wherein the precursor layers are selected from the group consisting of Al, Al_2O_3, AlN, AlON, an Al-containing precursor, Al-alloys, CuAl, TiAlN, TaAlN, Ti, TiAlC, TiO_2, TiON, TiN, a Ti-containing precursor, Ti-alloys, and combinations thereof.

16. The method of claim 11, wherein the first and second layers of the material contain SiO_2.

17. The method of claim 11, wherein the second precursor gas includes a silanol gas.

18. The method of claim 17, wherein the silanol gas is selected from the group consisting of tris(tert-pentoxy) silanol, tris(tert-butoxy) silanol, and bis(tert-butoxy)(isopropoxy) silanol.

19. The method of claim 11, wherein the exposing the substrate to the second precursor gas includes:

in the absence of any oxidizing and hydrolyzing agent, exposing the substrate at a substrate temperature of approximately 150°C or less, to a process gas containing a silanol.

20. The method of claim 11, wherein the plasma-excited halogen-containing gas includes Cl_2, BCl_3, CCl_4, HCl, HBr, or $TiCl_4$, or a combination thereof.

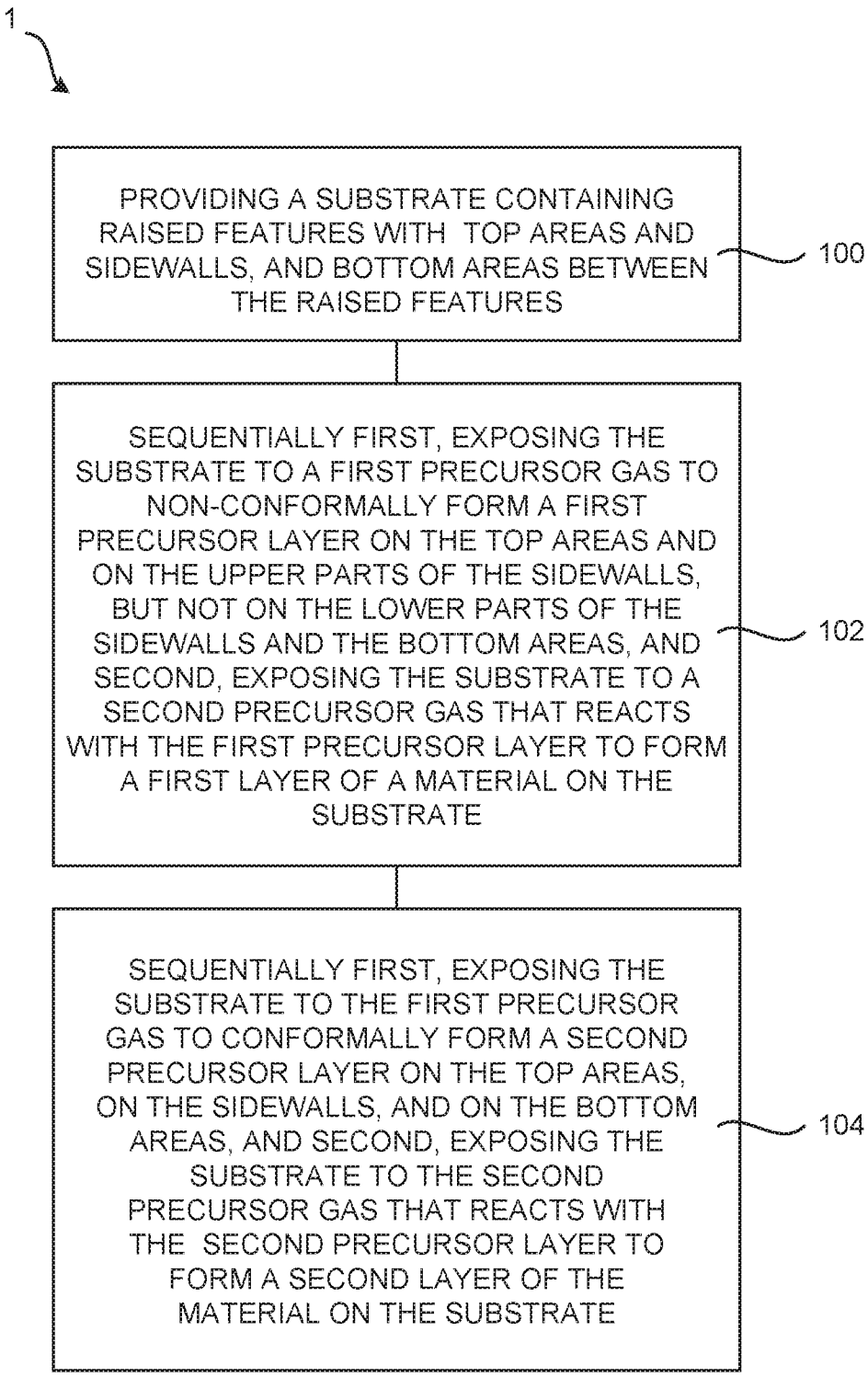
1
PROVIDING A SUBSTRATE CONTAINING RAISED FEATURES WITH TOP AREAS AND SIDEWALLS, AND BOTTOM AREAS BETWEEN THE RAISED FEATURES
100
SEQUENTIALLY FIRST, EXPOSING THE SUBSTRATE TO A FIRST PRECURSOR GAS TO NON-CONFORMALLY FORM A FIRST PRECURSOR LAYER ON THE TOP AREAS AND ON THE UPPER PARTS OF THE SIDEWALLS, BUT NOT ON THE LOWER PARTS OF THE SIDEWALLS AND THE BOTTOM AREAS, AND SECOND, EXPOSING THE SUBSTRATE TO A SECOND PRECURSOR GAS THAT REACTS WITH THE FIRST PRECURSOR LAYER TO FORM A FIRST LAYER OF A MATERIAL ON THE SUBSTRATE
102
SEQUENTIALLY FIRST, EXPOSING THE SUBSTRATE TO THE FIRST PRECURSOR GAS TO CONFORMALLY FORM A SECOND PRECURSOR LAYER ON THE TOP AREAS, ON THE SIDEWALLS, AND ON THE BOTTOM AREAS, AND SECOND, EXPOSING THE SUBSTRATE TO THE SECOND PRECURSOR GAS THAT REACTS WITH THE SECOND PRECURSOR LAYER TO FORM A SECOND LAYER OF THE MATERIAL ON THE SUBSTRATE
104

FIG. 1

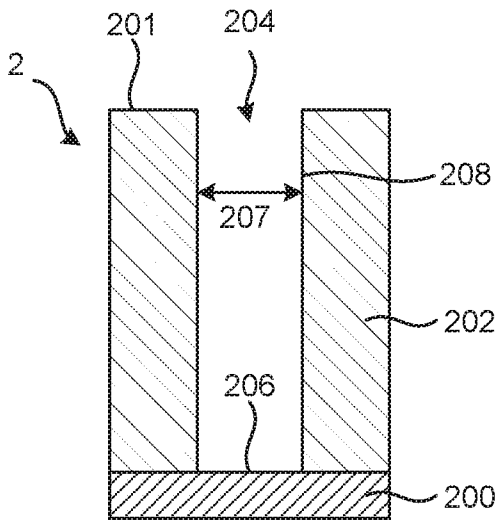

FIG. 2A

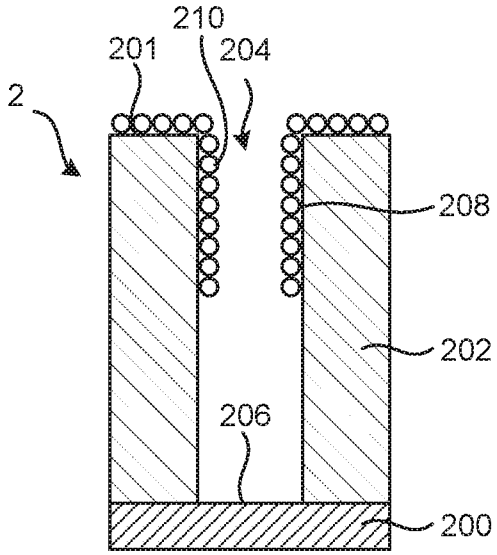

FIG. 2B

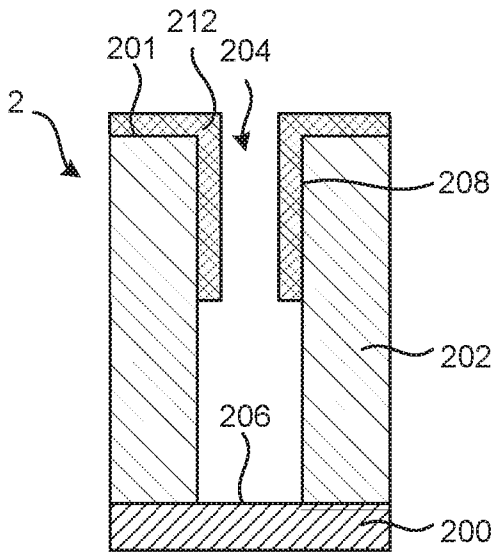

FIG. 2C

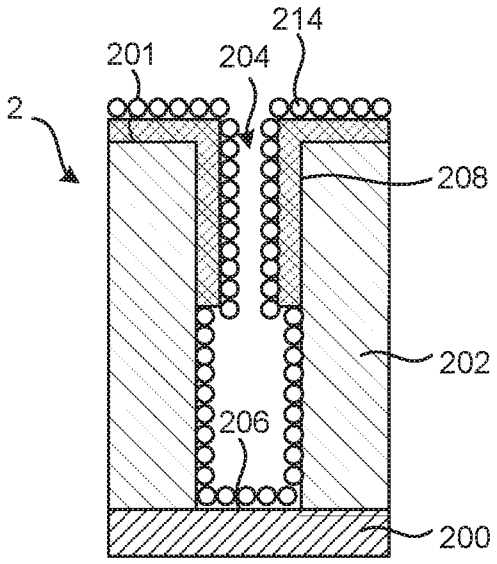

FIG. 2D

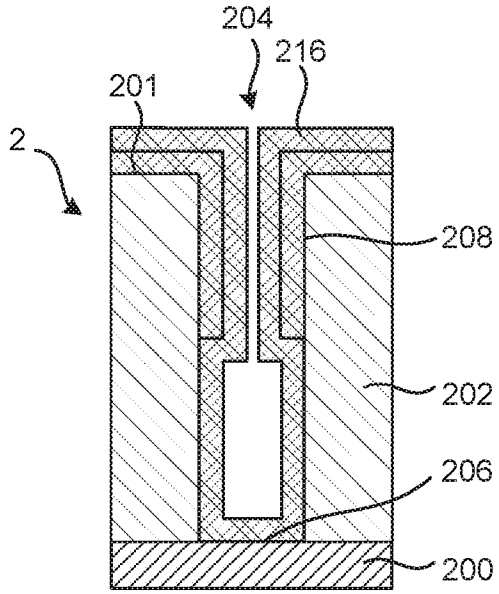

FIG. 2E

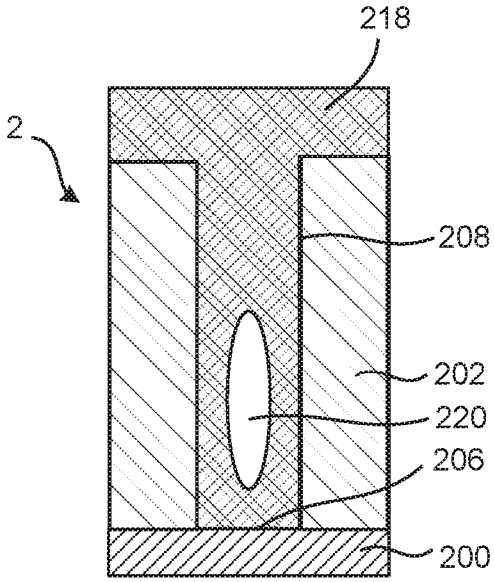

FIG. 2F

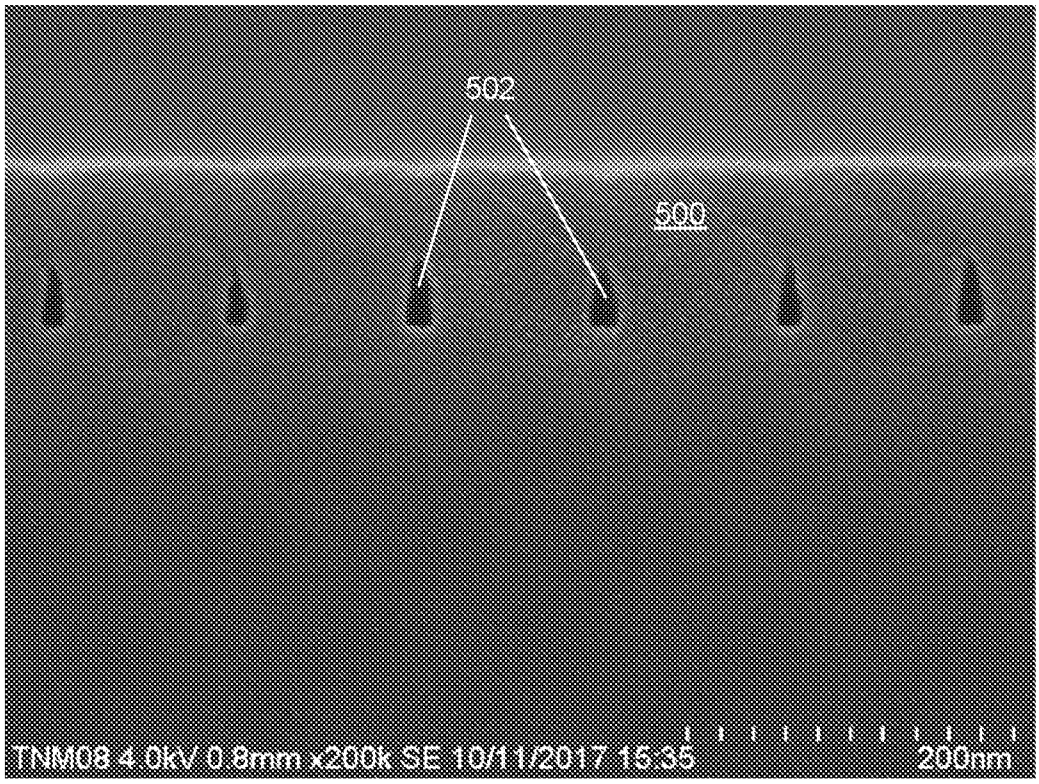

FIG. 5

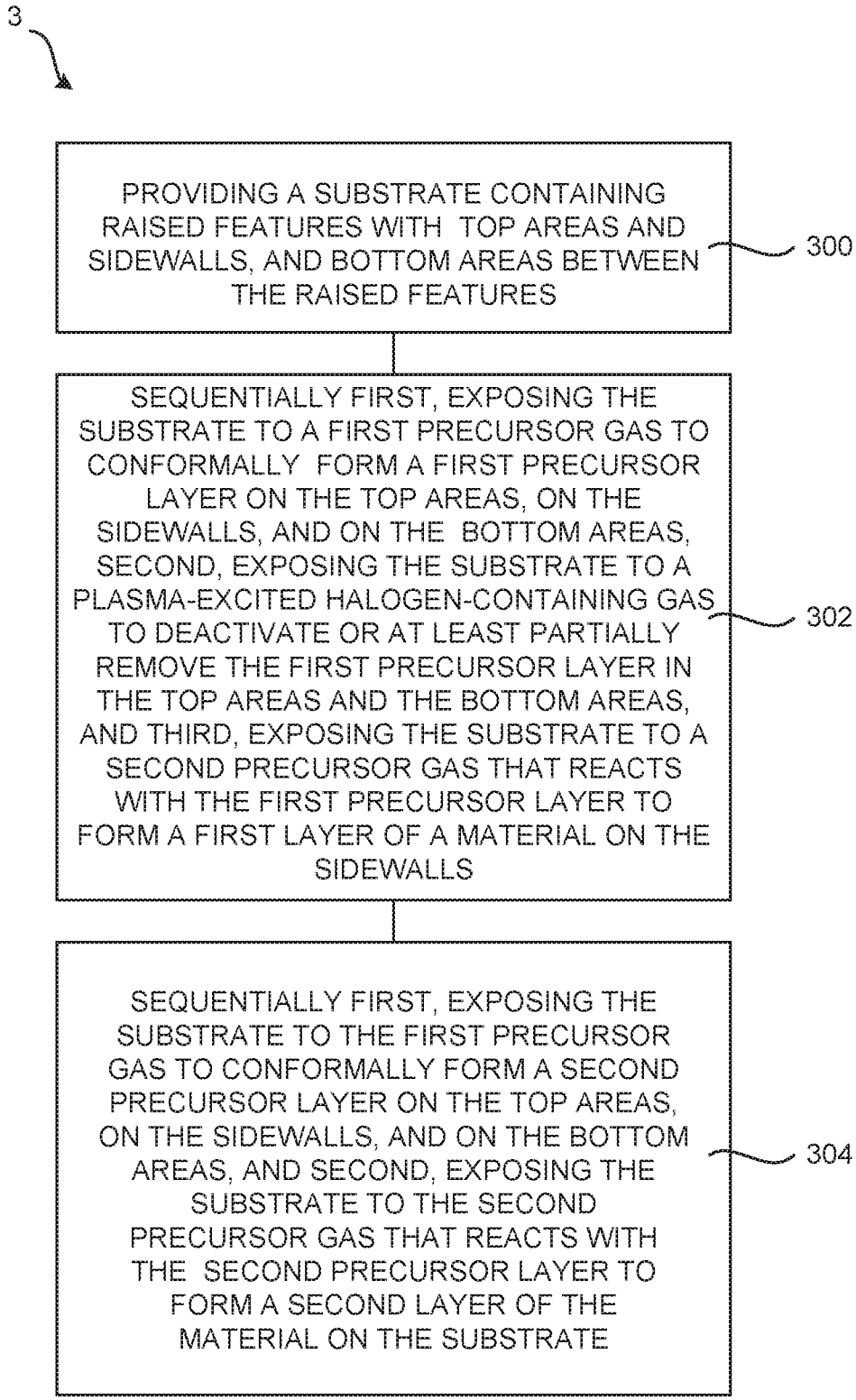
3
PROVIDING A SUBSTRATE CONTAINING RAISED FEATURES WITH TOP AREAS AND SIDEWALLS, AND BOTTOM AREAS BETWEEN THE RAISED FEATURES
300
SEQUENTIALLY FIRST, EXPOSING THE SUBSTRATE TO A FIRST PRECURSOR GAS TO CONFORMALLY FORM A FIRST PRECURSOR LAYER ON THE TOP AREAS, ON THE SIDEWALLS, AND ON THE BOTTOM AREAS, SECOND, EXPOSING THE SUBSTRATE TO A PLASMA-EXCITED HALOGEN-CONTAINING GAS TO DEACTIVATE OR AT LEAST PARTIALLY REMOVE THE FIRST PRECURSOR LAYER IN THE TOP AREAS AND THE BOTTOM AREAS, AND THIRD, EXPOSING THE SUBSTRATE TO A SECOND PRECURSOR GAS THAT REACTS WITH THE FIRST PRECURSOR LAYER TO FORM A FIRST LAYER OF A MATERIAL ON THE SIDEWALLS
302
SEQUENTIALLY FIRST, EXPOSING THE SUBSTRATE TO THE FIRST PRECURSOR GAS TO CONFORMALLY FORM A SECOND PRECURSOR LAYER ON THE TOP AREAS, ON THE SIDEWALLS, AND ON THE BOTTOM AREAS, AND SECOND, EXPOSING THE SUBSTRATE TO THE SECOND PRECURSOR GAS THAT REACTS WITH THE SECOND PRECURSOR LAYER TO FORM A SECOND LAYER OF THE MATERIAL ON THE SUBSTRATE
304

FIG. 3

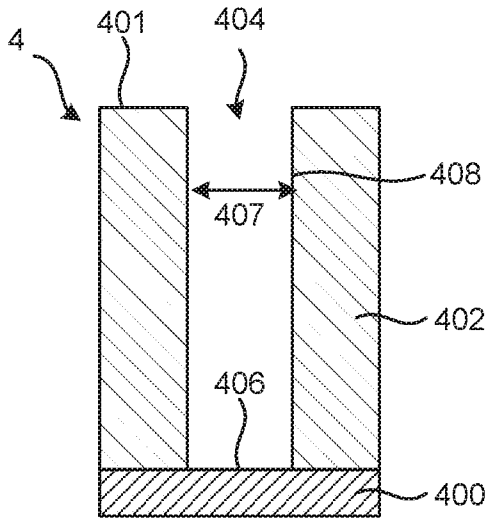

FIG. 4A

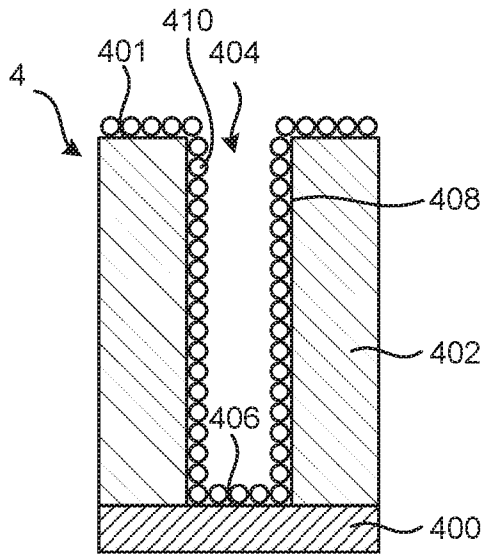

FIG. 4B

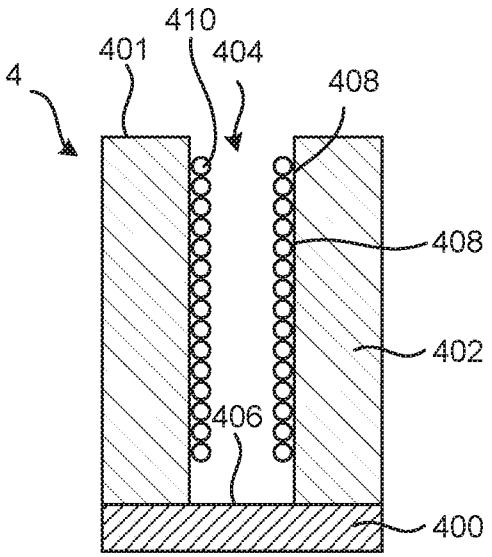

FIG. 4C

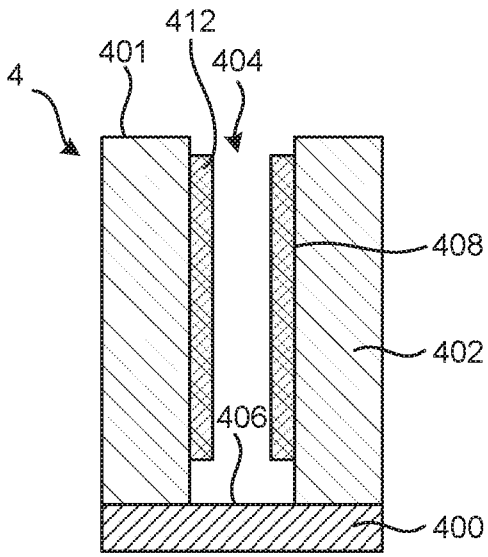

FIG. 4D

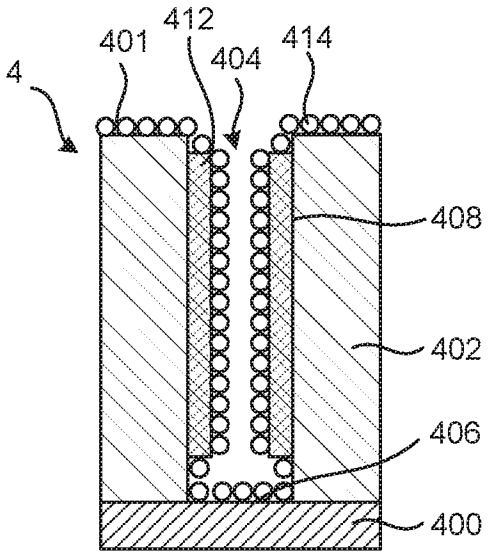

FIG. 4E

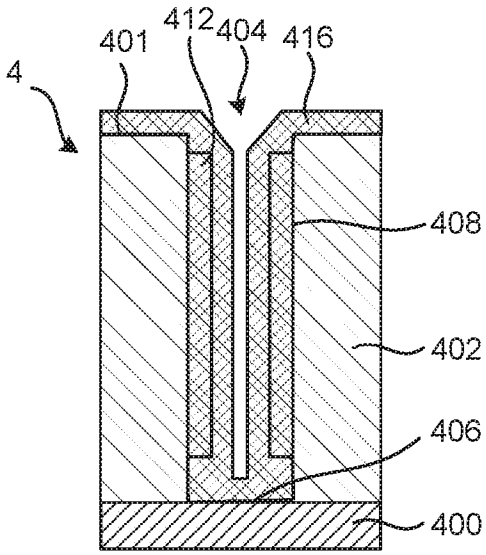

FIG. 4F

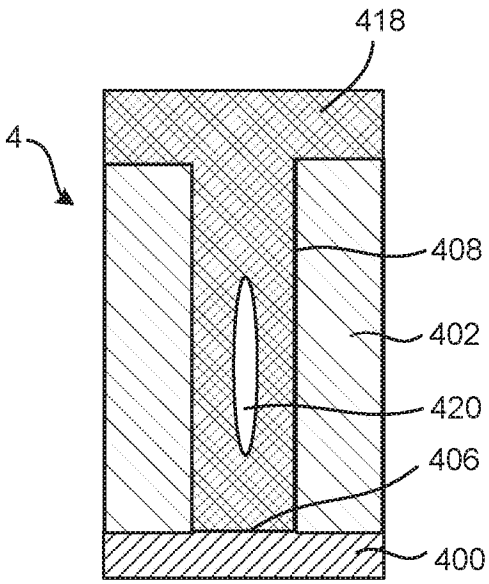

FIG. 4G

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2019/026590

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/768(2006.01)i, H01L 21/02(2006.01)i, H01L 21/324(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/768; H01L 21/28; H01L 21/31; H01L 21/3205; H01L 21/76; H01L 21/764; H01L 27/108; H01L 21/02; H01L 21/324

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: air gap, feature, precursor, non-conformal, conformal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2012-0040534 A1 (ARTHUR J. MCGINNIS et al.) 16 February 2012 See claim 1 and figures 3-6.	1-20
A	US 2014-0070293 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 13 March 2014 See paragraphs [0021], [0030], [0035], [0042].	1-20
A	US 9159606 B1 (APPLIED MATERIALS, INC.) 13 October 2015 See claim 1 and figures 1F-1H.	1-20
A	US 2017-0358481 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.) 14 December 2017 See paragraphs [0032]-[0039] and figures 8, 9.	1-20
A	KR 10-1402962 B1 (KOREA INSTITUTE OF INDUSTRIAL TECHNOLOGY) 03 June 2014 See paragraphs [0038]-[0045] and figures 1a-1h.	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 July 2019 (22.07.2019)	**22 July 2019 (22.07.2019)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2019/026590

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		US 2019-0139812 A1	09/05/2019
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